ST-8000

HF MODEM

TECHNICAL

MANUAL

VOLUME I

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ST-8000

HF MODEM

TECHNICAL MANUAL

VOLUME I

870-08001

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INTRODUCTION

This manual is the technical and maintenance companion to the "ST8000 OPERATOR'S MANUAL" and "ST8000 OPERATOR'S GUIDE". Operation and installation of the ST8000 are fully described in these documents. Technical, test, and maintenance information are contained in this ST8000 TECHNICAL MANUAL.

Because of the size and quantity of technical drawings for the ST8000, this TECHNICAL MANUAL is published in two volumes. VOLUME I contains Chapters 1 through 5 (Specifications, Technical Description, Test and Alignment, Maintenance, and Parts Lists). VOLUME II contains the pictorial and schematic diagrams of the ST8000. The diagrams in VOLUME II are arranged with the schematic diagram for a given circuit section on the right-hand page and the corresponding pictorial for parts location on the left-hand facing page. The texts of Chapter 2, 3, and 4 are keyed to this page arrangement.

It is assumed that the reader has an electronic equipment servicing background and has access to the required test equipment. Please use EXTREME CAUTION when testing to avoid damaging the ST8000 circuitry. In particular, CMOS microcircuits are used in sections of the ST8000 and the technician should use all accepted grounding and static electrical discharge prevention techniques available to him.

In some cases, particularly when testing the CRT Assembly, DANGEROUS HIGH VOLTAGES will be exposed. Use EXTREME CAUTION when performing these tests to avoid POTENTIALLY LETHAL HIGH VOLTAGE shocks.

All of the described tests may be performed with standard test equipment. However, the accuracy of the measurements is determined by the accuracy of the test instruments themselves. Assure yourself of your test equipment's accuracy and reliability before assuming "incorrect measurements" are due to an ST8000 circuit failure.
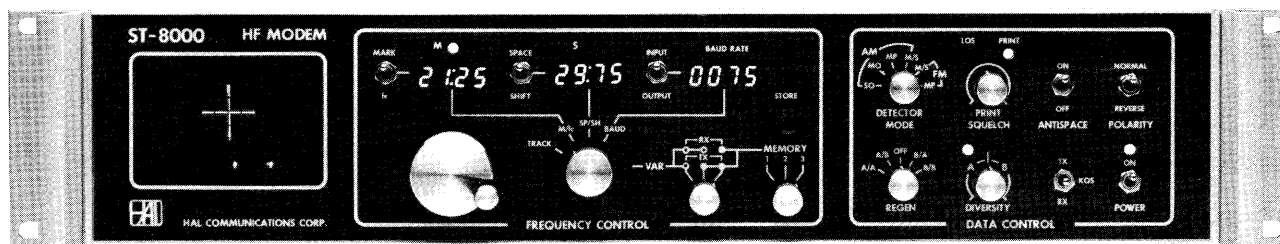
FIGURE 1.1   ST8000 HF MODEM

CHAPTER 1.   SPECIFICATIONS

INPUT DATA:
   Data Rate: 10 to 1200 baud
   Frequency: 400 - 4000 Hz
   Impedance: 8 or 600 ohms, bal. or unbal.
                  5K ohms, unbalanced
   Dynamic Range: -65 to +10 dBm (580 uV to 2.5 V)

RECEIVE PROCESSING:
   Mode: Hard-limiting FM (-54 dBm threshold)
                  AGC controlled AM (-65 dBm threshold)
   Input Filters: 4 filters: 6-pole 1/3, 1/2, 1 Octave
                  bandwidth - tunable and tracked to
                  center frequency of selected Mark and
                  Space tones; 400 - 4000 Hz fixed tuned.
   Tone Filters: Matched 4-pole tunable filters, set to
                  selected Mark and Space frequencies
                  from 400 to 4000 Hz in 1 Hz increments.
                  M/S filter bandwidths set in 32 steps,
                  automatically tracked with Baud and
                  Shift selected.

DATA PROCESSING:
   Detectors: Matched full-wave active detectors.
                  Outputs for Mark Only, Space Only,
                  M/S differential, or Digital Multi-Path
                  Correction.
   LP Filters: Matched separate Mark and Space 7-pole
                  linear phase tunable low-pass filters.
                  Cut-off frequencies set by Input Baud
                  rate control.
   Antispace: Prevents "open loop" on interference.
   Print Squelch: Adjustable Print Squelch threshold;
                  returns to Mark-hold with no signal (LOS).
   Diversity: Infinite Resolution Diversity Control for two
                  receiver selection diversity system.
   Regeneration: Dual digital UART regenerator for ASCII or
                  Baudot data; also provides code and speed
                  conversion (45 - 1200 bd).
   Clock Recovery: Recovered receive data clock output.

TUNING FEATURES:
  Control: Frequencies derived from quartz crystal
                  synthesizers. Set Mark, Space, Shift,
                  and Center frequencies, Input or Output
                  Baud in 1 Hz or 1 Baud increments.
  Modes: BAUD   - set Input or Output Baud rate
                  SP/SH   - set Space or Shift frequency
                  MARK/Fo - set Mark or Center frequency
                  TRACK   - Maintain Shift and set Mark,
                               Space, and Fo frequencies.
  Memories: Eight - non-volatile and programmable.
                  Each memory stores Mark, Space, Fo,
                  Shift, Input Filter, M/S Bandwidth,
                  LP Filter Frequency, Input Baud, Output
                  Baud, and M/S AFSK transmit frequencies.
  Memory Modes: TX/RX variable, RX variable, TX memory,
                  TX/RX memory.
  Remote Control: Separate terminal port for control of
                  all demodulator parameters. (Serial
                  ASCII; 300-9600 Baud).

TRANSMIT FEATURES:
  AFSK Tones: 400 to 4000 Hz in 1 Hz increments.
                  Track receiver tones or fixed by
                  memory selection.
  AFSK Level: -40 to +10 dBm (rear panel control)
                  (7.8 mV to 2.5 V rms at 600 ohms).
  Impedance: 8 or 600 ohms, balanced or unbalanced,
                  transformer coupled or DC isolated output.
  PTT Control: Relay closure to ground; internal KOS,
                  terminal KOS, RS232C RTS, or manual front
                  panel switch control; +/- 50V, 0.5A max.
  FSK Output: Logic voltage to drive direct FSK input
                  on transmitter. Polarity and voltage
                  level selectable (open collector, +5V,
                  or +8V for Mark or Space).

DISPLAYS:
  Tuning: 1.50 x 2.00 inch rectangular CRT;
                  crossed-ellipse Mark/Space and
                  Spectra Tune   500-3500 Hz spectral
                  display of received signals; CRT beam
                  turned off on LOS (Loss Of Signal).
  Frequency: Three 4-digit displays show Mark or Fo,
                  Space or Shift, and Input or Output Baud.
  LED: Mark, Space, LOS, Print On, A or B
                  Diversity, TX on, and Power on.

INPUT/OUTPUT CONNECTIONS:

TERMINAL DATA: Shielded DB-25S socket-type connector.
                  RS232C: TXD, RXD, RTS, CTS,
                             CD, DSR, recovered RXC
                  MIL-188C: TXD, RXD
                  TTL: TXD, RXD
                  Misc: Terminal KOS, Motor Control,
                             FSK output.

DIVERSITY: Shielded DE-9S socket to connect second
                  ST8000 in two-channel diversity system.

REMOTE CONTROL: Shielded DB-25S socket for serial remote
                  control of all front panel parameters.

RECEIVE AUDIO: Stereo 1/4" phone jack for audio input.

TRANSMITTER: 4-pin shielded mic. connector; transmit
                  audio and PTT or transmit FSK and PTT.

POWER: IEC AC power connector; shielded and
                  filtered.

PHYSICAL DATA:

Cabinet Finish: Natural aluminum with irridite finish;
                  black vinyl front panel.

Cabinet Style: 19" rack mounting or table-top
                  with tilt-bail and feet.

Size: 3.50 H x 14 D x 19 W (rack mtg)
                  (8,9 x 35.6 x 48.3 cm)
                  4.125 H x 14 D x 17 W (table case)
                  (10.5 x 35.6 x 43.2 cm)

Weight: 13 lbs (5.9 kg) net,
                  19 lbs (8.6 kg) shipping.

Power: 100-120 or 200-240 VAC, 44-440 Hz;
                  36 Watts; IEC style AC Connector.

Power Line   Fused with type 3AG, 1.0A SB Fuse;
Protection: Type 1EF2 RFI/EMI Filter (22dB at
                  0.15 mHz, 49 dB at 30 mHz).

CHAPTER 2. TECHNICAL DESCRIPTION

This chapter presents a detailed explanation of the circuitry of the ST8000. Frequent references will be made to the schematic and pictorial diagrams in Chapter 6 (VOLUME II). These references will be given at the head of each subsection of the discussion in the form [6.x] where "6.x" is the figure number. Additional illustrations will be included in this Chapter as necessary. Drawing conventions used in this manual are shown in Figure 6.1.

2.1 ST8000 ORGANIZATION [6.2]

The ST8000 is constructed of 5 subassemblies: MODEM (A1), CONTROL (A2), FRONT PANEL (A3), CRT (A4), and CABINET (A5). Each assembly is connected to the other with the cables shown in Figures 6.53 and 6.54. All of the audio and data processing detection circuitry for receive and transmit operation are contained on the MODEM (A1) assembly. Master control and frequency generating synthesizer circuits are on the CONTROL (A2) assembly. Cathode Ray Tube (CRT) control and amplifier circuits are on the CRT assembly (A4). Front panel switches, controls, and decoding circuits are on the FRONT PANEL assembly (A3). Low voltage power for the MODEM, CONTROL, FRONT PANEL, and CRT assemblies is obtained from regulators on the MODEM assembly (A1). High voltages and filament voltage for the CRT are obtained from the CRT assembly (A4). The CABINET assembly (A5) contains only the AC power input components, the power transformer, and the +5 volt regulator. With the exception of the CRT itself, all ST8000 circuits operate from supply voltages of +8 VDC (+V), -8 VDC (-V), (all analog circuits) and +5 VDC (all digital circuits).

2.2 MODEM ASSEMBLY A1 [6.3 through 6.26]:

The MODEM assembly is the lower of two large circuit boards in the right center section of the cabinet. It may accessed by removing the ST8000 top cover, three thumb-screws from the upper CONTROL assembly, and swinging the CONTROL assembly to a vertical position. Steps to obtain access to the MODEM assembly are described in detail in Section 2.1 of the ST8000 OPERATOR'S MANUAL.

2.2.1 INPUT FILTER [6.3, 6.4]:

Audio signals from the radio receiver are connected to the rear panel RCVR AUDIO connector (J12). The input characteristics may be set with option DIP switch S1-1 through S1-5 for 600 ohm or 8 ohm impedance, balanced or unbalanced or 5,000 ohms, unbalanced. The setting procedure is explained in Section 2.2 of the ST8000 OPERATOR'S MANUAL. Transformer T1 provides impedance matching and balanced-to-unbalanced transformation of the input signal. Input levels marked on the schematic diagrams assume a 2000 Hz, -10.0 dBm input signal.

Input signals with levels greater than +12 dBm are clipped by diodes D69 through D71, providing input overload protection for the demodulator. Amplifier U50a provides input isolation and approximately 5 dB gain. Stage U50b is a two-pole active low-pass filter to prevent aliasing problems in following Switched Capacitor Filters (SCF's). TP1 provides a test point for the input amplifier and low-pass filter performance.

Switches U51 and U44 provide electronic selection of one of four bandpass filters (U41, U42, U43, and U52). Switching of U51 and U44 is controlled by the microprocessor on the CONTROL assembly through J2-19 and J2-20.

Stages U41, U42, and U43 are monolithic integrated circuit Switched Capacitor Filters (SCF). Each contains a 6-pole Chebyshev Class II bandpass filter. The filters have the following fixed Q's:

STAGE	BANDWIDTH	Q	IC TYPE
U41	1/3 OCTAVE	4.5	R5614/RF5614
U42	1/2 OCTAVE	3.0	R5615/RF5615
U43	1.0 OCTAVE	1.5	R5616/RF5616

The center frequency of each filter is controlled by the synthesized Input Filter Clock, supplied on J2-1 from the CONTROL assembly (A2). This clock frequency is nominally 54 times the desired Input Bandpass Filter center frequency. The selection of the filter and choice of the clock frequency is controlled by the microprocessor on the CONTROL assembly.

A fourth filter, U52, is much wider to allow processing of wide shift and high data rate RTTY signals. Section U52a is a two-pole active low-pass filter with a cut-off frequency of 4200 Hz. Section U52b is a two-pole high-pass filter with an 380 Hz cut-off frequency. The two sections form a wide bandpass filter for signals between 380 and 4200 Hz.

Stage U32 is a low-pass filter to remove all clock noise from the outputs of filter stages U41, U42, and U43. U32 also provides two additional poles of low-pass filtering for stage U52, increasing the skirt selectivity of the wide filter. Test points TP4 and TP5 allow monitoring of the signal output of the Input Bandpass Filter stages. Typical frequency response curves for the four input filters are shown in Figure 2.1.

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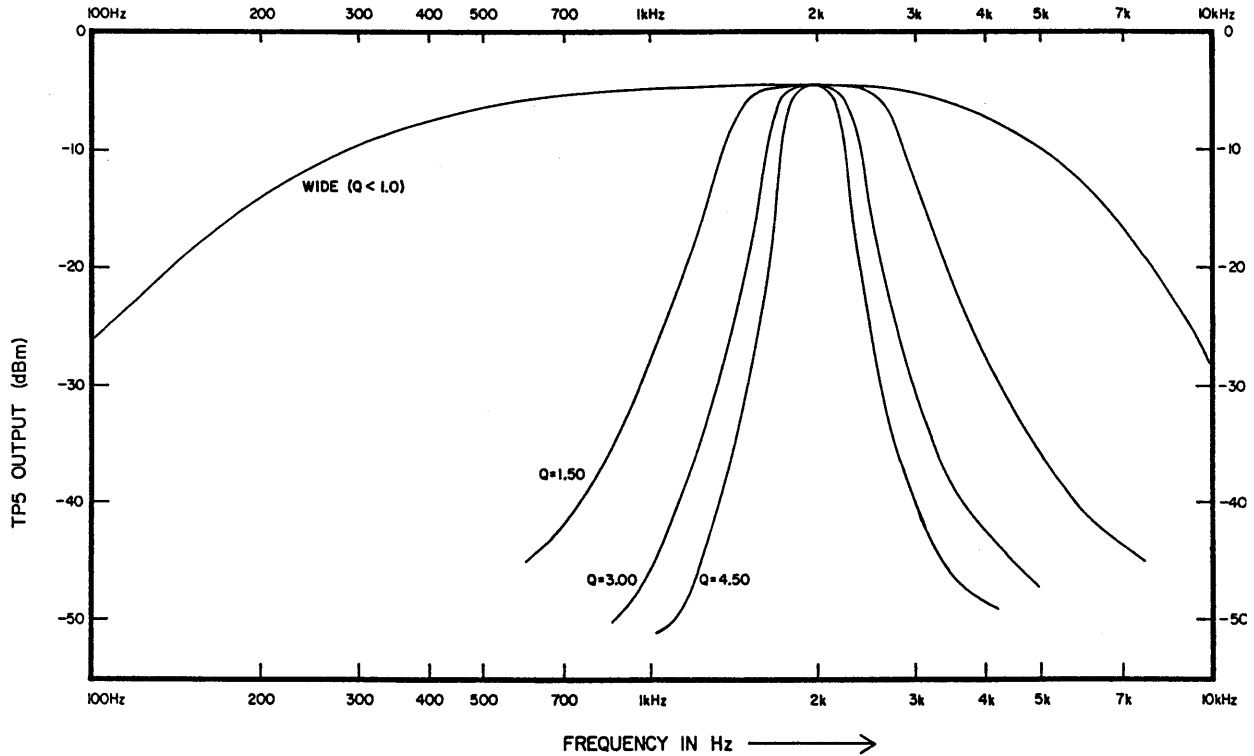
FIGURE 2.1   INPUT BANDPASS FILTERS

2.2.2   LIMITER & AGC [6.5, 6.6]:

The signal from TP5 of the Input Bandpass Filter drives both a hard Limiter stage (U31) and an AM Automatic Gain Control (AGC) stage (U30, U21, U22, U13, and U3). The input levels to both stages are set for optimum dynamic range with dividers R187/R177 (Limiter) and R190/R184 (AGC).

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Limiter stage U31 is operated as a very high gain (>70 dB) compensated amplifier. The limiter threshold of U31 is typically -53 dBm, referred to the receiver input (J12). Control R182 is adjusted for symmetrical limiting on weak signals at TP6 or TP8. U23 is a two-pole anti-aliasing low-pass filter to prevent harmonics generated in the limiter from reaching the MARK and SPACE channel filters. Resistive divider R116/R96 sets the limited signal amplitude to be compatible with the output of the AGC amplifier. Typical limiter output vs receiver input level is shown in Figure 2.2.
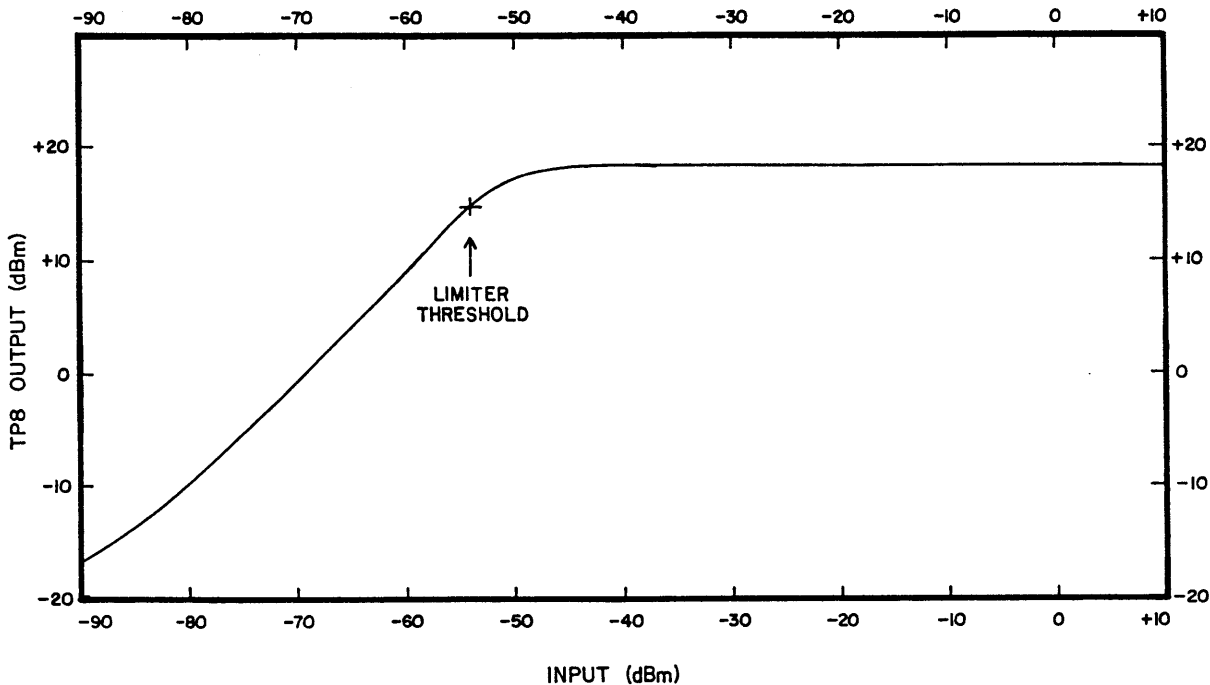
FIGURE 2.2   LIMITER OUTPUT CHARACTERISTICS (TP8)

An AGC dynamic range of +10 to -65 dBm is obtained in stages U30, U21, U22, and U13. The total gain of amplifiers U30 and U22 is controlled by a DC voltage from the output of U21 (TP11). Stages U21a, U13a, and U13b provide gain and high-pass/low-pass filtering in the AGC loop. The output audio signal is detected in diodes D2 through D5. The approximate 3.0 volt drop in the diode chain sets the regulation voltage level output of the AGC amplifier system at +10.0 dBm. Amplifier U21b provides the feedback gain controlling voltage to U30 and U22 with time constant set by R104 and C46.

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Amplifier stages U3a and U3b condition the AGC voltage to be within the range of 0 to +5 VDC. The resulting output (TP12) is used to drive the DIVERSITY selection circuits of two ST8000's in a two-channel diversity system. Control R102 is set for a reference voltage of 0.56 VDC at R3 and control R103 is set for +5.0 VDC at TP12 with a 0 dBm receiver input signal on J12 [6.4]. Typical AGC voltage at TP12 vs input signal level is shown in Figure 2.3.
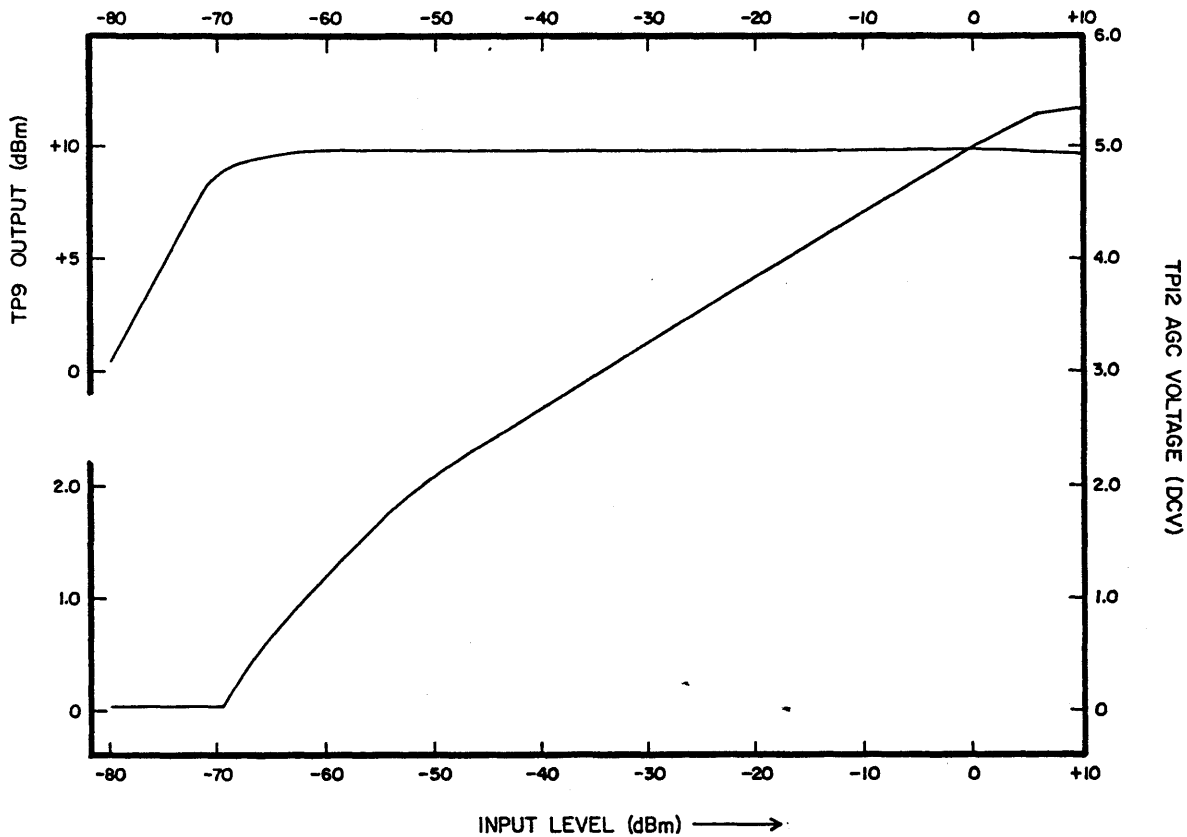
FIGURE 2.3   AGC CHARACTERISTIC (TP4)

The output of the Limiter (from R116/R96) and AGC (TP9) stages are selected electronically by switch U14. This switch is controlled via J2-7 by the microprocessor on the CONTROL assembly (A2). The front panel DETECTOR MODE switch or REMOTE CONTROL commands select AM or FM mode.

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2.2.3 MARK AND SPACE FILTERS [6.7 - 6.10]

The MARK and SPACE discriminator filter stages are identical.
Only the MARK circuit will be discussed with SPACE filter
references in parenthesis ().

Stages U17a (U26a) and U17b (U26b) are cascaded two-pole SCF
filters.   The center frequency of the filters is set by a
synthesized clock, whose frequency is nominally 50 times the
desired center frequency. The clock signal is supplied via J1-20
(J2-5) from the MARK (SPACE) synthesizer on the CONTROL assembly
(A2).   Controls R85 (R123) and R86 (R124) allow precise
adjustment of the center frequency of the filters, compensating
for any variations in the clock-to-center frequency ratio of the
SCF microcircuits. Stage U9 (U18) is a 2-pole low-pass filter to
remove any residual clock noise from the filter output.   Control
R132 (R131) provides DC offset compensation of the output at TP46
(TP41).

The bandwidth of the MARK (SPACE) filter is controlled by
resistor networks U15 (U24) and U7 (U33) in conjunction with
resistors R94 (R95), R13 (R165), R81-R83 (R125-R128), R18 (R30),
and R19 (R31).   The shunt resistance to ground of U15 (U24) and
U7 (U33) is controlled by switches U5 (U16) and U6 (U25).   A
total of 16 different shunt resistances and therefore filter Q's
may be selected with the 4-bit data input on J1-13,15,17, and 20
(J2-12,14,16, and 18).   In addition, switches U2c (U2b) and U2d
(U2a) provide selection between a HIGH and LOW range of Q-values
with control input on J1-20 (J1-6).   The effectively 5-bit
control line sets MARK (SPACE) Q values between 32.7 and 1.9 as
shown in the Table on Figure 6.8 (6.10). When used in the HIGH-Q
range, stages U17a (U26a) and U17b (U26b) are both used as
variable-Q, 2-pole filters.   In the LOW-Q range, stage U17a
(U26a) is used as a variable Q filter, but the Q of stage U17b
(U26b) is fixed at Q = 1.00. Precision resistances are used for
all Q-determining circuits and no Q adjustments are required.
Typical HIGH-Q curves are shown in Figure 2.4 and LOW-Q curves in
Figure 2.5.
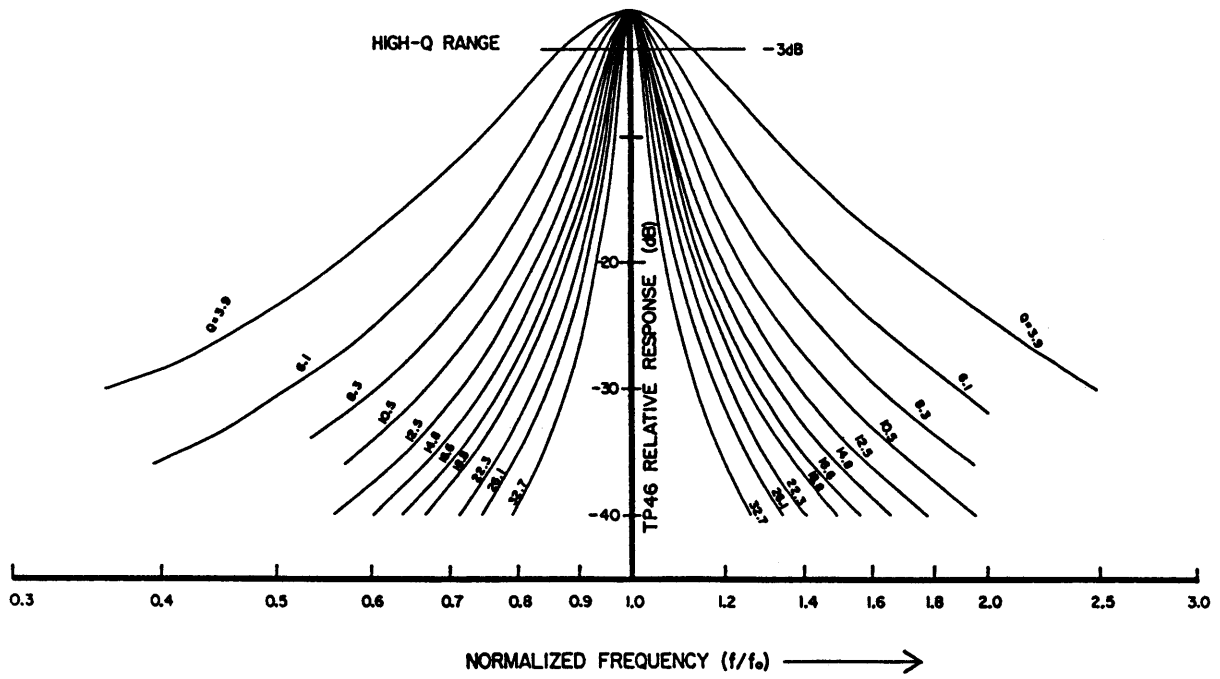
FIGURE 2.4   MARK/SPACE FILTER - HIGH-Q RANGE
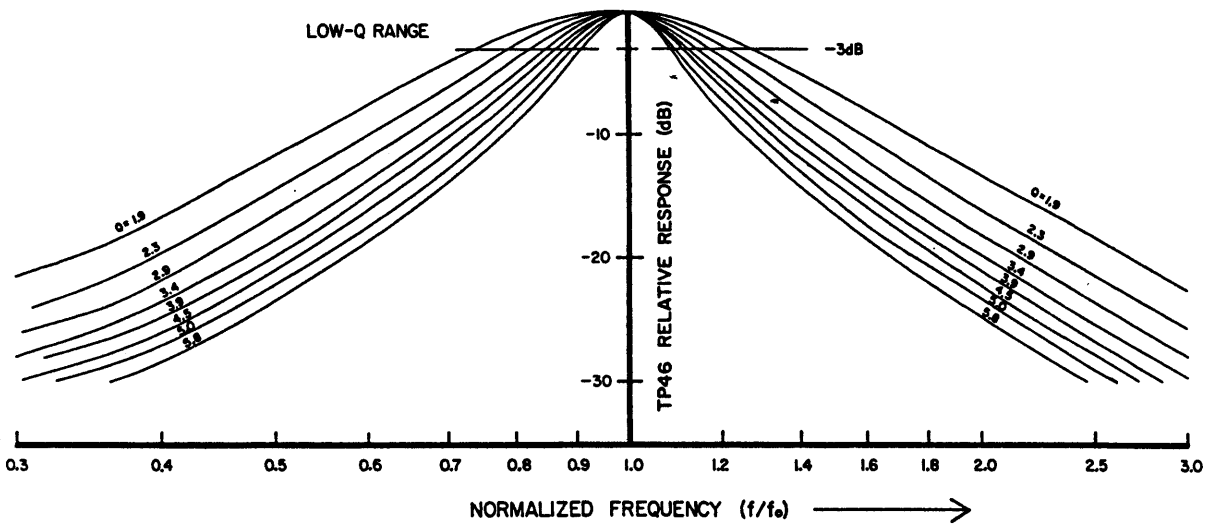
FIGURE 2.5   MARK/SPACE FILTER - LOW-Q RANGE

2.2.4 MARK/SPACE DETECTORS & LP FILTERS [6.11, 6.12]:

The outputs of the MARK (TP46) and SPACE (TP41) filters drive identical but opposite polarity full-wave ideal-diode detectors (U10 and U37). These detector circuits have a dynamic range of greater than 40 dB, adding to the wide-dynamic range performance of the ST8000. Stages U10b and U37b serve the dual function of summing ports for the full-wave rectifier and low-pass filters to remove residual audio components from the rectified MARK and SPACE pulses.

Stages U11 and U27 are identical 7-pole linear-phase SCF low-pass filters. The cut-off frequency of these filters is controlled by a synthesized clock whose frequency is 128 times the desired cut-off frequency. The clock is obtained via J2-17 from a synthesizer on the CONTROL assembly (A2). Stages U12 and U28 are 2-pole low-pass filters to remove any residual clock noise from the low-pass filter output. Controls R65 and R68 are used to compensate for DC offset at TP45 and TP37. Control R63 allows adjustment of the SPACE detected signal level so that MARK and SPACE detected signal voltages may be balanced. The variable low-pass cut-off frequency is normally set to 0.75 times the INPUT BAUD rate, but may be set to other values using the REMOTE CONTROL feature. The frequency response of the low-pass filter is shown in Figure 2.6.

2.2.5 PULSE DETECTORS, PRINT SQUELCH, DMPC [6.13, 6.14]:

The outputs of the low-pass filters (TP45 and TP41) drive four different pulse detectors to provide MARK ONLY (MO), SPACE ONLY (SO), MARK/SPACE (M/S) and PRINT SQUELCH (+/+) outputs. In addition, the MO and SO outputs are combined to provide a Digital Multi-Path Correction (DMPC) output.

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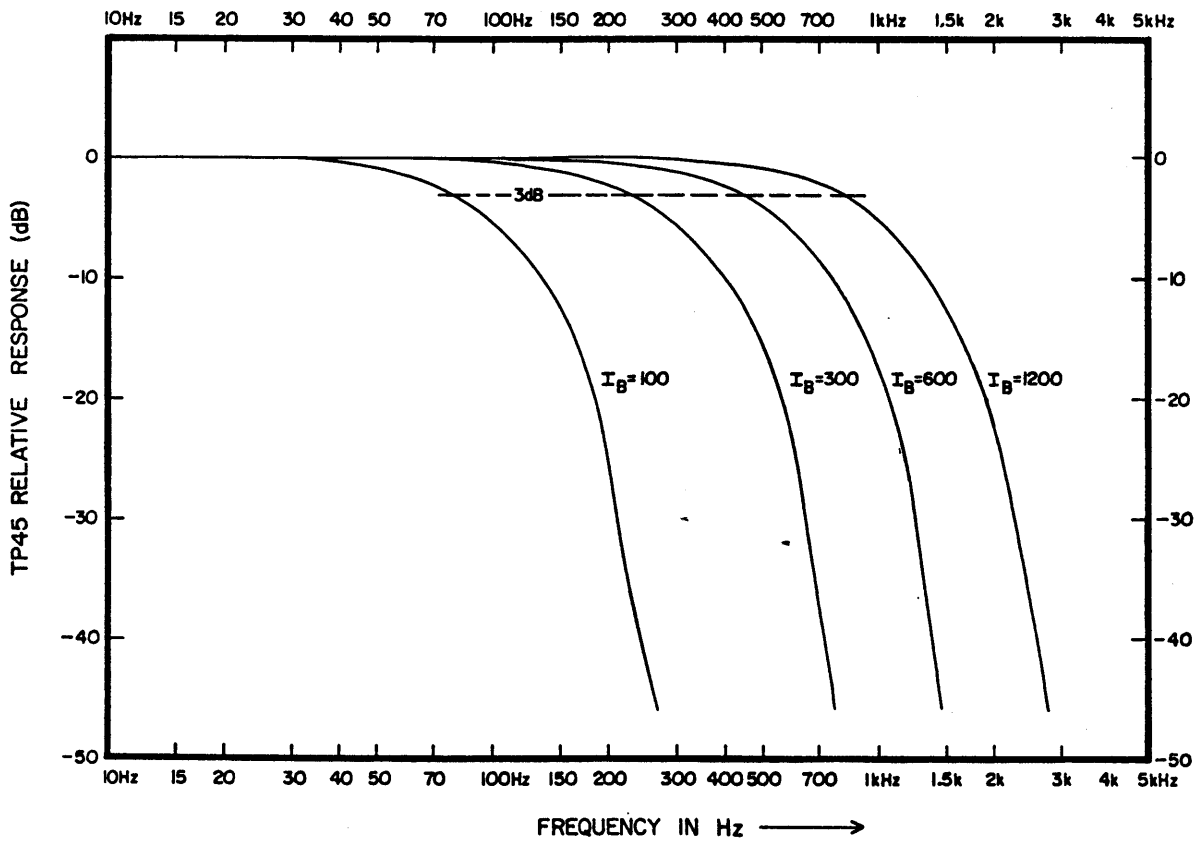
Figure 2.6   Low-Pass Filter Response

2.2.5.1 MO/SO DETECTORS [6.13, 6.14]:

The MARK ONLY and SPACE ONLY detectors are identical except for
diode and output pulse polarity.   To simplify the explanation,
the positive voltage pulse output of the SPACE detector will be
described.   Corresponding references to the MARK ONLY detector
will be shown in parenthesis (#).   Refer to Figure 2.7 for
waveforms used in the following discussion.
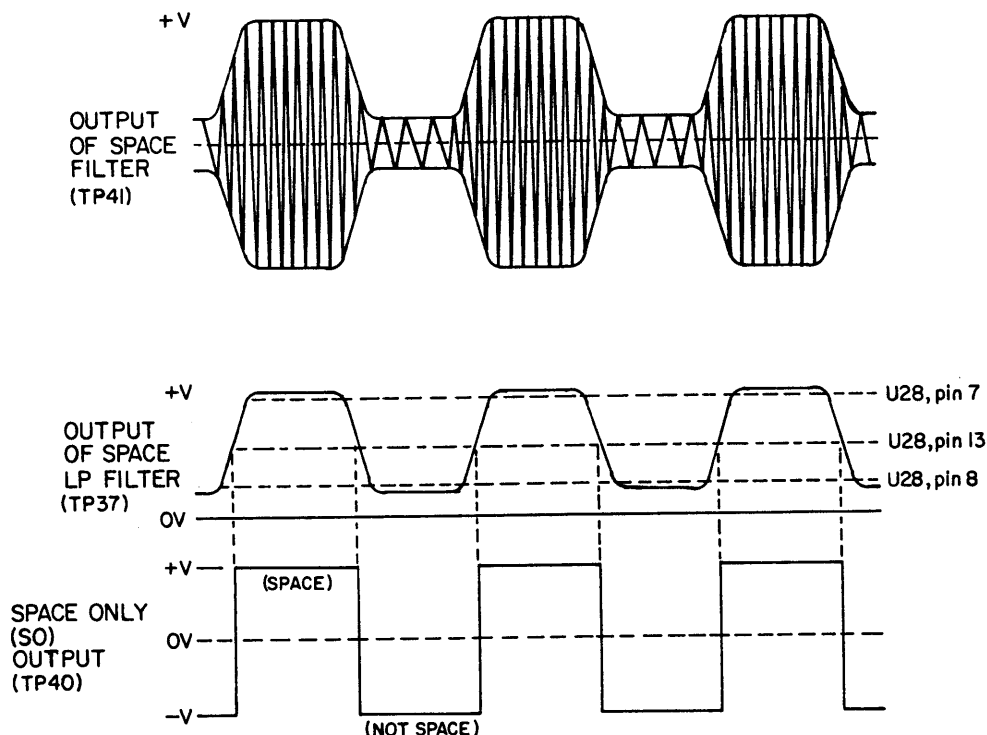
FIGURE 2.7   SPACE ONLY DETECTOR WAVEFORMS

Circuit U28 (U12) forms the SPACE ONLY detector. Diode D53 (D12)
peak detects the positive (negative) SPACE (MARK) pulse output,
presenting a DC voltage proportional to the peak signal level at
pin 5 of U28b (U12b).   Diode D52 (D10) peak detects the
difference between the data pulse and +V (-V), producing a
voltage proportional to the amplitude of the "valley" between
SPACE (MARK) pulses.   This voltage is applied to pin 10 of U28c
(U12c).   Stages U28b (U12b) and U28c (U12c) are isolation
amplifiers,   used to prevent loading of the peak detected
voltages.   Resistors R140 (R45) and R139 (R46) present the mid-
voltage difference between the "peak" and "valley" values of the
pulse to the positive input of comparator U28d (U12d).   The
original detected SPACE (MARK) signal from TP37 is connected to
the negative input of U28d (U12d).   The "sliced" and threshold-
corrected SPACE ONLY (MARK ONLY) signal is the output of U28d
(U12d) at TP40 (TP44).

In this manner, a sliced +/- output is obtained from comparator U28d (U12d) using a reference that is proportional to the average mid-voltage between pulse maxima and minima. This technique prevents loss of data due to rapid signal fades and for high data rate conditions when MARK and SPACE filter bandwidths are so large that there is considerable filter output from the opposite channel signal. Diodes D28, D30, and D31 (D14, D18, D19) provide a clamp on the magnitude of the "valley" voltage to prevent it from rising to meet the peak value during extended periods of constant SPACE (MARK) condition. Time constants of the peak detectors are set to 200 ms, corresponding to typical HF RTTY signal fades. The time constant of the "valley" detector is set to 1 second to minimize biasing effects of "spike" noise.

The sliced SPACE ONLY output of U28d has a polarity of +V = SPACE signal present and -V = SPACE not present. The MARK ONLY output of U12d is +V = MARK signal present and -V = MARK not present. These +/- voltages are converted to +5V logic levels by transistors in microcircuit U19. The SPACE ONLY (SO) output is further inverted in stage U49a. The resulting logic level outputs (U19, pin 2 and U49 pin 2) both have the polarity of +5V = SPACE and 0V = MARK. The MARK ONLY and SPACE ONLY detectors should always be used with AM signal processing and are best used for OOK (ON-OFF KEYED) signals such as CW or when heavy interference blocks one data signal.

2.2.5.2 M/S DETECTOR [6.13, 6.14]:

The outputs from the MARK (TP45) and SPACE (TP37) low-pass filters are of opposite polarity. These two signals are summed at the input to U20a, a unity-gain inverting amplifier. The resulting bipolar signal is coupled through the ATC (Automatic Threshold Correction) circuit (D20-23, C19-20, R48-49) to the input of the high gain comparator, U20b. The ATC circuit provides DC level restoration and balance, even when either the MARK or SPACE signal strength fades with respect to the other. The +/- output of U20b is converted to logic levels in transistor U19a, resulting in a signal polarity of MARK = 0V, SPACE = +5V. The MARK/SPACE detector gives consistent low-distortion data output for most signal conditions using either AM or FM processing. The detector with AM processing is particularly effective for recovery of weak signals with heavy differential MARK/SPACE fading.

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2.2.5.3 PRINT SQUELCH DETECTOR [6.13, 6.14]:

The opposite polarity MARK (TP45) and SPACE (TP37) signals are
differentially summed in stage U29a, producing a voltage at TP38
that is positive if a signal is present at EITHER the MARK or
SPACE frequency. If either MARK or SPACE is weaker or not
present, the signal at TP38 will show variations at the data
rate.   This "+/+" signal is detected and filtered by D26, C21,
and R146 to give a slowly varying DC voltage, applied to pin 5 of
U29b.   When a valid MARK/SPACE RTTY signal is received, the
voltage at pin 5 will be positive and at a maximum, non-varying
level.   If BOTH MARK and SPACE pulses are not presented in
alternate fashion, the voltage at pin 5 will be lower than
maximum and vary. Therefore, noise or signals in just one of the
two MARK/SPACE channels will not produce a steady high-amplitude
voltage.   Also, if the RTTY signal is mistuned so that the tones
do NOT match those of the MARK and SPACE filters, this voltage
will also be low and vary.

The pin 6 input to comparator U29b is a voltage that is set by
the front panel PRINT SQUELCH control. When the smoothed "+/+"
voltage at pin 5 is greater than that on pin 6 from the PRINT
SQUELCH control, TP39 (output of U29b) is positive, indicating
PRINT ON condition. When the "+/+" voltage falls BELOW the PRINT
SQUELCH value, TP39 swings rapidly negative to the NON-PRINT
condition.   Adjustment of the PRINT SQUELCH control adjusts the
this threshold value. Since the absolute outputs of the MARK and
SPACE filters do vary with selected filter Q, the optimum PRINT
SQUELCH setting will vary with data rate selected.   The bipolar
squelch signal at TP39 is converted to logic levels in transistor
U19, producing the logic signal "SQA" (SQUELCH - CHANNEL A).

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2.2.5.4 DMPC CIRCUIT [6.13, 6.14]:

The logic-level outputs of the MARK ONLY and SPACE ONLY signals are combined in stages U39a and U40 to provide correction for multi-path distortion of the RTTY signal. Multi-path propagation of an RTTY signal may cause differential fading or severe pulse distortion of the signal. In the case of differential fading, use of AM and the M/S detector is usually adequate. In the second case, the propagation path-lengths may be sufficiently different that the received composite signal has a noticeable time-overlap between MARK and SPACE pulse conditions. This pulse-overlap condition is corrected by the DMPC circuit. Refer to Figure 2.8 for the following explanation.

The MARK and SPACE ONLY signals are applied to XOR gate U39a, producing an output ONLY when the two signals are different. The two signals are then gated by U39a output (U40a,b) and applied to a set-reset flip-flop (U40c,d). The resulting output at TP49 will ONLY change states when there is no time-overlap between MARK and SPACE data. As shown in Figure 2.8, the resulting data signal is shifted in time by the amount of the overlap, but is NOT otherwise distorted with MARK or SPACE bias.
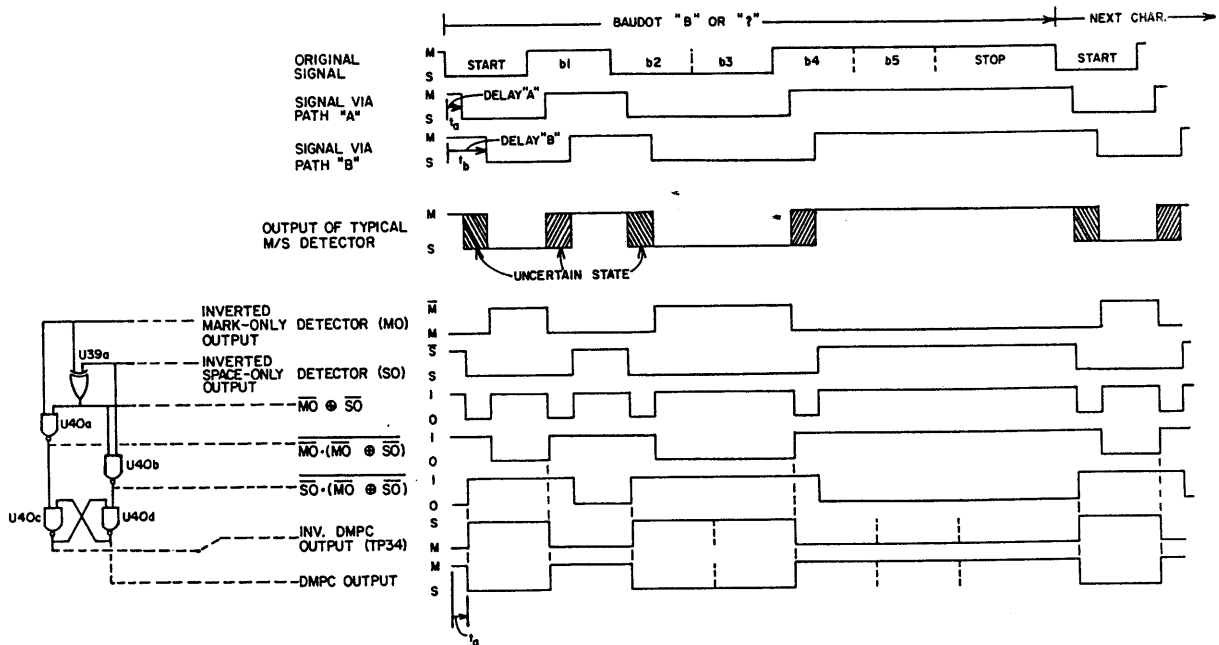
FIGURE 2.8 DMPC WAVEFORMS

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2.2.5.5 DETECTOR MODE SELECT [6.13, 6.14]:

The outputs of the 4 data detectors - MARK ONLY (MO), SPACE ONLY (SO), MARK/SPACE ATC (M/S), and DIGITAL MULTI-PATH CORRECTION (DMPC) - are selected under processor control by switch stage U38. A two-bit control line from the control board (J2-9 and J2-10) sets the detector selection. Either the front panel DETECTOR MODE switch or a REMOTE CONTROL command are used to select the desired detector output and AM or FM processing. The two controls are normally inter-locked so that MO and SO modes are only available in AM mode. However, if DIRECT CONTROL (DC) mode is used with REMOTE CONTROL commands, each switch may be set without inter-locking (see Chapter 3 of ST8000 OPERATOR'S MANUAL). The output polarity at TP34 is MARK = TTL logic high (>3.5 VDC) and SPACE = TTL logic low (< 0.45 VDC).

2.2.6 RX DATA CONTROL [6.15, 6.16]:

The outputs of several data and data control circuits are combined in the circuitry of Figure 6.16 to produce the data outputs to the TERMINAL DATA connector (J9). This circuitry includes selection of data polarity, Antispace, Print Squelch, Diversity data source, CRT trace ON/OFF, Printer Motor ON/OFF, and signals to drive various front panel indicators.

2.2.6.1 POLARITY, REGEN, ANTISPACE [6.15, 6.16]:

Stage U39b is used to provide front panel selection of data polarity. The front panel POLARITY switch controls BOTH receive and transmit data polarity to assure true transceive operation. If opposite receive/transmit polarities are required, this can be achieved by either programming different transmit and receive Mark/Space tones or by using RS232 for receive and MIL-188 or TTL I/O for transmit.

The receive data output of U39b is passed through the data Regeneration circuit on the CONTROL board (A2) via J2-4 and J2-2. NOTE: Jumper JP4 is used ONLY for test situations when the CONTROL board is NOT connected. This jumper should not be in place when the MODEM and CONTROL assemblies are connected together. The jumper pins do serve, however, as convenient test pins for REGEN data input/output.

The ANTISPACE circuit is enabled by the front panel ANTISPACE switch via J2-11. When enabled, the circuit tests for a long period of Space pulse condition (logic low at pin 7 of U49c). When the SPACE data condition persists for more than approximately 200 ms, the data output of U48a is forced to a continuous MARK condition (MARK-Hold). The ANTISPACE circuit has no effect when the front panel switch is OFF.

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2.2.6.2 PRINT SQUELCH and DIVERSITY CONTROL [6.15, 6.16]:

Receive data from the control board REGEN circuit is passed through inverter U48c and gate U48a. As discussed above, the output of U48a is controlled by the Antispace circuit. In addition, a PRINT/NOT-PRINT signal is derived from Squelch and Diversity signals to also force the output of U48a to MARK-Hold whenever a valid signal is not detected.

The outputs of the Print Squelch circuit (SQA and NOT-SQA) [6.13, 6.14] are combined with outputs from the Diversity and AGC Squelch circuit (to be described in section 2.2.7). The combinational logic of stages U49b, U49d, U49e, U59, and U60 produce outputs to drive PRINT/NOT-PRINT gate U48a and Diversity selection gate U58.

When a single ST8000 is used in a non-diversity system, the diversity circuit serves as a signal-strength squelch, driven by the ST8000 AGC voltage. In this case, BOTH the Print Squelch (NOT-SQA) and Local Signal (SIGA) must be asserted for a PRINT condition to be passed to gate U48a. This condition also sets diversity gate U58c to pass receive data from the internal ST8000 to the data I/O interface amplifiers. If EITHER Print or AGC Squelch conditions are not positive, a NOT-PRINT condition is passed to U48a and the data output of the ST8000 is placed in MARK-Hold.

When two ST8000's are connected for diversity and both are turned ON, the Print Squelch Signals from both demodulators are compared with the DIVERSITY/NOT-DIVERSITY and A/B signals to produce the desired PRINT/NOT-PRINT and A/B control signals. In this case, if A channel (this ST8000) is selected AND NOT-SQA is low, data is passed through U48a and "A" channel is selected in U58. If NOT-SQA is high, U48a is placed in MARK-Hold. If B channel (other ST8000) is selected and NOT-SQB is low, data from the other ST8000 is selected and passed to the data output.

Automatic PRINT SQUELCH control of data flow may be over-ridden by SEL-CAL control (J1-7) from the CONTROL board (A2). The SEL-CAL feature is programmed using the REMOTE CONTROL feature of the ST8000. Note that SEL-CAL control will force the ST8000 print data circuits ON, but that OFF control is logically OR'ed with the internal sensing circuits.

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2.2.6.3 RXD I/O INTERFACE [6.15, 6.16]:

Stages U57 and U39 are I/O amplifiers used to convert the +5V logic data signals to the required I/O levels. The output of U57a produces RS232-C compatible bipolar signals (J9-3). This signal is -7 VDC for MARK and +7 VDC for SPACE. U39d and U57b provide MIL-188C compatible data output at J9-10, with levels of +7 VDC (MARK) and -7 VDC (SPACE). Stage U39c provides a TTL-compatible output signal at J9-16. Since both MARK/SPACE polarities are commonly used in various TTL-based data systems, either polarity may be selected with jumper JP2. The normal (N) polarity of the TTL output is for MARK = CMOS high logic level (>3.5 V) and SPACE = CMOS low logic level (<1.5 V). The input to all three data output amplifiers is obtained from the RXD ECHO circuit [6.19, 6.20]. Normally, this is simply the output of diversity gate U58a.

Stage U57c also provides an RS232-C Carrier-Detect (CD) output to J9-8. This output is high (+7 VDC) when EITHER Print Squelch or AGC Squelch conditions are active. It is low (-7 VDC) when BOTH conditions are not met. A TTL NOT-CD signal is also available on J9-21. This signal is low whenever Print Squelch is affirmative and is NOT controlled by AGC squelch. This output gives a rapidly switched ON/OFF Carrier Detect signal, useful for ARQ, Packet, and other burst-transmission modes.

2.2.6.4 MOTOR CONTROL [6.15, 6.16]:

The ST8000 does not include a high-voltage loop or provision for direct control of the AC power to a printer motor. However, these features are provided by the LP1200 Loop Power Supply option. An output is provided on J9-12 that may be used to drive a relay to switch printer motor power. Stage U35d and Q3 provide a delayed open-collector switch for relay control. The collector of Q3 is in an ON state (low impedance to ground) when EITHER Print Squelch or AGC Squelch are affirmative. Approximately 18 seconds after BOTH Print Squelch and AGC Squelch fail, the output of Q3 turns OFF (high impedance to ground). Q3 may be used to switch a positive voltage (<+50 VDC) to ground (current <+100 ma). If two ST8000's are used in a diversity connection, the printer motor output will remain ON whenever a valid signal is present from the selected demodulator output (A or B).

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2.2.6.5 CRT TRACE CONTROL [6.15, 6.16]:

The trace of the CRT Tuning Indicator is automatically controlled to prevent "burning" of the phosphor when no signals or a continuous MARK signal is received. In addition, the trace is automatically restored for approximately 10 seconds whenever any front panel switch or tuning adjustment is changed. Stage U60c senses the receive data output and turns the CRT trace OFF (through gate U59b) whenever a MARK condition longer than approximately 10 seconds occurs. Since the input to U60c is derived after the Antispace circuit, a long SPACE condition will also turn-off the CRT if ANTISPACE is turned ON. The CRT trace is also turned OFF whenever PRINT SQUELCH is OFF (output of U60d). An output from the CONTROL board (J1-5) forces the CRT trace ON whenever ST8000 tuning controls or switches are changed or when commanded by the REMOTE CONTROL CRT-ON command. External grounding of J9-25 turns the CRT trace OFF, over-riding ALL internal CRT trace control states. Similarly, grounding of J9-18 forces the CRT trace ON, regardless of internal control states.

2.2.6.6 INDICATORS [6.15, 6.16]:

Four front panel indicators are driven by this circuitry (MARK, SPACE, LOS, and PRINT). The MARK lamp signal indicates the data state of the output of U48a and therefore shows the effect on the signal of the ANTISPACE and PRINT SQUELCH circuits. The SPACE lamp indicates the data status of the I/O amplifiers. The SPACE lamp condition therefore reflects the data state of the selected diversity channel (A or B) as well as the data obtained from the RX ECHO circuit.

The PRINT lamp is ON whenever valid signals are to be printed. The PRINT lamp is used to set the threshold level of the PRINT SQUELCH control. The LOS lamp will be ON only when both Print Squelch and AGC Squelch fail. The LOS lamp indication is the complement of the RS232-C CD output (J9-8).

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2.2.7 DIVERSITY AND AGC SQUELCH [6.17, 6.18]:

The AGC voltage output from U3b [6.4, 6.5] is used in both single-channel, non-diversity systems (one ST8000) and in two-channel diversity systems (two ST-8000's with Diversity cable). In a non-diversity system, the AGC voltage drives a signal-strength squelch circuit. When diversity is used, the AGC voltages of each demodulator are compared to determine channel selection.

NOTE: JP1 MUST be installed for a single-channel ST8000 to operate properly.

The AGC voltage from U3b [6.6] is connected through JP1 to isolation amplifier U36a. The output of U36a drives one end of the front panel DIVERSITY potentiometer. When a second ST8000 is connected for diversity combination, its AGC voltage is buffered and inverted by stage U36b and applied to the other end of the DIVERSITY potentiometer. The wiper of the potentiometer then drives comparator stages U46a and U45a (diversity) or U46b and U45b (non-diversity).

2.2.7.1 NON-DIVERSITY SQUELCH [6.17, 6.18]:

If a second ST8000 is not connected to J10, the DIVERSITY rear panel connector, or is connected AND turned OFF, the zero voltage from J10-9 is sensed by U47a, setting the output high (NOT-DIV at TP33). Q2 then turns ON and biases U36b to produce a constant negative voltage at TP35. The DIVERSITY potentiometer therefore becomes a level control for only the AGC voltage of the local ST8000 (AGC-A). Stages U46b and U45b then serve as an integrating threshold detector for the non-diversity condition. The switch threshold at TP23 is at approximately zero volts and is proportional to the difference between the AGC-A voltage and the negative bias at TP35. Therefore, adjustment of the DIVERSITY control changes the amount of AGC-A voltage required to produce a negative-to-positive transition at TP23. The switch time constant for signal/no-signal non-diversity operation is approximately 0.1 second for signal acquisition and 1.0 second for signal loss. U45b is a high-gain threshold detector and transistor U53b performs the required bipolar to TTL level conversion.

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2.2.7.2 DIVERSITY MODE [6.17, 6.18]:

When two ST8000's are connected for diversity AND both units are
turned ON, the presence of a positive voltage at AGC-B (J10-9)
sets U47a to the DIV state (TP33 to negative level).   This turns
Q2 OFF and allows U36b to act as an inverting buffer for the
AGC-B voltage.   Since the two AGC voltages are applied with
inverse polarities to either end of the DIVERSITY control, the
wiper setting is proportional to the voltage difference.   As in
the non-diversity case, the threshold point occurs when the
voltage at TP23 passes through zero volts. A negative voltage at
TP23 causes selection of channel B (other ST8000) and a positive
voltage corresponds to selection of the A channel.   Changing the
DIVERSITY control therefore sets the ratio of the two voltages
required to produce the zero-voltage switch condition.

Stages U46a and U45a are the integrating threshold detector for
diversity operation.   U46a and its diode bridge (D42-D45) form a
dual-gain amplifier. For input voltages less than +/- 0.2 volts,
the gain is low (approximately 1/3).   When the input voltage
exceeds these limits, the voltage gain is increased   to
approximately 5.   The output of U46a drives the bipolar
integrator R206/C72/C73 with a time constant of approximately 1
second.   If the difference between the A and B channel AGC
voltages at TP23 is high, the gain of U46a is also high and
C72/C73 are rapidly charged.   As the capacitor voltage passes
through zero volts, threshold detector U45a provides a rapid
channel switch.   If the difference between AGC voltages at TP23
is low, U46a gain is low and change in the C72/C73 capacitor
voltage is much slower.   This dual time-constant effect thus
prevents "chatter" or "hunting" effects of rapid back-and-furth
channel switching which might otherwise occur on two slowly
varying signals. However, if one signal undergoes a rapid change
(such as in a deep prolonged fade), the higher gain condition of
U46a takes over and the data is rapidly switched to the other
channel.   Stage U53a provides level conversion from bipolar to
TTL levels.   Gate U34 is driven by the two threshold detectors
and the DIV/NON-DIV output of U47a to provide the required A/B
channel switch signal for U58 [6.15, 6.16].

Front panel indicator A is ON whenever the local signal is
present and selected.   Indicator B will be ON only when DIV mode
is selected AND B channel is selected.   The B indicator will not
turn ON when a single channel (non-diversity) system is used.

2.2.8 TXD CONTROL, KOS, & ECHO [6.19, 6.20]:

This section of the ST8000 includes I/O interface drivers for RS232-C, MIL188C, or TTL data input, transmit-receive PTT control, receive and transmit data ECHO control, transmit data to the AFSK oscillator, and FSK output signals.

2.2.8.1 TXD I/O INTERFACE [6.19, 6.20]:

Transistors Q5 and Q6 and gates U54a and U54b provide I/O interface for three different data I/O electrical interfaces. RS232C TXD signals from J9-2 are sensed and converted to +5 volt logic levels by Q6. The required input signal levels are: SPACE >1.2 VDC, MARK< 0.6 VDC. The input signal may be either bipolar or positive within these limits. The MIL188C (J2-9) and TTL (J2-14) inputs have the same voltage limitations, but include an additional inversion. Note that ONLY one of the three possible inputs may be used at a time. The output of the TXD I/O circuits drives the REGEN circuit on the CONTROL circuit board (A2) through J1-1 and J1-2. Jumper JP3 is provided ONLY for test conditions when the MODEM and CONTROL boards are not connected. JP3 should be OMITTED whenever the two boards are connected.

2.2.8.2 TX/RX PTT CIRCUIT [6.19, 6.20]:

The ST8000 includes a relay that is used to switch the radio system from receive to transmit condition. This is normally accomplished by switching the transmitter push-to-talk (PTT) circuit to ground to transmit. The PTT relay may be controlled from several sources: (1) Front Panel PTT switch, (2) internal Keyboard Operated Switch (KOS) automatic circuit, (3) by an external switch to ground (TERMINAL KOS), and (4) by the RS232C RTS (Request To Send) signal.

The ST8000 Keyboard Operated Switch (KOS) circuit is made up of stages U63, U56a, and U64a. Automatic send-receive control is achieved by sensing the state of the input transmit data (TXD). When a Mark-to-Space transition is detected, U63a, U63b, U56a, and U64a produce a transmit ON condition. The ON condition continues until after an adjustable delay following the last data transition. This delay is controlled by timer stages U63e and U64a and is adjustable from 1-10 seconds with control R226 (factory set at minimum). The time delay may be increased to compensate for extended periods between TXD pulses, particularly when hand-typing data. A rapid return to receive, over-riding the delay, is available if the transmit data source is held in SPACE condition for longer than 0.5 second (U63c and U63d).

The front panel PTT switch and stages U56b and U64b allow selection of either receive only (RX), Keyboard Operated Switch (KOS), or continuous transmit (TX) conditions. The automatic KOS circuit may only be used when this switch is in KOS position.

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Two external control signals may also be used to set transmit mode, Terminal KOS and RS232C RTS. If the Terminal KOS (J9-19) input is grounded, the PTT relay is switched to TX-ON condition. When RTS input (J9-4) is driven to greater than +3 VDC, TX-ON condition is set. Both TERMINAL KOS and RTS inputs over-ride the RX or KOS positions of the PTT front panel switch. The TERMINAL KOS input is commonly used with the KOS and KY outputs of the DS3100 terminal to provide compatible transmit/receive switching.

The front panel TX lamp is ON whenever the ST8000 PTT relay is in TX condition. Option switch S4-5 also allows ON/OFF control of the AFSK tones by the PTT circuit. When this switch is ON (factory setting), AFSK tone output is produced only when the ST8000 is in TX state. If S4-5 is set OFF, the AFSK tone output is always ON, regardless of ST8000 PTT state.

2.2.8.3 ECHO CONTROL [6.19, 6.20]

Gates U54c, U54d and U55 allow selection of data sources to drive both the AFSK tone generator, FSK Output, and RXD output to the data terminal. Option switch S3-1 through S3-5 allows choice of normal full- and half-duplex options. The S3 Factory setting is: S3-1 and S3-5 ON, S3-2, S3-3, and S3-4 OFF. This is the recommended setting for a full-duplex (FDX) system such as the DS3100 terminal. Note that BOTH S3-1 and S3-2 should NOT be set ON at the same time. Similarly, only one of the S3-3, S3-4, and S3-5 switch sections may be set ON at a given time.

2.2.8.4 AFSK AND FSK DATA OUTPUT [6.19, 6.20]:

Transmit data output from the echo circuit is set to either polarity by the front panel switch and stage U62a. This polarity is matched to that of the receive data as discussed in section 2.2.6. The output signal is used to drive the AFSK Mark/Space switch on the control board through J1-11.

The transmit data output also drives the FSK output circuit of stages U62b and Q7. Option switch S4-1 through S4-4 allows choice of the level and polarity of the FSK output signal. The S4 Factory setting is S4-2 and S4-3 ON, producing a +5 VDC output on MARK and 0 volts on SPACE transmit data conditions.

2.2.9 AFSK OSCILLATOR [6.21, 6.22]:

The setting of MARK and SPACE transmit tone frequencies is
controlled by the synthesizer on the CONTROL board (J2-6). The
synthesized signal at 10 times the output frequency drives U61, a
ten-step sine-wave synthesizer. The resulting stepped-waveform
is filtered and smoothed in amplifier/low-pass filter stages U65a
and U65b. Rear panel control R295 sets the output level of the
AFSK tone signal. Transformer T2 and option switch S2 allow
setting of two AFSK levels and choice of balanced or unbalanced
output. Switch S2-5 also allows connection of the FSK rather
than AFSK signal to the rear panel XMTR connector (J11a). The
PTT relay is also connected to J11a. The factory setting for S4
is for 600 ohms, unbalanced with the level set for 0 dBm (S4-1,
S4-2, and S4-4 ON; S4-3 and S4-5 OFF). If FSK output is desired,
set S4-1, S4-4, and S4-5 ON and S4-2 and S4-3 OFF.

2.2.10 POWER SUPPLY [6.23, 6.24]:

With the exception of the high voltages and filament voltage for
the CRT, all other operating voltages for the ST8000 are obtained
from the modem board power supplies. The ST8000 uses +8 VDC (+V)
and -8 VDC (-V) for all analog circuitry and +5 VDC for all
digital and display circuits. Standard three-terminal integrated
circuit regulators are used for all three supply voltages. The
+8 and -8 volt regulators (U67 and U66) are mounted on the MODEM
board and bolted to the rear panel for heat conduction. The +5
volt regulator (LM323) is part of assembly A5-REG (960-08309),
mounted directly to its heat sink on the rear panel.

All operating voltages, including those for the CRT are obtained
from the power transformer mounted in the left rear section of
the cabinet. The transformer primary may be connected for either
100-130 VAC or 200-260 VAC power line input. Power line
frequencies between 44 and 440 Hz may be used. Both sides of the
AC power input are filtered to prevent RFI to or from the ST8000.
Both power wires are switched by the AC POWER switch on the
ST8000 front panel.

2.2.11 MODEM ASSEMBLY INTERCONNECTIONS [6.25, 6.26]:

All interconnections between the MODEM assembly (A1) and other
assemblies or external connectors are shown in Figure 6.26. The
connector numbers correspond to those on the schematic diagrams
and on the screened markings on the circuit board itself. In
addition, page references are given to the corresponding
schematic diagram title-block page for each signal. Arrows on
the signal lines indicate the predominate direction of signal
flow with respect to the connector on the MODEM board.

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2.3 CONTROL ASSEMBLY (A2) [6.27 - 6.46]:

The ST-8000 Control Board is a Z80A (or equivalent) based microprocessor system with 16K bytes of firmware EPROM memory and 2K bytes of battery backed up RAM memory. This processor controller polls the front panel switches and tuner and tests for changes, refreshes the front panel seven segment LED displays, generates the Modem Board filter oscillators, and sets various internal operational latch bits. In addition, all serial control port communication and terminal serial transmit and receive data regeneration is controlled by the Control Board microprocessor system.

In the following sections detailed descriptions of the Control Board circuitry are presented. References are made to the schematic diagrams located in Volume II of this Technical Manual; having that volume handy will aid understanding.

2.3.1 Microprocessor Controller [6.27, 6.28]:

The ST-8000 Control Board uses a conventional dedicated single microprocessor design architecture with 16K bytes EPROM and 2K bytes of RAM memory (see Figure 6.28). The Z80A microprocessor uses a 2.4576 MHz clock (PCLK) derived from the 4.9152 MHz common system clock illustrated in Figure 6.34 for a cycle time of 407 ns. The Control Board uses both memory mapped and IO port mapped buffers and latches as shall be discussed in subsequent sections. The microprocessor operates with no wait states.

The Z80A has two interrupt sources: the serial channel controller (INT) and the refresh timer (NMI) illustrated in Figure 6.32. The RESET signal is generated by a "deadman" timer and power on circuit illustrated in Figure 6.30.

Note the 10K pullup resistors on U23-16, -21, and -22, in Figure 6.28. These resistors hold the -WR (NOT-WR signal) and -RD (NOT-RD) lines high when the processor is in the RESET or power on condition where these lines may be in the high impedance tri-state condition. Without the pullup resistors, a -WR signal might cause a false memory write signal into the battery backup RAM parameters corrupting stored data.

Two pullup resistors are included on the -BUSREQ and -WAIT inputs to hold these inputs high. Since all components on the processor board operate full speed, there is no need for a processor wait signal. -BUSREQ is used only in DMA or multi-processor application, thus that input is held high in the ST-8000.

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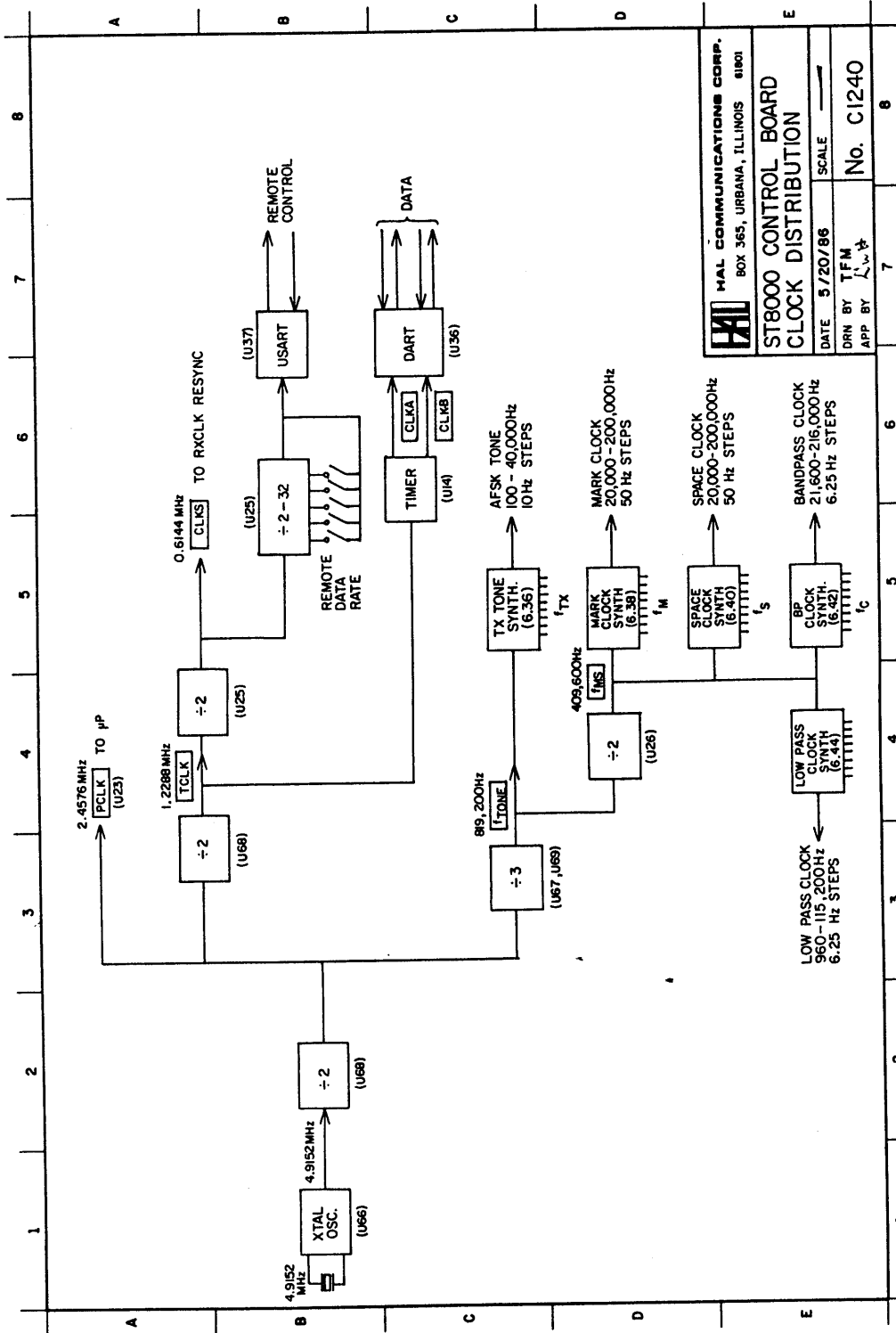
Figure 2.9 Clock Distribution

2.3.2 System Clocks [6.33, 6.34]:

The entire Control Board operates with a single crystal clock as
shown in Figure 2.9, a block diagram of the clock distribution in
the ST-8000.   Since all timing signals are based on the same
crystal oscillator, all clocks remain as stable as the crystal
reference.

As illustrated Figure 6.34, two sections of U66 form a 4.9152 MHz
crystal oscillator with a buffered output on U66-8.   A D-type
flip-flop, U68, divides this clock output by 2 to produce PCLK, a
50% duty cycle square wave 2.4576 MHz (406.9 ns) processor clock
and synthesizer reference clock.

The processor clock, PCLK, is buffered once again by U49 in
Figure 6.28 since the clock input to the Z80A requires a 330 ohm
pullup resistor to +5 volts.   This same clock output from U49-2
provides the system timing clock for the regeneration dual serial
receiver/transmitter (DART) chip, U36-20, in Figure 6.32.

The frequency synthesizers require two reference timing clocks;
FTONE at 819,200 Hz (1.22 us) and FMS at 409,600 Hz (2.44 us).
PCLK is divided by 3 with the dual D flip-flop U67 and one gate
from U69.   U67-5 and U67-9 form a 2 bit ripple counter triggered
by the rising edge of PCLK on U67-3.   When the count reaches 3,
both U67-5 and U67-9 are high, U69-11 goes low resetting the
count to 0. Thus, U67-9 has a period of three cycles of PCLK and
a frequency of 819,200 Hz.   FTONE is not a 50% duty cycle
waveform; it is low for two cycles (813.8 ns) and high for one
cycle (406.9 ns) of PCLK.

The FMS timing signal is generated by dividing FTONE by 2.   U26,
a D flip-flop, uses FTONE as an input on U26-11 and generates the
409,600 Hz (2.44 us) timing signal on U26-9.   FMS is a 50% duty
cycle waveform.

2.3.3 RESET and Sanity Timer [6.29, 6.30]:

The RESET and Sanity Timer circuit is found in Figure 6.30.   The
sanity timer is used to reset the ST-8000 processor when an
operational glitch has occurred.

When the power is first turned ON, capacitor C26 is fully
discharged so the voltage across the capacitor is close to 0
volts.   With U71-11,12 low, the output of the invertor on U71-13
will be high which holds the four bit decade counter U70 output
set to 9.   The high level inputs on U71-5,6 drive U71-4 low which
holds the -RESET (U71-4) line low, and RESET (U71-1) high.   As
long as the -RESET line is low, the Z80A microprocessor is held
in the reset state.

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As soon as C26 charges to about 2.4 volts through R7, U71-13 will
go low releasing the set to 9 input on U70. U69, an astable
multivibrator oscillator, generates a timing clock input for the
decade counter on U70-10. Once U71-13 goes low, the counter will
begin to count up on the next falling edge of U69-3. This next
clock edge will increment the counter to a count of 0 so that
both U71-5 and U71-6 are low resulting in U71-4 going high and
U71-1 low. Thus, -RESET goes high and RESET goes low allowing
the microprocessor to start.

During operation, the firmware periodically writes the memory
address E007H to reset the decade counter to zero. A write to
that location pulses U2-7 low and U71-10 high, resetting the U70
counter (DEADT). Since the U69 timer continues to run, U70 will
keep trying to count up. If the DEADT signal does not pulse low
before counter U70 reaches a count of 8, U70-8 will go high which
causes U71-4 to go low resulting in a processor reset signal.

The frequency of U69-3 is not critical; the components shown
yield a frequency of about 60 Hz (17 ms). When the ST-8000 is
idle and no front panel switches are changed, the DEADT counter
reset signal has a frequency of about 2240 Hz (446 us). Note,
however, that the period of this waveform is dependent on what
specific tasks the processor is performing at the time and it
will vary greatly. In no case should the U70 counter cause a
system reset unless a glitch has occurred.

2.3.4 Memory and I/O Map [6.27 - 6.30]:

The control board uses both memory and I/O port mapping for the
system memory, control bits, and peripheral interface devices.
Listed below are the board addresses and the specific function
associated with each address.

Memory addresses are decoded by U3, U4, and U24. I/O port
addresses are decoded by U9. All addresses below are in HEX.

                    MEMORY ADDRESS MAP

        ADDRESS   DESCRIPTION
        -------------   --
        0000H - 1FFFH   U10; 2764 firmware EPROM 0, read only
        2000H - 3FFFH   U11; 2764 firmware EPROM 1, read only
        4000H - 5FFFH   U12; (not installed)
        6000H - 6800H   U13; 2K x 8 battery RAM, read/write
        8000H - 8007H   U3; Synthesizer control (see below)
        A000H - A007H   U4; Synthesizer control (see below)
        E000H - E007H   U2; Sanity Timer and Modem Latch (see below)

MEMORY MAPPED CONTROL REGISTERS

ADDRESS	DESCRIPTION
8000H	U3-15; MARK transmit tone, low byte
8002H	U3-13; SPACE transmit tone, low byte
8003H	U3-12; MARK/SPACE transmit tone, high nibbles
8004H	U3-11; MARK filter synthesizer, low byte
8006H	U3-9; SPACE filter synthesizer, low byte
8007H	U3-7; MARK/SPACE filter synth., high nibbles
A000H	U4-15; Band pass filter synthesizer, low byte
A001H	U4-14; Band pass filter synthesizer, high byte
A002H	U4-13; Low pass filter synthesizer, low byte
A003H	U4-12; Low pass filter synthesizer, high byte
A004H	U4-11; Front panel, Baud Rate digits (DS2)
A044H	U4-11; Front panel, MARK digits (DS0)
A005H	U4-10; Front panel, Common Cathode select (DS3)
A045H	U4-10; Front panel, SPACE digits (DS1)
A006H	U4-9; MARK/SPACE filter Q select low nibbles
A007H	U4-7; Modem control register
E000H	U2-15; Modem board options
E007H	U2-7; Sanity timer

I/O PORT ADDRESS MAP

ADDRESS	DESCRIPTION
00H	U9-12; Front panel switch input 0
04H	U9-13; Front panel switch input 1
08H	U9-14; Front panel switch input 2
0CH	U9-15; Front panel switch input 3
10H	U9-11; Refresh timer enable latch
14H-17H	U9-10; Baud rate and refresh timer
18H-1BH	U9-9; Regeneration serial controller
1CH-1DH	U9-7; Command port serial controller

2.3.5 EPROM and RAM Memory [6.27, 6.28]

The ST-8000 memory address map is presented below:

                      MEMORY ADDRESS MAP

        ADDRESS   DESCRIPTION
        -------------   --
        0000H - 1FFFH   U10; 2764 firmware EPROM 0, read only
        2000H - 3FFFH   U11; 2764 firmware EPROM 1, read only
        4000H - 5FFFh   U12; (not installed)
        6000H - 6800H   U13; 2K x 8 battery RAM, read/write

Figure 6.28 illustrates the firmware and RAM memory components.
U10 and U11 use industry standard 2764 8K x 8 450 ns access time
EPROM's for firmware storage. -ROM0 and -ROM1 enable signals are
decoded from address bits A15, A14, and A13 by U24.   Note that
the -MRQ signal on U24-5 enables the address decoder only during
memory accesses, not during I/O port access cycles.   ROM0 is
enabled for any address between 0000H and 1FFFH or the first 8K
address locations. ROM1 is enabled between 2000H and 3FFFH. The
processor read signal -RD is connected directly to the output
enable inputs on ROM0 and ROM1 pin 22.   A byte of data is gated
to the data bus when one of the EPROM chip select inputs is low
and -RD goes low for a program instruction fetch.

The ST-8000 is capable of addressing two 2K x 8 bit RAM chips at
U12 and U13.   In the current product, only U13 is installed, and
a device is employed that has an internal battery backup.   As
with the firmware memory, the chip select -RAM1 is enabled for
memory read and write operations between address 6000H and 7FFFH
although only 6000H to 67FFH is used presently. No special input
signals are needed to handle the battery backup operation since
it takes over automatically when the +5 volts on pin 24 falls
below 4.5 volts.

2.3.6 Modem Board Latched Interface Bits [6.29, 6.30]:

               MEMORY MAPPED CONTROL REGISTERS

        ADDRESS   DESCRIPTION
        -------   --
        A006H   U4-9, U18-11; MARK SPACE filter Q select
        A007H   U4-7, U22-11; Modem control register

        E000H   U2-15, U1-11; Modem board options

Several static control signals on the modem board are set by the control board processor to select various filter and operational modes. For example, these bits select the type of input filter used, what detector mode is optioned, and the filter Q settings. Each set of control bits are set based on front panel switch settings, the MARK and SPACE tones, and the data rate. Three latches in Figure 6.30 set these operational bits: U1, U18, and U22.

2.3.6.1 MARK/SPACE Filter Q Select bits [6.29, 6.30]:

The Q's of the input and bandpass filters on the modem board are selected with control bits latched on the control board. The MARK and SPACE bandpass filters each require 5 bits while the input band pass filter uses 2. Summarized below are the control bit locations for each filter.

                  MARK/SPACE BANDPASS FILTER Q

        PIN   DESCRIPTION
        ------   --
        U18-9   MARK Filter Q Bit 0 to J1-15 (inverted)
        U18-5   MARK Filter Q Bit 1 to J1-13 (inverted)
        U18-16   MARK Filter Q Bit 2 to J1-17 (inverted)
        U18-12   MARK Filter Q Bit 3 to J1-19 (inverted)
        U22-19   MARK Filter Q Bit 4 to J1-20

        U18-6   SPACE Filter Q Bit 0 to J2-18 (inverted)
        U18-2   SPACE Filter Q Bit 1 to J2-16 (inverted)
        U18-19   SPACE Filter Q Bit 2 to J2-14 (inverted)
        U18-15   SPACE Filter Q Bit 3 to J2-12 (inverted)
        U22-2   SPACE Filter Q Bit 4 to J1-6

Bits 0 to 3 of the MARK and SPACE filter Q inputs are inverted sense signals where the all 1's condition selects the lowest Q value and all 0's selects the highest value. A total of 16 Q steps in each of two ranges selected by bit 4. The low range is enabled when bit 4 is logic 0, and the high range is enabled with bit 4 set to logic 1. A summary of available values is presented in the Figure 6.8 and 6.10 tables.

The MARK Q latched bits drive selection circuitry shown in Figure 6.8 and the SPACE Q bits are presented in Figure 6.10. A calculation is performed in the firmware to set the Q values to the proper setting for every combination of MARK/SPACE frequencies and data rate. As these parameters change, the Q values will change accordingly.

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2.3.6.2 CRT Control [6.29, 6.30]:

                        CRT CONTROL BIT

     PIN   DESCRIPTION
     ------   ---
     U22-6   CRT Control Bit to J1-5

The CRT control bit may be used to force the tuning scope output
to the ON condition under firmware control.   The tuning scope is
enabled for about 10 seconds each time a front panel control is
changed. A TTL logic 1 on this latched bit will enable the trace
control in Figure 6.16 forcing the CRT trace ON.   A TTL logic 0
on this bit is ignored.

2.3.6.3 Regeneration Control Bit [6.29 - 6.32]:

                   REGENERATION CONTROL BIT

     PIN   DESCRIPTION
     ------   ---
     U22-12   RXRGEN Control bit

In any of the regeneration modes, the serial data path between
the modem board and the serial data terminal is interrupted by
the DART U36 shown in Figure 6.32.   When RXGEN is TTL logic 1
(REGEN OFF), U50-1 selects a bypass mode whereby serial data from
the terminal on U50-3 is connected directly to U50-4 then J1-2
and the modem board transmit signal TXD.   In addition, serial
data from the modem on RXD, U50-6, is connected directly to U50-7
and J2-2 for the RXD signal to the terminal connected to the main
board.   When the regeneration function is OFF, U36 takes no
active part in the serial data path.

When regeneration is enabled, RXRGEN and U50-1 is logic 0.   In
this mode, serial data from the attached data terminal is read
from U36-12 at the terminal data rate, but the output to the
modem board is through U36-26 at the modem data rate.   Serial
data from U36-26 is connected to U50-2 and U50-4 which is TXD to
the modem board through J1-2.   Receive data from the modem is
received by U36-28 at the modem data rate, and passed to the data
terminal by U36-15 at the terminal data rate.   U50 connects the
receive data output on U50-4 to U50-7 and the RXD signal to the
modem board on J2-2.

2.3.6.4 Normal and Reverse Control Bit [6.29, 6.30]:

NORMAL/REVERSE CONTROL BIT

PIN	DESCRIPTION
U22-16	NORM/REV to J2-15

The NORMAL/REVERSE control bit is used to set the sense of the
serial input and output data. When NORM/REV is logic 0, a MARK
input on the data terminal will transmit the MARK tone and a MARK
tone input to the modem will produce a MARK condition on the
serial RXD output. This is NORMAL mode.

In REVERSE mode, the operation of the MARK and SPACE tones are
exchanged. Thus, a MARK input on the TXD line will produce a
SPACE tone and the SPACE tone input will generate a MARK output
signal on RXD.

The NORM/REV signal is found on Figure 6.16 for the modem board.

2.3.6.5 Input Filter Bandwidth [6.29, 6.30]:

INPUT FILTER BANDWIDTH

PIN	DESCRIPTION
U22-9	INPUT Filter bit A to J2-20
U22-5	INPUT Filter bit B to J2-19

One of four different input filter bandwidths is selected with
the A/B signals from U22. A table in Figure 6.4, where these
signals terminate, summarizes the four available options. 00 is
the most narrow filter while 11 is the widest.

2.3.6.6 Selective Call Control Bit [6.29, 6.30]:

SELECTIVE CALL CONTROL BIT

PIN	DESCRIPTION
U1-16	SEL-CAL to J1-7

The operation of the SEL-CAL bit is similar to the CRT control
bit in that this control bit will force the printer motor control
ON but cannot keep it off. When this signal is 1, the ST-8000
motor control output shown on Figure 6.16 will be enabled. If
SEL-CAL is TTL logic 0, this control signal is ignored.

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Using ST-8000 Remote Control commands, a user may optionally load
a selective call string that will activate this signal whenever
that string of characters is received by the modem board.   This
motor control signal is set to logic 0 when the programmed SEL-
CAL OFF string (default = "NNNN") is received by the modem board
or if the ST-8000 power is cycled.

2.3.6.7 Detector Mode Control [6.29, 6.30]:

DETECTOR MODE CONTROL

PIN	DESCRIPTION
U1-12	AM/FM mode control bit to J2-7
U1-9	Detector mode B bit to J2-9
U1-5	Detector mode A bit to J2-10

The input limiter on the modem board is controlled by the AM/FM
mode control bit.   In the FM mode, AM/FM is TTL logic 0, a hard
limiter is optioned between the input bandpass filter and the
discriminator. The AGC circuit is selected when this control bit
is set to logic 1 for AM mode.   The AM/FM signal is set under
firmware control based on the option selected by the front panel
switch.   AM/FM terminates in Figure 6.6 at the AM/FM selection
logic gates.

The ST-8000 permits four different detector modes; MARK only,
SPACE only, MARK/SPACE, and Digital Multi-path correction. Bits
B and A select the modem board detector mode by driving a
selection gate illustrated in Figure 6.14.   A table in that same
figure summarizes the mode settings.   A and B are set by the
firmware based on the front panel switch setting.

2.3.6.8 Antispace [6.29, 6.30]:

ANTISPACE CONTROL BIT

PIN	DESCRIPTION
U1-19	Antispace control bit to J2-11

The Antispace control is used to force the terminal output to a
MARK state after a long spacing period on the modem input.   To
enable the antispace feature, ANTISPACE is set to TTL logic 1; to
disable, it is set to logic 0. The antispace circuitry is found
on Figure 6.16 in the modem section.   The firmware controls this
signal directly based on the front panel switch setting.

2.3.6.9 Push to Talk Mode Control   [6.29, 6.30]:

                    PUSH TO TALK CONTROL

        PIN   DESCRIPTION
        ------   ---
        U1-15   PTT mode bit B to J2-8
        U1-6   PTT mode bit A to J2-13

The PTT transmitter control on the modem board may be optioned
for one of three modes using the PTT A and B bits. The PTT relay
is located in Figure 6.20. A table in that same figure
summarizes the available operational modes. The states of the
PTT A/B bits is set under firmware control based on the three
position front panel selection switch.

2.3.6.10 CTS Control Bit [6.29, 6.30]:

                    CTS CONTROL OUTPUT

        PIN   DESCRIPTION
        ------   --
        U1-2   CTS Control bit to J1-12 via U65

The CTS control bit directly controls the CTS output on the
serial terminal RS-232C port through the line driver output shown
in Figure 6.30 on pin U65-8. Typically, this control signal is
logic 0 so that the actual RS-232C output level will be HIGH or
ON. If regeneration is selected and there is either code or data
rate conversion optioned, a means of flow control is needed to
temporarily halt the serial input data when the internal buffers
begin to fill. The firmware monitors the buffer level, and will
turn the CTS control bit to logic 1 forcing the CTS output to LOW
or OFF to stop the attached terminal transmission of serial data.
CTS is set HIGH or ON when regeneration is turned OFF.

2.3.7 Regeneration and Control Port Controllers 6.31, 6.32]:

SERIAL CONTROL REGISTERS

ADDRESS	DESCRIPTION
14H	U14-11; CLKA control register
15H	U14-11; CLKB control register
16H	U14-11; NMI control register
17H	U14-11; Mode control register
18H	U36-35; Regen Channel A data
19H	U36-35; Regen Channel A control
1AH	U36-35; Regen Channel B data
1BH	U36-35; Regen Channel B control
1CH	U37-11; Control Port data
1DH	U37-11; Control Port control

Figure 6.32 illustrates the DART, U36, used for the regeneration modes and the USART, U37, connected to the control port. The timer, U14, generates the serial data clocks for U36, while the 8 bit counter U25 produces a clock for the control port serial controller U37. SW1 selects the control port data rate by connecting one of the counter outputs to the clock input on U37. Note that all of the asynchronous clocks operate at 16 times the actual data rate.

The regeneration DART U36 is active only when the ST-8000 is operating in regeneration mode and RXRGEN is logic 0. In regeneration mode, serial data from the terminal on TXD is loaded on channel A of the DART at the data rate set by CLKA for processing by the microprocessor controller. The actual serial data passed to the modem board for TXD is transmitted from the channel B side of the DART running at the CLKB rate. In a similar fashion, serial data from the modem board on RXD is read by the channel B side of the DART and passed to the terminal from the channel A TXA output on U36-15.

The regeration DART device operates in an interrupt driven mode where receive characters on channel A or B cause the INT output on U36-5 to go to logic 0. The microprocessor controller firmware operates in interrupt mode 2 (IM2) which is a vectored interrupt mode permitting more efficient response to the received character. Both TXA and TXB are polled for output, rather than interrupt driven.

The Remote Control port is connected through RS-232C line driver U65 and line receiver U64 to the U37 serial controller. As is the case with the regeneration controller, the control port USART is interrupt driven for incoming serial data. The receiver ready signal, U37-14, is connected to the CTSA input signal on U36 so that any change on that signal will generate an interrupt. Since

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this is the only control signal input connected on U36, that
vector location is used to read the serial data and process the
character. Any serial data that must be transmitted by the
control port is handled by polling the internal transmitter ready
status bit.

The clock for the control port is generated by U25, an 8 bit
binary counter. Exactly one position of SW1 must be closed for
the serial port to operate properly.

NMI on U14-10 is a square wave signal used to initiate a front
panel display refresh cycle. It has a frequency of approximately
250 Hz (4 ms). The NMI signal is gated by the input on U14-16, a
latched bit from U26-5. During power up, this input is held LOW
so that the NMI clock is disabled. Once all of the refresh
routines are loaded, the NMI clock is enabled by a write to U26
forcing the G2 input on U14 HIGH. The ST-8000 firmware never
disables the NMI clock; only the RESET signal on U26-1 will turn
off the refresh clock.

2.3.8 Synchronous Data Clocks [6.33, 6.34]:

Figure 6.34 illustrates the receive data clock RXCLK recovery
circuit for serial data received by the modem board. Basically,
this circuit synchronizes an internal clock to edges in the
serial receive data from the modem card.

The system clock, CLKS, moves the receive data through a 2 bit
shift register, U51, to locate serial data changes. The output
of the XOR gate U55-8 is forced to logic 1 each time U51-5 and
U51-9 differ, indicating a transition in the receive data. Since
U55-8 is connected to the reset input on U72, a 4 bit binary
counter, the output on U72-8 is reset to logic 0 on each data bit
transition. U72-8 will change from logic 0 to 1 on the 8th
falling edge of CLKB, the 16 times modem data rate clock. This
output will change at near the middle of the receive data bit,
where the transition on the RXCLK output clock should occur.
Thus, the internal clock is synchronized with the serial data
stream every time a data transition occurs. The only time that
the clock recover circuit will operate properly is when the
internal modem data rate clock has been set to the received
serial data rate. Unpredictable results occur if the CLKB signal
is not correct. In cases where the alternate phase of the RXCLK
is required, a jumper at J6 is provided to select the NORM or INV
clock sense.

The synchronous transmit clock is generated by the other half of
U72 by simply dividing the CLKA signal by 16. The output on U6-6
is converted to RS-232C levels by U65-6. Since the serial
transmit clock may use a local clock reference, there is no
correlation between the transmit clock and the recovered receive
data clock.

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2.3.9   MARK/SPACE Tone Generator   [6.35, 6.36]:

The MARK/SPACE transmit tone generator illustrated in Figure 6.36
is a 13 bit full adder operating as a digital signal synthesizer
with the output frequency set to 10 times the desired transmit
tone.   Two sets of latches store the constants for the MARK and
SPACE tones.   A single control signal, AFSK TXD, selects which
tone frequency is passed to the AFSK TONE output for the modem
board.

This digital synthesizer is a 13 bit full adder implemented with
three 4 bit full adders, U38, U39, and U40, and an XOR from U55
to handle the carry output.   On each rising edge of FTONE, the
current 13 bit sum is latched into U52 and U53.   These latched
outputs are then added to the tone constant stored in either the
MARK or SPACE tone latch depending on the state of AFSK TXD.
When this signal is a logic 1, the MARK latch U16 and part of U15
are selected by U27, U28, and U29.   If this signal is logic 0,
the SPACE latch U17 and part of U15 are selected.   The constant
value is summed with the previous sum latches in U52 and U53 to
form a new sum to be latched on the next rising edge of FTONE.
The cycle is complete.   Each falling edge on U53-12 increments
the decade counter U54 by one, thus the output of the synthesizer
at U53-12 has a nominal frequency of 100 times the desired tone
frequency.   Figure   2.10 summarizes the digital frequency
synthesizer operation.

The digital synthesizers generate their output frequency through
addition.   The frequency is determined by the magnitude of the
constant loaded into the input latches and the clock frequency
driving the adder.   For example, if a constant 001 hex is loaded
into the MARK latch, and AFSK TXD is logic 1, then the sum at the
output of latches U38, U39, and U40 will be incremented by 1 on
each rising edge of the 819,200 Hz FTONE clock.   After only 4096
rising edges, the U53-12 output will go to TTL logic 1, and the
total count to 4096 requires 1/200 second.   After another 4096
rising edges on FTONE, U53-12 will go to logic 0.   Thus, the
period of the waveform at U53-12, assuming an input constant of
001 hex, is 1/100 second or the frequency is 100 Hz.   When U54
divides this output by 10, the resulting waveform at U54-9 has a
frequency of 10 Hz.   If a constant value of 002 hex is loaded
rather than 001, the resulting waveform at U54-9 has a frequency
of 20 Hz.   Using this circuit, we can generate any waveform
frequency in 10 Hz steps starting with 10 Hz.   This output
frequency is again divided by 10 in the sine wave synthesizer
(Figure 6.22).   Thus the AFSK output frequency mau be set in
increments of 1.0 Hz.

Figure 2.10 Synthesizer Operation

For very long counts, or when the constant is an exact divisor of 4096, the output waveform will be a 50% duty cycle square wave. However, if the constant is not an integer divisor, the individual period of each cycle will vary depending on the relationship between the constant and FTONE. Any jitter on this clock will be visible on an oscilloscope connected to U53-12, but by the time this output is divided by 10 then 10 again in the tone output sine wave synthesizer, the jitter causes no problems. A counter connected to U54-6 or J2-6 will read a value equal to 10 times the constant loaded in either the MARK or SPACE input register, depending on which is active.

During operation, the MARK/SPACE synthesizer generates tones between 40,000 Hz and 400,000 Hz at U54-9 which produce ST-8000 transmit tones between 400 and 4000 Hz. For each tone generated by the ST-8000, the constant loaded into the MARK or SPACE latch is the output tone in Hertz expressed as a hex number.

            MARK TONE CONSTANT = MARK TONE FREQUENCY (Hz)
            SPACE TONE CONSTANT = SPACE TONE FREQUENCY (Hz)

For example, 1000 Hz output tone is produced by a 3E8 hex constant. The lowest output tone constant is 190 hex (400 Hz) and the highest is FA0 hex (4000 Hz). Note that the frequency at U54-9 or J2-6 is 10 times the output tone, and U53-12 is 100 times the output tone frequency.

The AFSK TXD signal on J1-11 originates on Figure 6.20 while the AFSK TONE output on J2-6 drives the AFSK output tone sine wave synthesizer illustrated in Figure 6.22.

2.3.10 MARK Filter Synthesizer [6.37, 6.38]:

Figure 6.38 illustrates the digital synthesizer that produces the clock used to set the center frequency of the MARK band pass filter on the modem board. The operation of this synthesizer is identical to the transmit tone synthesizer described in section 2.3.9 except that it has a single latched input constant, there is no output divider, and the state clock FMS is 409,600 Hz.

The input latches U21 and part of U19 hold the constant for the full adders U33, U34, and U35. On each FMS rising edge, the previous sum is latched into U43 and U44. The output is taken from U43-12 which goes via J1-18 to the modem board and the switched capacitor filter (SCF) in Figure 6.8.

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In the ST-8000 the switched capacitor MARK and SPACE filters require a 50 times clock to set the center frequency of the filter. The MARK filter synthesizer provides an output clock with a frequency of between 20,000 Hz and 200,000 Hz in 50 Hz increments. For a given MARK filter center frequency, that frequency, expressed as a hex constant, is loaded in the constant latches.

        MARK FILTER CONSTANT = MARK FREQUENCY (Hz)

As the MARK frequency for the ST-8000 demodulator is tuned, the constant loaded in U19 and U21 varies from a low of 190 hex (400 Hz) to FA0 hex (4000 Hz). This output waveform may have a noticeable amount of jitter at the upper end of this tuning range, but has a minimal effect on the filter performance due to the divide by 50 nature of the SCF filter.

2.3.11 SPACE Filter Synthesizer [6.39, 6.40]:

Figure 6.40 illustrates the SPACE filter synthesizer. The input latches U20 and part of U19 hold the constant for full adders U30, U31, and U32. The state sums are latches in U41 and U41 on the rising edge of the FMS state clock. The synthesizer output, running at 50 times the SPACE demodulator frequency, originates at U41-12 and passes via J2-5 to the modem board SCF in Figure 6.10.

The SPACE filter synthesizer is identical in operation to the MARK oscillator described in Section 2.3.10.

        SPACE FILTER CONSTANT = SPACE FREQUENCY (Hz)

The output frequency varies between 20,000 Hz and 200,000 Hz as the SPACE center frequency moves between 400 Hz and 4000 Hz.

2.3.12 BAND PASS Filter Synthesizer [6.41, 6.42]:

The Band pass filter synthesizer, shown in Figure 6.42, sets the center frequency for the SCF input filter shown in Figure 6.4. This synthesizer operates in the same manner as the ones previously described except that the adder resolution is increased from 13 to 16 bits. The constant is latched in U59 and U60 for the adders U57, U58, U61, and U62. Each state clock sum is latched in U56 and U63; the output is connected to U56-12 via J2-1 to the band pass SCF in Figure 6.4.

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The band pass filter requires a clock set to 54 times the center frequency. This synthesizer generates clock frequencies between 21,600 Hz and 216,000 Hz in 6.25 Hz steps. At each center frequency, the constant loaded in the latches is calculated with the following equation:

        BAND PASS FILTER CONSTANT = [54 x CENTER FREQ] / 6.25

Thus, a 1000 Hz center frequency uses a latched constant value of 21C0 hex. This contant will vary between D80 hex for 400 Hz and 8700 hex for 4000 Hz.

2.3.13 LOW PASS Filter Synthesizer [6.43, 6.44]:

Figure 6.44 illustrates the low pass filter synthesizer that controls the corner frequency of the SCF low pass filters shown in Figure 6.12. The output of this synthesizer is set to 96 times the selected modem data rate. Just as described in Section 2.3.12, this synthesizer is 16 bits in length and the output is set to 6.25 Hz resolution.

U45 and U8 form the input latches for the full adders U6, U7, U46, and U47 with state sum latches U5 and U48. The output on U48-15 is nominally 96 times the data rate and it connects via J2-17 to the low pass filter found in Figure 6.12.

For a given data rate, the constant is calculated as shown below:

        LOW PASS FILTER CONSTANT = [128 x BAUD RATE] / 6.25

This output varies between 960 Hz for 10 bits per second and 115,200 Hz for 1200 BPS. The loaded constant varies between 00CC hex for 10 BPS and 6000 hex for 1200 BPS.   -

2.4 FRONT PANEL ASSEMBLY (A3) [6.47 - 6.48]:

The front panel circuitry illustrated in Figure 6.48 is divided into two sections: the seven segment LED display drivers and the switch input buffers. Seven additional single LED indicators, DS1 to DS7, are present on the front panel, but they are all driven directly by control outputs on the modem board. Two potentiometers on the front panel set the PRINT SQUELCH (R8) and the DIVERSITY (R9) levels for the modem board circuitry. Only the components controlled or read by the control processor board are described in the following paragraphs.

2.4.1 Front Panel Switches:

All of the switches and the softpot tuning control are read by the microprocessor on the control processor board through buffers on the front panel. U12, U13, U17, and U18 have a single input bit for each position on the rotary switches or toggle switches. Note that 10K pullup resistors are included on all switch inputs for added noise immunity since the common terminal on the rotary switches is grounded. Each switch position is detected by searching for the 0 input level.

SW10, the detector mode switch, is a 6 position rotary switch that employs only 4 bits on U18. Diodes D1 to D4 encode the M/S and the MP positions as two simultaneous 0 bits. In addition, the memory select switch, SW9, is converted by U15 from 1 of 8 to a 3 bit code read by U12.

2.4.2 Front Panel Displays

The MARK, SPACE, and BAUD RATE displays are composed of multiplexed 4 digit, seven segment, common cathode LED's. The microprocessor on the control board refreshes these digits directly by loading a latch with the segment image then turning ON the digit using a transistor switch. Each individual display window has four digits and the common cathode outputs for each display digit are connected together so that one digit in each display window will be ON at the same time.

Each display window of four digits has an 8 bit latch to hold the segment information. For DS9, the latch is U9 and the segment output signals control the LED segment drivers in U1 and U2. A 1 signal on any latched output will turn the corresponding LED segment ON when the common cathode connection is grounded. The cathode transistor switch is selected by loading a 1 in the common cathode latch U11 which enables an output of U8 and saturates one of the Q1 to Q3 cathode driver transistors. Only one transistor may be turned on at a time.

During ST-8000 operation, a digit in each window is displayed for
4 ms so that the entire digit window is refreshed each 16 ms or
about 60 times per second.   The refresh operation requires three
steps: first, U11 is loaded with all 0 to disable the front
panel displays, then U7, U9, and U10 are loaded with the segment
image for the next display digit in each window, finally, a 1 bit
is latched into U11 turning ON only 1 common cathode driver
transistor.   Each 4 ms, the cycle repeats.   The digits are
scanned from left to right.

2.5 CRT ASSEMBLY (A4) [6.49, 6.50]:

The CRT Assembly (A4) is composed of the CRT and its shield and
the small circuit board mounted under the CRT. The circuit board
contains high voltage power supplies, deflection amplifiers, the
Spectra-Tune circuit, trace switching circuitry, and controls
for adjustment of the CRT display.

***** CAUTION *****

USE EXTREME CARE WHEN TESTING OR ADJUSTING THE CRT ASSEMBLY.
LETHAL VOLTAGES IN EXCESS OF 1500VDC ARE EXPOSED ON THE CRT
CIRCUIT BOARD AND ON THE CRT SOCKET CONNECTIONS.

2.5.1 CRT POWER SUPPLIES

The CRT (Cathode Ray Tube) operates from -1400 and +135 VDC.
These voltages are obtained from a high-voltage winding on the
power transformer.   Both supplies are designed for low-current
output (1.2 ma for -1400V and 6.0 ma for +135V).   Half-wave
rectifiers and high capacitance filters are used to give a DC
voltage close to the peak value of the transformer AC output.

***** CAUTION *****

THE HIGH VOLTAGE SUPPLIES REQUIRE APPROXIMATELY 30 SECONDS TO
DECAY TO SAFE LEVELS AFTER POWER IS TURNED OFF. DO NOT TOUCH ANY
HIGH-VOLTAGE COMPONENT WITHOUT FIRST REMOVING AC POWER FROM THE
ST-8000 AND SHORTING BOTH -1400V (C1 NEG. LEAD) AND +135V (C6
POS. LEAD) OUTPUTS TO CHASSIS GROUND.

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Neither the -1400V or the +135V supply is regulated and the exact voltage will vary with the power line AC voltage. Voltage readings on the schematic were taken with 120.0 VAC line voltage. The high-voltages will therefore vary when other AC input voltages are used. Neither high voltage value is critical and variations of +/- 15% are permissible. Some re-adjustment of INTENSITY, FOCUS, HORIZ, and VERT position controls may be required for AC line voltages consistently differing from 115-125 VAC (230-250 VAC). ST-8000's supplied for use with 220 VAC, 50Hz power have been adjusted for this line input. Conversion of these ST-8000's to 120 VAC will require adjustment of the above CRT controls AFTER the power transformer taps have been changed. A second winding on the power transformer supplies 6.3 VAC for the filament of the CRT itself. The filament is connected to the CRT cathode and therefore the 6.3 VAC winding has a DC potential of approximately -1400 VDC.

The required +8 and -8 VDC for the amplifiers and Spectra-Tune is obtained via connector J2 from the MODEM circuit board (A1). The +5 VDC power supply voltage is NOT used in the CRT assembly.

2.5.2 CRT CONTROLS

The INTENSITY, FOCUS, and ANTISTIG controls make up the high-voltage CRT divider. Use an insulated screw-driver when adjusting these controls. As with all CRT devices, adjustment of FOCUS and ANTISTIG will vary somewhat with INTENSITY setting, particularly if very high CRT intensity is used. When adjusting these controls, first set a moderate CRT trace INTENSITY and then balance FOCUS and ANTISTIG for best over-all trace clarity. Adjustment is easiest when a valid RTTY signal is displayed.

2.5.3 DEFLECTION AMPLIFIERS

The deflection amplifiers are made up of transistors Q4 and Q5 (Vertical) and Q6 and Q7 (Horizontal). Transistors Q3 and Q8 are constant current sources, setting the zero-signal bias point for each amplifier transistor to a collector current of 0.80 ma. Controls R31 (Vertical) and R30 (Horizontal) provide DC position information to the deflection amplifiers. Transistor Q1 is a switch that forces the vertical position of the trace off-screen in a negative direction (down) when the CRT trace is turned OFF by the circuitry on the demodulator and control boards. A logic low input on J2-11 forces the CRT trace OFF.

Integrated circuit U4 provides impedance isolation to drive the deflection amplifiers (U4a = Vertical, U4b = Horizontal). The vertical and horizontal drive signals may be monitored at TP5 and TP4, respectively.

2.5.4 TRACE SWITCHING

Integrated circuit U3 is used as an electronic switch to allow alternate display of the X-Y tuning ellipses and the Spectra-Tune output (U3a = Vertical, U3c = Horizontal, U3b = not used). Controls R53 (Y) and R59 (X) allow adjustment of the amplitude of the vertical and horizontal tuning ellipses, respectively.

Integrated circuit U1b is an oscillator that generates the switching signal for switches U3a and U3c. The oscillator operates at a frequency of approximately 100 Hz. The duty cycle of the switching signal is set so that the X-Y ellipses are displayed for 70% and the Spectra-Tune for 30% of the cycle to obtain a perceived balance of intensity between the two modes.

2.5.5 SPECTRA-TUNE T.M.

Integrated circuits U1a and U2 make up the Spectra-Tune circuit. IC U1a is a medium-gain, wide-bandwidth limiter. The input signal for this limiter is the wide-band receiver audio output, buffered by IC U50a (Figure 6.4). This signal is NOT filtered by any of the ST8000's input or MARK/SPACE filters to preserve the desired full-spectrum receiver output. Control R28 sets limiter balance as observed at TP1.

The output of the limiter (TP1) drives the input of U2, a frequency-to-voltage converter. U2 is biased by diode string D8-D11 and adjusted with R29 so that the output at TP2 is zero volts DC for a 2000 Hz input frequency. This corresponds to the horizontal center of the CRT screen. Control R54 then adjusts the amplitude and therefore CRT horizontal deflection from center screen for frequencies differing from 2000 Hz. These controls should always be adjusted in the order of R29 first (center screen at 2000 Hz) and then R54 (3000 Hz graticule mark with 3000 Hz input frequency).

The output of the limiter (TP1) also drives the divider R41/R40 and Spectra-Tune position control R32 (FREQ V. POS). This produces the small vertical lines, positioned above the Spectra-Tune frequency scale on the CRT.

2.5.6 TRACE ROTATION

Transistor Q2 is an adjustable current source to drive the trace rotation coil inside the CRT shield. Control R22 is adjusted so that the X-Y ellipses line-up with the CRT graticule lines. This adjustment is necessary to compensate for production variations in mechanical alignment of the deflection plates in the CRT itself. Either direction of trace rotation may be compensated for by reversing plug J3.

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2.6 CABINET ASSEMBLY (A5) [6.51 - 6.54]:

The ST-8000 cabinet uses aluminum extrusions for maximum strength. Iridite plating is used on the cabinet parts to assure good electrical shielding properties. In addition, all I/O connections are filtered to further reduce susceptibility to radio frequency interference. The resulting ST8000 package is very RFI quiet and tests show that it exceeds FCC Part 15, Subpart J, Type B emissions by more than 17 dB.

The majority of the ST8000 circuitry is contained on four circuit boards, described in detail in the previous sections. The power transformer, AC line filter, AC fuse, +5V regulator and heat sink, and Main-tuning control are mounted on or in the cabinet and connected to the proper circuit boards. Careful consideration has been given to the placement and mounting of the circuit boards to assure ready access for service and alignment. All circuit boards and cabinet-mounted parts are interconnected with cables as shown in Figure 6.53 and 6.54. When reconnecting the 20-conductor ribbon cables, be sure that the plug and socket pins are properly aligned and are not displaced by one pin or one row.

2.6.1 ELECTROSTATIC PRECAUTIONS

ADVANCED CMOS AND MOS CIRCUITRY IS USED THROUGHOUT THE ST8000. USE OF AN ELECTROSTATICALLY PROTECTED WORK STATION IS HIGHLY RECOMMENDED IF ANY OF THE CIRCUIT BOARDS ARE REMOVED FROM THE ST8000. A PROPER ELECTROSTATICALLY PROTECTED WORK STATION INCLUDES GROUNDED TABLE AND FLOOR MATS AS WELL AS A GROUNDED WRIST BRACELET.

IF A CIRCUIT BOARD IS REMOVED FOR SHIPMENT BACK TO HAL, IT SHOULD BE PLACED INSIDE A BLACK CONDUCTIVE PLASTIC ENVELOPE WHILE AT THE GROUNDED WORK STATION. THE BOARD MAY THEN BE HANDLED FOR FURTHER PACKAGING AT AN UNGROUNDED WORK STATION (BOX REQUIRED). FAILURE TO FOLLOW THESE PROCEDURES MAY CAUSE DAMAGE TO THE ST8000 CIRCUITRY AND VOIDS ALL HAL WARRANTIES. UNLESS THE TECHNICIAN HAS BOTH AN ELECTROSTATIC WORK STATION AND TRAINING IN ITS PROPER USE, IT IS HIGHLY RECOMMENDED THAT THE ENTIRE ST8000 BE RETURNED TO THE FACTORY FOR ALL BOARD-LEVEL REPAIRS.

WHEN THE CIRCUIT BOARDS ARE MOUNTED IN THE CABINET, THE ST8000 IS NO MORE SUSCEPTIBLE TO ELECTROSTATIC DISCHARGE DAMAGE THAN ANY OTHER PIECE OF ELECTRONIC EQUIPMENT. IT MAY BE OPERATED AND TESTED WITHOUT REQUIREMENT FOR ANY ELECTROSTATIC WORK STATION PROTECTION. HOWEVER, SUCH FACILITIES DO PROVIDE ADDITIONAL PERSONNEL AND EQUIPMENT PROTECTION AND ARE THEREFORE RECOMMENDED FOR ALL TEST AND REPAIR SITUATIONS.

2.6.2 CABINET FINISH PROTECTION

The iridite cabinet finish allows limited finish protection while
still affording electrically conductive surfaces. Under normal
careful equipment handling procedures, the cabinet should remain
mar-free for many years of use. However, iridite surfaces
scratch more easily than similarly appearing anodized surfaces
which are not electrically conductive. Therefore, use extra care
to avoid scratching the cabinet surfaces of your ST-8000.
Fingerprints and minor marks are easily cleaned with a good
quality, non-abrasive window cleaner.

The polycarbonate front panel of the ST8000 is specially treated
to be mar-resistant. However, the smooth finish required for the
CRT and frequency display windows may be easily scratched by
abrasive cleaners. Use a good quality, non-abrasive and plastic
rated window cleaner if these front panel areas require cleaning.

2.6.3 CABINET VENTILATION

The ST8000 consumes only 36 Watts of power and all major heat
producing components are mounted directly to the cabinet
(transformer and power supply regulators). In addition, top and
bottom cover ventilation holes are provided that use transformer
heat to establish convection currents to cool all circuitry of
the ST8000. Arrange the ST8000 so that both the bottom and top
ventilation holes are unobstructed. When placed on a table, the
supplied feet provide the required bottom clearance. Do not
cover the top ventilation holes. When rack mounting, place the
ST8000 above and below equipment that is physically less deep
than the the ST8000 cabinet, allowing free-air access to the
ventilation holes. Forced air cooling should not be necessary
unless the installation results in restricted air flow or
unusually high ambient temperatures. Consult the factory for
recommendations about operation in high ambient temperature or
humidity environments.

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CHAPTER 3. TEST AND ALIGNMENT

The following pages provide complete data for test and alignment
of the ST8000 HF Modem.   Under normal use, the ST8000 should not
require re-alignment.   Periodic test or alignment is neither
required   nor recommended.   However,   if it should become
necessary, the following steps must be followed in detail to
assure   top performance.   Chapter 4 notes those   critical
components whose replacement requires at least partial re-
alignment.

3.1   PREPARATION

3.1.1 Test Equipment

The following test instruments or their equivalents are essential
to proper completion of the described tests:


```
    HP400FL AC VOLTMETER (+30 to -80 dBm @ 600 ohms)
    HP3311 FUNCTION GENERATOR (20 to 20,000 Hz, +10 to -30 dBm)
    HP5381A FREQUENCY COUNTER (20 Hz to 10 mHz)
    HP122A OSCILLOSCOPE (DC to 10 mHz)
    FLUKE 77 MULTIMETER (AC & DC VOLTS 20 mV to 1500 V)
    FLUKE 80K-6 HV PROBE (6kV AC/DC probe)
    600 Ohm Step Attenuator (0 to -70 dB in 1 dB steps)
    Source of RS232C Digital Data (DS3100 ASR Terminal)
    Source of Audio RTTY Signals (Radio Receiver or Audio Tape)
    Electrostatic Work Station with Grounded Floor and Table
       Mats, Grounded Wrist Bracket (3M  #8031 kit).
```


3.1.2 Access to MODEM Board

Refer to Section 2.1 of the ST8000 OPERATOR'S MANUAL and remove
the top cover of the cabinet and pivot the top board (CONTROL
assembly A1) to vertical position.   Use an insulated rod (10"
long) to hold the control circuit board in a vertical position.


```
*****************************************************************
```

CAUTION: HIGH VOLTAGES ARE EXPOSED WHEN TESTING THE ST8000.
           USE EXTREME CARE WHEN MAKING THE FOLLOWING ADJUST-
           MENTS AND MEASUREMENTS.

```
*****************************************************************
```

3.1.3 Remote Terminal Connection

The REMOTE CONTROL port will be used to set-up test conditions.
Therefore, temporarily remove the REMOTE connector from the
ST8000 rear panel and plug it back into it's mating connector
(J7) on the CONTROL board (See Figure 3.2).   The REMOTE control
terminal (DS3100) should be connected to the REMOTE DB25
connector and set for 1200 baud ASCII, FDX operation.

3.2 VOLTAGE TESTS

Remove all external connectors from the ST8000 rear panel except
for the AC power cord. With AC power applied and the front panel
POWER switch turned ON, make the following voltage measurements
at the points indicated in Figure 3.1.   Measured voltages should
agree with those in Table 3.1 within a tolerance of +/- 15% with
a 120 VAC, 60 Hz power line input.
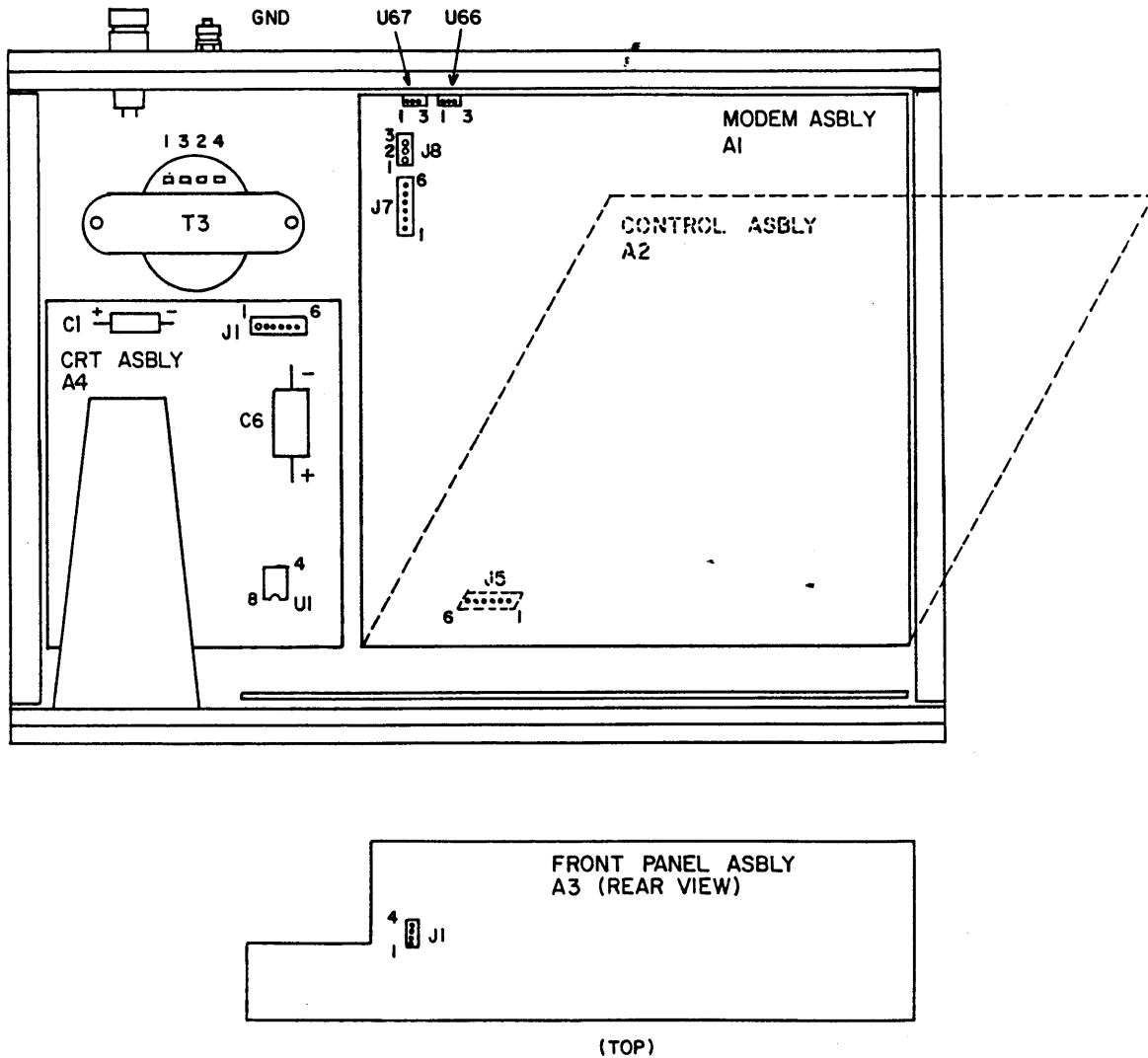
FIGURE 3.1 ST8000 VOLTAGE TEST POINTS

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TABLE 3.1

ST8000 VOLTAGE MEASUREMENTS

PARAMETER	CONNECTION	VOLTAGE	COMMENTS
LINE	T3-1 to T3-2	120 VAC	- SAME FOR 120/240 LINE

AC MEASUREMENTS - DEMODULATOR CIRCUIT BOARD (A1)

+5 AC1	J7-1 to GND	9.0 VAC	+/- 1.0 VAC
+5 AC2	J7-2 to GND	9.0 VAC	+/- 1.0 VAC
+/-V AC1	J7-4 to GND	10.5 VAC	+/- 1.5 VAC
+/-V AC2	J7-6 to GND	10.5 VAC	+/- 1.5 VAC

AC MEASUREMENTS - CRT CIRCUIT BOARD (A4)   -- CAUTION! --

CRT FIL	J1-1 to J1-2	6.3 VAC	+/-0.5 VAC
+150 AC	J1-3 to GND	115 VAC	+/-5.0 VAC
HV AC	J1-6 to GND	1100 VAC	+/- 50 VAC

DC MEASUREMENTS - DEMODULATOR CIRCUIT BOARD (A1)

+5 UNREG	J8-2 to GND	+ 9.6 VDC	+/- 1.0 VDC
+5 REG	J8-3 to GND	+ 5.0 VDC	4.90 to 5.10 VDC
+V UNREG	U67-1 to GND	+12.5 VDC	+/- 1.5 VDC
+V REG	U67-3 to GND	+ 8.0 VDC	7.90 to 8.25 VDC
-V UNREG	U66-2 to GND	-12.5 VDC	+/- 1.5 VDC
-V REG	U66-3 to GND	- 8.0 VDC	-7.90 to -8.25 VDC

DC MEASUREMENTS - CRT CIRCUIT BOARD (A4)   -- CAUTION! --

+135V	C6(+) to GND	+ 135 VDC	+/- 5 VDC
-1400V	C1(-) to GND	-1400 VDC	+/- 50 VDC
+V REG	U4-8 to GND	+ 8.0 VDC	7.90 to 8.25 VDC
-V REG	U4-4 to GND	- 8.0 VDC	-7.90 to -8.25 VDC

DC MEASUREMENTS - DIGITAL CONTROL CIRCUIT BOARD (A2)

+5 REG	J5-3/4 to GND	+ 5.0 VDC	4.85 to 5.10 VDC
+V REG	J5-1 to GND	+ 8.0 VDC	7.90 to 8.25 VDC
-V REG	J5-2 to GND	- 8.0 VDC	-7.90 to -8.25 VDC

DC MEASUREMENTS - FRONT PANEL CIRCUIT BOARD (A3)

+5 REG	J1-1/2 to GND	+ 5.0 VDC	4.85 to 5.10 VDC

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3.3 MODEM TESTS

3.3.1 Initial Set-Up

(1) Set the DIP switches as follows:

Modem Assembly A1:

S1: 2,3,5 = ON; 1,4 = OFF
S2: 1,2,4 = ON; 3,5 = OFF
S3: 1,5   = ON; 2,3,4 = OFF
S4: 2,3,5 = ON; 1,4 = OFF

Control Assembly A2:

SW1: 2 = ON, 1,3,4,5 = OFF (1200 baud)

(2) Refer to Figure 3.2 and connect the test equipment as shown.
Set the test oscillator for:

Frequency = 2000.0 Hz
Waveform = Sinewave
Input Amplitude to ST8000 = -10 dBm

(3) Set the ST8000 front panel switches as follows:

POWER = ON
POLARITY = NORMAL
ANTISPACE = OFF
PTT = RX
DETECTOR MODE = AM M/S
REGEN = OFF
MEMORY = 3
VAR RX/TX = VAR (left position)
MARK/fo = MARK
SPACE/SHIFT = SPACE
INPUT/OUTPUT = INPUT
TUNING MODE = BAUD
TUNING KNOB = Any position
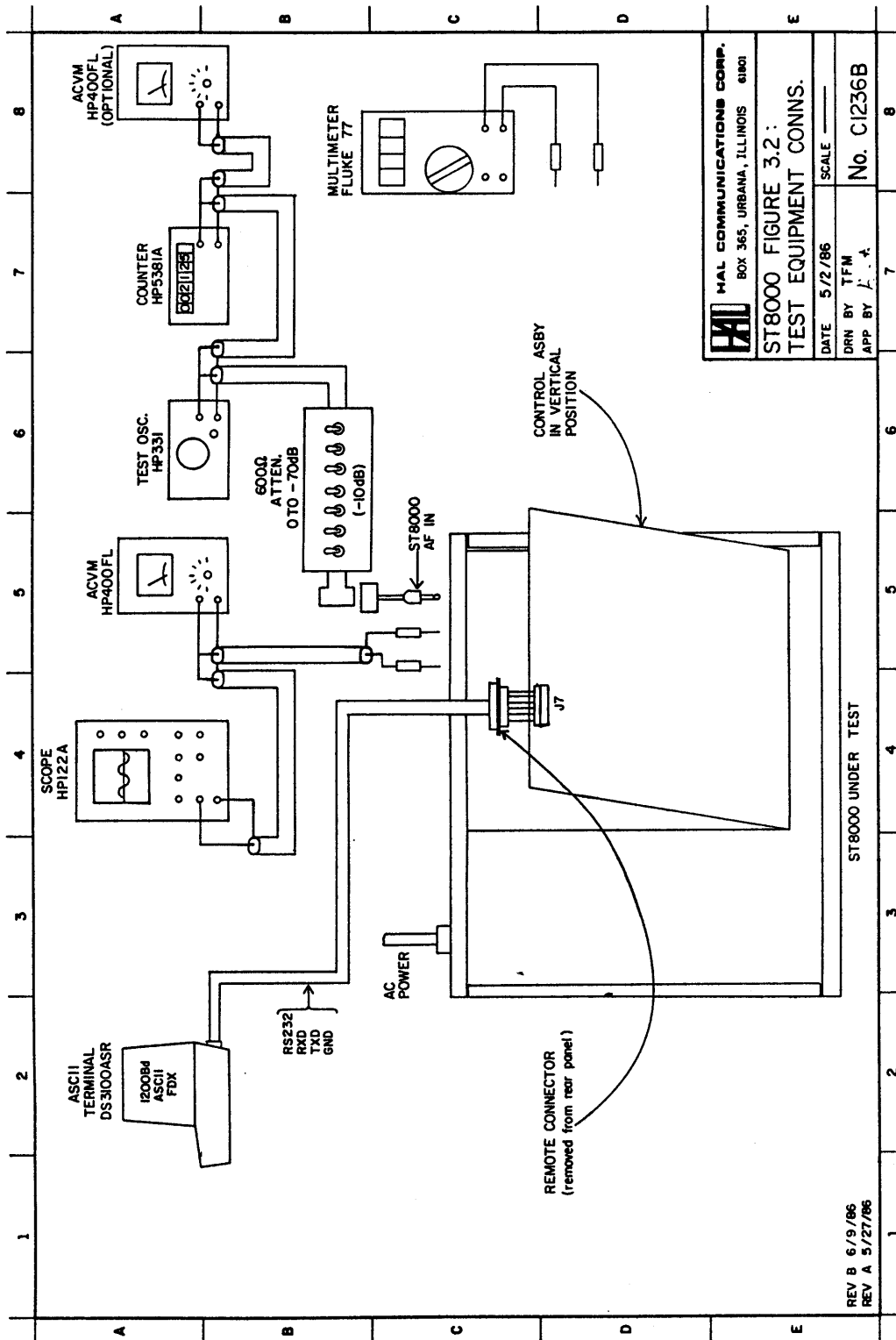
Figure 3.2   TEST EQUIPMENT CONNECTIONS

(4)   Use the Remote terminal to enter the following command
stream EXACTLY as follows (one continuous line):

        DC;TR OFF;TXL OFF;M2000;SP4000;C2000;XM2000;XSP4000;
            QI1;QM40;QS40;DM AM[CR]

        [CR] = Carriage Return, New Line, Enter, etc.

The Remote control feature will be used for testing the ST8000.
It is important that you NOT change any of the front panel switch
settings while the test is under way. If any switches are
changed during the test, the ST8000 will automatically exit
Remote control mode and the above command stream must be re-
entered.

(5)   A sample of the factory alignment form is shown in Figures
3.3 and 3.4. The measurements should recorded on this form. The
same format used in Chapter 2 will be used to refer to the
pertinent schematic and pictorial diagrams([x.y] = Figure No.).

Figure 3.3   TYPICAL ST8000 MODEM MEASUREMENTS

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ST8000 MODEM ASSEMBLY (A1) TEST LOG

MARK & SPACE FILTER TESTS:

MARK FILTER:
Vin = -10 dBm, 2000 Hz, 600 ohms
ST8000: M = 2000, SP = 4000, C = 2000,
QM = QS = 32.3, QI = 1.0, DM = AM MS

TP13 _____ dBm   TP15 _____ dBm   TP46 _____ dBm

QM	TP46 (dBm)	Fh (Hz)	F1 (Hz)	BW (Hz)	Fc (Hz)	Qmeas
32.3						
3.9						
5.8						
1.9						

SPACE FILTER:
Vin = -10 dBm, 2000 Hz, 600 ohms
ST8000: M = 4000, SP = 2000, C = 2000,
QM = QS = 32.3, QI = 1.0, DM = AM MS

TP16 _____ dBm   TP17 _____ dBm   TP41 _____ dBm

QM	TP41 (dBm)	Fh (Hz)	F1 (Hz)	BW (Hz)	Fc (Hz)	Qmeas
32.3						
3.9						
5.8						
1.9						

AFSK TEST:
MARK Data Input, PTT = TX, XM = 2125, XSP = 2975
Set R295 (AFSK LEVEL) to 0 dBm at output (600 ohm load)
J11a, pin 1: 600 ohms = 0.0 dBm (set) LOW-Z _____ dBm
TP28: _____ dBm   TP29: _____ dBm

TIMERS:
MOTOR _____ sec.   CRT _____ sec. MARK _____ sec.

POWER SUPPLIES: +5V _____ +V _____ -V _____

ST8000 MODEM ASSEMBLY (A1) TEST LOG
(REV 17 APRIL 1986)

BOARD S/N _____   TECH _____

DATE ___-___-___   TIMES: START ___:___ AP STOP ___:___ AP

INITIAL POWER TEST: +5V _____ +V _____ -V _____

LEVEL AND BANDPASS TESTS

TP1: _____ dBm (Vin = -10 dBm, 2000 Hz)

Q1	TP4 (dBm)	TP5 (dBm)	Fh (Hz)	F1 (Hz)	BW (Hz)	Fc (Hz)	Qmeas
4.5							
3.0							
1.5							
1.0							

SET Q1 = 1.0 (WIDE)

TP8: _____ dBm; LIM THRESHOLD: _____ dBm (Vin)
TP9: _____ dBm (Vin = -10 dBm)

TP10: AM _____ dBm   FM _____ dBm

Vin (dBm)	TP12 (AGC) (VDC)
0	
-10	
-20	
-30	
-40	
-50	
-60	
-65	
-70	

Figure 3.4   ST8000 MODEM TEST LOG

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3.3.2 INPUT FILTER STAGES [6.3, 6.4]:

(1)   Connect the oscilloscope and ACVM to TP1.   This signal
should be a 2000 Hz sine-wave with -4.5 to -5.5 dBm amplitude.
Record the voltage measured. If the waveform is distorted or has
an improper amplitude, check:

      a. S1 settings
      b. Cable to oscillator
      c. Oscillator output itself
      d. U50 and its associated components

(2)   Connect the counter and oscilloscope to TP2.   A 108,000 Hz
square wave should be observed with TTL compatible amplitude.
This is the clock signal for filter stages U41, U42, and U43.
Its frequency should always be 54 times the chosen center
frequency (2000 Hz for this test). If this signal is not present
or has the wrong frequency:

      a.   Re-enter the command stream from the Remote terminal
      b.   Check for loose connector at J1 or J2.
      c.   A problem exists on the control board. Discontinue
         this test and skip to sections 3.4 and 4.5 to fix the
         problem.

(3)   Connect the oscilloscope and ACVM to TP4 (reconnect counter
to oscillator output and re-affirm that it is still set to 2000.0
Hz).   Measure and record the observed signal amplitude for each
of the following input filter Q's:

REMOTE COMMAND	QI	TP4
QI1[CR]	1.0	measure and record
QI+[CR] or +[CR]	1.5	measure and record
QI+[CR] or +[CR]	3.0	measure and record
QI+[CR] or +[CR]	4.5	measure and record

The voltage at TP4 should be approximately -5 dBm for all filter
bandwidths.   A variation of as much as 0.5 dB between filters is
acceptable. The signal waveform will appear dotted for the three
higher Q tests (QI of 1.5, 3.0 and 4.5), showing the affect of
the sampling filters.

(4)   Move the oscilloscope and ACVM to TP5.   The waveforms will
no longer show the dotted sinewave - it has been smoothed by LP
filter U32.   Check that the oscillator frequency is still 2000 Hz
and record the amplitude for all four bandwidths as above.
Again, the amplitudes should be approximately -5.5 dBm and the
variation between filters should be less than 0.5 dB.

REMOTE COMMAND	QI	TP5
QI4.5[CR] or QI+++[CR]	4.5	measure and record
QI-[CR] or -[CR]	3.0	measure and record
QI-[CR] or -[CR]	1.5	measure and record
QI-[CR] or -[CR]	1.0	measure and record

(5) With the oscilloscope and AVCM still connected to TP5, note
the amplitude reading and then change the oscillator frequency
above and below 2000 Hz to determine the -3 dB response
frequencies.   Record the -3 dB F(high) (high frequency) and
F(low) (low frequency) for each of the four filters.   Use the
Remote terminal to step through the four filters, recording the -
3 dB frequencies for each filter.

(6)   Compute the bandwidth (BW), center frequency (Fc) and Q
(Qmeas) for each using the following formulas:

$$
\begin{aligned}
BW &= F(high) - F(low) \\
Fc &= (BW/2) + F(low) \\
Qmeas &= (Fc/BW)
\end{aligned}
$$

The computed Q's for QI=4.5, 3.0, and 1.5 should be within +/-0.5
of the selected value.   The center frequencies will not
necessarily be exactly 2000 Hz.   The narrow filter (QI=4.5)
center frequency is typically 1980 Hz, +/-10 Hz; the medium
filter (QI=3.0) = 2000 Hz +/-10 Hz, and the wide filter (QI=1.5)
= 2080 Hz, +/- 50 Hz. The low-Q input filter is fixed tuned and
neither its center frequency or Q is critical, but the -3dB
frequencies should be approximately 4100 Hz and 390 Hz, +/- 100
Hz. Any further variations in filter amplitude or bandpass is
generally indicative of a defective IC (U41, U42, U43, or U52).

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3.3.3 Limiter and AGC Alignment [6.5, 6.6]:

(1)   Use the REMOTE control terminal to select the wide input
filter:

        QI 1[CR]   or QI---[CR]

(2)   Check to be sure that the oscillator frequency is set to
2000 Hz.

(3) Connect the oscilloscope and ACVM to TP8. Observe a 2000 Hz
square wave with an amplitude of approximately +18 dBm (+/- 0.5
dB). Record this amplitude.

(4) Change the input level to the ST8000 to -52 dBm and observe
the waveform at TP8.   Adjust R183 (LIMITER BALANCE) for
symmetrical positive and negative peak clipping.   Further reduce
the input level to the ST8000 until the waveform is at the
clipping threshold.   Measure and record this input level.   It
should be -53 dBm +/- 2 dB.

Failure to obtain this value of limiter threshold or lack of
LIMITER BALANCE is indicative of:

    a.   Defective U31 (LM709) or U23 (LM741)
    b.   Defective R812 potentiometer (LIMITER BALANCE)
    c.   Defective D36 or D37 (1N4733)

(5) Increase the input to the ST8000 back to -10 dBm and recheck
to be sure that the oscillator frequency is 2000.0 Hz.

(6)   Move the oscilloscope and ACVM inputs to TP9.   Observe a
2000 Hz sine-wave of approximately +10 dBm amplitude (+/- 1 dB).
Record this amplitude.

(7) Connect the DCVM to pin 3 of U3a. The voltage should be set
to 0.560 VDC using control R4 (+/- 0.02 VDC).

(8) Connect the DCVM to TP12 and increase the audio input to the
ST8000 to 0 dBm (+/- 0.0 dB).   Set the voltage at TP12 to 5.00
VDC (+/- 0.05 VDC) with control R103.   This is the AGC voltage
output of the ST8000.

(9)   Measure and record the TP12 DC voltage for input levels of
10, 0, -20, -30, -40, -50, -60, -65, and -70 dBm. The voltages
should be similar to those shown in Figure 3.3.

(10) Set the input level to the ST8000 to -50 dBm and change the
input frequency from 100 Hz to 10,000 Hz while observing the
oscilloscope waveform at TP9.   The waveform amplitude should
remain fairly constant from 400 to 4000 Hz and decrease gradually
beyond these boundaries.   The output should not exhibit signs of
a pulsed low frequency oscillation (squegging) at any frequency
in this range.   If so, replacement of U30 (MC3340) is indicated.
Failure of this or of test (6) through (10) may be caused by:

    a.   Defective U30, U22, U21, U13, or U3.
    b.   Incorrect settings of R4 or R103.
    c.   Failure of D2-D5.
    d.   Failure of C46 or C89.

(11)   Reset the input to the ST8000 to 2000.0 Hz and -10 dBm.
Connect the oscilloscope and ACVM to TP10.

(12) Enter REMOTE command DM AM[CR] and observe a sine waveform
with an amplitude of 10 dBm (+/- 0.5 dB).   Record this value for
AM mode.

(13)   Enter REMOTE command DM FM[CR] and observe a square
wavefrom with an amplitude of 10 dBm (+/- 0.5 dB).   Record this
vaule for FM mode.   Failure of steps (12) or (13) is indicative
of:

    a.   Defective U14
    b.   No control signal from the control board via J2-7

(14) Enter REMOTE command DM AM[CR].

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3.3.4 Mark/Space Filter Alignment [6.7 - 6.10]

This section describes how to adjust the Mark and Space filter center frequency. These adjustments determine the ultimate accuracy and performance of the ST8000 receive demodulator. It is extremely important that the oscillator frequency be set to exactly 2000.0 Hz and that it not be allowed to drift. A frequency error of only 2 Hz will seriously affect the ST8000's performance at narrow bandwidths (low baud rates). It is therefore highly recommend that the test oscillator be allowed to warm up for at least 4 hours before starting these tests and that its frequency be monitored continuously and corrected if necessary. Do NOT attempt these adjustments if a stable and easily set oscillator is not available. Experience has shown that the ST8000 adjustments do not drift and will need changing only if filter components shown in Figures 6.8 and 6.10 are changed.

3.3.4.1 Mark Filter Alignment [6.7, 6.8]

(1)   Re-enter the REMOTE command sequence:

        DC;TR OFF;TXL OFF;M2000;SP4000;C2000;XM2000;XSP4000;
            QI1;QM40;QS40;DM AM[CR]

(2) Connect the oscilloscope and counter to TP14. Observe a TTL level square wave signal at 100,000.0 Hz. This is the Mark filter clock signal. It should always have a frequency that is 50 times the selected Mark center frequency. If this signal is NOT observed, discontinue further tests, skip to section 3.4, and fix the problem.

(3)   Connect the oscilloscope and ACVM to TP46.   Check to see that the input to the ST8000 is 2000.0 Hz and -10 dBm.

(4)   Observe a sine wave at TP46 with an amplitude of approximately 7.3 dBm +/- 1.0 dB.   There should be NO DC level offset of the sine wave.

(5)   Recheck that the oscillator frequency is exactly 2000 Hz and adjust controls R85 and R86 for maximum output at TP46. Unless a component has been changed in the Mark filter circuit, these settings should be the same as before adjustment.   The two controls will interact slightly -- do repeated adjustment of both to assure that the absolute maximum is obtained.

(6) Move the ACVM to TP13 and measure the amplitude.   It should be +8.9 dBm (+/- 0.5 dB). Record this value.

(7) Move the ACVM to TP15 and measure the amplitude.   It should be +7.8 dBm (+/- 1.0 dB). Record this value.

(8)   Reconnect the ACVM to TP46 and measure the amplitude.   It
should be +7.3 dBm (+/- 1.0 dB).   Record this value (two places
on form).

(9) Enter REMOTE command QM[CR] and confirm that the response is
QM = 32.7. If not, enter QM33[CR].

(10)   Note the amplitude value at TP46 at 2000.0 Hz (value of
step (8)).   Change the oscillator frequency above and below 2000
Hz to determine the -3 dB response frequencies F(high) and
F(low). Record these frequencies.

(11)   Compute and record the bandwidth (BW), center frequency
(Fc), and Q (Qmeas) using the following formulas:

        BW = F(high) - F(low)
        Fc = (BW/2) + F(low)
     Qmeas = (Fc/BW)

The Q value obtained should be 32.7 (+/- 1.5).   The center
frequency should be 2000 Hz (+/- 1.0 Hz).

(12)   Reset the oscillator to exactly 2000.0 Hz and recheck that
the amplitude at TP46 is the same as measured in step (8).   The
REMOTE input will now be used to decrease the Q (increase
bandwidth) in the increments shown in Figure 6.8.   The amplitude
at TP46 will increase as the Q is decreased. Each step change in
Q should show a slight increase in TP46 amplitude. The amplitide
will increase by approximately 2 dB over the total Q range.
Since there are two, 16-step Q ranges available, the bandwidth of
only 4 filter Q's are measured -- the maximum and minimum values
of each range.   If a wide change in amplitude is noted while
stepping through the Q range, a problem needs to be fixed in the
Q-selection circuitry (U5, U6, U7, U15, Ula, Ulb, U2c, or U2d).
The user may also elect to check the -3 dB bandwith of all 32 Q
steps if time and patience permit.

(13)   Note the amplitude at TP46 with Q = 32.7.   Use the REMOTE
command QM-[CR] to decrement Q to QM = 31.3.   Note that the
amplitude increases slightly, the sine wave form continues, and
that there is no change in the DC level of the sine wave.
Continue decrementing QM one step at a time with the QM-[CR]
command until QM = 6.1 and then QM = 3.9 is obtained.   The
amplitude should continuously increase to a value of +9.5 dBm
(+/- 0.5 dB) at QM = 3.9. This is the minimum value of the high-
Q range.   (NOTE - the next decrement value of QM is 5.8,
indicating a switch to the low-Q range.   If this is noted,
increase QM with the QM+[CR] command to get QM = 3.9).   Record
the TP46 amplitude for QM = 3.9.

(14)   Use the techniques of steps (10) and (11) to measure and
record the -3 dB frequencies. Compute and record the BW, Fc, and
Qmeas values for QM = 3.9.   It is normal for the center frequency
(Fc) to be greater than 2000 Hz - 2005 to 2010 Hz are typical
values.   Because of the extremely wide bandwidth of the filters
at low-Q's, this is NOT a detrimental effect. However, the Qmeas
should be 3.9 (+/- 0.25).

(15)   Decrement QM again with QM-[CR] to get QM = 5.8.   This is
the maximum Q value for the low-Q range.   The amplitude at TP46
will decrease by approximately 0.2 dB from the value found in
step (13). Observe that the sine wave with no DC offset is still
present at TP46.   Record the amplitude value for QM = 5.8.

(16)   Use the techniques of steps (10) and (11) to measure and
record the -3 dB frequencies. Compute and record the BW, Fc, and
Qmeas values for QM = 5.8.   Again, it is normal for the center
frequency to be slightly different from 2000 Hz.   The Qmeas
should be 5.8 (+/- 0.25).

(17)   Decrement QM again in 15 steps with QM-[CR] to finally get
QM = 1.9. As in step (13), the amplitude will gradually increase
as the Q is decreased.   QM = 1.9 is the minimum Q value for the
low-Q range.   The amplitude at TP46 will increase   by
approximately 0.3 dB from the value found in step (15).   Observe
that the sine wave with no DC offset is still present at TP46.
Record the amplitude value for QM = 5.8.

(18)   Use the techniques of steps (10) and (11) to measure and
record the -3 dB frequencies. Compute and record the BW, Fc, and
Qmeas values for QM = 1.9.   As before, it is normal for the
center frequency to differ from 2000 Hz (typically as high as
2040 Hz, +/- 15 Hz).   Because of the very wide bandwidth of the
filter, the percentage error and therefore effect on performance
is very small. The QM value should be 1.9 (+/- 0.1).

(19)   Enter the REMOTE command QM33[CR] and observe that the same
amplitude of step (8) is measured (+/- 0.2 dB).

(20)   Enter the REMOTE command EX[CR] to exchange Mark and
Space filter frequencies.   Increase the oscilloscope gain and
check the scope's zero volt DC reference.   Adjust control R132
(DC BAL) to obtain zero volts DC at TP46.

(21)   Move the oscilloscope to TP45 (Figures 6.11 and 6.12).
Adjust control R65 (LP OFFSET) for zero volts DC at TP45.

This completes alignment of the Mark filter.

3.3.4.2 Space Filter Alignment [6.9, 6.10]

The steps of this section are identical to those performed above
for the Mark filter.   They are repeated below with appropriate
changes in TP and component references.

(1)   Enter the REMOTE command sequence:

         DC;TR OFF;TXL OFF;M4000;SP2000;C2000;XM2000;XSP4000;
                QI1;QM40;QS40;DM AM[CR]

Note that the Mark and Space filter frequencies have been
interchanged from those used in section 3.3.4.1.   This command
need not be entered if the final settings used for Mark filter
alignment remain in place.   If in doubt, enter the above command
stream.

(2) Connect the oscilloscope and counter to TP18. Observe a TTL
level square wave signal at 100,000.0 Hz.   This is the Space
filter clock signal.   It should always have a frequency that is
50 times the selected Space center frequency.   If this signal is
NOT observed, discontinue further tests, skip to section 3.4, and
fix the problem.

(3)   Connect the oscilloscope and ACVM to TP41.   Check to see
that the input to the ST8000 is 2000.0 Hz and -10 dBm.

(4)   Observe a sine wave at TP41 with an amplitude   of
approximately 7.3 dBm +/- 1.0 dB.   There should be NO DC level
offset of the sine wave.

(5) Recheck that the oscillator frequency is exactly 2000 Hz and
adjust controls R123 and R124 for maximum output at TP41. Unless
a component has been changed in the Space filter circuit, these
settings should be the same as before adjustment.   The two
controls will interact slightly -- do repeated adjustment of both
to assure that the absolute maximum is obtained.

(6) Move the ACVM to TP16 and measure the amplitude.   It should
be +8.9 dBm (+/- 0.5 dB). Record this value.

(7) Move the ACVM to TP17 and measure the amplitude.   It should
be +7.8 dBm (+/- 1.0 dB). Record this value.

(8)   Reconnect the ACVM to TP41 and measure the amplitude.   It
should be +7.3 dBm (+/- 1.0 dB).   Record this value (two places
on form).

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(9)   Enter REMOTE command QS[CR] and confirm that the response is QS = 32.7. If not, enter QS33[CR].

(10)   Note the amplitude value at TP41 at 2000.0 Hz (value of step (8)).   Change the oscillator frequency above and below 2000 Hz to determine the -3 dB response frequencies F(high) and F(low). Record these frequencies.

(11)   Compute and record the bandwidth (BW), center frequency (Fc), and Q (Qmeas) using the following formulas:

$$BW = F(high) - F(low)$$
$$Fc = (BW/2) + F(low)$$
$$Qmeas = (Fc/BW)$$

The Q value obtained should be 32.7 (+/- 1.5).   The center frequency should be 2000 Hz (+/- 1.0 Hz).

(12)   Reset the oscillator to exactly 2000.0 Hz and recheck that the amplitude at TP41 is the same as measured in step (8).   The REMOTE input will now be used to decrease the Q (increase bandwidth) in the increments shown in Figure 6.10. The amplitude at TP41 will increase as the Q is decreased. Each step change in Q should show a slight increase in TP41 amplitude. The amplitude will increase by approximately 2 dB over the total Q range. Since there are two, 16-step Q ranges available, the bandwidth of only 4 filter Q's are measured -- the maximum and minimum values of each range.   If a wide change in amplitude is noted while stepping through the Q range, a problem needs to be fixed in the Q-selection circuitry (U16, U25, U24, U33, U1b, U1c, U2a, or U2b).   The user may also elect to check the -3 dB bandwidth of all 32 Q steps if time and patience permit.

(13)   Note the amplitude at TP41 with Q = 32.7.   Use the REMOTE command QS-[CR] to decrement Q to QS = 31.3.   Note that the amplitude increases slightly, the sine wave-form continues, and that there is no change in the DC level of the sine wave. Continue decrementing QM one step at a time with the QS-[CR] command until QS = 6.1 and then QS = 3.9 is obtained.   The amplitude should continuously increase to a value of +9.5 dBm (+/- 0.5 dB) at QS = 3.9. This is the minimum value of the high-Q range.   (NOTE - the next decrement value of QS is 5.8, indicating a switch to the low-Q range. If this is noted, increase QS with the QS+[CR] command to get QS = 3.9).   Record the TP41 amplitude for QS = 3.9.

(14)   Use the techniques of steps (10) and (11) to measure and record the -3 dB frequencies. Compute and record the BW, Fc, and Qmeas values for QS = 3.9. It is normal for the center frequency (Fc) to be greater than 2000 Hz - 2005 to 2010 Hz are typical values.   Because of the extremely wide bandwidth of the filters at low-Q's, this is NOT a detrimental effect. However, the Qmeas should be 3.9 (+/- 0.25).

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(15) Decrement QS again with QS-[CR] to get QS = 5.8. This is the maximum Q value for the low-Q range. The amplitude at TP41 will decrease by approximately 0.2 dB from the value found in step (13). Observe that the sine wave with no DC offset is still present at TP41. Record the amplitude value for QS = 5.8.

(16) Use the techniques of steps (10) and (11) to measure and record the -3 dB frequencies. Compute and record the BW, Fc, and Qmeas values for QS = 5.8. Again, it is normal for the center frequency to be slightly different from 2000 Hz. The Qmeas should be 5.8 (+/- 0.25).

(17) Decrement QS again in 15 steps with QS-[CR] to finally get QS = 1.9. As in step (13), the amplitude will gradually increase as the Q is decreased. QS = 1.9 is the minimum Q value for the low-Q range. The amplitude at TP41 will increase by approximately 0.3 dB from the value found in step (15). Observe that the sine wave with no DC offset is still present at TP41. Record the amplitude value for QS = 5.8.

(18) Use the techniques of steps (10) and (11) to measure and record the -3 dB frequencies. Compute and record the BW, Fc, and Qmeas values for QS = 1.9. As before, it is normal for the center frequency to differ from 2000 Hz (typically as high as 2040 Hz, +/- 15 Hz). Because of the very wide bandwidth of the filter, the percentage error and therefore effect on performance is very small. The QS value should be 1.9 (+/- 0.1).

(19) Enter the REMOTE command QS33[CR] and observe that the same amplitude of step (8) is measured (+/- 0.2 dB).

(20) Enter the REMOTE command EX[CR] to exchange Mark and Space filter frequencies. Increase the oscilloscope gain and check the scopes's zero volt DC reference. Adjust control R131 (DC BAL) to obtain zero volts DC at TP41.

(21) Move the oscilloscope to TP37 (Figures 6.11 and 6.12). Adjust control R68 (LP OFFSET) for zero volts DC at TP41.

This completes alignment of the Space filter. The AFSK generator and transmit data circuitry will now be checked so that the ST8000 AFSK output may be used as the test signal source.

3.3.5   AFSK Generator Tests [6.21, 6.22; 6.35, 6.36]

The AFSK generator circuit is split between the control circuit board [Figures 6.35 and 6.36] and the demodulator circuit board [6.21 and 6.22]. The generation of the AFSK signal and its frequency change from Mark to Space is controlled by the synthesizer on the control circuit board. For this series of tests, it is assumed that this synthesizer and Mark/Space selection circuitry is functioning correctly. If not, skip to section 3.4 and fix the problem before continuing.

The AFSK signal from the control circuit board is a digital waveform at 10 times the desired output frequency. A ten-step sinusoidal waveform is synthesized in U61 and its associated resistor ladder (R268 through R277), filtered in stage U65a, and amplified in stage U65b on the demodulator circuit board. The following steps test the operation of this circuitry.

(1)   Use the ST8000 front panel controls to set the following conditions   (Frequencies stored in Memory Channel 3 of factory prepared units):


```
              MARK = 2125 Hz
             SPACE = 2975 Hz
         VAR RX/TX = VAR (left position)
       TUNING MODE = BAUD
            MEMORY = any channel
      INPUT/OUTPUT = 075 Baud
          DETECTOR = FM M/S
             REGEN = OFF
     PRINT SQUELCH = "9 O'Clock"
         DIVERSITY = Full CCW
         ANTISPACE = OFF
          POLARITY = NORMAL
               PTT = TX (TX LED ON)
             POWER = ON
```


In addition, be sure that the DIP switches are set as shown in section 3.3.1 and that there is no connection to the TERMINAL I/O connector on the ST8000 rear panel. The terminal should remain connected to the REMOTE CONTROL connector.

(2)   Refer to Figure 3.5 and connect the AFSK output to the ST8000 audio input through a step attenuator set to -10 dB.

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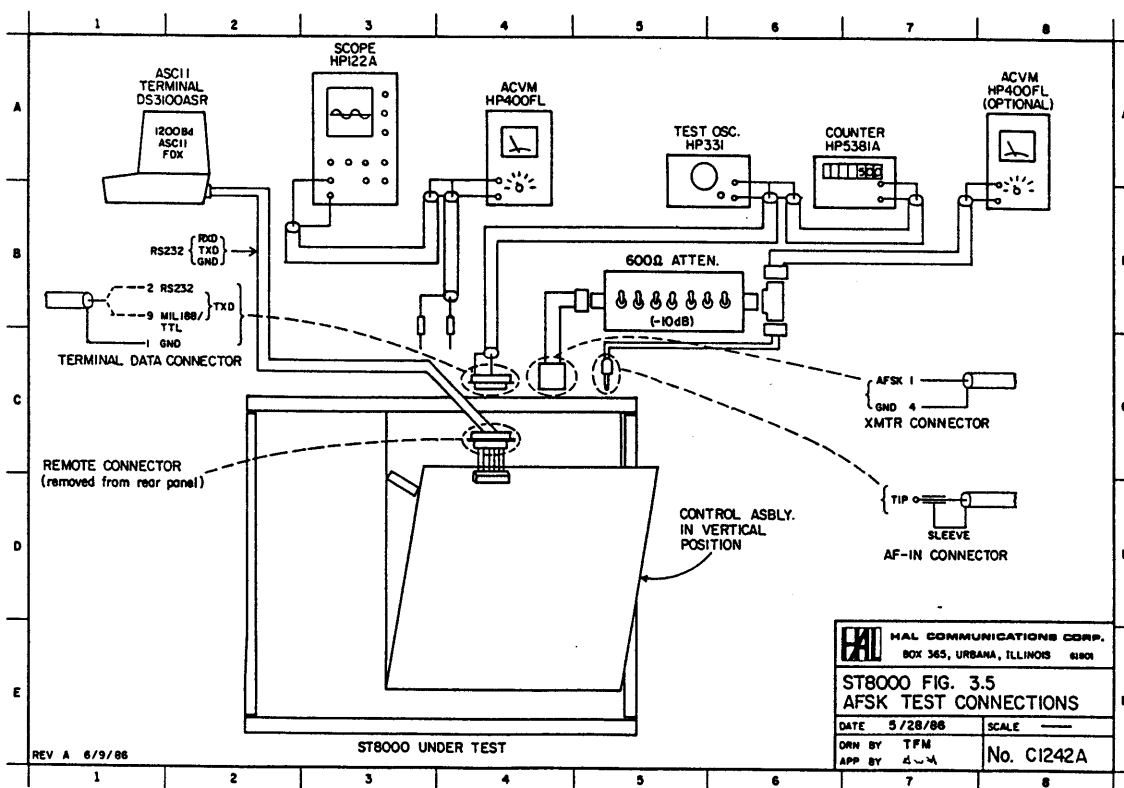
FIGURE 3.5   AFSK TEST GENERATOR CONNECTIONS

(3)   Connect the oscilloscope and ACVM to TP28. Observe a synthesized sinusoidal waveform with the positive peak slightly less than zero volts (waveform displaced negatively). Use the counter to measure the output frequency. It should be 2125.0 Hz (+/- 0.5 Hz).

(4)   Measure and record the amplitude at TP28. It should be +1.0 dBm (+/- 0.5 dB).

(5)   Change the POLARITY switch to REVERSE and measure the output frequency. It should be 2975.0 Hz (+/- 0.5 Hz).

(6)   Return the POLARITY switch to NORMAL. Connect the ACVM in parallel with the audio input to the ST8000. Adjust control R295 (AFSK LEVEL - rear panel hole near XMIT connector) so that a level of -10 dBm is set at the ST8000 input. Measure and record the amplitude of the signal at J11-2 (XMIT connector). It should be 0 dBm (+/- 1.0 dB).

(7)   Change DIP switch S2 so that S2-1, S2-3, and S2-4 are ON and S2-2 and S2-5 are OFF. Measure and record the amplitude at J11-2 (XMIT connector). It should be -16 dBm (+/- 1.0 dB).

(8)   Change DIP switch S2 back to: S2-1, S2-2, S2-4 = ON; S2-3, S2-5 = OFF.

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(9) Connect the oscilloscope and ACVM to TP29. A smooth
sinewave with zero DC offset should be observed. Measure and
record the amplitude at TP29. It should be +3.5 dBm (+/- 1.0
dB).

This completes test and adjustment of the AFSK output circuitry.

3.3.6 Transmit Data Input Circuitry [6.19, 6.20]

These tests will be concerned with testing only the signal path
of transmit data from the TERMINAL I/O connector (J9) to the AFSK
generator. Other features shown in Figures 6.19 and 6.20 will be
tested in a later section. It is assumed that all of the
connections and adjustments remain as set at step (9) of section
3.3.5.

(1) Set the test oscillator for square wave output at a
frequency of 50.0 Hz (+/- 1.0 Hz). Adjust the amplitude to be
symmetrical about zero volts DC with peak amplitude of +5 to -5V
or greater (+/- 20V maximum). Connect the oscillator output to
pin 2 of the TERMINAL I/O connector (J9 - RS232C TXD input).
Connect the oscilloscope external sweep trigger to the oscillator
output and adjust the controls for proper triggering.

NOTE: jumper JP3 MUST NOT be installed for proper operation of
the ST8000. This jumper is ONLY used when the demodulator
circuit board must be tested independently of the control circuit
board.

(2) Connect the oscilloscope probe to pin 2 of jumper JP3 or pin
3 of U63 and observe a TTL-level signal, synchronized with the
oscillator 50Hz square wave. If this signal is NOT observed,
connect the oscilloscope to pin 1 of JP3 or pin 3 of U54.
Presence of the signal at U54-3 and not at U63-3 indicates that
either REGEN is not OFF or that there is a problem on the control
board. If so, fix the problem before continuing.

(3) Change the oscillator connection from pin 2 to pin 9 of J9
(TERMINAL I/O connector). Observe the same TTL-level signal at
JP3-2 as in step (2), but reversed in polarity.

(4) Readjust the oscillator output to a TTL-level signal (0 to
+5V) and change its connection to pin 14 of J9. Again observe
the TTL-level signal at JP3-2 with polarity reversed from step
(2) but the same as step (3).

(5) Reconnect the oscillator to J9-2 and reset its output to +/-
5V peak-to-peak.

(6) Check that DIP switch S3-1 is ON and S3-2 is OFF. Connect
the oscilloscope to TP27 and observe the presence of a TTL-level
signal, synchronized with the oscillator output.

(7) Change the POLARITY switch to REVERSE and note a polarity
reversal in the signal at TP27.

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(8) Reset the POLARITY switch to NORMAL.

This completes the test of transmit data input circuits.   Retain
these settings and connections for the following tests.

3.3.7 Detector and LP Filter Tests [6.11, 6.12]

The following tests assume continuation of parameters set-up in
sections 3.3.5 and 3.3.6.   Before continuing, confirm that these
parameters have been so set.

(1)   Set the oscillator frequency to 37.5 Hz (+/- 0.5 Hz) and
confirm that it is connected to J9-2 and has a square wave output
with a minimum peak-to-peak amplitude of +/- 5V.   Also confirm
that the ST8000 PTT switch is in TX position and that receive and
transmit Mark = 2125, Space = 2975, and INPUT BAUD = 075.

(2) Connect the oscilloscope and counter to TP50, use internal
sweep trigger, and observe a TTL-level 7200 Hz square wave. This
is the LP Filter clock signal. It should always have a frequency
that is 96 times the indicated INPUT Baud rate.   If this signal
is NOT observed or is at the wrong frequency, recheck the above
settings and then skip to sections 3.4 and 4.5 to fix the
problem. Do not continue if this step does not check.

(3)   Trigger the oscilloscope on the test oscillator output and
connect the vertical input to TP45.   Observe a rounded pulse
between 0 and -3.5V, synchronized with the oscillator output.
The negative deflection period is the "MARK" condition of the
input waveform.

(4)   Connect the second vertical input of the oscilloscope to
TP37 and observe a rounded positive pulse between 0 and +3.5V.
The positive deflection period is the "SPACE" condition of the
input waveform. The positive deflection should occur at the same
time as the negative deflection of the Mark signal at TP45.

(5)   Set the two oscilloscope input amplifiers to the same gain
and adjust vertical positioning so that the two traces over-lap.
Adjust control R63 (SPACE BAL) for close match between the two
waveforms.   This control is typically set at or near its maximum
position (CCW). A match within 0.3V should be achievable.

(6)   Adjust the oscilloscope trace positions so that the Mark
(TP45) and Space (TP37) signals are separated on the screen. Set
the TUNING MODE front panel switch to BAUD and the INPUT/OUTPUT
switch to INPUT. Adjust the INPUT BAUD rate with the MAIN TUNING
control and note that the waveforms become sinusoidal with
increasing DC offset as INPUT BAUD is decreased and become more
squared as the BAUD rate is increased.   Both the Mark (TP45) and
Space (TP37) waveforms should have the same shape as the INPUT
BAUD parameter is changed.   This tests the operation of the LP
Filter stages (U11 and U27).

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(7)   Increase the oscillator frequency to 300 Hz and change the
INPUT Baud setting of the ST8000 to 600 Baud.   Observe similar
waveforms to those for 75 Baud, except at a higher frequency.
Return the oscillator to 37.5 Hz and the ST8000 INPUT Baud to 075
when done.

This completes tests of the detectors and low-pass filters.   Do
not change the ST8000 and oscillator settings as they will be
used in the following sections.

3.3.8 MO, SO, M/S, DMPC, and Print Squelch Tests [6.13, 6.14]

This section continues the tests of sections 3.3.5, 3.3.6, and
3.3.7.   It is assumed that the previously used connections and
parameters remain set. If not, review these sections and set the
equipment accordingly.

(1)   Connect one channel of the oscilloscope to TP45 and trigger
the sweep from either this signal or directly from the test
oscillator output. Use the second channel vertical input to make
the following measurements.   NOTE: Negative deflection of the
TP45 signal corresponds to a Mark signal condition.

(2)   Connect the second channel of the oscilloscope to TP44 and
observe a +/- 7.5V signal that is positive during Mark signal
condition at TP45.   Change the input to the ST8000 from 0 dBm to
-60 dBm and observe that the signal is always present. Return to
-10 dBm input when done.   This tests the MO (Mark Only) detector
output.

(3)   Connect the second channel input to TP40 and observe a +/-
7.5V signal that is positive during Space signal condition.
Change the input level to the ST8000 from 0 dBm to -60 dBm and
observe that the signal is always present.   Return to -10 dBm
input when done. This tests the SO (Space Only) detector output.

(4)   Connect the second channel input to TP42 and observe a +/-
7.5V signal that is positive during Mark signal condition.
Change the input level to the ST8000 from 0 dBm to -60 dBm and
observe that the signal is always present.   Return to -10 dBm
input when done. This tests the M/S (Mark/Space) ATC detector
output.

(5) Connect the second channel input to TP49 and observe a TTL-
level signal that is positive during Space signal condition.
Change the input level to the ST8000 from 0 dBm to -60 dBm and
observe that the signal is always present.   Return to -10 dBm
input when done.   This tests the DMPC (Digital Multipath
Correction) detector output.

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(6) Connect the second channel input to TP34 and observe a TTL-level signal that is positive during Mark signal condition. Change the DETECTOR MODE front panel switch for various input levels between 0 dBm and -60 dBm and observe that the signal is always present. Return to -10 dBm input and FM M/S Mode when done. This tests the Detector and AM/FM mode selection circuitry. It is normal for the oscilloscope ellipses to show greater deflection for AM compared to FM modes.

(7) Connect the second channel input to TP39 and slowly rotate the PRINT SQUELCH front panel control clockwise. The voltage at TP39 should change from approximately +7.5V to -7.5V as the control is changed. This tests the PRINT SQUELCH (+/+) detector and control. Reset PRINT SQUELCH to the "9 O'Clock" position when done.

This completes the tests for the detectors and PRINT SQUELCH circuitry. Leave these settings for tests in the following sections.

3.3.9 RX Data Control [6.15, 6.16]

The tests described in this section assume continuation of tests and equipment connections of sections 3.3.5 through 3.3.8. Review these sections if you have skipped to these steps.

NOTE: Jumper JP4 MUST NOT be installed for normal operation of the ST8000. This jumper is used only when the demodulator circuit board must be tested independently of the control circuit board. Be sure that JP4 is NOT installed for the following tests.

(1) Connect the second oscilloscope vertical input to pin 2 of JP4 (or U48-11 or U49-7) and observe a TTL-level digital signal, synchronized with the signal at TP45. If the signal is not observed, connect to pin 1 of JP4 (or U39-4). Presence of the signal at U39-4 and not at U48-11 is indicative of either not having REGEN set OFF or a more serious problem on the control circuit board. If the problem appears to be on the control board, discontinue these tests and skip to section 3.4.

(2) Observe JP4-2 and change the POLARITY switch from NORMAL to REVERSE. The polarity of the TP45 signal will change, but the signal polarity at JP4-2 should not change (except for a short switching transient that may not be observable). Reset POLARITY to NORMAL when done.

(3) Connect the oscilloscope input to TP32 and observe a TTL-level signal, synchronized with that from TP45 with Mark having the positive polarity. If no signal is observed, set PRINT SQUELCH to minimum (full CCW) and check that DIVERSITY is also at the full CCW position. If the signal is still not observed, test that both U48-8 and U58-9 have a "high" (+4V) logic level. If both of these signals are not "high", skip to section 3.3.10 (next section) and test the diversity circuit.

(4)   Slowly increase the PRINT SQUELCH in a clockwise direction
until the signal at TP32 stops.   It should stop with a positive
polarity (approximately +4V).   Decreasing PRINT SQUELCH (CCW)
should allow the signal to resume at TP32.   Reset PRINT SQUELCH
to "9 O'Clock" when done.

(5)   Slowly increase the DIVERSITY control in a clockwise
direction while observing TP32.   At approximately the "3 O'Clock"
position, the signal at TP32 will go to a continuous "high" logic
level.   The time constant of the diversity and AGC squelch
circuit is quite long and therefore this condition may take
several seconds to be noted.   If a shut-off of data at TP32
cannot be obtained for full CW rotation of the DIVERSITY control,
skip to section 3.3.10 and fix the problem in the Diversity
circuitry before returning to the next step.   Return the
DIVERSITY control to full CCW position when done.

(6)   Observe that the "M" (Mark) and "S" (Space) front panel
lamps flash with the data signal.

(7)   Connect the oscilloscope to TP31 and check to see that the
TTL-level signal has a Mark positive polarity and is also
controlled by the PRINT SQUELCH and DIVERSITY controls as
described above in steps (4) and (5).   If the signal is observed
at TP32 but not at TP31, DIP switch S3 may be set incorrectly
(S3-5 = ON; S3-3, S3-4 = OFF).

(8)   Connect the oscilloscope to pin 3 of J9 (TERMINAL I/O -
RS232C RXD) and observe a +/- 7.5V signal with negative Mark
polarity.

(9)   Connect the oscilloscope to pin 10 of J9 (TERMINAL I/O -
MIL188C RXD) and observe a +/- 7.5V signal with positive Mark
polarity.

(10)   Connect the oscilloscope to pin 16 of J9 (TERMINAL I/O -
TTL RXD) and observe a TTL-level signal with positive Mark
polarity.   Change Jumper JP2 from the "N" to "R" position and
observe that the TTL RXD signal now has positive Space polarity.
Reset JP2 to "N" when done.

(11)   Connect the oscilloscope to pin 8 of J9 (TERMINAL I/O - CD)
and observe a continuous positive output.   Reset BOTH PRINT
SQUELCH and DIVERSITY controls to maximum CW (clockwise)
positions.   After a short delay note that: (a) J9-8 goes to a
negative voltage, (b) the front panel LOS lamp is turned ON, (c)
the PRINT, "A", and "B" lamps are all OFF, and (d) only the "M"
(Mark) lamp is on.

(12)   Change the PRINT SQUELCH control only back to full CCW
position and observe that: (a) J9-8 goes to a positive voltage,
(b) the LOS lamp turns OFF, (c) neither the PRINT, A, or B lamps
turn ON, and (d) only the "M" (Mark) lamp is on.

(13)   Reset PRINT SQUELCH TO maximum CW and then decrease
DIVERSITY to full CCW position.   Observe that: (a) J9-8 goes
negative and then back positive, (b) LOS comes ON and then turns
OFF, (c) the "A" diversity lamp turns ON, (d) the PRINT lamp does
NOT turn ON, and (e) only the "M" (Mark) lamp is on.

(14)   With DIVERSITY at full CCW position, change PRINT SQUELCH
to also be in full CCW position.   Observe: (a) J9-8 stays
positive, (b) LOS is OFF, (c) "A" lamp is ON, (d) the PRINT lamp
turns ON, and (e) the "M" (Mark) and "S" (Space) lamps again
flash with the data.

(15)   Connect a 12VDC relay coil (100 ohms minimum) between pin
12 of J9 (TERMINAL I/O) and a +12VDC power supply.   The relay
should be activated (contacts pulled-in).   Change both the PRINT
SQUELCH and DIVERSITY controls to full CW position.   Start a
timer when the controls are advanced.   After a 15-20 second
delay, the relay should de-energize (contacts open). Record the
time delay on the test log.   Disconnect the relay and reset both
PRINT SQUELCH and DIVERSITY to full CCW positions when done.

(16)   Observe the CRT display.   Mark/Space ellipses and the
Spectra-Tune bars should be seen.   If not, check to see that
connector J6 is correctly attached and then skip to section 3.6
to repair the CRT circuitry before continuing.

(17)   Observe the CRT and increase PRINT SQUELCH to full CW
position, starting a timer at this time.   After an 8-11 second
delay, the scope trace should turn OFF.   Record this CRT time
delay on the test log.   Reset PRINT SQUELCH to full CCW when
done, restoring the CRT trace.

(18)   Observe the CRT trace and disconnect the test oscillator
input to the TERMINAL I/O connector.   After an approximate 10
second delay, the CRT trace will turn OFF.   Record this "long
Mark" delay time on the test log.   Leave the test oscillator
disconnected for the following step.

(19)   Use the terminal connected to the REMOTE CONTROL input to
send the following command stream:

     FP;CRT ON[CR]

The CRT trace should immediately turn on as the command is
executed.   It will stay ON for as long as the REMOTE command
"CRT=ON" is active.   Reset the REMOTE CRT control with the
following command stream:

     FP;CRT AUTO[CR]

The CRT trace will now turn OFF. Reactivate the CRT by returning
PRINT SQUELCH to full CCW position.

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(20)   Set PRINT SQUELCH to full CW position and wait until the
CRT trace turns OFF.   Change any front panel switch (except
POWER) or control (except PRINT SQUELCH and DIVERSITY) and note
that the CRT trace is turned ON.   After 10 seconds, the trace
will again turn OFF.   This tests microprocessor CRT trace
restoration when any tuning adjustments are made (control via J1-
5 to U59-12).

(21)   Let the CRT trace turn OFF again and then temporarily
ground pin 18 of J9 (TERMINAL I/O connector).   The CRT trace
should turn ON and remain ON when this pin is grounded.   Reset
PRINT SQUELCH to full CCW position when done.

(22)   With the test oscillator still disconnected from J9, set
the ANTISPACE front panel switch ON.   Connect the oscilloscope to
TP30 and observe a Mark condition (TTL high level).   Temporarily
short pin 14 of J9 (TERMINAL I/O) to ground and observe that the
TP30 signal changes to Space and then back to Mark condition
after a short delay.   The same effect should be noticed on the
"M" (Mark) and "S" Space lamps. Turn ANTISPACE OFF and note that
the TP30 signal remains in Space condition for as long as J9-14
is shorted to ground. Remove the jumper from J9-14 and reconnect
the test oscillator to J9-2 when done.

(23) With the test oscillator reconnected, check to see that the
CRT trace again shows the normal signal patterns and that PRINT
SQUELCH and DIVERSITY controls are set to full CCW positions.
Temporarily short pin 25 of J9 (Terminal I/O connector) to ground
and observe that the CRT trace turns OFF whenever this pin is
grounded.   This is the external CRT trace-OFF control connection.
Remove the ground lead when done.

(24)   Set PRINT SQUELCH to full CW position and observe the
signal at TP31 with the oscilloscope.   TP31 should remain in a
Mark-high state.   Using the REMOTE terninal, enter the following
command stream:

     FP;PRINT ON[CR]

The data   output   to TP31 should resume when this command is
executed, independent of the setting of PRINT SQUELCH.   This
tests the Selective Call and REMOTE Print Squelch over-ride
features.   When done, enter the following command stream:

     FP;PRINT AUTO[CR]

This completes testing of the RX Data Control Circuitry.   Leave
the connections and test set-up as they will be used in the
following sections. Set PRINT SQUELCH to full CCW position.

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3.3.10   Diversity and AGC Squelch Tests [6.17, 6.18]

3.3.10.1   Non-diversity AGC Squelch Tests [6.17, 6.18]

The non-diversity squelch feature of the ST8000 may be tested
without the requirement for simulation of the connection of a
second ST8000 demodulator.   NO CONNECTION should be made to the
DIVERSITY rear panel connector for the following tests.

(1)   Check that a digital Mark/Space signal is observed at TP31
and that the CRT display is normal for a received signal. If not,
review the previous section and make the required adjustments.

(2)   Be sure that jumper JP1 is installed.   The ST8000 will not
function properly if this jumper is removed.   This jumper should
ONLY be removed if it is desired to use receiver AGC rather than
ST8000 AGC to drive the AGC Squelch and Diversity circuitry.

(3)   Connect the DCVM to TP47 and confirm that the AGC voltage
from TP12 is also at TP47.

(4)   Connect the oscilloscope to TP33 and confirm this signal is
at a positive level (+7.5V +/- 0.5V).

(5)   Connect the DCVM to TP35 and confirm that it is at
approximately -1.5 VDC.

(6)   Connect the DCVM to TP23 and observe the voltage while
rotating the DIVERSITY control through its full range.   TP23
should be at the same potential as TP47 at the full CCW position
of the DIVERSITY control and at the potential of TP35 at the full
CW position.

(7)   Connect the oscilloscope to TP21 and observe the signal
while SLOWLY rotating the DIVERSITY control from CCW to CW
positions.   At approximately the "9 O'Clock" position, TP21
changes from a negative (A signal present) to a positive voltage
(LOS).   Set the DIVERSITY control until TP21 has just changed
from positive (no signal) to negative (signal present) state.
Add 10 dB of attenuation to the input to the ST8000 (-20 dBm
level) and note that TP21 returns to the no-signal state
(positive).   Reset the DIVERSITY control for the signal-on state
(negative) and add another 10 dB of attenuation (-30 dBm input).
TP21 should again change to the positive (no-signal) state.
Continue adjusting the DIVERSITY control and the input signal
level down to -60 dBm signal input. It should be possible to set
a signal/no-signal threshold at each level.   Return the input
signal to -10 dBm when done.

(8)   With -10dBm input signal level, adjust the DIVERSITY control
through the threshold point as shown at TP21 while observing the
"A" channel LED indicator.   The "A" indicator should turn OFF
when the no-signal state is set and ON when in the signal-on
state. The "B" channel LED should NOT turn ON at any time during
these tests.

(9) Connect the oscilloscope to TP30 and observe the Mark/Space data stream. The data should stop in a Mark condition (TTL logic high) whenever the "A" channel LED is OFF, indicating the no-signal condition. Signal flow should resume whenever the "A" LED in ON.

This completes testing of the non-diversity AGC squelch feature.

3.3.10.2 Diversity Selection Testing [6.17, 6.18]

Testing of the diversity section of the ST8000 will require a second digital signal source simulation of the AGC voltage of the second ST8000 normally used in a diversity system. In particular, a 5K linear taper potentiometer and a test oscillator capable of generating a TTL-level square wave at 100 Hz will be required in addition to the equipment listed in section 3.1.1. The test connection for testing the diversity equipment is shown in Figure 3.6 below.
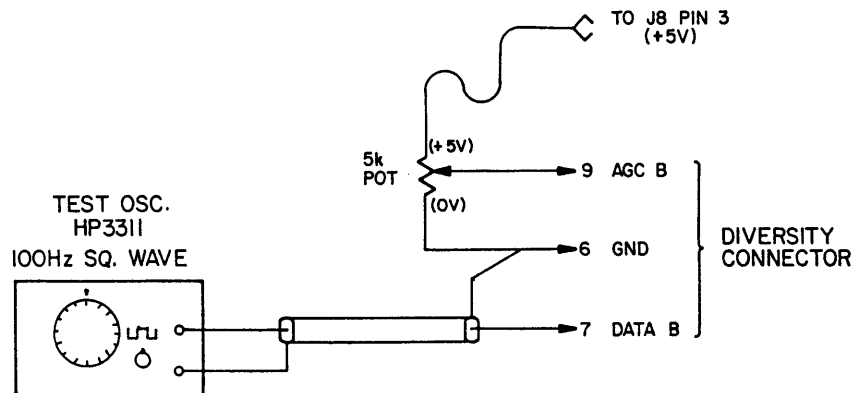
FIGURE 3.6 DIVERSITY TEST CONNECTIONS

(1) Connect the second test oscillator and 5K potentiometer as shown in Figure 3.6. The +5 VDC required for the potentiometer may be obtained by a temporary clip connection to pin 3 of J8. Be very careful to avoid shorting out this connection to adjacent pins of J3 or to any other components. The potentiometer is used to simulate the AGC voltage of a second ST8000 in a diversity system and the additional test oscillator simulates the data stream of that demodulator.

(2) Set the potentiometer so that zero volts DC is applied to pin 9 of J10 (DIVERSITY connector). Repeat the tests of the previous section to assure that the ST8000 is in the non-diversity mode of operation.

(3) Increase the potentiometer until +1.0 VDC is applied to J10-9. Observe TP33 with the oscilloscope and confirm that the signal is negative (DIV mode).

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(4)   Increase the potentiometer to +5V at J10-9 and adjust the
DIVERSITY control until a negative voltage is observed at TP23.
The "B" channel LED should now be ON and the "A" LED OFF.

(5) Connect the oscilloscope to TP31 and observe that the output
of the second test oscillator is now available, rather than that
from the original test oscillator.   This will be easy to see
since the frequencies of the two sources are different and the
oscilloscope sweep is triggered from the first rather than the
second test oscillator.

(6)   Move the DIVERSITY control in a CCW direction (toward "A")
until the "A" LED turns ON and the signal at TP31 is again that
of the original test oscillator.   The "A" and "B" LED's should
NOT be both ON at the same time.

(7)   Set the DIVERSITY control so that it is just barely on the
"A" side of the switch point. Decrease the signal level into the
ST8000 by 10 dB (to -20 dBm) and observe that the ST8000 switches
to Channel B. Reset the input level to -10 dBm when done.

(8)   Set the DIVERSITY control so that it is just barely on the
"B"   side of the switch point.   Decrease   the   external
potentiometer setting and observe that the ST8000 switches back
to channel A.   Repeat this procedure for several levels of input
to the ST8000 (-10 to -60 dBm). Reset the input level to -10 dBm
when done.

This completes testing of the diversity circuit.   Disconnect the
external potentiometer and second test oscillator. Leave   the
other test equipment connected for the following tests.

3.3.11 TX Control and Echo Circuits [6.19, 6.20]

(1)   Connect an RS232C data source to J9-2 (TERMINAL DATA
connector) and monitor pin 3 of J11a (XMTR connector) with a
continuity tester to ground.   Continuity indicates that the
ST8000 is in transmit-ON condition.

(2)   Set the front panel TX/KOS/RX switch to RX.   The ST8000
should be in RECEIVE mode (no continuity).   The front panel TX
LED should be OFF.

(3)   Set the front panel TX/KOS/RX switch to TX.   The ST8000
should be in TRANSMIT mode (continuity).   The front panel TX LED
should be ON.

(4)   Set the front panel TX/KOS/RX switch to KOS.   If the RS232
data source is generating MARK/SPACE data, the ST8000 should be
in TRANSMIT mode (continuity and TX LED ON).

(5)   Set the RS232 data source to continuous MARK condition.
After a short delay, the ST8000 should change from TRANSMIT
(continuity and TX LED ON) to RECEIVE (no continuity and TX LED
OFF). The length of this delay is controlled by R226, KOS DELAY.
Adjust R226 to the desired delay time (minimum setting is
recommended for most operation).

(6)   Briefly change the state of the RS232 data source from MARK
to SPACE and then back to MARK condition (SPACE time between 5
and 250 ms).   The ST8000 should change to TRANSMIT mode and then
back to RECEIVE after the KOS delay.   This tests the SPACE turn-
ON section of the KOS circuit (U63c, U63d).

(7)   Set the RS232 data source to send MARK/SPACE data.   The
ST8000 should return to TRANSMIT state. Interrupt the data input
with a period of continuous SPACE condition lasting several
seconds (0.5 second minimum).   The ST8000 should change to
RECEIVE mode approximately 0.5 second after the change to
constant SPACE condition.   This tests the SPACE turn-OFF
circuitry (U63a, U63b, U56a). The ST8000 should resume transmit
mode when the continuous SPACE condition is over.

(8)   Set the RS232 data source for MARK/SPACE data and the front
panel TX/KOS/RX switch to RX.   Use a ground clip to ground J9-19
(Terminal KOS input to TERMINAL DATA connector).   The ST8000
should be in TRANSMIT mode whenever J9-19 is grounded.

(9) Remove the ground clip from J9-19 and connect a clip between
J9-4 (RTS) and J9-6 (DTR = +5V).   The ST8000 should be in
TRANSMIT mode whenever J9-4 is held at a positive voltage
(V > 3.6V).

(10) Remove the clip from J9-4 and J9-6.   Observe the AFSK tone
output at TP29 with the oscilloscope. When option switch S4-5 is
ON, the tones should be present ONLY when the ST8000 is in
TRANSMIT mode.   If S4-5 is OFF, the tones should be present for
EITHER TRANSMIT or RECEIVE modes. The factory setting is for S4-
5 ON (tones ON when transmitting but not receiving).

This completes the tests of the ST8000 PTT Circuit.

(11)   With the RS232 data source still connected to J9-2 and
generating MARK/SPACE data, observe TP27 with the oscilloscope.
Set option switch S3-1 ON and S3-2 OFF.   The data pulses should
be at TP27 for either TRANSMIT or RECEIVE modes of the ST8000
(test using front panel TX/KOS/RX switch.

(12)   Change the option switch setting to S3-1 OFF and S3-2 ON.
Data should now be observed at TP27 only when in TRANSMIT mode.

(13)   Set the TX/KOS/RX switch to RX and insert a TTY signal into
the AF INPUT of the ST8000 (radio receiver RTTY output, etc).
With S3-1 OFF and S3-2 ON, the received data signal should be
observed at TP27 when in RECEIVE mode.

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(14)   Change to TRANSMIT mode (TX switch position) and note that
TP27 now reflects the RS232 input data to J9-2. When S3-1 is OFF
and S3-2 is ON, the data at TP27 (FSK and AFSK data source) is
the input transmit data in TRANSMIT mode and demodulated receive
data in RECEIVE mode.   This mode can be used when terminal echo
of TXD is required or when it is desired to record regenerated
AFSK tone data from the demodulated receive signal.   The factory
setting is with S3-1 ON and S3-2 OFF, the normal FDX, no-echo
condition for the DS3100 terminal.

(15)   The receive echo control operates in a similar manner.
Monitor the output receive data at TP31.   Set S3-5 ON and S3-3
and S3-4 OFF.   In this condition, ONLY the demodulated data will
appear at TP31, regardless of TX/RX state of the ST8000.

(16) Set S3-4 ON and S3-3 and S3-5 OFF.   In this case, RXD is
output to the terminal from demodulated data ONLY when in RX
state.

(17)   Set S3-3 ON and S3-4 and S3-5 OFF.   This is the echo
condition.   The terminal RXD output reflects demodulated data
when the ST8000 is in receive mode and transmit data when in
transmit mode. The factory setting is with S3-5 ON and both S3-3
and S3-4 OFF - no echo and no TX/RX control of RXD.

This completes the tests of the ST8000 echo circuits.

3.3.12 Power Supply [6.23, 6.24]

After completing ALL of the above tests, review section 3.3 and
remeasure the +5, -8, and +8V power supply output voltages. Log
these measurements. Compare the measurements with those of
section 3.2.   There should be no more than a +/- 0.1 VDC
difference.

3.4 CONTROL BOARD TEST [6.27 - 6.46]:

The ST-8000 Control Assembly (A2) is the microprocessor based controller for the entire modem. All of the SCF filters on the modem board use clocks generated by the control assembly synthesizers and most front panel displays and controls are handled by this controller. As is the nature of digital circuitry, there are no adjustments required on the controller board; it will either work correctly or not. Testing of the control board is only required if a failure has occured.

In this section a series of steps are outlined to insure that the on board synthesizers are working properly and are on the correct frequency. The testing of front panel switches and LED displays is contained in Section 3.5; those items will not be covered in this section. The tests require the following pieces of test equipment, or equivalent:

> FLUKE Digital Voltmeter
> HP5381 Frequency Counter
> TEKTRONIX 465 Oscilloscope

Before starting to measure oscillator frequencies, confirm that the +5 VDC supply is correct by connecting the digital volt meter between one of the ground pins on the board and the + end of the 100 uF capacitor near the 6 position power connector. The reading should be within +/- 0.25 volts of +5VDC. If the power connector is loose or improperly installed, the supply voltage may be too low for proper operation of the control board.

3.4.1 System Clock:

The system clock shown in Figures 6.33 and 6.34 controls the operation of the entire ST-8000. Both the microprocessor and the synthesizers use the same 4.9152 MHz crystal reference. To check the crystal oscillator for correct frequency, connect the frequency counter to U66-8 and measure about 4.9152 MHz. The actual processor clock is one-half this value or 2.4576 MHz which can be measured at U23-6 (Figures 6.27 and 6.28).

The transmit tone synthesizer reference clock is FTONE (819,200 Hz) from U67-9. As shown in Figures 6.33 and 6.36, the frequency counter should measure 819,200 Hz when connected to U53-11 and U52-11, the inputs to the summing latches.

All of the other synthesizers use the reference clock FMS (409,600 Hz) from U26-9 in Figure 6.34. Using the counter, confirm that the reference clock is present on U5-11, U41-11, U42-11, U43-11, U44-11, U48-11, U56-11, and U63-11. This state clock is required for the synthesizers to operate properly.

3.4.2 Synthesizer Tests:

If the synthesizer reference clocks are correct and the controller board processor is working, that is, the front panel display is correct and switch changes are recognized, the front panel may be used to set the synthesizer test values.

Each synthesizer has an input latch, a 13 or 16 bit full adder, and output state latches. The synthesizer works by continually adding the input latch value to the previous state sum to form a new sum to be latched in the output latch on the next reference clock rising edge. If a latch or an adder fails, the correct frequency will not be read on the output of the synthesizer. To test the synthesizers, two alternating bit patterns are loaded into the input latch, and the output frequency is measured.

Listed below are the counter locations, and the front panel or control port settings for each test.

MARK/SPACE Tone Generator (Fig 6.36): Counter on U54-9

        MARK = 2730   Measure: 27,300 Hz
        MARK = 1365   Measure: 13,650 Hz

MARK Filter (Fig 6.38): Counter on U43-12

        MARK = 2730   Measure: 136,500 Hz
        MARK = 1365   Measure: 68,250 Hz

SPACE Filter (Fig 6.40): Counter on U41-12

        SPACE = 2730   Measure: 136,500 Hz
        SPACE = 1365   Measure: 68,250 Hz

BAND PASS Filter (Fig 6.42): Counter on U56-12

        CENTER = 2525   Measure: 136,350 Hz
        CENTER = 1264   Measure: 68,232 Hz

LOW PASS Filter (Fig 6.44): Counter on U48-15

        IBAUD = 1066   Measure: 102,200 Hz
        IBAUD = 533   Measure: 51,000 Hz

If the synthesizer output frequencies are measured as above, the synthesizers are working correctly and do not have any stuck or shorted bits. Even a single bit error will disturb the output frequency at either the upper or the lower measurement depending on which bit is stuck.

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3.4.3 Latched Control Bits:

Figure 6.30 shows all of the latched control bits set by the
microprocessor on the control assembly board. Most of these bits
are indirectly controlled by front panel switches, thus they may
be tested with a logic probe or oscilloscope on a selected bit
while the front panel switch is operated.

In the following table, the location for the logic probe or
oscilloscope is listed with the corresponding switch that
controls the bit state. Each bit may be tested in turn.

SIGNAL	PROBE	TEST STATE
CRT CTRL	U22-6	Initially LOW. Change any front panel switch to force HIGH for 10 seconds. CRT should turn ON.
RXRGEN	U22-12	HIGH when REGEN=OFF LOW when REGEN not OFF.
NORM/REV	U22-16	LOW when POLARITY=NORMAL HIGH when POLARITY=REVERSE
AM/FM	U1-12	HIGH when DETECTOR MODE=AM LOW when DETECTOR MODE=FM
DET MODE B	U1-9	HIGH when DETECTOR MODE=MP or M/S LOW when DETECTOR MODE=MO or SO
DET MODE A	U1-5	HIGH when DETECTOR MODE=MO or M/S LOW when DETECTOR MODE=SO or MP
ANTISPACE	U1-19	HIGH when ANTISPACE=ON LOW when ANTISPACE=OFF
PTT A	U1-15	HIGH when KOS=TX LOW when KOS=RX or OFF
PTT B	U1-6	HIGH when KOS=RX LOW when KOS=TX or OFF
CTS	U1-2	LOW always

3.4.4 Latched Q Control Bits:

The modem board filter Q's are set using bits latched on the
control board as shown in Figure 6.30.   To test the Q control
bits it is necessary to connect an asynchronous terminal to the
control port so that the Q's may be directly entered, rather than
attempting to set them using the front panel controls.   At the
command prompt, enter DC for the direct control mode.

```
        *** HAL ST-8000  V?.?  ***
        AT YOUR COMMAND >> DC

        *** Direct Control Mode ***

        DC: [] >> _
```

In the table below, the Q signal, probe location, and commands
are listed.   For each setting, one value sets the bit HIGH and
the other will set the bit LOW.   If you inadvertently change a
front panel control, you will immediately be returned to monitor
mode, and will have to re-enter direct control mode.

SIGNAL	PROBE	TEST SETTING	
		QI5	QI1
		-------	-------
INPUT B	U22-5	HIGH	LOW
		QI3	QI1.5
		-------	-------
INPUT A	U22-9	LOW	HIGH
		QM33	QM1
		-------	-------
QMKHL	U22-19	LOW	HIGH
		QS33	-QS1
		-------	-------
QSPHL	U22-2	LOW	HIGH
		QS25	QS15
		-------	-------
QSPACE 3	U18-15	LOW	HIGH
QSPACE 2	U18-19	HIGH	LOW
QSPACE 1	U18-2	LOW	HIGH
QSPACE 0	U18-6	HIGH	LOW
		QM25	QM15
		-------	-------
QMARK 3	U18-12	LOW	HIGH
QMARK 2	U18-16	HIGH	LOW
QMARK 1	U18-5	LOW	HIGH
QMARK 0	U18-9	HIGH	LOW

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3.5 FRONT PANEL TEST [6.47, 6.48]:

Testing the front panel involves checking all the front panel
controls for correct operation and insuring that the LED displays
are functioning properly.   While many front panel switches and
lamps may be exercised during normal use, a better method for
testing front panel switches requires an asynchronous terminal
connected to the control port on the rear of the ST-8000.

To perform the following tests, connect an asynchronous terminal
set for 1200 bps to the control port on the ST-8000.   Set the
MARK/fc,   SPACE/SHIFT, and INPUT/OUTPUT switches in the UP
position.   Press a RETURN key to confirm that the ST-8000 is
properly connected.

                    *** HAL ST-8000 V?.? ***
                    AT YOUR COMMAND >> _

3.5.1 Display Tests:

It should be obvious whether the three frequency displays are
operating correctly.   However, several simple commands will show
missing display segments.   To turn all significant front panel
segments ON, enter the following commands:

                    *** HAL ST-8000 V?.? ***
                    AT YOUR COMMAND >> FP

                    *** Front Panel Mode ***

                    FP: []>> SH1000;M2888;IB888<CR>
                    FP: [IBAUD=0888]>> _

Now, check for any segments that are not lit.   If there are no
bad segments, the front panel display digits should show the
following frequencies:

          MARK   SPACE   BAUD RATE
          ----   -----   ---------
          2888   3888   0888

Enter the exchange command to confirm that the left most digit in
the MARK display is operating correctly:

               FP: [IBAUD=0888]>> EX
               FP: [IBAUD=0888]>> _

The front panel should display:

MARK	SPACE	BAUD RATE
3888	2888	0888

If the front panel digits display these values correctly, there
are no dead segments in the three display windows. To test other
digits, frequencies may be entered on the terminal for immediate
display on the front panel.

3.5.2 Front Panel Switches:

The operation of several front panel switches may be tested using
the control terminal. Return the control terminal to monitor
mode by changing some front panel switch. If the control port
was in Front Panel mode, it will return to monitor mode with the
message:

        *** Leaving Console Control Mode ***

To see the current front panel switch settings, enter the status
command:

            *** HAL ST-8000 V?.? ***
            AT YOUR COMMAND >> STC

A summary of all front panel rotary and toggle switches is
presented in response to this command. Each switch, in turn, may
be changed and that change should be reflected the next time the
STC command is issued. For example, if the current status shows
that the ANTISPACE switch is OFF, press the switch ON and enter
the STC command. The "ANTISP=ON" listing will appear in the
summary if the switch is working properly. Should some switch
changes not cause status summary changes, it is possible that the
switch or buffer has failed.

The display selection mode switches may be tested by operating
the switch and observing a change in the corresponding display.
For example, if the MARK/fc switch is moved from UP to DOWN, the
MARK display should change from the MARK frequency to the center
frequency. If no change occurs, the switch may have failed.

The tuning mode switch may be tested by actually changing the
MARK, SPACE, and BAUD RATE displays using the front panel tuning
knob. When the ST-8000 is in the VAR tuning mode, some display
should change when the tuning mode control is in each position.
The correct display is shown on the front panel legend.

The memory selection switch may be tested by selecting the fixed
memory mode, then changing the memory selection. The front panel
should change to the setup parameters stored in each of the 10
memories. After selecting one of the memories, press the STORE
button to confirm that the front panel displays flash indicating
that the STORE button is working.

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3.6 CRT ALIGNMENT AND TEST [6.49, 6.50]:

Test and alignment of the CRT Assembly (A4) should be done only
if the MODEM (A1), CONTROL (A2), and FRONT PANEL (A3) assemblies
are in proper operating condition.   If any of these assemblies
are suspect, refer to the previous sections of this chapter and
fix the problems before attempting alignment of the CRT assembly.

***** CAUTION *****

USE EXTREME CARE WHEN TESTING OR ADJUSTING THE CRT ASSEMBLY.
LETHAL VOLTAGES IN EXCESS OF 1400 VDC ARE EXPOSED ON THE CRT
CIRCUIT BOARD AND ON THE CRT SOCKET CONNECTIONS.   THE HIGH
VOLTAGE POWER SUPPLIES REQUIRE APPROXIMATELY 30 SECONDS TO DECAY
TO SAFE LEVELS AFTER AC POWER IS TURNED OFF.   DO NOT TOUCH ANY
HIGH-VOLTAGE COMPONENTS WITHOUT FIRST TURNING AC POWER OFF AND
SHORTING BOTH -1400V (C1 NEG. LEAD) AND +135V (C5 POS. LEAD)
OUTPUTS TO CHASSIS GROUND.

3.6.1 Initial Set-up:

Review section 3.3.5 of this chapter and confirm that the ST8000
switches and parameters are set as described.   Connect the test
equipment as shown in Figure 3.5. The ST8000 AFSK generator will
be used as the signal source for these tests. Set the data input
test oscillator to a frequency of 50 Hz with peak amplitudes of
+5 and -5 V.

3.6.2 CRT Trace Control Adjustments:

(1)   Observe the CRT trace.   It should show a crossed ellipse
with Spectra-Tune   display line.

NOTE: The INTENSITY, FOCUS, and ASTIG control settings will
interact to some degree.   In the following steps, choose the
desired setting of INTENSITY and then adjust FOCUS and ASTIG as
required.   Repeat the following 3 steps until optimum balance is
achieved.

(2)   Adjust the INTENSITY control (R7) for your preferred trace
brightness.

(3)   Adjust the FOCUS control (R9) for best focus of the CRT
trace. For a first setting, adjust for best trace clarity at
center screen and then re-adjust after setting ASTIG (following
step).

(4)   Adjust the ASTIG control (R10) to improve trace focus over
the whole screen. This control will interact with the setting of
the FOCUS control.   The effect of the ASTIG control is best seen
at the ends of the ellipses and in the Spectra-Tune   section of
the trace.

Repeat steps (2), (3), and (4) as required to get best trace presentation.

(5) Observe the X-Y ellipses on the CRT screen. They should be centered on the crossed graticule lines at the center of the screen. If not, adjust the HORIZ (R30) and VERT (R31) position controls so that the ellipses are centered.

(6) The X-Y ellipses should be aligned with the graticule lines in vertical and horizontal directions. The TRACE ROT control (R22) should be adjusted to rotate the trace for best X-Y alignment. If adjusting R22 rotates the trace in the wrong direction, unplug connector J3 from the CRT board, reverse the plug, and reconnect it to the circuit board. Adjust TRACE ROT for best X-Y alignment.

(7) Be sure that the ST8000 DETECTOR MODE switch is set to FM-M/S mode and observe the length of the horizontal and vertical ellipses on the CRT. Adjust "X" (R52) and "Y" (R53) controls so that both ellipses have a length of 4 graticule marks (+/- 2 marks about center).

3.6.3 CRT Spectra-Tune   Adjustments

(1) Disconnect the data test generator from the TERMINAL DATA connector (J9). The AFSK generator should be in the MARK state at 2125 Hz as indicated by a horizontal ellipse on the CRT X-Y display.

(2) Connect the oscilloscope vertical input to TP1 on the CRT circuit board. A square wave form at 2125 Hz should be observed. Decrease the input level to the ST8000 until the waveform is sinusoidal with slight clipping of the peaks. Adjust the BAL control (R28) to obtain symmetrical clipping of the sine wave. It may be necessary to readjust the input level slightly to maintain clipping of both the positive and negative peaks. The limiting threshold typically occurs at an input level of -40 to -30 dBm and is not critical.

(3) Connect the oscilloscope to TP6 and observe a 90-120 Hz rectangular waveform. The duty cycle of this waveform is approximately 30%. This is the chopper oscillator output that controls the switching of the CRT trace between the crossed-ellipse and Spectra-Tune displays. If this waveform is NOT present, refer to section 3.8 and fix the problem before continuing the following steps.

(4) Observe the vertical position of the Spectra-Tune bar at the bottom of the CRT display. Adjust the FREQ V. ADJ control (R32) so that this bar is positioned above the horizontal frequency graticule line.

(5)   Set the ST8000 VAR-RX/TX switch to the left hand position
and the TUNING MODE switch to TRACK. Use the MAIN TUNING knob to
reduce the indicated MARK frequency to 2000 Hz.   Observe the
horizontal position of the Spectra-Tune bar and adjust the CENTER
SCALE control (R29) so that the bar is positioned at the 2 kHz
graticule calibration mark.

(6) Use the MAIN TUNING knob to set the indicated MARK frequency
to 3000 Hz.   Observe the horizontal position of the Spectra-
Tune bar and adjust the SCALE CAL control (R54) so that the bar
is positioned at the 3 kHz graticule calibration mark.   NOTE:
ALWAYS make the adjustment of step (5) before setting the SCALE
CAL control.

(7) Check the frequency scale calibration by retuning the ST8000
to 1000 Hz (MARK frequency).   The Spectra-Tune bar should be
positioned at the 1 kHz graticule calibration mark.

This completes the alignment of the CRT assembly (A4).

3.7   OTHER ST8000 TESTS AND MEASUREMENTS

The previous six sections have described all of the standard
alignment tests required for the ST8000 HF MODEM.   Successful
completion of the steps should assure that the ST8000 is
operating at factory specification. A number of additional tests
have been performed at the factory to confirm ST8000 performance.
It should not be necessary for the user to conduct these tests,
but their results are included in this section.

3.7.1   Receive Data Processing Delay

Whenever signals pass through filter and processing stages, a
time delay is added to the signal.   If the time delay is uniform
between MARK and SPACE pulses and does not vary with signal
amplitude, the delay does not contribute distortion and has no
net effect on the data printed. Great care has been taken in the
design of the ST8000 to assure that the MARK and SPACE signals
are processed through circuits with equal bandwidth and equal
time delay.

The major contributors to time delay in the ST8000 are the filter
stages, in particular the MARK and SPACE tone filters and post-
detection low-pass filters.   The total time delay is therefore
controlled primarily by the setting of the INPUT BAUD control
which controls the bandwidth of the tone and low-pass filters.
When the front panel controls of the FP mode of REMOTE control is
used, the time delay is approximately equal to the width of the
select pulse of the chosen data rate.   Using a lower indicated
INPUT BAUD setting increases the delay and a higher setting
reduces the delay.   Typical time delays measured on the ST8000
demodulator circuitry are shown in Table 3.2.

TABLE 3.2
TYPICAL ST8000 DEMODULATOR TIME DELAYS

DATA RATE (Baud)	INPUT BAUD SETTING	---- DELAY (msec) ----	
		2125/2295	2125/2975
45	45	19.6	17.6
45	75	12.4	11.6
45	100	10.0	8.7
50	50	18.1	16.1
75	75	12.4	11.6
100	100	10.0	8.7
150	150	7.5	6.2
200	200	6.2	4.8
300	300	4.6	3.6
300	300	[2225/2025] ----	4.6
300	300	[1270/1070] ----	4.6
450	450		2.8
600	600		2.1
900	900		1.70
1200	1200		1.56
1200	1200	[1200/2200] ----	1.70

A difference in the demodulation delay between MARK and SPACE conditions appears in the data output as bias distortion. Measurements of the ST8000 have shown that such bias distortion is of the order of 1.5 to 2.0 % SPACE bias.

The delay associated with MARK/SPACE switching of the AFSK transmit tones is very minor since the tone frequency is divided by 100 after M/S switching. The worst case AFSK tone delay is equal to 0.01 times the period of the lower of the two tone frequencies (4.7 usec for 2125/2295 Hz tones, for example). This corresponds to less than 0.02% MARK bias distortion at 45 baud and 1.0% for 1200 baud and 1200/2200 Hz tones.

3.7.2 BIT ERROR RATE TESTS

The measurement of demodulator bit error rate (BER) for various signal-to-noise ratios (S/N) is a common criteria for judgment of demodulator performance. In this test, a known amplitude of RTTY signal is mixed with a controlled amount of random noise. The demodulated output data stream is then compared with that sent and the number of bit errors counted in a Bit Error Rate Tester (BERT). Typically, the test is run for a total of 10,000 to 1,000,000 bits and the result is expressed graphically on plots of BER vs S/N. Several different measurement standards are used, particularly when expressing the bandwidth of the data and noise signals.

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Bit Error Rate test have been conducted on the ST8000 under the following conditions:

            Number of samples = 1E5 or 1E6 (100,000 or 1,000,000)
                  Data Format = 2047 random bit pattern,
                                 synchronous data
                    Data Rate = as indicated
             Signal Bandwidth = determined by the ST8000
                                 INPUT BAUD control
              Noise Bandwidth = 2100 Hz (standard HF radio
                                 receiver bandwidth)
          Signal input level = -10 dBm
          AFSK Signal Source = ST8000 AFSK generator
           Noise input level = -10 dBm = 0 dB S/N,
                                 varied for other S/N values.

Figure 3.7 shows typical measured Bit Error Rates for various data rates. These are typical values and may vary from unit-to-unit by +/- 0.5 dB. These curves are within 1.0 dB of the theoretical optimum values for incoherent FSK demodulation. It is informative to note the following general rules:

   1. For each doubling of the data rate, the required S/N is
       increased by 3 dB to maintain a constant Bit Error Rate.

   2. The slope of the BER curves at error rates of 1E-5 to 1E-4
       is approximately 1 dB for each octave of BER; a 1 dB
       decrease in S/N will approximately double the number of
       errors printed.

   3. Decreasing the demodulator bandwidth with the INPUT BAUD
       control will decrease the BER, but ONLY at the expense of
       increased inter-symbol distortion (not apparent from BER
       curves). The ST8000 bandwidth at 0.75 the data rate is
       a proven compromise between minimum BER at 0.5 the data
       rate and minimum inter-symbol errors at a higher bandwidth.

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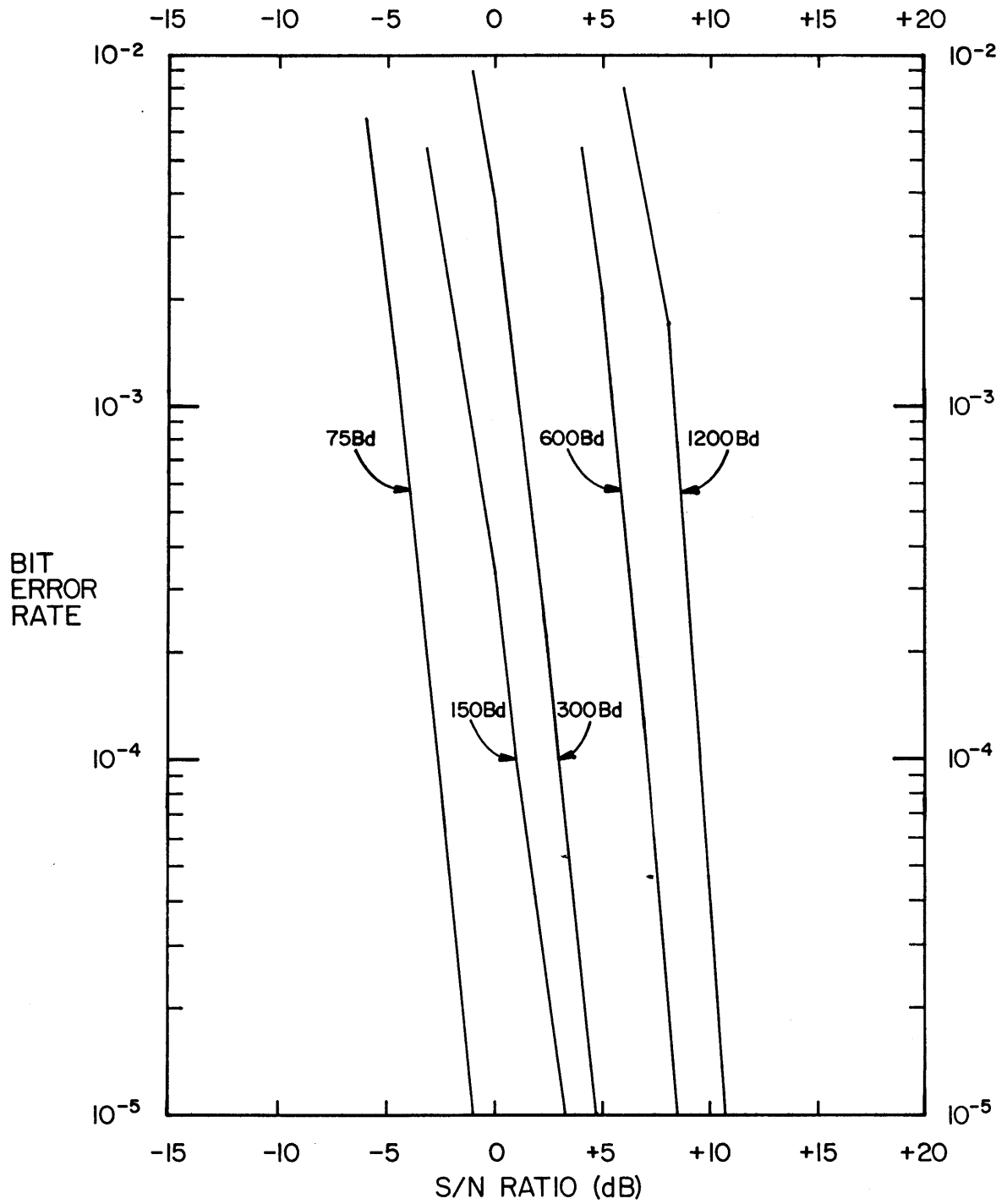
FIGURE 3.7   BER TESTS

The reader is cautioned that, although Bit Error Rate
measurements are a recognized indicator of modem performance, the
results obtained may not give a true indication of the actual
modem capabilities on typical high-frequency data signals.
Received radio FSK signals experience fading, distortion, and
burst noise phenomena which is not simulated by use of a constant
output random noise source. Observation of actual off-the-air
signals must remain an important test of modem performance.
Comparative tests of modems with similar BER curves on off-the-
air signals have shown a considerable difference in printed error
rates between the otherwise similar units. Several tests run at
HAL on the ST8000 and other modems of comparable performance and
price have shown the ST8000 to have a consistently lower rate on
off-the-air signals. The performance difference varies between a
factor of 2:1 for a MPC1000 and 100:1 for a 1280 demodulator.
These tests are, by nature, subjective and the user is encouraged
to make his own comparative tests.

It is the observation of HAL and HAL's customers that HF Modem
performance is related to BOTH low distortion (low Bit Error
Rate) and a high dynamic range. As shown in Figures 2.2 and 2.3,
the ST-8000 has a very wide dynamic range achieved by close
attention to receiver design practices. The depth of
high frequency differential Mark/Space fades often exceeds 50 dB.
The noise floor of current heterodyne-type HF demodulators is -30
or -40 dBm at best, giving poor recovery of deep selective fading
signals. The -70 dBm noise floor of the ST8000 provides 30 to
40 dB of additional dynamic range, assuring improved signal
recovery. The ST-8000 therefore exhibits a low Bit Error Rate
over this very wide dynamic range.

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CHAPTER 4. MAINTENANCE AND REPAIR

Typical repair and trouble-shooting techniques are presented in this Chapter. Frequent references will be made to sections of Chapter 2 (Technical Description), Chapter 3 (Test and Alignment), and to the diagrams in Chapter 6. A thorough study of Chapters 2 and 3 is recommended before attempting repair of the ST8000 HF MODEM.

4.1 ESD PRECAUTIONS

As noted earlier, the ST8000 uses CMOS and other Electrostatic Discharge Sensitive (ESDS) devices. The following precautions must be observed when repairing the ST8000.

ADVANCED CMOS AND MOS CIRCUITRY IS USED THROUGHOUT THE ST8000. USE OF AN ELECTROSTATICALLY PROTECTED WORK STATION IS HIGHLY RECOMMENDED IF ANY OF THE CIRCUIT BOARDS ARE REMOVED FROM THE ST8000 CABINET. AN ELECTROSTATIC PROTECTED WORK STATION INCLUDES GROUNDED TABLE AND FLOOR MATS AS WELL AS A GROUNDED WRIST BRACELET.

IF A CIRCUIT BOARD IS REMOVED FOR SHIPMENT TO HAL, IT SHOULD BE PLACED IN A BLACK CONDUCTIVE PLASTIC ENVELOPE WHILE AT THE ESD WORK STATION. THE BOARD MAY THEN BE HANDLED FOR FURTHER PACKAGING AT AN UNGROUNDED WORK STATION (BOX REQUIRED). FAILURE TO FOLLOW THESE PROCEDURES MAY CAUSE DAMAGE TO THE ST8000 CIRCUITRY AND VOIDS ALL HAL WARRANTIES. UNLESS THE TECHNICIAN HAS BOTH AN ELECTROSTATIC WORK STATION AND TRAINING IN ITS PROPER USE, IT IS HIGHLY RECOMMENDED THAT THE ENTIRE ST8000 BE RETURNED TO THE HAL FACTORY FOR ALL BOARD-LEVEL REPAIRS.

WHEN THE CIRCUIT BOARDS ARE MOUNTED IN THE CABINET, THE ST8000 IS NO MORE SUSCEPTIBLE TO ESD THAN OTHER ELECTRONIC EQUIPMENT. IT MAY BE OPERATED AND TESTED WITHOUT REQUIREMENT FOR AN ESD WORK STATION. HOWEVER, THE ST8000 CABINET AND ALL TEST EQUIPMENT MUST HAVE THEIR CABINETS INTERCONNECTED THROUGH A COMMON GROUND SYSTEM (AC GROUND PLUG IS ACCEPTABLE). FURTHERMORE, THE ADDITIONAL PROTECTION OFFERED BY AN ESD WORK STATION IS HIGHLY RECOMMENDED FOR ALL SERVICE AND MAINTENANCE PROCEDURES.

PARTICULAR CARE IS REQUIRED WHEN REMOVING AND INSERTING KNOWN ESDS DEVICES. IN THIS CASE, THE TECHNICIAN MUST USE AN ESD WORK STATION, WEAR THE GROUNDED WRIST BRACELET, AND USE ACCEPTED HANDLING TECHNIQUES FOR ESDS DEVICES. IN PARTICULAR, THE COMPONENTS LISTED IN TABLE 4.1 ARE RECOGNIZED ESDS DEVICES AND REQUIRE SPECIAL HANDLING:

TABLE 4.1
ELECTROSTATIC SENSITIVE DEVICES

PART	DESIGNATOR(S)	SCHEMATIC	ASSEMBLY
Z80A	U23	6.28	A2 (CONTROL)
2764	U10, U11	6.28	A2 (CONTROL)
LM2917	U2	6.50	A4 (CRT)
4001	U60	6.16	A1 (MODEM)
	U56	6.20	A1 (MODEM)
4002	U64	6.20	A1 (MODEM)
4011	U40	6.14	A1 (MODEM)
	U58	6.16	A1 (MODEM)
	U34	6.18	A1 (MODEM)
	U54, U55	6.20	A1 (MODEM)
4017	U61	6.22	A1 (MODEM)
4023	U48	6.16	A1 (MODEM)
4025	U59	6.16	A1 (MODEM)
4030	U39	6.14	A1 (MODEM)
	U39	6.16	A1 (MODEM)
	U62	6.20	A1 (MODEM)
4049	U49	6.14	A1 (MODEM)
	U35, U49	6.16	A1 (MODEM)
	U35	6.18	A1 (MODEM)
	U63	6.20	A1 (MODEM)
4052	U51, U44	6.4	A1 (MODEM)
4053	U14	6.6	A1 (MODEM)
	U3	6.50	A4 (CRT)
4066	U2, U5, U6	6.8	A1 (MODEM)
	U2, U16, U25	6.10	A1 (MODEM)
R5613	U11, U27	6.12	A1 (MODEM)
R5614	U41	6.4	A1 (MODEM)
R5615	U42	6.4	A1 (MODEM)
R5616	U43	6.4	A1 (MODEM)
R5621	U17	6.8	A1 (MODEM)
	U26	6.10	A1 (MODEM)
74HC151	U38	6.14	A1 (MODEM)
74HCT374	U1, U18, U22	6.30	A2 (CONTROL)
	U15, U16, U17	6.36	A2 (CONTROL)
	U19, U21	6.38	A2 (CONTROL)
	U19, U20	6.40	A2 (CONTROL)
	U59, U60	6.42	A2 (CONTROL)
	U8, U45	6.44	A2 (CONTROL)
	U7, U9, U10, U11	6.48	A3 (F.PANEL)
8251	U37	6.32	A2 (CONTROL)
8253	U14	6.32	A2 (CONTROL)
8470A	U36	6.32	A2 (CONTROL)
9128	U12, (U13)	6.28	A2 (CONTROL)

4.2 FACTORY RETURN PROCEDURES

In the event that the ST8000 must be returned to the HAL factory
for repair, the following procedures must be followed:

1. Write or phone the HAL factory (217-367-7373) and discuss the
problem with our staff.   We may be able to fix some obvious
problems without returning the ST8000 to the factory.

2.   If return is required, HAL will issue return authorization
(verbally   or in writing).   HAL will need the   following
information before authorizing return of any equipment:

     (a)   NAME of firm or individual
     (b)   SHIPPING ADDRESS for UPS return shipping
           (NO P.O. BOX numbers, please)
     (c)   Model and serial number of unit to be returned.
     (d)   When and where the unit was purchased.
     (e)   A brief description of the problem.
     (f)   An acceptable means of payment for the repair.
           (Check or Charge Card No. for individuals, check
           or P.O. number for credit approved firms.)

(3) The payment policy for HAL factory repairs are as follows:

     (a)   The is NO charge for repairs covered under the
           HAL LIMITED WARRANTY (see last page of ST8000
           OPERATOR'S MANUAL).

     (b)   If an otherwise in-warranty piece of equipment
           is returned to HAL and our personnel can discover
           NO problems with the unit, there WILL BE a charge
           for the time required to test the equipment.

     (c)   Non-warranty repairs or repairs necessitated by
           non-warranty applications (improper treatment,
           lightning, etc.) will be billed at the prevailing
           HAL labor plus materials rates. Arrangements for
           payment of this bill MUST be made before the equipment
           will be shipped to the customer.

     (d)   Shipping charges for shipment of the equipment to
           HAL must be paid by you, the customer. This policy
           is the same for in-warranty or non-warranty equipment.

(e) Shipping charges for return of valid warranty repaired
    equipment to the customer will be paid by HAL. This
    policy is limited to shipment to addresses within
    the 48 continental United States for "Brown" UPS or
    equivalent shipping. Express shipping is available at
    customer expense.

(f) Shipping charges for return of non-warrant repaired
    equipment to the customer are to be paid by the customer.
    Shipping charges will be added to the customer's repair
    bill. Please specify the preferred method of shipment.

(g) HAL cannot give estimates of repair costs. The
    true costs are not known until the repair is complete.
    If requested, HAL will visually inspect the equipment
    upon receipt and contact the customer if extensive
    repair costs are anticipated.

4. Carefully package the ST8000 in the original carton or
equivalent. Be sure to REMOVE the spinner knob from the MAIN
TUNING control on the ST8000. Do NOT return any accessories
unless you suspect that they are related to the problem. Include
INSIDE the carton a written copy of the information listed above
in item number 2.   Be sure to put your or your firm's name and
address on BOTH the internal note and on the OUTSIDE of the
shipping carton.   Insure the complete package for the full
purchase price with your shipping carrier.   In the continental
U.S. use UPS shipping if at all possible.

5. The factory shipping address is as follows:

            HAL COMMUNICATIONS CORP.
            1201 W. KENYON RD.
            URBANA, IL 61801
              ATTN: REPAIR DEPARTMENT

            DO NOT USE THE P.O. BOX NUMBER
            FOR A RETURN SHIPPING ADDRESS!

6. The time required for repairs varies greatly with
availability of parts and current repair personnel work-load.
HAL will do all in its power to assure a timely return of
repaired equipment.

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4.3 TEST EQUIPMENT

The following test instruments or their equivalents are essential
to proper test and repair of the ST8000 HF MODEM:

```
HP400FL AC VOLTMETER (+30 to -80 dBm @ 600 ohms
HP3311 FUNCTION GENERATOR (20 to 20,000 Hz, +10 to -30 dBm)
HP5381A FREQUENCY COUNTER (20 Hz to 10 mHz)
HP122A OSCILLOSCOPE (DC to 10 mHz)
FLUKE 77 MULTIMETER (AC, DC VOLTS, 20 mV to 1500 V)
FLUKE 80K-6 HV PROBE (6 kV AC/DC probe)
600 Ohm Step Attenuator (0 to -70 dB in 1 dB steps)
Source of RS232C Digital Data (DS3100 ASR Terminal)
Source of Audio RTTY Signals (Radio Receiver or Tape)
Electrostatic Work Station (3M 8031 Kit)
```

4.4 MODEM ASSEMBLY MAINTENANCE

Repair of any electronic device requires two steps: (1) the
problem must first be isolated to a general area of the
circuitry, and then (2) the defective part(s) must be located and
replaced.   Execution of all the alignment and test instructions
in Chapter 3 will lead to a logical isolation of the problem
area.   However, a careful study of the block diagram coupled with
a working knowledge of information in Chapters 2 and 3 will often
produce a more rapid isolation of the problem area.   This section
presents some typical failure modes and obvious areas to be
checked.

4.4.1 Power Supply

Problems in the ST8000 power supply section will generally be
quite obvious, evidenced by failure of front panel lamps, CRT
trace, or totally improper ST8000 operation.   Consider the
following suggestions:

(a) Check the power cord, fuse, AC power switch, and transformer
primary connections.

(b) Check for loose connectors and other obvious physical
problems.

(c) Refer to section 3.2 and check the voltages.   A high, low,
or zero voltage output is indicative of a failure of the power
transformer, rectifiers, filter capacitors, regulator IC's, or a
short-circuit on the power supply bus. Shorts on the +5V and +/-
8V power buses can be isolated to a given circuit board assembly
by selectively disconnecting power connectors on the MODEM board
(A1). The appropriate connectors and cables are shown in Figures
6.52 and 6.53.

(d) The three-terminal regulator IC's in the ST8000 have internal high-current protection. In the case of a current overload, their output voltage will reduce to a low value (1.0 volt or less) without damage to the regulator IC itself. If very low output voltages are measured, first test for a current overload BEFORE replacing the IC. However, an output voltage more than 10% greater than the nominal value is usually indicative of a defective regulator IC, particularly if the AC ripple on the regulated output is the same as that on the unregulated input to the IC.

(e) A failure of the tantalum capacitors on the unregulated input of any of the regulator IC's (1.0 uF for +5V and 0.33 uF for +8V and -8V regulators) may cause the regulator IC's to oscillate. The oscillation may cause an abnormal output voltage (low or high) as well as a high frequency signal superimposed on the DC output. Some defective regulator IC's may also oscillate, even with a good input capacitor.

(f) A failure of the -1400V or +135V high voltage power supplies on the CRT assembly (A4 - Figures 6.49 and 6.50) is generally caused by failure of a filter capacitor (C1 through C6), although it may also be caused by a defective power transformer, rectifier(s), or arcing on the CRT board or socket.

4.4.2 Receive Data Filters

Refer to the block diagram of Figure 6.2 and note the flow of the signal from the AUDIO INPUT jack to the MARK and SPACE detectors. If proper MARK and SPACE ellipses are shown on the CRT, the input signal has been passed by the intermediate stages. If proper MARK and SPACE ellipse are NOT observed, the following suggestions are offered.

(a) Check that the cable between the receiver or other audio RTTY source is properly connected and plugged into the ST8000 AUDIO INPUT jack.

(b) Check that the proper settings are made on option switch S1 (see section 2.2 of the ST8000 OPERATOR'S MANUAL).

(c) Refer to section 3.3.2 and perform the indicated tests. Tracing of the signal through TP1, TP4, TP5, TP8, TP9, and TP10 will help isolate the problem to one stage. If the signal is traced through TP10 (both AM and FM modes) and no X-Y ellipses are observed on the CRT, be sure that PRINT SQUELCH and DIVERSITY are set at full CCW (counter clock-wise) positions and then skip to sections 3.6 and 4.7 to fix the CRT assembly (A4).

(d)   Failure of the signal to pass through any of the Switched
Capacitor Filters (SCF - U41, U42, U43, U17, or U26) indicates
either lack of clock signal (TP2 for U41, U42, and U43; TP14 for
U17; TP18 for U26) or failure of the IC itself.   If the clock
signal(s) is not found, skip to sections 3.4 and 4.5 to fix the
appropriate   synthesizer   on   the   CONTROL   assembly   (A2).
Replacement of U41, U42, or U44 does not require re-alignment,
but it is desirable to re-check the filter bandwidths as
explained in section 3.3.2.   Replacement of any component in the
MARK or SPACE filters requires realignment as described in
section 3.3.4.

(e)   Problems in the LIMITER stage (U31) are generally related
to a failure of U31, a type 709 operational amplifier. If U31 is
replaced, the LIMITER must be re-aligned (section 3.3.3).

(f) AGC amplifier problems are generally related to U30 or U22,
type MC3340 IC's.   In particular, a defective U30 device may
produce low-frequency oscillation of the AGC-regulated output at
TP9. If U30 or U22 are replaced, the AGC amplifier must be re-
aligned and calibrated (section 3.3.3).

(g)   Receive a valid RTTY signal (2125/2975, 50-100 baud) and
observe the crossed ellipses on the CRT while changing the INPUT
BAUD setting from a low to a high data rate. The ellipses should
gradually become wider at the higher data rates, increasing in
small increments.   Lack of change in the ellipse size or drastic
changes are indicative of either a problem in the Q selection
circuits (U2, U5, and U6 for MARK at TP45; U2, U16 and U25 for
SPACE at TP41) or in the control signals from the CONTROL board
(A2).   Replacement of any component in the MARK or SPACE filters
[6.8 to 6.10] requires complete re-alignment and calibration of
the affected filter (section 3.3.4).

4.4.3 Receive Data Processing

A failure of the tests described in sections 3.3.7 will generally
be related to a defective IC (Figure 6.12) or to lack of the LP
FILTER clock signal at TP50.   If any of these IC's are replaced,
the alignment procedures of section 3.3.7 must be repeated.
Refer to sections 3.4 and 4.5 if a clock signal is not observed
at TP50.

Performance of the tests described in section 3.3.8 will isolate
any detector problems to the affected stage.   Any of the IC's
shown in Figure 6.14 may be replaced without realignment. If the
PRINT SQUELCH circuit fails, be sure to check that the control
voltage from the front panel control is actually present at U29,
pin 6.

Many control signals interact in the RX DATA CONTROL circuitry shown in Figure 6.16. Follow the tests of section 3.3.9 and note carefully the point at which proper signal flow ceases. Faults in these circuits will be due to either a failure of an IC shown in the diagram or failure of a signal from another circuit (DIV, SQA, etc.). Correct signal polarities are shown on Figure 6.16 to assist to tracing data and control signals. No re-alignment is required for replacement of any parts shown in Figure 6.16. Because of their direct connection to a potentially "hostile" outside environment through the TERMINAL DATA connector (J9), the IC's on the right-hand side of Figure 6.16 should be given careful evaluation. This is especially important if lightning or power-line transients are suspected to be the cause of an ST8000 failure.

4.4.4 Diversity Circuitry

Refer to section 3.3.10 and perform the tests indicated. Be SURE that jumper JP1 is installed. The diversity circuit will NOT work without this jumper in place! Failure of the non-diversity mode of operation may be due to a defect in U46b, U45b, U53b, U47a, U53f, U35, U34, or C100 (see Figure 6.18). Failure of the diversity mode of operation may be caused by a defect in U46a, U45a, U47a, U53a, U53f, U35, U34 C72, or C73 (see Figure 6.18). Failure of BOTH modes may be caused by lack of a jumper at JP1 or a failure in stages U36, U47, U53, or U34. No re-alignment is necessary when components of the diversity stage are replaced.

4.4.5 TXD Control

Failures associated with transmit data (TXD) input are most likely associated with failures of transistors Q5 or Q6 due to application of improper input voltages or transients. Also, check that JP3 is NOT installed (not used for normal operation) and that pulses pass through the REGEN circuit on the CONTROL assembly (A1).

Check to see that the TXD pulses are observed at TP27. If not, check the setting of option switches S3-1, S3-2 and S3-3. Only ONE of these switches should be ON at a time (S3-1 = ON is normal). Review section 2.3 of the ST8000 OPERATOR'S MANUAL for option choices. If TXD pulses are still not observed at TP27, IC62 may be defective.

Observe the FSK output pulses at J9-11. Be sure that either S4-3 or S4-4 are ON (NOT both) and that S4-1 or S4-2 is ON (NOT both). Failure of this output is probably due to failure of transistor Q7. Review switch setting instructions in section 2.3 of the ST8000 OPERATOR'S MANUAL for proper option switch settings.

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4.4.6 AFSK Generator

The AFSK generator (Figure 6.21) synthesizes a sine wave from a signal provided by the synthesizer on the CONTROL assembly (A2). Perform the tests described in section 3.3.5 and note deviations from the specified values. Be SURE that the front panel TX/KOS/RX switch is in the TX position. Also, recheck the settings of option switch S2 as described in section 2.3 of the ST8000 OPERATOR'S MANUAL. In particular, switches S2-2 and S2-3 must not both be ON and switch S2-5 should be OFF when AFSK output is tested. If S2-5 is ON (FSK output), BOTH S2-2 and S2-3 must be OFF and S2-4 ON. Lack of AFSK output may be caused by defective components U61, U65, T2, or by no input AFSK signal at TP26 from the CONTROL assembly (A2). No output may also be caused by incorrect setting of the AFSK LEVEL control (R295) or by improper settings of options switch S2. Replacement of components in the AFSK section (Figure 6.36) does not require re-alignment although you may wish to re-set the AFSK LEVEL control (R295) to the desired level.

4.4.7 Transmitter PTT Control

Refer to section 3.3.11 and perform the indicated tests. Failure of the TX/RX switching circuitry is most probably due to a defective PTT relay (KY1) or to a failure of stage U56b (no front panel TX/RX control) or to stage U64b (no switch, KOS or RTS control). Failure of the KOS circuit is probably due to improper setting of control R226 (KOS delay), but may also be due to a failure in stages U63, U56a, and U64a. Also, check capacitors C140 and C106 in case of KOS circuit failure.

4.5 CONTROL ASSEMBLY MAINTENANCE

The ST-8000 control board is a microprocessor based controller for the HF modem board and the front panel. Since most of the front panel displays and switches are under the direct control of this processor, many failures on the control board will result in readily apparent operational problems.. It is important to analyze the failure characteristics before attempting to isolate the problem. Spending additional time examining the problem will hasten unit repair.

Generally, the control assembly problems fall in one of two classes: component failure or hardware interconnection failure. This section will deal with both areas. Since there are no analog adjustments on the control board, it is not possible for any circuit to fall out of alignment. As is the nature of digital circuits, the control board should provide trouble free operation for the lifetime of the product.

In this section, only the control assembly is considered; see Section 4.6 for a discussion of front panel problems.

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4.5.1 Component Failure

Component failure where a component is destroyed fully or partially may be due to natural aging and heat, line voltage transients, static discharge, or vibration. Clearly, a destroyed component may cause operational problems. However, not all failures are necessarily due to a component failing; it may simply cease to function properly in the circuit. Usually, the later problem is caused by the unintentional bending under of a pin on an integrated circuit when it is installed. During all the production tests and burn-in, the unit performs to specifications, but over a period of time, vibration or temperature cycling may cause the bent pin to pull away from the socket connection. When attempting to isolate board failures, examine suspect integrated circuits for bent pins.

The control board is designed with LS, HCT, and NMOS components. All of these parts are relatively immune to normal power supply variations and handling, however when removing any circuit from the control board, be certain that you are well grounded to avoid introducing a static discharge on the board. Since all of the integrated circuits are socket mounted, replacement is straight forward. All HCT components should be replaced with HCT not LS to avoid internal bus loading problems.

4.5.1.1 Clock/Reset Failures

Since the control board is microprocessor based, a crystal oscillator operating at 4.9152 MHz is provided to control both the microprocessor and the synthesizer clocks. Without this oscillator, shown in Figure 6.34, the entire ST-8000 will appear to be dead, the front panel flashing colons will not be functioning, and one or more display digits will be OFF.

To test the clock, measure the clock frequency at U66-8 and confirm that it is near 4.9152 MHz. Either the crystal or U66 may have failed if this clock is not present.

If the crystal is oscillating, measure the frequency at U68-5 and confirm that it is near 2.4576 MHz. If this clock is present, but the unit is not working, the microprocessor U23 may have failed. If the clock is not present, replace U68.

The ST-8000 uses a Sanity Timer/Reset circuit to reset the unit should a glitch cause the microprocessor to be confused. The sanity timer/reset circuit, shown in Figure 6.30, is composed of a astable multivibrator, U69, and a decade counter, U70. If the ST-8000 does not operate, use a logic probe or oscilloscope to measure the level at U41-1. This point should be LOW or 0 or should be oscillating very slowly. When the processor is running properly, this output will be LOW at all times except when the power is first turned ON.

If U69 fails, the processor will never leave the reset condition.
Whenever power is applied, there should be square wave on U69-3
with a very long period. In normal operation, U70-2 should be
LOW to allow the counter to operate. If U71 or C26 has failed
the counter will not be able to function. In addition, if the
counter itself fails, the unit may stay in the reset state or
continually show the reset front panel display. Replacing U70
may fix the problem.

4.5.1.2 Synthesizer Failure

All of the SCF filters on the modem board are controlled by
clocks generated in the control assembly. Problems in this area
are characterized by filters failing to function or failing to be
on the correct frequency. All of the synthesizers use the
microprocessor crystal clock as a time base, thus if the
processor is working, that oscillator is working.

Two clock frequencies are connected to the synthesizers, as shown
in Figure 6.34. The transmit tone synthesizer uses a 819,200 Hz
clock but all the other synthesizers use a 409,600 Hz reference.
Both of these clocks must be present for the synthesizers to
function properly.

The testing of the individual synthesizers is described in
Section 3.4 under the control assembly tests. Without going into
that detail again, there are several simple tests that may be
performed.

If you connect a frequency counter to U54-6, the transmit tone
output, and set the front panel to change the MARK tone, you
directly control this oscillator. Increasing the MARK tone will
produce a higher frequency at this output and it will always be
10 times the front panel MARK tone setting. The other
oscillators may be checked in the same manner. In no case should
an increasing frequency cause the synthesizer frequency to go
down or jump drastically. Typical problems in the synthesizers
involve failures with the input latches, full adders, or output
latches. After checking for bent pins, the suspect part may be
exchanged with a known good part and the test performed again.

Note that the synthesizer should be tested before the SCF on the
modem board is tested. The SCF filter will not function without
the synthesizer clock input.

4.5.1.3 Other Components

Other component failures may be more difficult to locate. If one
of the latched bits fails, that function may not perform as
expected. The simpliest way to deal with these latches is to
replace the suspect component and determine whether the problem
has been fixed.

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4.5.2 Interconnection Problems

A number of problems may be caused by incorrect re-installation
of flat ribbon jumper cables after they have been removed for
testing.   Front panel difficulties result if the jumper cable is
not   correctly   installed   on the headers at   both   ends.
Unpredictable results occur when the cable to the modem is not
correctly installed.

Before looking deeper into any functional problem, confirm that
all of the flat ribbon cables are correctly installed and are not
frayed or other wise damaged.   In addition, confirm that the
power connection on the left front of the control board is
correctly installed.   Loose connectors or damaged cables may
cause operational problems.

4.6   FRONT PANEL MAINTENANCE

Front panel circuit board failures will generally fall into one
of four areas: display failure, switch failure, integrated
circuit failure, or mechanical connection failure. Observing the
failure symptoms will speed repair.

4.6.1 Display Failure

The front panel of the ST-8000 has three 4-digit LED display
devices and 8 discrete LED's.   The first indication that there
may be a discrete LED failure is when an indicator does not turn
ON when it should or when it used to turn ON.   For example, a
failure in either the MARK or SPACE LED is apparent when a valid
RTTY signal is being received yet only one of the LED's is
flashing.   If LOS fails to light when no signal is present and
the unit print squelch is activated, the LED indicator may be
bad.

Replacing the individual LED's requires disassembly of the front
panel to gain access to the front panel indicators.   When
replacing the indicator, be certain to adjust the lead length to
the circuit board so that the LED fits close to the front panel
face plate.

The ST-8000 MARK, SPACE, and BAUD RATE displays are multiplexed
such that one digit in each display is active at any given
moment.   The most common failure here may be a single digit
segment going bad and remaining OFF always.   If segments in only
one digit on the front panel are bad, that 4-digit display
package must be replaced. If the same segment is off in all four
digits in one display window, the segment driver circuitry for
that segment may be bad and it must be replaced.   If the same
digit is always OFF or always ON in all three display windows,
there may have been a failure in the common cathode driver
transistors.   If the same digit is always OFF, the corresponding
transistor may be an open circuit.   If, however, the driver has
shorted, that display digit will appear to be the sum of all the
active segments in the other three displays.

The 4-digit displays are mounted in sockets on the front panel display card. To replace a display, the front panel circuit board must be removed from the front panel to gain access to the front of the printed circuit board. When installing the new display device, remember to adjust the height of the device so that it matches the height of the other two front panel displays.

4.6.2 Front Panel Switches

The ST-8000 uses toggle, push button, and rotary switches on the front panel. For the most, switch failures will be mechanical and not due to failures in the buffer devices. With the toggle switches, a failure is indicated when operating the switch does not result in the expected change or when the toggle handle feels loose or sloppy. The single push button switch failure is suggested when pressing the button to store setup parameters does not cause the front panel display to momentarily flash. To replace the toggle switches or push button switch, the front panel circuit board must be removed to gain access to the front of the circuit board. The switches are soldered to the board, so the existing defective switch must be removed so that another may be installed. Note that the front panel mounting depends on all of the switches being the correct length and in the correct mounting position so that they fit easily through the corresponding holes in the front panel faceplace.

The rotary switches control many operational functions on the front panel. A switch failure is generally indicated when one or more switch positions fail to work as expected or when the switch operation itself seems to feel sloppy compared to the other front panel switches. To replace the front panel rotary switches, the front panel circuit board must be removed to gain access to the front of the board. All pins on the existing switch must be unsoldered before removing the old switch. When installing the new switch, carefully note the switch orientation and be certain that the switch stop is in the same place on the new switch.

4.6.3 Front Panel Integrated Circuits

There is always the possibility that a latch or display digit driver on the front panel will fail. While it is difficult to predict the symptoms of such a failure, observing what does and does not work will help isolate the problem.

If several of the switches fail to work, but others do function, the problem might be the buffer device connected to the switches. Since the front panel uses sockets, substituting another device for the suspect buffer is the simplest repair technique. If some or all of the display digits fail, test segment driver circuits and the common cathode transistor driver circuits. An oscilloscope may prove valuable in locating this type of failure.

4.6.4 Mechanical Failure

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The front panel is connected to the modem board and the control
board with flat ribbon jumper cables.   If no LED's on the front
panel light, check the power connection to the front panel near
the softpot.   If this connector is not correctly installed, or
has been removed, none of the front panel LED's are powered.   If
the three display windows function correctly, but the individual
LED indicators are not lit, check the modem board connection
cable.   Be certain that the cable is installed correctly on both
the modem board header and the front panel header.   If the
individual LED's seem to be working but the digits are not, check
the cable to the control board for proper connection at both
ends.   If this cable is not correctly installed, the front panel
displays and switches will exhibit operational problems.

A failure of the tuning knob may be either a component failure or
a loose cable.   If the tuning knob does not seem to work, first
be certain that the ST-8000 is not in the fixed TX/RX mode since
the tuning knob is locked out in that mode.   Next, check the
cable between the softpot on the front panel and the display
board.   If this cable is loose, or incorrectly installed, the
tuning may be erratic.

4.7 CRT ASSEMBLY MAINTENANCE

Section 3.6 of this manual gives step-by-step alignment and test
procedures for the CRT assembly (A4).   Follow these steps to
isolate CRT problems.

***** CAUTION *****

POTENTIALLY LETHAL VOLTAGES ARE PRESENT ON THE CRT CIRCUIT BOARD
AND CRT SOCKET.   USE EXTREME CARE TO AVOID ELECTRICAL SHOCK OR
ACCIDENTAL CONNECTION OF A HIGH VOLTAGE POINT TO OTHER ST8000
CIRCUITRY.

4.7.1 CRT Replacement

Since the CRT itself is a vacuum-tube, it is by nature fragile
and has a limited life time.   The automatic trace ON/OFF control
will prolong tube lifetime, but replacement may be necessary
after several years of continuous service.   Before replacing the
CRT, be sure that all voltages and other alignment instructions
match those shown in Figure 6.50 and discussed in section 3.6.
Symptoms of a defective CRT are:

(a) Open CRT filament (no trace and no continuity between pins 1
and 2 of the CRT with the socket removed).   TURN OFF POWER AND
GROUND HIGH VOLTAGES BEFORE DISCONNECTING THE CRT SOCKET.

(b) Burned screen phosphor. This will be noticeable as lines or dark areas on the CRT face, even when the ST8000 is turned OFF. Some amount of phosphor deterioration is normal as the CRT ages and the CRT will provide useful tuning indications long after the first phosphor burn is noticed.

(c) Inability to focus at higher intensity settings. The intensity of the CRT trace fades as the tube ages. It is normal for both focus and intensity adjustments to change over the life of the tube. At the time when satisfactory focus can not be achieved at the desired intensity, the CRT must be replaced. NOTE: defects in the high voltage power supply may also cause these symptoms. Be sure that the voltages on the CRT socket are correct BEFORE replacing the CRT.

(d) Mechanical damage to the CRT. The tube has a blown glass envelope and is therefore susceptible to cracks or breakage due to mechanical or thermal stress. Be particularly careful when removing or installing the CRT socket as stress on the tube pins may crack the glass-to-metal seals. The ST8000 CRT is shock-mounted in its magnetic shield and therefore should not be damaged in the course of normal handling of the ST8000. However, sudden shocks such as dropping the ST8000 should definitely be avoided.

The following steps should be followed EXACTLY when replacing the Cathode Ray Tube (CRT). Use extreme care when handling the fragile tube to avoid cuts.

(a) Disconnect ALL cables from the ST8000.

(b) Wait 5 minutes to be sure that ALL power supply voltages have decayed to zero volts. Confirm this fact by measuring the -1400V and +135V test points (see Figure 3.1). Connect a ground clip to both the -1400V and +135V test points.

(c) Remove the top and bottom covers of the ST8000 cabinet (12 4-40 screws on each cover).

(d) Remove the rack mounting adapter on the LEFT side of the ST8000 cabinet, if installed (2 10-32 screws).

(e) Remove the left side of the ST8000 cabinet itself (4 6-32 screws).

(f) Unplug the socket from the rear of the Cathode Ray Tube. Use extreme care to avoid bending the pins or breaking the CRT glass envelope.

(g) Unplug the TRACE ROT connector (J3) from the CRT circuit board.

(h) Remove the CRT and its shield from the ST8000 front panel (3 6-32 nuts).   The front face of the face may have attached itself to the ST8000 front panel surface. GENTLY pull the CRT away from the polycarbonate panel surface.

(i) Press the CRT out of the shield assembly by applying GENTLE pressure against the rear of the tube. Use care to avoid bending the pins or breaking the CRT envelope.

(j) Set the defective CRT aside in a protected location so that it will not be accidentally broken. The defective tube may be discarded at your convenience. NOTE: There is NO trade-in allowance for small CRT devices and please do NOT return the defective CRT to HAL unless specifically requested to do so.

(k) Locate the replacement CRT and note the gap in the pin circle. This gap must face UP when the CRT and shield are installed in the cabinet. Also note that the TRACE ROT lead must be on the RIGHT side of the shield when installed. Orient the CRT and shield correctly and GENTLY press the tube into the shield. Be very careful to avoid breaking the tube or catching (and breaking) the fine wires of the TRACE ROT coil with the CRT pins. The face of the CRT should extend approximately 1/16" beyond the front edge of the shield.

(l) Fasten the CRT and shield assembly to the ST8000 front panel (3 6-32 nuts). Check that the gap in the tube pin circle is UP and that the TRACE ROT connector is on the RIGHT side of the shield. Correct the orientation if necessary before proceeding.

(m) GENTLY press on the rear of the CRT until the face is flush with the front panel viewing area (sense front panel with fingers).

(n) Reconnect the TRACE ROT connector to the CRT circuit board. Either polarity may be used as this will be set when re-aligning the CRT controls.

(o) Reconnect the CRT socket. Use EXTREME care to avoid bending the tube pins or breaking the glass-to-metal seals

(p) Fasten the side panel to the ST8000 cabinet (4 6-32 screws). Either orientation of the side panel may be used.

(q) Fasten the bottom cover on the ST8000 cabinet (12 4-40 screws).

(r) Remove the ground clips from the -1400V and +135V test points.

(s) Refer to section 3.6 and re-align the CRT assembly. It is normal for all adjustments to be slightly different for each tube. This is particularly true for all adjustments in section 3.6.2. The Spectra-Tune adjustments (3.6.3) have probably not changed, but should be checked as well.

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(t)   Fasten the rack mounting adapter to the left side of the
ST8000 cabinet, if desired (2 10-32 screws).

(u)   Fasten the top cover on the ST8000 cabinet (12 4-40 screws).

4.7.2 Other CRT Repairs

Problems other than a defective CRT will generally be due to
failures of a high-voltage component or of an integrated circuit.
All integrated circuits are installed in sockets and may
therefore be replaced without removal of the CRT circuit board
from the cabinet.   Note, however, that IC's U3 and U4 are under
the CRT shield. Follow steps (a) through (h) of section 4.7.1 to
remove the CRT and shield to gain access to U3 and U4.

If other components must be changed, the CRT circuit board must
be removed.   Follow steps (a) through (h) of section 4.7.1,
disconnect plugs from J1 (transformer) and J2 (cable to MODEM
assembly), and then remove the four screws at the corners of the
CRT board.   When resoldering any high-voltage component
(capacitors, diodes, etc) be very careful to make very smooth
solder joints that do not have sharp protrusions that might
become corona discharge points.   Be sure to make full use of all
of the test points shown in Figures 6.49 and 6.50 to isolate the
problem BEFORE removing the circuit board.

In any failure in which the CRT intensity, focus, or trace
distortion is noted, always first check the high voltage power
supplies first.   As with the CRT itself, high voltage
electrolytic capacitors have a limited lifetime.   A lower than
normal high voltage magnitude may be caused by (1) bad filter
capacitors (C1 through C6) or (2) high current drain (short to
ground or defective Q4, Q5, Q6, or Q7). Zero output volts from
either high voltage supply may be caused by the above or by a
failure of the transformer windings or in the rectifier diodes
(D1 through D5).

Distorted CRT traces (ellipses in particular) is generally caused
by problems in the +135V supply or in the deflection amplifier
circuits (U3,   Q3 through Q8,   and associated components).
Improper or missing Spectra-Tune output is caused by either mis-
adjustment of R32 or by failures of U1, U2, or U4 and the
associated circuitry.   Be sure to check TP6 and confirm that the
trace switching signal is indeed present before assuming further
problems with the Spectra-Tune circuit.   Lack of CRT ON/OFF
control may be caused by either a failure of Q1 or lack of a
control signal from the MODEM assembly via J2-11.

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CHAPTER 5. PARTS LISTS

The following pages list the parts used in the ST8000, organized by
assemblies. When appropriate, acceptable commercial part number
equivalents are specified. However, some components are custom to HAL
Communications and the ST8000 HF MODEM. These parts must be obtained
from the HAL factory. A cross-reference of the listed FSCM (Federal
Supply Code for Manufacturers) is given at the end of this chapter. The
following is a list of the assemblies used in the ST8000. Separate
parts lists for each assembly follow on subsequent pages.

PARTS LIST - PLO8000   HAL COMMUNICATIONS CORP.   REV DATE 860310
                             URBANA, ILLINOIS   REV NO. 1A
10 JUNE 1986   FSCM NO. 63256   PAGE 1 of 26

5.1 ST8000 HF MODEM - P/N 900-08000

ASSEMBLIES PARTS LIST

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A1	1	63256	C1112	934-08000	MODEM Assembly
A2	1	63256	C1112	932-08000	CONTROL Assembly
A3	1	63256	C1112	920-08000	FRONT PANEL Asbly
A4	1	63256	C1112	915-08000	CRT Assembly
A5	1	63256	C1112	910-08000	Cabinet Assembly
A6	1	63256		970-08000	ST8000 Accessories
A5-REG	1	63256	A1578	960-08308	5V Regulator Asbly
A5-W1	1	63256	A1578	960-08302	A1 to A3 Power Cable
A5-W2	1	63256	A1578	960-08303	A1 to A2 Power Cable
A5-W3	1	63256	A1578	960-08304	A3 to SOFTPOT Cable
A5-W4	1	63256	A1578	960-08305	A1 to A3 Data Cable
A5-W5	1	63256	A1578	960-08305	A2 to A3 Data Cable
A5-W6, A5-W7	2	63256	A1578	960-08306	A1 to A2 Data Cable
A5-W8	1	63256	A1578	960-08307	A2 to J7a Data Cable
A5-W9	1	63256	A1578	960-08309	A1 to J11a Data Cble
A5-W10	1	63356	A1578	960-08310	A1 to A4 Data Cable
SPARE PARTS KIT	1	63256		980-08001	Spare Parts Kit

5.2 MODEM ASSEMBLY A1 - P/N 934-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A1CB	1	63256	D1093	050-11930	MODEM Circuit Board
C1, C2, C3, C5, C6, C8, C10, C11, C28, C29, C33, C34, C35, C36, C37, C39, C40, C42, C43, C44, C47, C48, C52, C53, C56, C57, C59, C69, C70, C75, C78, C79, C84, C85, C88, C90, C91, C92, C93, C94, C95, C96, C97, C109, C110, C113, C114, C116, C117, C118, C121, C139, C165, C166, C167	55	04222		111-10450	0.1uF/50V Mono-lythic Capacitor
C4, C31, C74, C130	4	15450		110-12211	0.0012uF Ceramic Capacitor
C7, C27, C76	3	15450		110-33111	330 pF Ceramic Capacitor
C9, C65	2	56289		110-50211	0.005uF Ceramic Capacitor
C12, C13, C14, C17, C23, C25, C26, C30, C32, C61, C62, C63, C64, C67, C68, C71, C81, C82, C101, C102	20	56289		160-01035	1uF/35V Tantalum Capacitor
C15, C24	2	15450		110-56201	0.0056uF Ceramic Capacitor
C16, C22	2	15450		110-15211	0.0015uF Ceramic Capacitor
C18, C89	2	74840		152-10135	100uF/35V Electro-lytic Capacitor
C19, C20, C100, C106	4	74840		152-10035	10uF/35V Electro-lytic Capacitor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
C21, C60, C72, C73, C104	5	74840		152-22035	22uF/35V Electro-lytic Capacitor
C38, C50, C54, C66, C83, C87, C98, C99, C111, C112, C119, C125, C126, C127, C128, C129, C131, C132, C133, C134, C135, C136, C137, C138, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C164	42	56289		110-10211	0.001uF/1kV Ceramic Capacitor
C41, C45, C49	3	56289		110-22111	220pF Ceramic Capacitor
C46	1	56289		151-47916	4.7uF/16V Tantalum Capacitor
C51, C86, C140	3	74840		152-22950	2.2uF/50V Electro-lytic Capacitor
C55, C108	2	15450		110-68111	680pF Ceramic Capacitor
C58	1	15450		110-18111	180pF Ceramic Capacitor
C77	1	56289		110-03011	3pF Ceramic Capacitor
C80, C141	2	56289		110-47011	47pF Ceramic Capacitor
C103, C120	2	56289		160-47835	0.47uF/35V Tantalum Capacitor
C105, C162, C163	3	56289		160-33835	0.33uF/35V Tantalum Capacitor
C107	1	56289		110-50350	0.05uF Ceramic Capacitor
C115	1	15450		110-25111	250pF Ceramic Capacitor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
C122, C123, C124	3	56289		130-27201	0.0027uF Mylar Capacitor
C159, C160	2	74840		151-10225	1000uF/25V Electrolytic Capacitor
C161	1	74840		151-47225	4700uF/25V Electrolytic Capacitor
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D12, D14, D15, D16, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D30, D31, D32, D33, D34, D35, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48 D49, D50, D51, D52, D53, D54, D61, D62, D64, D65, D66, D67, D68, D69, D70, D71, D72	58	14433		615-04148	1N4148 Silicon Signal Diode
D11, D13, D36, D37, D61	5	14433		618-04733	1N4733 5.1V Zener Diode
D38, D57, D58, D59, D60, D63	6	04713		615-04005	1N4005 1A, 500 PIV Rectifier Diode
D55, D56	2	04713		615-03105	3S105 3A, 50 PIV Rectifier Diode
J1, J2, J3, J6	4	00779		332-20000	2x10x0.1 Straight Header Connector
J4	1	06383		327-04001	1x4x0.1 Right Angle Connector
J5, J7	2	06383		330-06000	1x6x0.156 Right Angle Connector
J8	1	06383		330-03000	1x3x0.156 Right Angle Connector

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
J9	1	59422		333-10256	DB25S Right Angle Shielded Connector
J10	1	59422		333-10095	DE9S Right Angle Shielded Connector
J11	1	06383		327-04000	1x4x0.1 Straight Connector
J12	1	83289		310-04912	PC Mntg Stereo Jack
JP1, JP3, JP4	3	00779		332-01000	1x2x0.1 Straight Connector
JP2	1	00779		332-03000	1x3x0.1 Straight Connector
KY1	1	94696		751-01911	SPST 5V DIP RELAY
Q1, Q2, Q4, Q5, Q6	5	04713		621-03395	MPS3395 NPN Small Signal Transistor
Q3, Q7	2	04713		621-00521	MJE521 NPN Power Transistor
Q8	1	04713		621-06518	MPS6518 PNP Small Signal Transistor
R1	1	57668		510-33020	33K, 1/4W, 5% R25X Film Resistor
R2, R98, R101, R108, R145, R161, R162, R206, R207, R214, R239, R266, R272, R274, R281, R288	16	57668		510-10030	100K, 1/4W, 5% R25X Film Resistor
R3, R4, R6, R33, R36, R47A, R60, R66, R67, R84, R135, R157, R163, R176, R181, R188, R189, R193, R194, R197, R198, R238, R241, R244A, R247, R262, R246	27	57668		510-47010	4.7K, 1/4W, 5% R25X Film Resistor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R180	1	57668		510-15010	1.5K, 1/4W, 5% R25X Film Resistor
R5, R7, R8, R16, R17, R32, R47, R57, R75, R109, R144, R148, R153, R158, R159, R160, R187, R190, R199, R200, R203, R208, R209, R210, R213, R215, R216, R217, R218, R228, R229, R232, R235, R240, R279, R282, R283, R285, R286	39	57668		510-10020	10K, 1/4W, 5% R25X Film Resistor
R9, R10, R11, R12, R22, R23, R24, R27, R29, R34, R35, R70, R73, R74, R91, R92, R93, R97, R100, R105, R107, R110, R112, R114, R115, R118, R133, R134, R151, R152, R169, R170, R171, R174, R178, R183, R185, R186, R191, R192, R196, R249, R250, R251, R254, R254A, R257, R258, R263	49	57668		510-10000	100 Ohm, 1/4W, 5% R25X Film Resistor
R13, R94, R95, R165	4	80031		515-33220	33.2K, 1/4W, 1% RN55 Resistor
R14, R15, R211	3	57668		510-33010	3.3K, 1/4W, 5% R25X Film Resistor
R18, R19, R30, R31	4	80031		515-24920	24.9K, 1/4W, 1% RN55 Resistor

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R20, R25, R28, R37, R69, R77, R87, R89, R117, R120, R122, R136, R150, R156, R167, R172, R173, R212, R255, R259, R290	21	57668		510-47020	47K, 1/4W, 5% R25X Film Resistor
R21, R38, R76, R113, R137, R168, R260	7	57668		510-24020	24K, 1/4W, 5% R25X Film Resistor
R26, R71, R72, R149, R154, R155 R253	7	57668		510-20020	20K, 1/4W, 5% R25X Film Resistor
R32A, R42, R147, R293	4	57668		510-47000	470ohm, 1/4W, 5% R25X Film Resistor
R39, R138	2	57668		510-56020	56K, 1/4W, 5% R25X Film Resistor
R40, R45, R46, R62, R116, R139, R140, R177, R184, R221, R224, R227	12	57668		510-10010	1K, 1/4W, 5% R25K Film Resistor
R41, R164, R201, R202, R204, R205, R219, R222	8	57668		510-10040	1 meg, 1/4W, 5% Film Resistor
R43, R44, R58, R59, R64, R166, R233, R242, R244, R245, R297	11	57668		510-22010	2.2K, 1/4W, 5% R25X Film Resistor
R48, R49, R50, R51, R55, R56, R141, R142, R220	9	57668		510-22020	22K, 1/4W, 5% R25X Film Resistor
R52, R99, R111	3	57668		510-75010	7.5K, 1/4W, 5% R25X Film Resistor
R53, R261	2	57668		510-11020	11K, 1/4W, 5% R25X Film Resistor
R61, R146, R223, R280	4	57668		510-22030	220K, 1/4W, 5% R25X Film Resistor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R63, R85, R86, R123, R124	5	80294		563-05020	5K, 1/2W Horizontal Trim Potentiometer
R65, R68, R182	3	80294		563-01030	10K, 1/2W Horiz. Trim Potentiometer
R78, R79, R129, R130, R175, R195	6	57668		510-04700	47ohm, 1/4W, 5% R25X Film Resistor
R80, R81, R82, R83, R125, R126, R127, R128	8	80031		515-10030	100K, 1/4W, 1% RN55 Resistor
R88, R90, R119, R121	4	57668		510-12020	12K, 1/4W, 5% R25X Film Resistor
R96	1	57668		510-68000	680ohm, 1/4W, 5% R25X Film Resistor
R102, R131, R132	3	80294		563-05010	500ohm, 1/2W, Horiz Trim Potentiometer
R103	1	80294		563-02530	25K, 1/2W, Horiz. Trim Potentiometer
R104	1	57668		510-27030	270K, 1/4W, 5% R25X Film Resistor
R106	1	57668		510-56010	5.6K, 1/4W, 5% R25X Film Resistor
R143, R230	2	57668		510-15020	15K, 1/4W, 5% R25X Film Resistor
R179, R231, R234, R237, R243, R278, R284, R291	8	57668		510-27020	27K, 1/4W, 5% R25X Film Resistor
R225, R289	2	57668		510-47030	470K, 1/4W, 5% R25X Film Resistor
R226	1	80294		563-01050	1meg, 1/2W Horiz. Trim Potentiometer
R236	1	57668		510-12030	120K, 1/4W, 5% R25X Film Resistor
R248, R264	2	57668		510-39020	39K, 1/4 W 5% R25X Film Resistor

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R252, R267	2	57668		510-15030	150K, 1/4W, 5% R25X Film Resistor
R256	1	57668		510-43010	4.3K, 1/4W, 5% R25X Film Resistor
R265	1	57668		510-36010	3.6K, 1/4W, 5% R25X Film Resistor
R268, R276	2	57668		510-24030	240K, 1/4W, 5% R25X Film Resistor
R269, R271	2	57668		510-20040	2meg, 1/4W, 5% R25X Film Resistor
R270, R275	2	57668		510-51020	51K, 1/4W, 5% R25X Film Resistor
R273, R277	2	57668		510-62020	62K, 1/4W, 5% R25X Film Resistor
R287, R292	2	57668		510-12010	1.2K, 1/4W, 5% R25X Film Resistor
R294, R296	2	57668		520-62000	620ohm, 1/2W, 5% R50X Film Resistor
R295	1	80294		564-01030	10K, 1/2W Vertical Trim Potentiometer
RN1, RN2, RN4, RN5	4	80294		525-47209	4.7Kx8, 1/4W SIP Resistor Pack
RN3, RN6	2	80294		525-10309	10Kx8, 1/4W SIP Resistor Pack
S1, S2, S3, S4	4	71450		725-07604	5xSPST DIP Switch
T1, T2	2	63256	A1539	800-01539	600:600:8 ohm Audio Transformer.
TP1 - TP50, TP(GND)	53	91505		355-00011	Test Point Pin
U1, U12, U28	3	04713		630-04741	4741 Quad OP-Amp Integrated Circuit
U2, U5, U6, U16, U25	5	02735		650-04066	4066 CMOS 4xSPST Integrated Circuit

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
U3, U10, U13, U20, U21, U29, U36, U37, U45, U46, U47, U50, U52, U65	14	04713		630-01458	1458 Dual Op-Amp Integrated Circuit
U4, U8, U57	3	04713		630-01488	1488 4xRS232 Driver Integrated Circuit
U7, U15, U24, U33	4	80294		525-33301	16x33.2K, 1% DIP Resistor IC
U9, U18, U23, U32	4	04713		630-00741	741 Op-Amplifier Integrated Circuit
U11, U27	2	34314		630-05613	R5613 LP Filter Integrated Circuit
U14	1	02735		650-04053	4053 3xDPDT CMOS SW Integrated Circuit
U17, U26	2	34314		630-05621	R5621 Adj BP Filter Integrated Circuit
U19, U53	2	02735		630-03081	CA3081 6xNPN Array Integrated Circuit
U22, U30	2	04713		630-03340	MC3340P AGC Amp. Integrated Circuit
U31	1	27014		630-00709	709 Op-Amplifier Integrated Circuit
U34, U40, U54, U54, U58	5	02735		650-04011	4011 4x2-NAND CMOS Integrated Circuit
U35, U49, U63	3	02735		650-04049	4049 6xINV CMOS Integrated Circuit
U38	1	02735		644-74151	74HC151 8IN Select Integrated Circuit
U39, U62	2	02735		650-04030	4030 4xX-OR CMOS Integrated Circuit
U41	1	34314		630-05614	R5614 1/3 Oct BPF Integrated Circuit
U42	1	34314		630-05615	R5615 1/2 Oct BPF Integrated Circuit

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
U43	1	34314		630-05616	R5616 1.0 Oct BPF Integrated Circuit
U44, U51	2	02735		630-04052	4052 2P4T CMOS SW Integrated Circuit
U48	1	02735		650-04023	4023 3x3 NAND CMOS Integrated Circuit
U56, U60	2	02735		650-04001	4001 4x2 NOR CMOS Integrated Circuit
U59	1	02735		650-04025	4025 3x3 NOR CMOS Integrated Circuit
U61	1	02735		650-04017	4017 Decade Counter Integrated Circuit
U64	1	02735		650-04002	4002 2x4 NOR CMOS Integrated Circuit
U66	1	07263		635-07908	7908 -8V Regulator Integrated Circuit
U67	1	07263		635-07808	7808 +8V Regulator Integrated Circuit
XU1, XU2, XU4, XU5, XU6, XU8, XU12, XU16, XU17, XU25, XU26, XU28 XU31, XU34, XU39, XU40, XU48, XU54, XU55, XU56, XU57, XU58, XU59, XU60, XU62, XU64, XK1	27	91506		340-01402	14 pin 800S Socket
XU3, XU9, XU10, XU11, XU13, XU18, XU20, XU21, XU22, XU23, XU27, XU29, XU30, XU32, XU36, XU37, XU41, XU42, XU43, XU45, XU46, XU47, XU50, XU52, XU65	25	91506		340-00802	8 Pin 800S Socket
XU7, XU14, XU15, XU19, XU24, XU33, XU35, XU38, XU44, XU49, XU51, XU53, XU61, XU63	14	91506		340-01602	16 Pin 800S Socket

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5.3 CONTROL ASSEMBLY A2 – P/N 932-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A2CB	1	63256	D1194	050-11940	CONTROL Circuit Bd.
C1, C2, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C22, C23, C25, C30	22	04222		111-10450	0.1uF/50V Mono-lythic Capacitor
C3	1	74840		151-10135	100uF/35V Electro-lytic Capacitor
C4, C27, C28, C29	4	56289		110-10211	0.001uF/1kV Ceramic Capacitor
C21	1	56289		110-30011	30pF Ceramic Capacitor
C24	1	56289		110-10311	0.01uF Ceramic Capacitor
C26	1	74840		151-10035	10uF/35V Electro-lytic Capacitor
D1	1	14433		615-04148	1N4148 Silicon Signal Diode
J1, J2, J3	3	00779		332-20000	2x10x0.1 Straight Header Connector
J4	–			----------	NOT USED
J5	1	06383		330-06000	1x6x0.156 Right Angle Connector
J6	–			----------	NOT USED
J7	1	00779		332-16000	2x8x0.1 Straight Header Connector

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R1	1	57668		510-33000	330ohm, 1/4W, 5% R25X Film Resistor
R2	1	57668		510-33010	3.3K, 1/4W, 5% R25X Film Resistor
R3, R4	2	57668		510-39000	390ohm, 1/4W, 5% R25X Film Resistor
R5, R6	2	57668		510-10030	100K, 1/4W, 5% R25X Film Resistor
R7, R8, R9, R10	4	57668		510-10020	10K, 1/4W, 5% R25X Film Resistor
RN1	1	80294		525-01030	10Kx8 1/4W SIP Resistor Pack
S1	1	71450		725-07605	5xSPST DIP Switch Assembly
TP(GND)	4	91506		355-00010	Swage Terminal
U1, U8, U15, U16, U17, U18, U19, U20, U21, U22, U45, U59, U60	13	27014		645-74374	74HCT374 8xD FF Integrated Circuit
U2, U3, U4, U9, U24	5	27014		643-74138	74LS138 3-8 Decoder Integrated Circuit
U5, U41, U42, U43, U44, U48, U52, U53, U56, U63	10	04713		643-74374	74LS374 8xD FF Integrated Circuit
U6, U7, U30, U31, U32, U33, U34, U35, U38, U39, U40, U46, U47, U57, U58, U61, U62	17	04713		643-74283	74LS283 4BIT BIN AD Integrated Circuit
U10, U11	2	01295		670-02764	2764 EPROM Integrated Circuit

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
(U12), U13 (see note)	1 (2)	H0001		670-01220	DS1220Y BATTERY RAM Integrated Circuit
U14	1	34649		680-08253	8253 INT TIMER Integrated Circuit
U23	1	56708		680-00080	Z80A CPU Integrated Circuit
U25, U72	2	04713		643-74393	74LS393 4BIT CNTR Integrated Circuit
U26, U51, U67, U68	4	04713		643-07474	74LS74 2xD FF Integrated Circuit
U27, U28, U29, U50	4	04713		643-74157	74LS157 4x2-1 MPLX Integrated Circuit
U36	1	56708		680-08470	Z8470 DART Integrated Circuit
U37	1	34649		680-08251	8251A USART Integrated Circuit
U49	1	04713		643-07404	74LS04 6xINVERTER Integrated Circuit
U54, U70	2	18324		643-74290	74LS290 DEC CNTR Integrated Circuit
U55	1	18324		643-07486	74LS86 4x2 XOR Integrated Circuit
U64	1	04713		630-01489	1489 4xRS232 RCVR Integrated Circuit
U65	1	04713		630-01488	1488 4xRS232 DRIVER Integrated Circuit
U66	1	18324		643-07400	74LS00 4x2 NAND Integrated Circuit
U69	1	27014		630-00555	NE555 TIMER Integrated Circuit
U71	1	18324		643-07402	74LS02 4x3 NOR Integrated Circuit

NOTE: U12 not used on current models ST8000.

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
X1	1	23875		200-04915	4.9152 mHz HC18 Quartz Crystal
XU1, XU5, XU8, XU15, XU16, XU17, XU18, XU19, XU20, XU21, XU22, XU41, XU42, XU43, XU44, XU45, XU48, XU52, XU53, XU56, XU59, XU60, XU63	23	91506		340-02002	20 Pin 800S Socket
XU2, XU3, XU4, XU6, XU7, XU9, XU24, XU27, XU28, XU29, XU30, XU31, XU32, XU33, XU34, XU35, XU38, XU39, XU40, XU46, XU47, XU50, XU57, XU58, XU61, XU62	26	91506		340-01602	16 Pin 800S Socket
XU10, XU11, XU12, XU13, XU37	5	91506		340-02802	28 Pin 800S Socket
XU14	1	91506		340-02402	24 Pin 800S Socket
XU23, XU36	2	91506		340-04002	40 Pin 800S Socket
XU25, XU26, XU49, XU51, XU54, XU55, XU64, XU65, XU66, XU67, XU68, XU70, XU71, XU72	14	91506		340-01402	14 Pin 800S Socket
XU69	1	91506		340-00802	8 Pin 800S Socket

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5.4 FRONT PANEL ASSEMBLY A3 - P/N 920-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A3FPM	1	63256	B1344	000-13440	Front Sub-Panel, Metal
A3FPPC	1	63256	B1345	000-13450	Front Panel, Poly-carbonate
A3CB	1	63256	D1195	050-11950	FRONT PANEL Circuit Board
C1	1	56289		110-10211	0.001uF/1kV Ceramic Capacitor
C2, C3	2	04222		111-10450	0.1uF/50V Mono-lythic Capacitor
C4	1	74840		152-10135	100uF/35V Electro-lytic Capacitor
D1, D2, D3, D4	4	14433		615-04148	1N4148 Silicon Signal Diode
DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8	8	59756		613-00564	CQV-564 Red LED Diode
DS9, DS10, DS11	3	H0004		614-00543	LN543RK 4x7-Segment Red LED Display
J1, J2	2	06383		327-04000	1x4x0.1 Straight Post Connector
J3, J4	2	00779		332-20000	2x10x0.1 Straight Header Connector
J5	1	06383		330-04000	1x4x0.156 Straight Post Connector
KN1	1	95146		850-18003	0.75" Knob
includes:	1	95146		850-18013	1/4-1/8 Adapter
KN2, KN3, KN4, KN5, KN6, KN7	6	95146		850-18004	0.5" Knob
KN8	1	95146		721-00005	BLK Cap - PB Switch
L1	1	13396		000-99151	CRT Trace Rotation Coil

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
P1	1	00779		332-02100	2x0.1 Header Plug Connector
(P1)	2	00779		332-87666	Crimp Pin for P1
Q1, Q2, Q3, Q4	4	04713		621-00521	MJE521 NPN Power Transistor
R1, R2, R3, R4	4	57668		510-10010	1K, 1/4W, 5% R25X Film Resistor
R5, R6	2	57668		510-47000	470ohm, 1/4W, 5% R25X Film Resistor
R7	1	57668		510-03900	39ohm, 1/4W, 5% R25X Film Resistor
R8, R9	2	12697		575-01030	10K RV6NAY-50-103A Potentiometer
RN1, RN2, RN3	3	80294		525-39000	39ohm, 1/4W SIP Resistor Pack
RN4, RN5, RN6, RN7	4	80294		525-01020	1K, 1/4W SIP Resistor Pack
RN8, RN9, RN10, RN11, RN13	5	80294		525-01030	10K, 1/4W SIP Resistor Pack
RN12	1	80294		525-47100	470ohm, 1/4W SIP Resistor Pack
S1, S2, S3, S12, S14	5	95146		710-00306	SPDT, PC MTG, Mini-toggle Switch
S4, S7	-			---------	NOT USED
S5, S6, S9, S10, S11	5	81073		715-00100	SP8T 55DP36-01-AJN Min Rot Switch
S8	1	95146		720-00103	SPDT, PC MTG, Mini-PB Switch
S13	1	95146		710-00106	SPDT, PC MTG, C-OFF Mini-toggle Switch
S15	1	95146		710-00406	DPDT, PC MTG, Mini-toggle Switch

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
SH1	1	H0003		000-99155	CRT Shield
SP1	1	H0005		575-00016	Softpot Digital Control
U1, U2, U3, U4, U5, U6, U8	7	27014		630-75491	75491 4xLED Driver Integrated Circuit
U7, U9, U10, U11	4	04713		645-74374	74HCT374 8xD FF Integrated Circuit
U12, U13, U16, U17	4	04713		643-74244	74LS244 8xBuffer Integrated Circuit
U14	1	18324		643-74138	74LS138 3-8 Decoder Integrated Circuit
U15	1	18324		643-74148	74LS148 8-3 Encoder Integrated Circuit
V1	1	13396		000-99150	D7-233GH Cathode Ray Tube
XDS9, XDS10, XDS11	6	51167		340-12435	12 Pin Elev. Strip Socket (2 per DS)
XU1, XU2, XU3, XU4, XU5, XU6, XU8	7	91506		340-01402	14 Pin 800S Socket
XU7, XU9, XU10, XU11, XU12, XU13, XU16, XU17	8	91506		340-02002	20 Pin 800S Socket
XU14, XU15	2	91506		340-01602	16 Pin 800S Socket

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5.5 CRT ASSEMBLY A4 – P/N 915-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A4CB	1	63256	D1196	050-11960	CRT Circuit Board
C1, C2, C3, C4	4	25243		151-80905	8uF/450V Electro-lytic Capacitor
C5	1	56289		130-10404	0.1uF/400V Mylar Capacitor
C6	1	25243		151-20003	20uF/350V Electro-lytic Capacitor
C7, C11	2	56289		110-50350	0.05uF Ceramic Capacitor
C8, C9, C10, C13, C14, C19, C20	7	04222		111-10450	0.1uF/50V Mono-lythic Capacitor
C12, C16	2	74840		151-10135	100uF/35V Electro-lytic Capacitor
C15	1	56289		130-47201	0.0047/100V Mylar Capacitor
C17	1	56289		130-33301	0.033uF/100V Mylar Capacitor
C18	1	56289		110-10301	0.01uF Ceramic Capacitor
D1, D2, D3, D4, D5	5	14433		615-04007	1N4007 1A, 700 PIV Rectifier Diode
D6, D7, D8, D9, D10, D11	6	14433		615-04148	1N4148 Silicon Signal Diode
J1	1	06383		330-06000	1x6x0.156 Straight Post Connector
J2	1	00779		332-20000	2x10x0.1 Straight Header Connector
J3	1	00779		332-01000	1x2x0.1 Straight Header Connector
Q1	1	04713		621-06518	MPS6518 PNP Small Signal Transistor
Q2	1	04713		621-03395	MPS3395 NPN Small Signal Transistor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
Q3, Q4, Q5, Q6, Q7, Q8	6	04713		621-00042	MPSA42 NPN HV Small Signal Transistor
R1, R2	2	57668		520-47000	470ohm, 1/2W, 5% R50X Film Resistor
R3, R4, R5, R6	4	04061		530-10040	1 meg, 1W, 10% R-11 Comp. Resistor
R7, R9	2	80294		563-01040	100K, 1/2W Horiz. Trim Potentiometer
R8, R19	2	57668		520-22030	220K, 1/2W, 5% R50X Film Resistor
R10	1	80294		563-02540	250K, 1/2W Horiz. Trim Potentiometer
R11	1	57668		510-82010	8.2K, 1/4W, 5% R25X Film Resistor
R12	1	04061		530-13030	130K, 1W, 10% R-11 Comp. Resistor
R13, R14	2	04061		530-22030	220K, 1W, 10% R-11 Comp. Resistor
R15	1	04061		530-27030	270K, 1W, 10% R-11 Comp. Resistor
R16, R17, R20, R21	4	04061		520-10030	100K, 1/2W, 5% R50X Film Resistor
R18	1	04061		520-68020	68K, 1/2W, 5% R50X Film Resistor
R22, R30, R31, R52, R53, R54	6	80294		563-05020	5K, 1/2W, Horiz. Trim Potentiometer
R23, R37, R56	3	57668		510-10010	1K, 1/4W, 5% R25X Film Resistor
R24	1	57668		510-30020	30K, 1/4W, 5% R25X Film Resistor
R25, R55	2	57668		510-47000	470ohm, 1/4W, 5% R25X Film Resistor
R26	1	57668		510-10000	100ohm, 1/4W, 5% R25X Film Resistor

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R27	1	57668		510-33020	33K, 1/4W, 5% R25X Film Resistor
R28, R29	2	80294		563-01030	10K, 1/2W Horiz. Trim Potentiometer
R32	1	80294		563-05010	500ohm, 1/2W Horiz. Trim Potentiometer
R33, R58, R59, R60	4	57668		510-47010	4.7K, 1/4W, 5% R25X Film Resistor
R34	1	57668		510-22020	22K, 1/4W, 5% R25X Film Resistor
R35, R36, R38, R39	4	57668		510-20020	20K, 1/4W, 5% R25X Film Resistor
R40	1	57668		510-33000	330ohm, 1/4W, 5% R25X Film Resistor
R41	1	57668		510-22030	220K, 1/4W, 5% R25X Film Resistor
R42	1	57668		510-22040	2.2meg, 1/4W, 5% R25X Film Resistor
R43, R67, R72	3	57668		510-15010	1.5K, 1/4W, 5% R25X Film Resistor
R44, R63, R64, R68, R69	5	57668		510-22010	2.2K, 1/4W, 5% R25X Film Resistor
R45, R46	2	57668		510-04700	47ohm, 1/4W, 5% R25X Film Resistor
R47	1	57668		510-82020	82K, 1/4W, 5% R25X Film Resistor
R48	1	57668		510-18030	180K, 1/4W, 5% R25X Film Resistor
R49	1	57668		510-20010	2.0K, 1/4W, 5% R25X Film Resistor
R50, R51, R75, R76, R77, R78	6	57668		510-10030	100K, 1/4W, 5% R25X Film Resistor
R57	1	57668		510-56000	560ohm, 1/4W, 5% R25X Film Resistor

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REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
R61	1	57668		510-15020	15K, 1/4W, 5% R25X Film Resistor
R62	1	57668		510-10020	10K, 1/4W, 5% R25X Film Resistor
R65, R70	2	57668		510-24010	2.4K, 1/4W, 5% R25X Film Resistor
R66, R71	2	57668		510-18010	1.8K, 1/4W, 5% R25X Film Resistor
R73, R74	2	57668		510-47020	47K, 1/4W, 5% R25X Film Resistor
TP1-TP6 GND1-GND3	9	91506		355-00010	Swage Terminal
U1, U4	2	04713		630-01458	1458 Dual Op-Amp Integrated Circuit
U2	1	27014		630-02917	LM2917 F-V Conv. Integrated Circuit
U3	1	02735		650-04053	4053 3xDPDT CMOS SW Integrated Circuit
XU1, XU4	2	91506		340-00802	8 Pin 800S Socket
XU2	1	91506		340-01402	14 Pin 800S Socket
XU3	1	91506		340-01602	16 Pin 800S Socket
XV1	1	13396		000-99015	13 Pin CRT Socket

5.6 CABINET ASSEMBLY A5 — P/N 910-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A5BC	1	63256	B1349	000-13490	Bottom Cover Panel
A5BR	2	63256	B1350	000-13500	Board Mounting Rail
A5FT	1	21604		850-40008	Feet and Tilt Bail
includes:	4	63256		440-09000	Non-slip Rubber Ft.
A5LFS	1	63256	B1354	000-13541	Left Side Panel
A5RM	2	63256	B1355	000-13550	Rack Mounting Ears
A5RP	1	63256	B1346	000-13460	Rear Panel
A5RTS	1	63256	B1347	000-13472	Right Side Panel
A5TC	1	63256	B1348	000-13480	Top Cover Panel
A5XB	1	63256	B1352	000-13521	Transformer Bracket
F1	1	75915		770-10001	1Amp SB 3AG Fuse
FH1	1	75915		770-00001	3AG Fuse Holder
FL1	1	05245		333-17251	1EF2 1A AC Filter
HS1	1	30161		850-01031	HS103 Heat Sink
J1, J2	2	06383		329-06000	6x1x0.156 Post Lock Plug
SP1, SP2, SP3, SP4	4	H0002		425-06161	6-32x1" Thd Spacer
SP5, SP6	2	59540		425-06162	6-32x1" M/F Thd. Spacer
SP7, SP8	2	59540		425-06242	6-32x1" Hinged Spacer
T1	1	63256	A1540	800-15400	Power Transformer
TS1, TS2, TS3	3	63256		425-96320	6-32 Thumb Screw
U1	1	27014		635-00323	LM323 5V, 3A Reg. Integrated Circuit

ASSEMBLIES USED AS PART OF CABINET ASSEMBLY A5:

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A5-REG	1	63256	A1578	960-08308	+5V Regulator Assembly
consists of:	1	91506		340-46011	TO3 IC Socket
	1	06383		329-03000	1x3x0.156 Post Lock Plug
	1	56289		160-01035	1uF/35V Tantalum Capacitor
	1	04222		111-10450	0.1uF/50V Mono-lythic Capacitor
A5-W1	1	63256	A1578	960-08302	MODEM-FRONT PANEL Power Cable
consists of:	2	06383		329-04000	4x1x0.1 Post Lock Plug
	4x7"	28105			No. 22 Str. Wire; 2xBLK, 2xRED
A5-W2	1	63256	A1578	960-08303	MODEM-CONTROL Power Cable
consists of:	2	06383		329-06000	6x1x0.156 Post Lock Plug
	6x3"	28105			No. 18 Str. Wire; 2xBLK, 2xRED, 1xGRN, 1xYEL
A5-W3	1	63256	A1578	960-08304	SOFTPOT-F.PANEL Cable
consists of:	2	06383		329-04000	4x1x0.1 Post Lock Plug
	4x3"	28105			No. 22 Str. Wire; RED, ORG, BLK, BLU
A5-W4, A5-W5	2	63256	A1578	960-08305	FRONT PANEL-MODEM, FRONT PANEL-CONTROL Cable
ea. consists of:	2	92194		332-20100	2x10x0.1 Ribbon Cable Connector
	4"	92194		830-20000	20 Conductor Ribbon Cable
A5-W6, A5-W7	2	63256	A1578	960-08306	MODEM-CONTROL Data Cable
ea. consists of:	2	92194		332-20100	2x10x0.1 Ribbon Cable Connector
	3"	92194		830-20000	20 Conductor Ribbon Cable

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A5-W8	1	63256	A1578	960-08307	CONTROL-REMOTE CONTROL Cable
consists of:	1	00779		333-10250	DB25S Connector
	1	00779		332-16100	2x8x0.1 Header Plug
	8	00779		332-87666	Crimp Pins
	8x2"	28105			No.22 Str. Wire; 2xBLK, BRN, RED, OR, GRN, GRY, BLU
A5-W9	1	63256	A1578	960-08308	MODEM-XMTR Cable
consists of:	1	H0006		310-04000	4 Pin Audio Conn.
	1	06383		332-04100	1x4x0.1 Post Lock Plug
	4x2"	28105			No. 22 Str. Wire; YEL, GRN, BLU, V
A5-W10	1	63256	A1578	960-08310	MODEM-CRT Cable
consists of:	2	92194		332-20100	2x10x0.1 Ribbon Cable Connector
	4"	92194		830-20000	20 Conductor Ribbon Cable

5.7 ACCESSORY ASSEMBLY A6 - P/N 970-08000

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
P1	1	H0006		310-04001	4 Pin Audio Plug
A6-W1	1	70903		333-17250	AC Power Cord
KN1	1	95146		850-18005	1.25" Spinner Knob
WR1	1	95146		850-80001	Allen Wrench
OP MAN	1	63256		870-08000	ST8000 OPERATOR'S MANUAL
OP GUIDE	1	63256		870-08002	ST8000 OPERATOR'S GUIDE

5.8 SPARE PARTS KIT - P/N 980-08001

The following spare parts kit is available for the ST8000:

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
A1	1	63256		930-08000	MODEM ASSEMBLY A1
A2	1	63256		932-08000	CONTROL ASSEMBLY A2
A3	1	63256		920-08000	FRONT PANEL ASBY A3
A4	1	63256		915-08000	CRT ASSEMBLY A4
A5-T1	1	63256		800-08001	Power Transformer
Ux	1 set	63256		980-08010	100% Spare Integrated Circuits

(Contents of Spare IC Kit on following page)

The recommended quantity of ST8000 Spare Parts Kits is as follows:

NUMBER of ST8000	NUMBER of SPARE KITS	COMMENTS
1 - 5	1	
5 - 10	1	1 Additional IC Kit recommended
10 - 20	2	
20 - 49	3	1 Additional IC Kit recommended
50 -100	4	
100 - up	4/100 units	Additional IC Kits as desired.

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Spare Integrated Circuits Kit (980-08010):

REFERENCE NO.	QUAN	FSCM	DWG NO	PART NO	DESCRIPTION
	1	27014		630-00709	709 OP-AMP
	4	04713		630-00741	741 OP-AMP
	16	04713		630-01458	1458 Dual OP-AMP
	4	04713		630-01488	1488 4xRS232 Driver
	1	04713		630-01489	1489 4xRS232 Rcvr
	1	27014		630-02917	LM2917 F-V Conv.
	2	02735		630-03081	CA3081 6xNPN Trans
	2	04713		630-03340	MC3340P AGC AMP
	3	04713		630-04741	4741 Quad OP-AMP
	2	34314		630-05613	R5613 LP Filter
	1	34314		630-05614	R5614 1/3 Oct BPF
	1	34314		630-05615	R5615 1/2 Oct BPF
	1	34314		630-05616	R5616 1.0 Oct BPF
	2	34314		630-05621	R5621 Adj BP Filter
	1	07263		630-07808	7808 +8V Regulator
	1	07263		630-07908	7908 -8V Regulator
	7	27014		630-75491	75491 4xLED Driver
	1	27014		635-00323	LM323 5V Regulator
	1	18324		643-07400	74LS00 4x2 NAND
	1	18324		643-07402	74LS02 4x3 NOR
	1	04713		643-07404	74LS04 6xINV
	4	04713		643-07474	74LS74 2xD FF
	1	18324		643-07486	74LS86 4x2 XOR
	6	27014		643-74138	74LS138 3-8 Decoder
	1	18324		643-74148	74LS148 8-3 Encoder
	4	04713		643-74157	74LS157 4x2-1 MPLX
	4	04713		643-74244	74LS244 8xBuffer
	17	04713		643-74283	74LS283 4Bit BIN AD
	2	18324		643-74290	74LS290 Decade Cntr
	10	04713		643-74373	74LS374 8xD FF
	2	04713		643-74393	74LS393 4Bit Cntr
	1	02735		644-74151	74HC151 8IN Select
	17	27014		645-74374	74HCT374 8xD FF
	2	02735		650-04001	4001 4x2 NOR
	1	02735		650-04002-	4002 2x4 NOR
	5	02735		650-04011	4011 4x2 NAND
	1	02735		650-04017	4017 Decade Counter
	1	02735		650-04023	4023 3x3 NAND
	1	02735		650-04025	4025 3x3 NOR
	2	02735		650-04030	4030 4x2 XOR
	3	02735		650-04049	4049 6xINV
	2	02735		650-04052	4052 2P4T CMOS SW
	2	02735		650-04053	3xDPDT CMOS SW
	5	02735		650-04066	4xSPST CMOS SW
	2	01295		670-02764	2764 EPROM
	1	H0001		670-01220	DS1220Y Battery RAM
	1	56708		680-00080	Z80 CPU
	1	34649		680-08251	8251A USART
	1	34649		680-08253	8253 Int. Timer
	1	56708		680-08470	Z8470 DART
	1	94696		751-01911	SPST 5V DIP Relay

5.9 FEDERAL SUPPLY CODES FOR MANUFACTURERS

The following is a list of the Federal Supply Codes for Manufacturers used in the preceding parts lists. Other manufacturers may be acceptable - check with the HAL factory before making substitutions. Firms that did not have a listed FSCM as of the April, 1985 edition of the FSCM index have been assigned sequential Hxxxxx numbers.

NUMERICAL ORDER:

FSCM	MANUFACTURER	CITY
00779	AMP, Inc.	Harrisburg, PA
01295	Texas Instruments	Dallas, Texas
02735	RCA Semiconductors	Sommerville, NJ
04061	Allen Bradley Co.	Chicago, IL
04222	AVX Corp.	Myrtle Beach, SC
04713	Motorola Semiconductor	Phoenix, Arizona
05245	Corcom, Inc. (CD)	Libertyville, IL
06383	Panduit Corp.	Tinley Park, IL
07263	Fairchild Semiconductor Div.	Mountain View, California
12697	Clarostat Mfg. Co.	Dover, New Hampshire
13396	Telefunken (Gmbh)	Hanover, Germany
14433	ITT Semiconductor	West Palm Beach, Florida
15450	ERIE / Murata Corp.	Erie, PA
18324	Signetics Corp.	Sunnyvale, California
21604	Buckeye Stamping Co.	Columbus, OH
25243	Cornell Dubilier Electronics	Sanford, NC
23875	M-TRON Industries	Yankton, SD
27014	National Semiconductor	Santa Clara, CA
28105	Dearborn Wire & Cable Corp.	Rosemont, IL
30161	AAVID Engineering Inc.	Laconia, NH
31433	Union Carbide Corp. (Kemet)	Greenville, NH
34314	E G & G Reticon	Sunnyvale, CA
34649	INTEL Corp.	Santa Clara, CA
51167	ARIES Electronics, Inc.	Frenchtown, NJ
56289	Sprague Electric Co.	North Adams, MA
56708	ZILOG Inc.	Campbell, CA
57668	R-OHM Corp.	Irvine, CA
59422	Holmberg Electronics	Irvine, CA
59756	Siemens Corp. (Litronics)	Anaheim, CA
63256	HAL Communications Corp.	Urbana, Illinois
70903	Belden Corp.	Geneva, IL
71450	CTS Corporation	Elkhart, IN
74840	Illinois Capacitor Inc.	Lincolnwood, IL
75915	TRACOR / Littlefuse Inc.	Des Plaines, IL
80031	MEPCO / ELECTRA Inc.	Morristown, NJ
80294	Bourns Instruments, Inc.	Riverside, CA

NUMERICAL ORDER (Continued):

FSCM	MANUFACTURER	CITY
81073	Grayhill, Inc.	La Grange, IL
83289	Switchcraft, Inc.	Chicago, IL
91506	AUGAT, Inc.	Attleboro, MA
91833	Keystone Electronics Corp.	New York, NY
92194	Alpha Wire Corp.	Elizabeth, NJ
94696	Magnecraft Electric Co.	Chicago, IL
95146	ALCO Electronic Products	North Andover, MA
H0001	Dallas Semiconductor	Dallas, TX
H0002	Herman H. Smith, Inc.	Brooklin, NY
H0003	Inter-Technical Group	Irvington, NY
H0004	Panasonic Optoelectronics	Secaucus, NJ
H0005	U.S. Digital	Los Alamitos, CA
H0006	VANCO Inc.	Lake Bluff, IL

ALPHABETICAL BY MANUFACTURER:

FSCM	MANUFACTURER	CITY
30161	AAVID Engineering Inc.	Laconia, NH
95146	ALCO Electronic Products	North Andover, MA
04061	Allen Bradley Co.	Chicago, IL
92194	Alpha Wire Corp.	Elizabeth, NJ
00779	AMP, Inc.	Harrisburg, PA
51167	ARIES Electronics, Inc.	Frenchtown, NJ
91506	AUGAT, Inc.	Attleboro, MA
04222	AVX Corp.	Myrtle Beach, SC
70903	Belden Corp.	Geneva, IL
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21604	Buckeye Stamping Co.	Columbus, OH
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05245	Corcom, Inc. (CD)	Libertyville, IL
25243	Cornell Dubilier Electronics	Sanford, NC
71450	CTS Corporation	Elkhart, IN
H0001	Dallas Semiconductor	Dallas, TX
28105	Dearborn Wire & Cable Corp.	Rosemont, IL
34314	E G & G Reticon	Sunnyvale, CA
15450	ERIE / Murata Corp.	Erie, PA
07263	Fairchild Semiconductor Div.	Mountain View, California
81073	Grayhill, Inc.	La Grange, IL
63256	HAL Communications Corp.	Urbana, Illinois
H0002	Herman H. Smith, Inc.	Brooklin, NY
59422	Holmberg Electronics	Irvine, CA
74840	Illinois Capacitor Inc.	Lincolnwood, IL
34649	INTEL Corp.	Santa Clara, CA
H0003	Inter-Technical Group	Irvington, NY
14433	ITT Semiconductor	West Palm Beach, Florida
91833	Keystone Electronics Corp.	New York, NY
23875	M-TRON Industries	Yankton, SD

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ALPHABETICAL ORDER (Continued):

FSCM	MANUFACTURER	CITY
94696	Magnecraft Electric Co.	Chicago, IL
80031	MEPCO / ELECTRA Inc.	Morristown, NJ
04713	Motorola Semiconductor	Phoenix, Arizona
27014	National Semiconductor	Santa Clara, CA
H0004	Panasonic Optoelectronics	Secaucus, NJ
06383	Panduit Corp.	Tinley Park, IL
02735	RCA Semiconductors	Sommerville, NJ
57668	R-OHM Corp.	Irvine, CA
59756	Siemens Corp. (Litronics)	Anaheim, CA
18324	Signetics Corp.	Sunnyvale, California
56289	Sprague Electric Co.	North Adams, MA
83289	Switchcraft, Inc.	Chicago, IL
75915	TRACOR / Littlefuse Inc.	Des Plaines, IL
13396	Telefunken (Gmbh)	Hanover, Germany
01295	Texas Instruments	Dallas, Texas
31433	Union Carbide Corp. (Kemet)	Greenville, NC
H0005	U.S. Digital	Los Alamitos, CA
H0006	VANCO Inc.	Lake Bluff, IL
56708	ZILOG Inc.	Campbell, CA

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