DS3100 ASR
CUSTOMER MAINTENANCE MANUAL

INSTRUCTION MANUAL

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HAL DS3100 ASR VIDEO DISPLAY TERMINAL

CUSTOMER MAINTENANCE MANUAL

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Preface:

This DS3100 Customer Maintenance Manual provides technical information about the circuitry of the DS3100 ASR terminal and presents a step-by-step troubleshooting guide. The DS3100 has been designed in a plug-in board, modular arrangement, and the troubleshooting guide is designed to isolate problems to specific boards whenever possible. When the defective module(s) is located, please contact the factory (or authorized HAL distributor in the case of European customers) so that arrangements can be made for repair of the module(s). This approach should expedite repairs of units and reduce the danger of shipping damage that might occur if the entire terminal were returned for repair. Since special test fixtures are required to test circuitry on each board, it is highly recommended that repair of the boards themselves be left to factory or authorized distributor technicians.

This manual is organized in six sections, presenting a discussion of the circuitry, disassembly procedures, specifications and limitations, trouble-shooting, adjustments and options, and schematic diagrams. It is recommended that you give all sections at least a cursory reading before beginning any tests or measurements.

The troubleshooting flow diagram has been prepared to utilize on-screen symptoms and I/O tests, minimizing the amount of external test equipment required. A good 20,000 ohms-per-volt VOM may be the only piece of test equipment you need! Other tests might require use of a frequency counter capable of measurement of up to 20 MHz. An oscilloscope is not required by the procedures given, but may prove useful.

Problems with the DS3100 can be placed in three general categories: those due to internal component failures, those due to a hostile environment, and those due to operator misunderstanding. As with all electronic equipment, some failure of internal circuitry may occur, particularly during the first few weeks of operation. However, the factory "burn-in" testing and the conservative design of the DS3100 have shown this mode of failure to be rare.

Equipment failures due to application of improper I/O connections or voltages, lightning strikes, or a hostile environment (water or excess heat), vary with the user. Experience has shown that the DS3100 problems can often be traced to these sources.

Experience has also shown that improper operator understanding of the many features of the DS3100 is often interpreted as an equipment malfunction. Please double check your operating procedures before "digging-into" the troubleshooting checks -- you may save yourself a lot of time and effort! If you discover a potentially confusing instruction in any of the manuals, please let us at the factory know so that future versions may be ammended. Use this DS3100 Customer Maintenance Manual in conjunction with your DS3100 Operator's Manual and Operator's Guide.

DS3100 ASR VIDEO DISPLAY TERMINAL

CUSTOMER MAINTENANCE MANUAL

CONTENTS:

FIGURES:

THE DS3100 ASR COMMUNICATIONS TERMINAL

1. SYSTEM DESCRIPTION

1.1 General Description

Circuitry of the DS3100 ASR is contained primarily on five printed circuit boards, which are connected by a backplane board and chassis wiring inside the ASR base section. The five boards or assemblies are the keyboard, video-display board (VDB), input/output board (I/O),central-processing-unit board (CPU), and power supply board. Fig. 1.1 shows the basic interconnections between these subassemblies. Each subassembly has a numerical designation, which is used to identify it. These designations appear on each printed circuit board to help make identification easier.

1.2 Central Processing Unit

The "heart" of the CPU board and the entire terminal is a type Z-80, silicon-gate, N-channel MOS, 8-bit microprocessor IC. The Z-80, along with the associated Read-Only Memory (ROM), Random-Access Memory (RAM), Electrically-Alterable ROM (EAROM), bi-directional bus drivers, programmable interval timer, Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and I/O device-select circuitry control all ASR operations (See Fig. 1.2). Communication between the above devices and the Z-80 is through the bi-directional data bus, address bus, and control signals such as I/O read/write and memory read/write. Operation of the Z-80 CPU requires that a multitude of commands, data and address information be communicated on a common multiconductor bus. An interrupt-based operating system is used to ensure that inter-device communications are carried out properly on this "party line". In this interrupt-based system, any of a number of devices can interrupt the processor. When the processor is interrupted, it reads the interrupt circuitry to determine "who" performed the interrupt. The processor then services the interrupting device.

The DS3100 ASR logic system uses acknowledge circuitry to verify communications. Each time the processor accesses a device, it WAITs until it receives an acknowledge from the device before continuing. Circuitry on the CPU board is shown in schematic form in drawings A-1330 through A-1334A.

1. Program Memory

All operations of the DS3100 ASR are performed by the Z-80 microprocessor as it performs sequential steps in the system program. This program, which contains all necessary instructions that the microprocessor must carry out, is contained in eight type 2708 Erasable Programmable ROMs (EPROMs). Typical subroutines stored in the ASR EPROMs are: Keyboard decoding, Morse-code decoding,

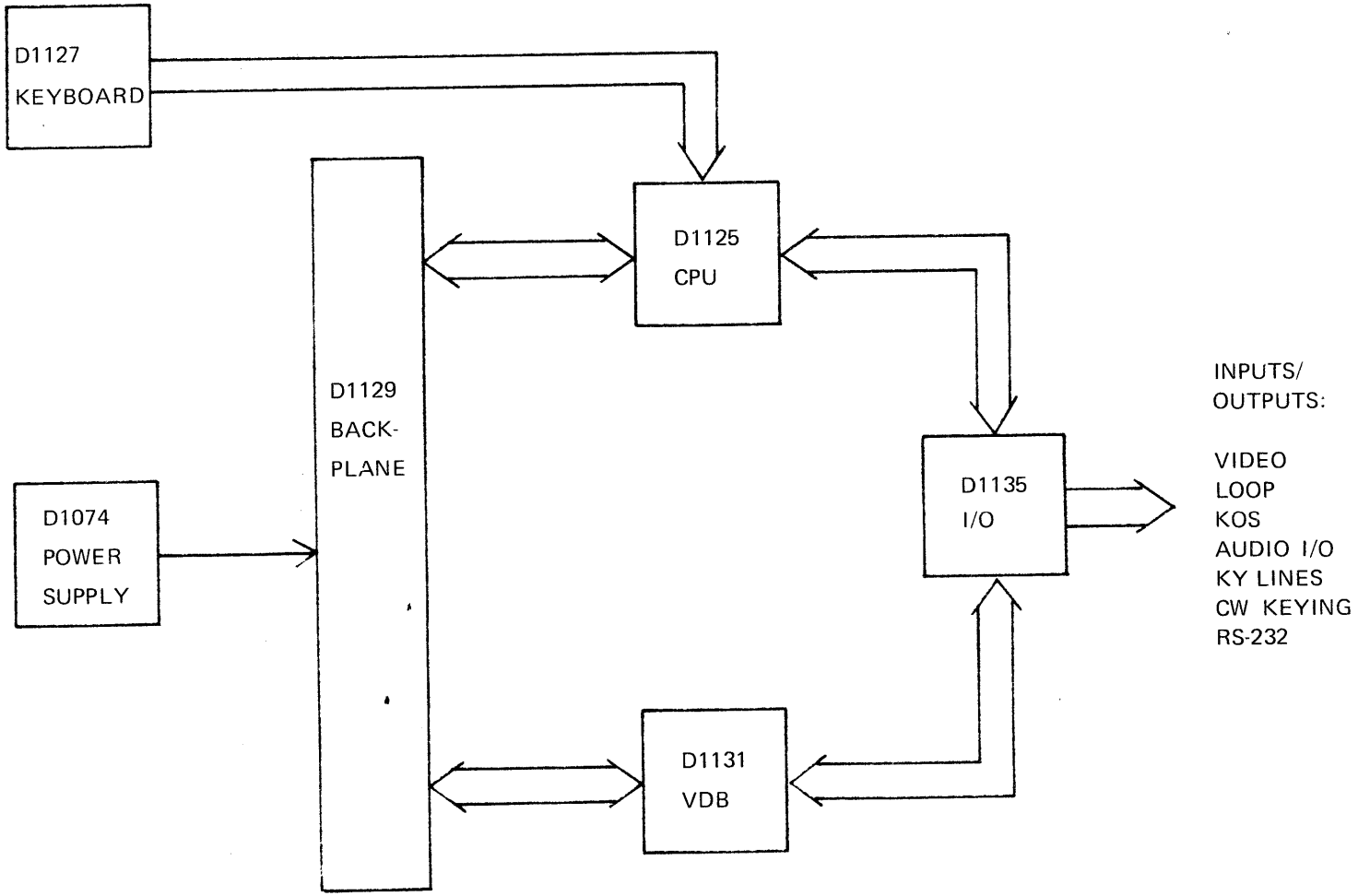


FIGURE 1.1 FUNCTIONAL BLOCK DIAGRAM OF THE DS3100 ASR

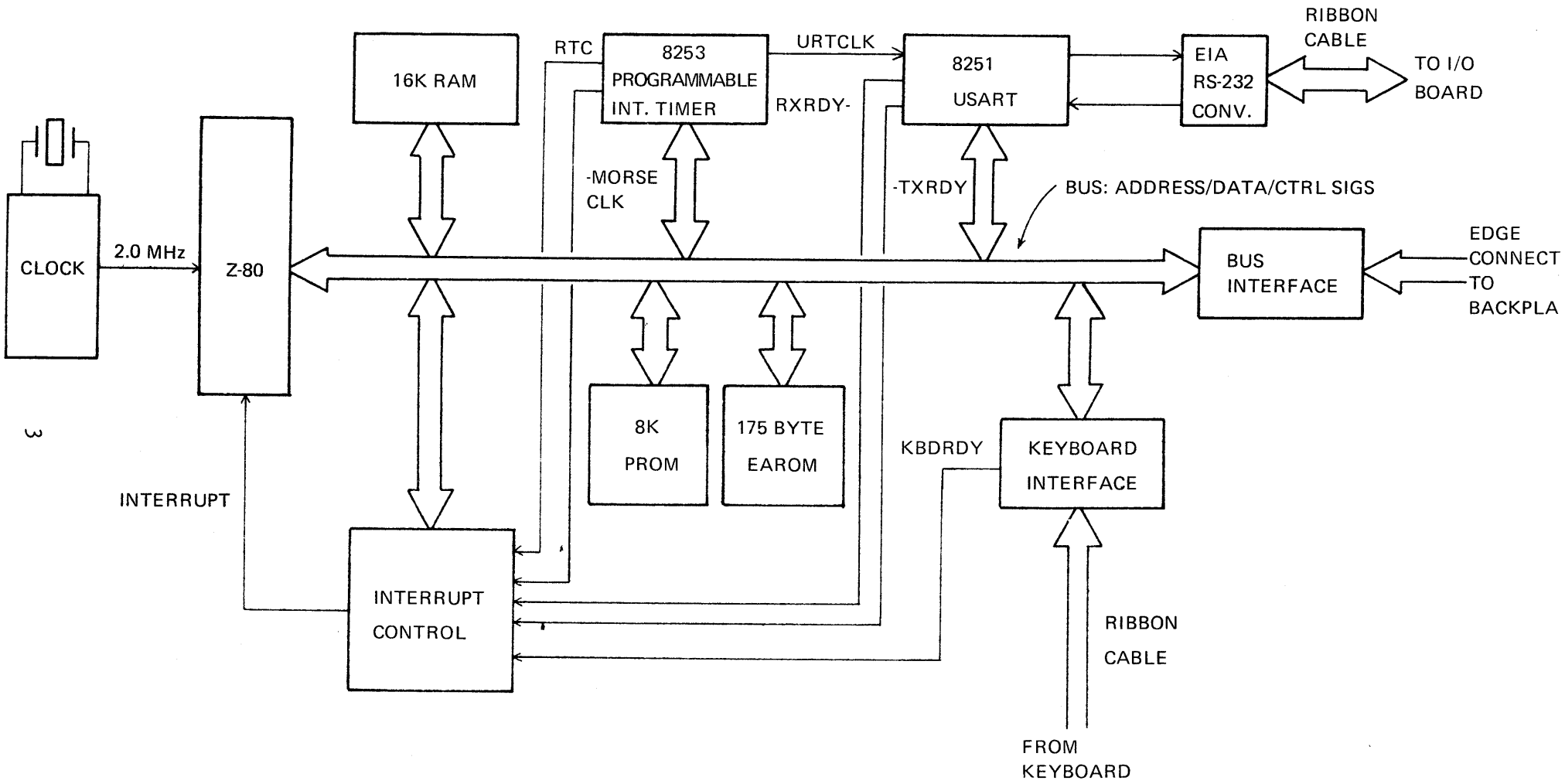


FIGURE 1.2 BLOCK DIAGRAM OF THE CPU SECTION OF THE ASR

I/O control, real-time clock, speed-change routines, and video-display management routines. The program information stored in memory devices is often referred to as "software" to differentiate from the hard-wired or "hardware" part of the system.

The software in the DS3100 ASR is installed in plug-in sockets, assuring simple replacement if future software updates are made available.

2. Text Storage Memory

The CPU board contains 16k bytes of memory, which is used to store all text in the 150-line receive buffer and the 50-line transmit buffer. Eight type 2117 dynamic RAM ICs (each 16k x 1 bit) are used to store all text, whether it is being displayed on the video screen or not. When a section of text is to be displayed (either transmit or receive buffer), the necessary data is copied or written from the proper addresses in CPU RAM to the display memories on the VDB.

3. Non-Volatile Memory

One other type of ancillary memory associated with the Z-80 microprocessor is the non-volatile memory or EAROM. Current versions of the ASR are supplied with one ER1400 IC (1400 x 1 bit) while early versions contained two NC7033 ICs (each 21 x 16 bits). All data is written to and read from the EAROM in serial form. The EAROM device stores initial-turn-on terminal operating conditions, WRU message memory, and the non-volatile HERE-IS messages.

4. I/O Device Selection Circuitry

Since several peripheral devices (such as the keyboard, USART, and EAROM) share the same data lines, there must be some way to enable only the desired device. This requirement is filled by a 74LS138 decoder that generates "chip enable" commands for each device by decoding address lines and control signals.

5. Speed Control and USART

A type 8251 USART IC performs the serial-to-parallel conversion of received data, and vice-versa for transmitted data. The 8251 also determines the bit length of a serial I/O word (5-unit for Baudot or 8-unit for ASCII), inserts start and stop bits as required and provides control signals indicating I/O status to the CPU. The 8253 programmable divider provides the USART clock and thereby determines data rates of the terminal. Up to 32 different I/O baud rates can be selected through bit patterns stored in ROM. Current ASR software provides for 5 baudot rates (45 - 100 Bd.), and 9 ASCII rates (110 - 9600 Bd.).

Input and output data from the USART is buffered to be compatible with EIA-standard RS-232C signal levels on the I/O interface board.

6. Programmable Interval Timer

A type 8253 IC is used to provide three clock signals used on the CPU board: TMRØ (timer zero), TMR1 (timer one), and BAUD CLOCK/URTCLK. Timer zero is used by the processor in updating the real-time-clock (RTC) display, timer one is used as a reference clock in decoding Morse code, and BAUD CLOCK/URTCLK is used to set the serial receive/transmit rates. Via the data lines, the processor provides the initial counter states, which determine the timing periods for the three counters. When each timer completes its timing period, it outputs a signal that interrupts the processor.

1.3 Video Display Board

The video display board contains display circuitry and memory, Morse-receive interface circuitry, KY switch outputs, KOS output, CW-keying outputs, sidetone oscillator, and retransmit-data circuitry. Figs. 1.3, 1.4, and 1.5 provide block diagrams of the three main sections of VDB circuitry.

1. VDB Display Section

Fig. 1.3 shows the video display section of the VDB board in block-diagram form. Video display memory consists of 16 type 2102AL-4 static RAM ICs (each 1k x 1 bit) for a total of 2k bytes. Timing of the video display circuitry is based on clock signals that are generated from a 14.1925-MHz crystal oscillator (13.9776-MHz in 50-Hz units) that is divided appropriately to the dot rate, horizontal-scan rate and vertical-scan rate. Two 8678 character generators generate the proper bit pattern required for each ASCII character as the characters are received from the data outputs of the static RAM. The serial video information is combined with vertical and horizontal sync and blanking signals in the video combiner section to produce composite video to drive the display.

The multiplexer passes memory addresses to the display memory. These addresses are obtained either from the display address counters or from the microprocessor address bus, depending upon the $\overline{\text{VIDACT}}$ input from memory address arbitration. The arbitration circuitry is used to manage the display memory, allowing the microprocessor to read or write the memory only when a horizontal or vertical retrace is occurring, or during empty scan lines between character lines. During all other times, the addresses from the counters are allowed to pass through to the display memory. The video display section of the VDB is shown schematically in drawings A-1341 through A-1344.

2. VDB CW/KY Switching Section

The block diagram in Fig. 1.4 displays the circuitry used to generate the retransmit-data, KY switch, CW-keying, KOS, and sidetone outputs.

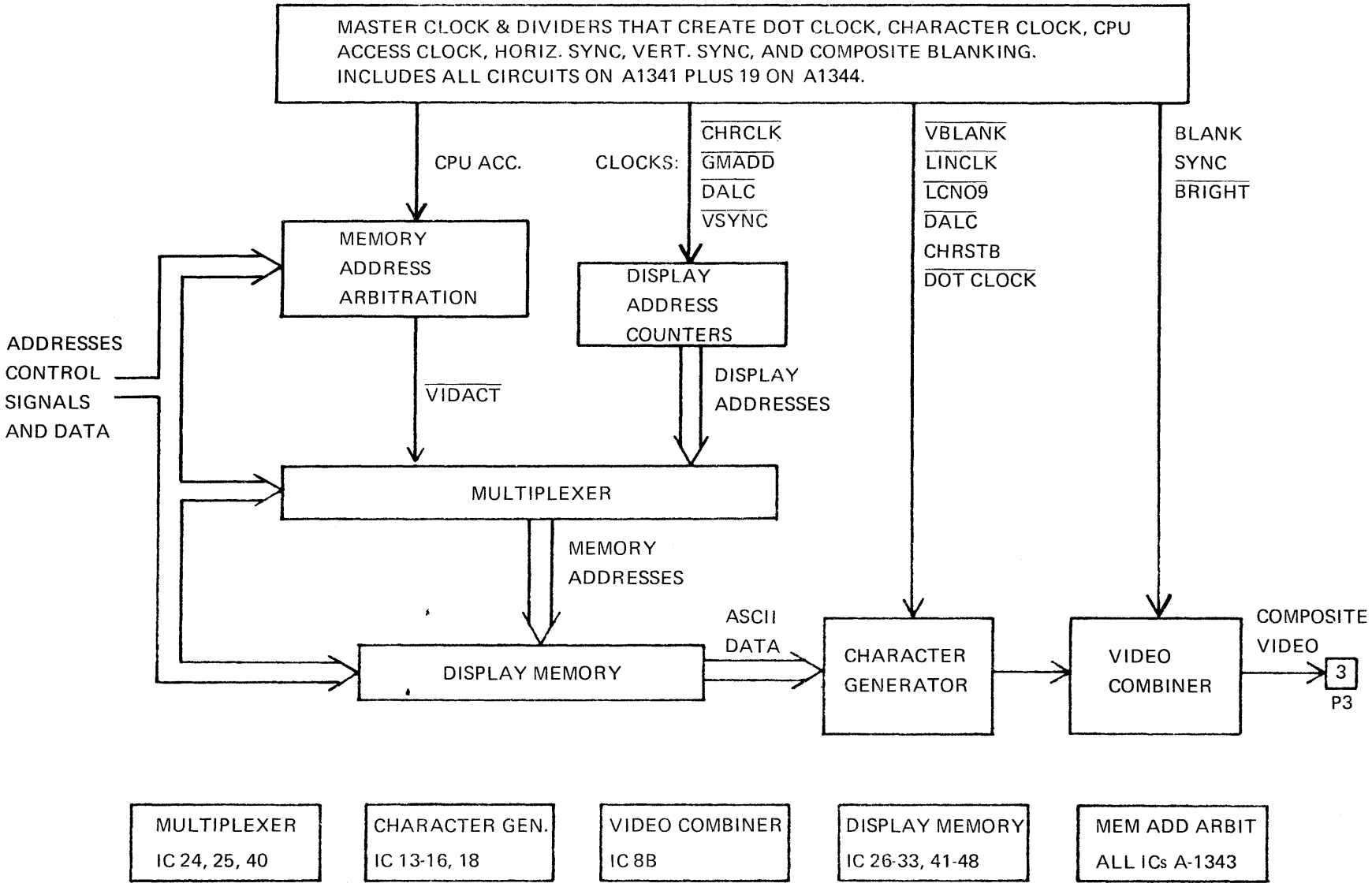


FIGURE 1.3 BLOCK DIAGRAM OF THE VIDEO SECTION OF THE VDB

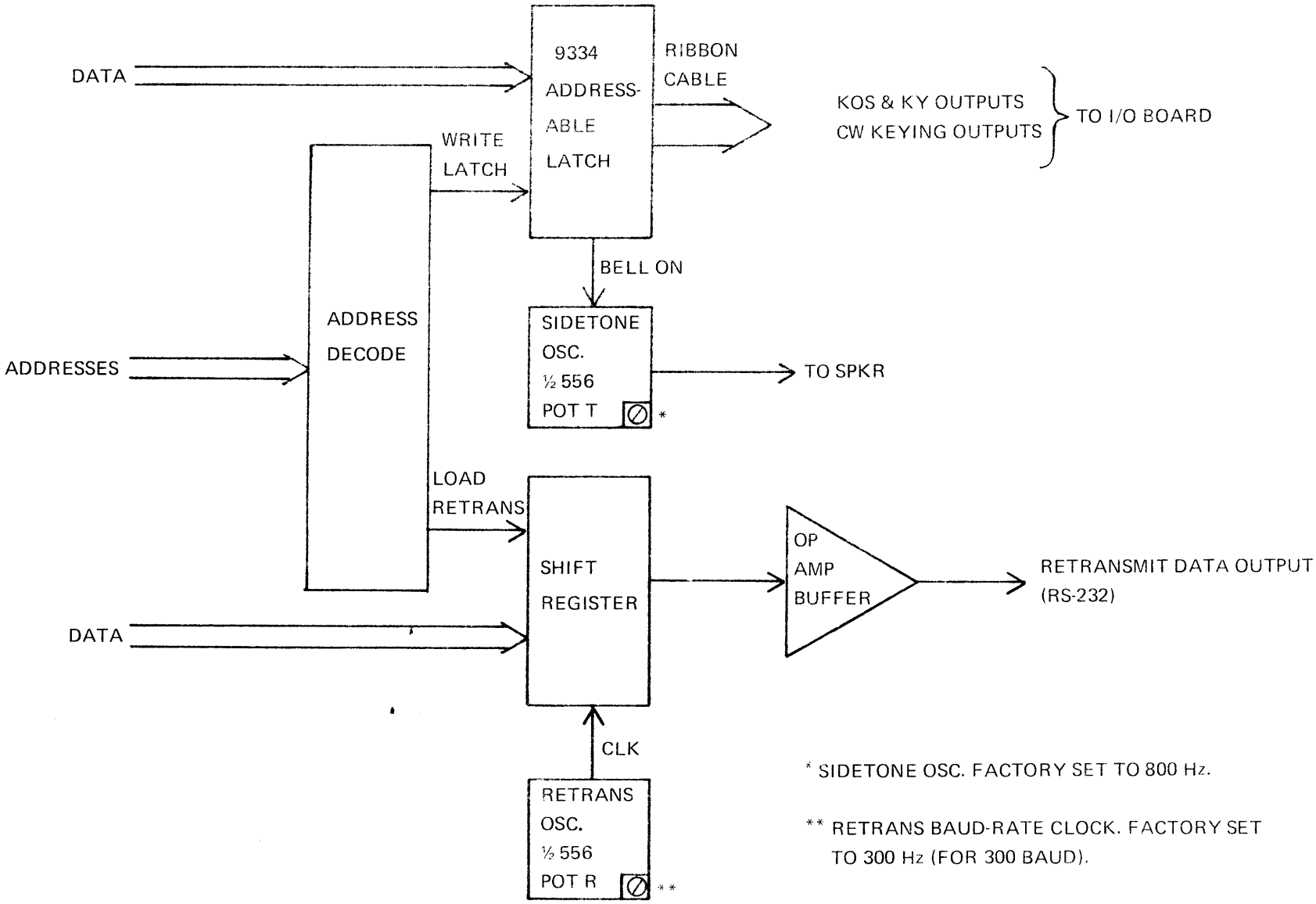


FIGURE 1.4 BLOCK DIAGRAM OF RETRANS-DATA, KOS, KY, CW KEYING ON VDB

Addresses from the backplane are decoded and used to generate the write-latch and load-retrans signals used to enable the addressable latch and shift register respectively. Outputs from the addressable latch are used to turn on KY switches, CW-keying outputs, the sidetone oscillator (bell) and KOS line.

The load-retrans signal causes the shift register to load an ASCII code in parallel from the data bus. Then it is shifted out serially through a buffer to be compatible with EIA-standard RS-232C. One half of a 556 dual timer IC is used to generate the clock pulses for the shift register. The other half generates the sidetone audio that is amplified by a complimentary pair of bipolar transistors. Drawing A-1338 provides a schematic diagram of this section of the VDB.

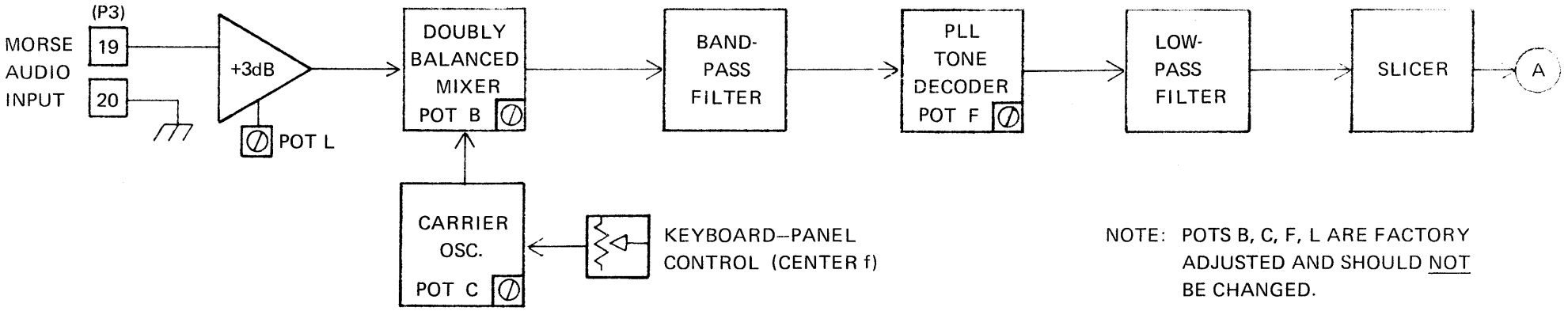
3. VDB Morse Receive Section

A block diagram depicting the Morse audio processing circuitry is contained in Fig. 1.5. Incoming audio is heterodyned with the local oscillator, with the sum of the two frequencies going through filtering before reaching the phase-locked-loop (PLL) tone decoder. In early ASR versions, all of the above circuitry, including the PLL decoder, is contained on a separate board attached to the VDB. Later versions contain video display boards that include all of the Morse receive circuitry. Details of both types are shown in the schematic diagrams of the VDB circuitry. Output from the PLL decoder is low-pass filtered before passing through a slicer stage, where the on-off keying information is "squared up" for use by the microprocessor system. An edge detector is then used to generate outputs for each transition (leading edge or trailing edge). These are used by the processor in determining the length of a code element, or how much time has passed between code elements. The specific key-down/key-up information is placed on data line DØ/. See drawings A-1337 and A-1337A for schematic presentation of the morse receive audio-input interface.

1.4 Keyboard

The keyboard circuitry is shown in block-diagram form in Fig. 1.6. The keyboard clock increments the keyboard counters, which generate sequential binary outputs that are input to the keyboard multiplexer and demultiplexer. These devices strobe the keyboard columns and rows until a depressed keyswitch is encountered. When a key is pressed and the multiplexer/demultiplexer strobes across it, the multiplexer outputs a keypress signal. This goes through a debouncing circuit, and then is used to inhibit keyboard clock pulses from incrementing the counters further. The key-debounce circuitry also generates the keyboard-ready signal that is used to interrupt the processor so that it can read the keyboard data.

The counters are held in their inhibited states for 5 mS by the debounce circuitry, while the microprocessor reads the counters. Collectively, these counter states represent the depressed key. CTRL, FN, HERE-IS, and SHIFT operations are handled by a separate buffer and are not part of the scanned keyboard. See drawing A-1335A for schematic diagram of keyboard circuitry.



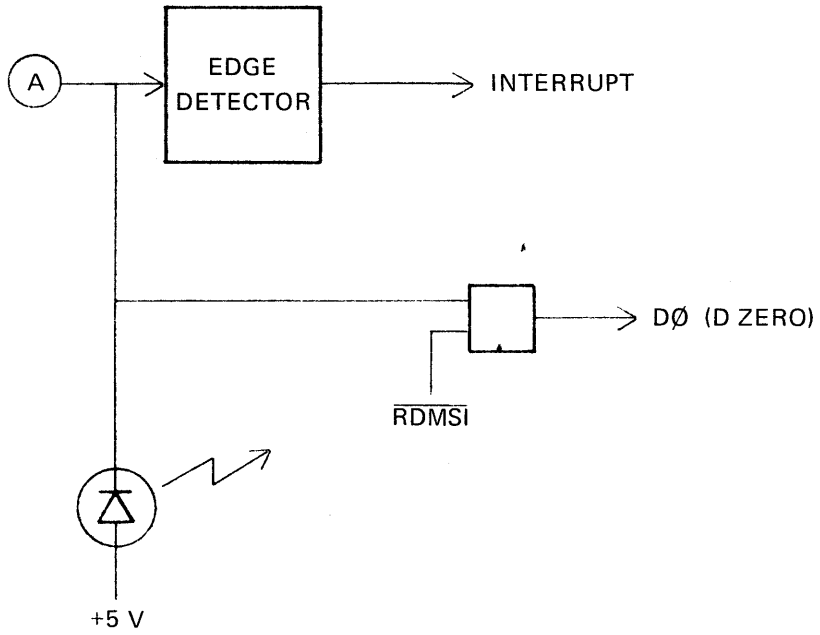


FIGURE 1.5 BLOCK DIAGRAM OF MORSE RECEIVE SECTION OF VDB

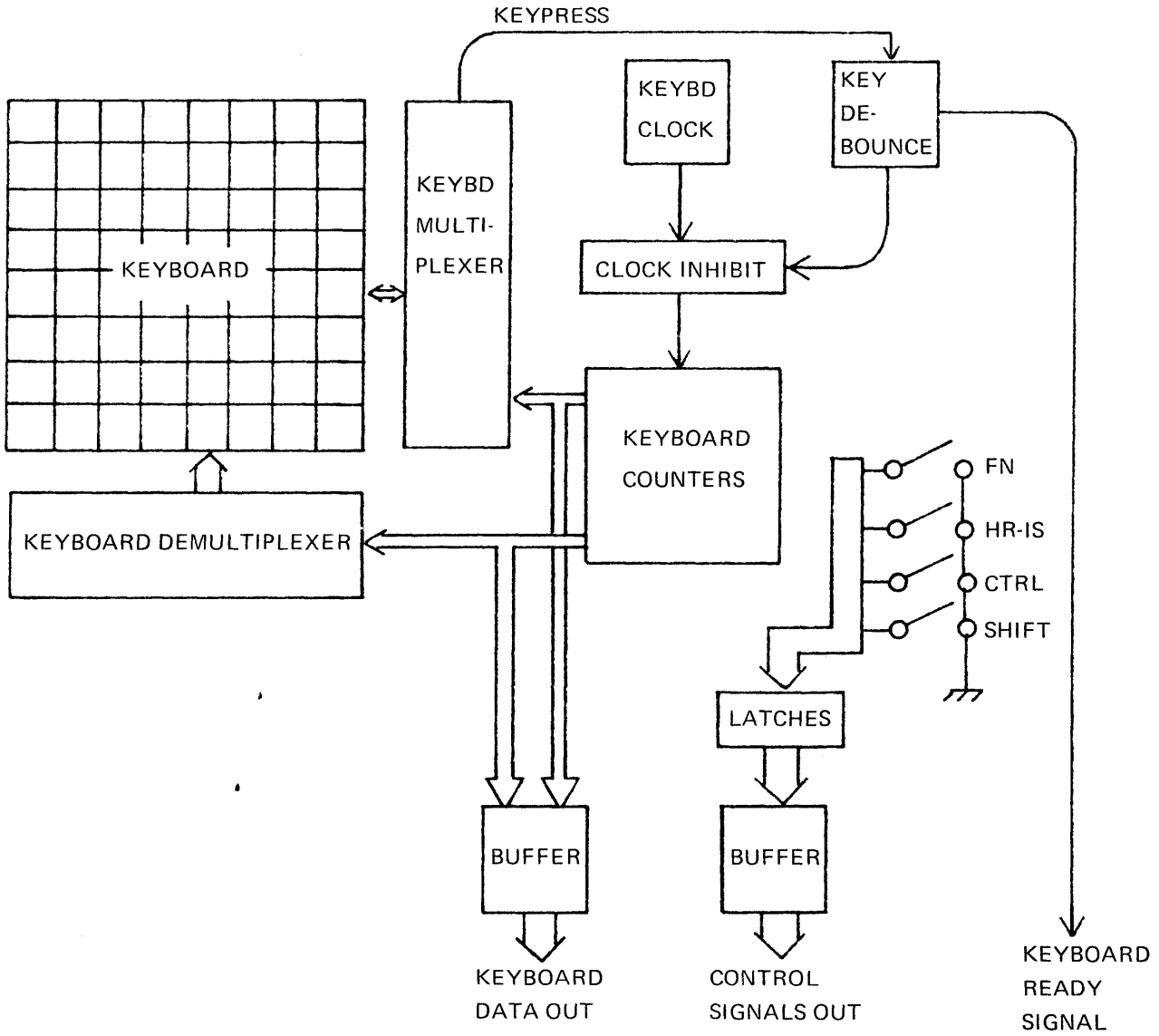


FIGURE 1.6 BLOCK DIAGRAM OF ASR KEYBOARD

1.5 Input/Output Board

As the name implies, the I/O board is used to interface the inputs and outputs associated with the DS3100 ASR to the outside world. Although most I/O board rear-panel connections are simply extended I/O lines from the VDB and CPU, two optical isolator circuits are also included. These opto-isolators are used to interface to external current-loop circuits, such as 60-mA Teletype-equipment loops. The I/O board circuitry is shown in schematic-diagram form in drawing A-1339.

1.6 Power Supply

The rectifiers, filter networks and voltage regulator ICs required to generate the +5, +12, and -12 supplies required by the ASR are contained in the power supply module. No adjustment should be necessary for operation of the power supply over power-line variations of 105 to 125 VAC. Operation over a range of 210 to 250 VAC is possible when transformer connections are made accordingly -- see Owner's Manual and Power-connections section of this manual. The power supply functions with either 50- or 60-Hz power input. The aluminum power-supply L-bracket serves as a heat sink for the regulator ICs and pass transistor. See drawing A-1261 for schematic presentation of the ASR power supply.

1.7 Backplane

The backplane board is used to connect address and data buses, control signals, and power-supply voltages to the VDB and CPU. The -5 V regulated supply required by the 2708 EPROMs, 2117 RAMs, and the early version of EAROMs is also generated on the backplane board. For schematic diagram, see drawing A-1340.

1.8 Cabinet Wiring

Wiring inside the ASR that is not contained on one of the previously mentioned assemblies, or in the interconnecting ribbon cables, consists of the transformer wiring, threshold potentiometer, CW-detect and power LEDs and the bell-tone speaker. These connections are shown schematically in drawing A-1345.

2. DISASSEMBLY OF THE DS3100 ASR

2.1

In the event that you need to open the ASR cabinet to check voltages, check connectors, or perform any other servicing function, BE SURE TO READ THE FOLLOWING INFORMATION FIRST:

```
**************************************
*              WARNING!              *
*  ALWAYS UNPLUG THE POWER CORD FROM *
*  THE DS3100 ASR AND DV3000 BEFORE  *
*  OPENING EITHER CABINET FOR SERVICE.*
*                                    *
**************************************
```

Before beginning any disassembly of the DS3100 ASR base section, first remove the DV3000 monitor, as described in the Owner's Manual. Turn off ASR power switch, disconnect non-captive line cord, and place ASR upside down on a protected work surface. Remove the 10 phillips-head screws that secure the bottom cover, lift off cover, and set it aside.

2.2 Removal of CPU and/or VDB

To remove either the VDB or CPU board from the card cage, first remove the retaining bracket held in place by two small screws (see Figs. 2.1 and 2.2). To remove the VDB from the card cage, first unplug the 26-pin plug on the ribbon cable from the socket on the video board. Next, loosen the board by rotating the two white plastic ejector levers outward simultaneously, and slide the board out of the card cage frame being careful to clear protruding components. To remove the CPU board, perform the same steps as above, removing the two ribbon cables from the CPU and the single cable from the VDB. Be sure that the ribbon cable plugs do not catch on any of the board components when the CPU board is removed.

2.3 Removal of card cage assembly

The VDB and CPU board should be removed from the card cage before the card cage/backplane assembly is unscrewed from the main chassis of the ASR. Unplug the mating molex connectors from the backplane and power supply before unscrewing the four screws that secure the card cage to the ASR chassis.

2.4 Removal of keyboard

To remove the keyboard from the ASR chassis, unplug the 20-pin ribbon cable from the keyboard and unscrew the four screws that secure the keyboard to the ASR chassis.

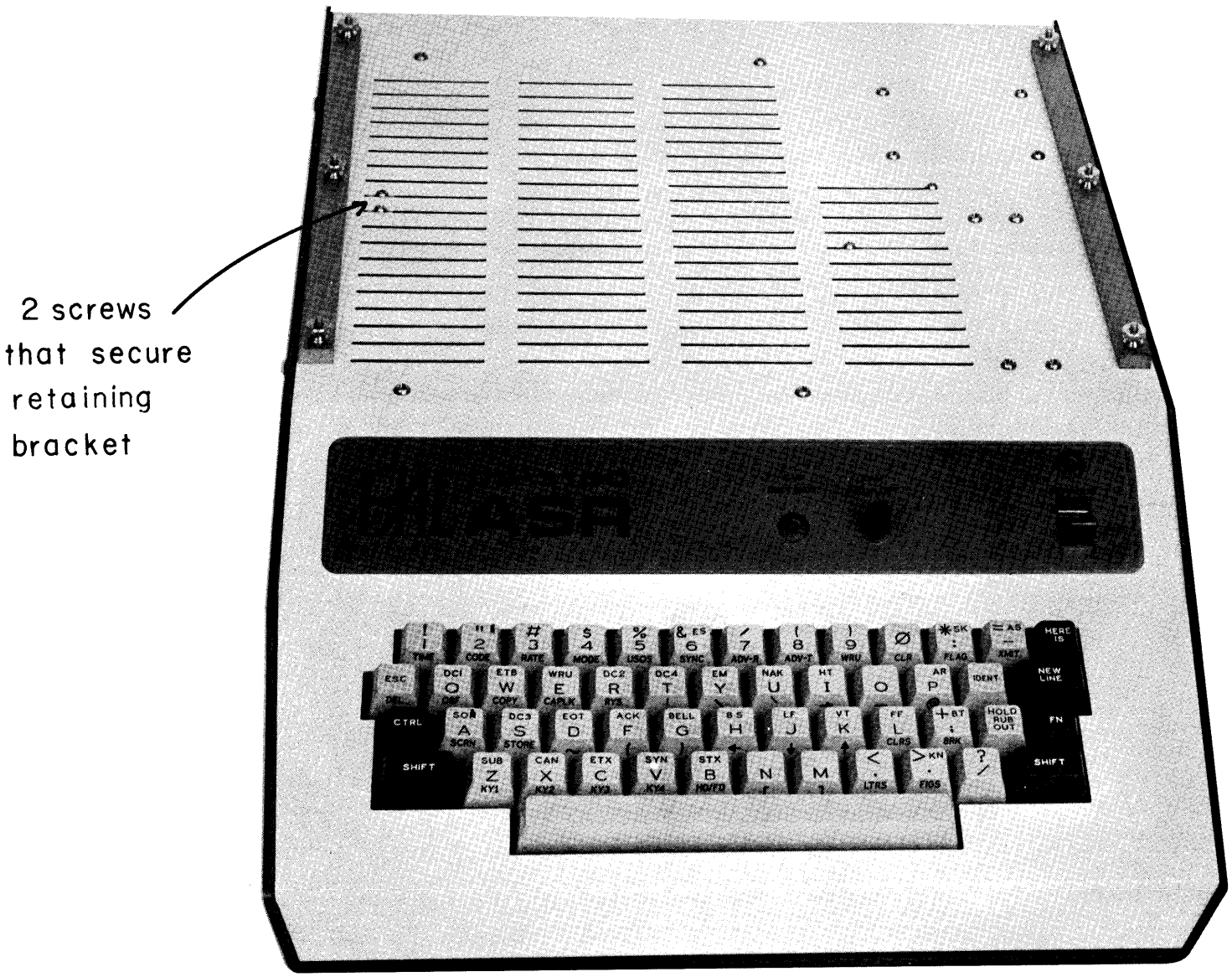


FIGURE 2.1 LOCATION OF SCREWS HOLDING BOARD-RETAINING BRACKET

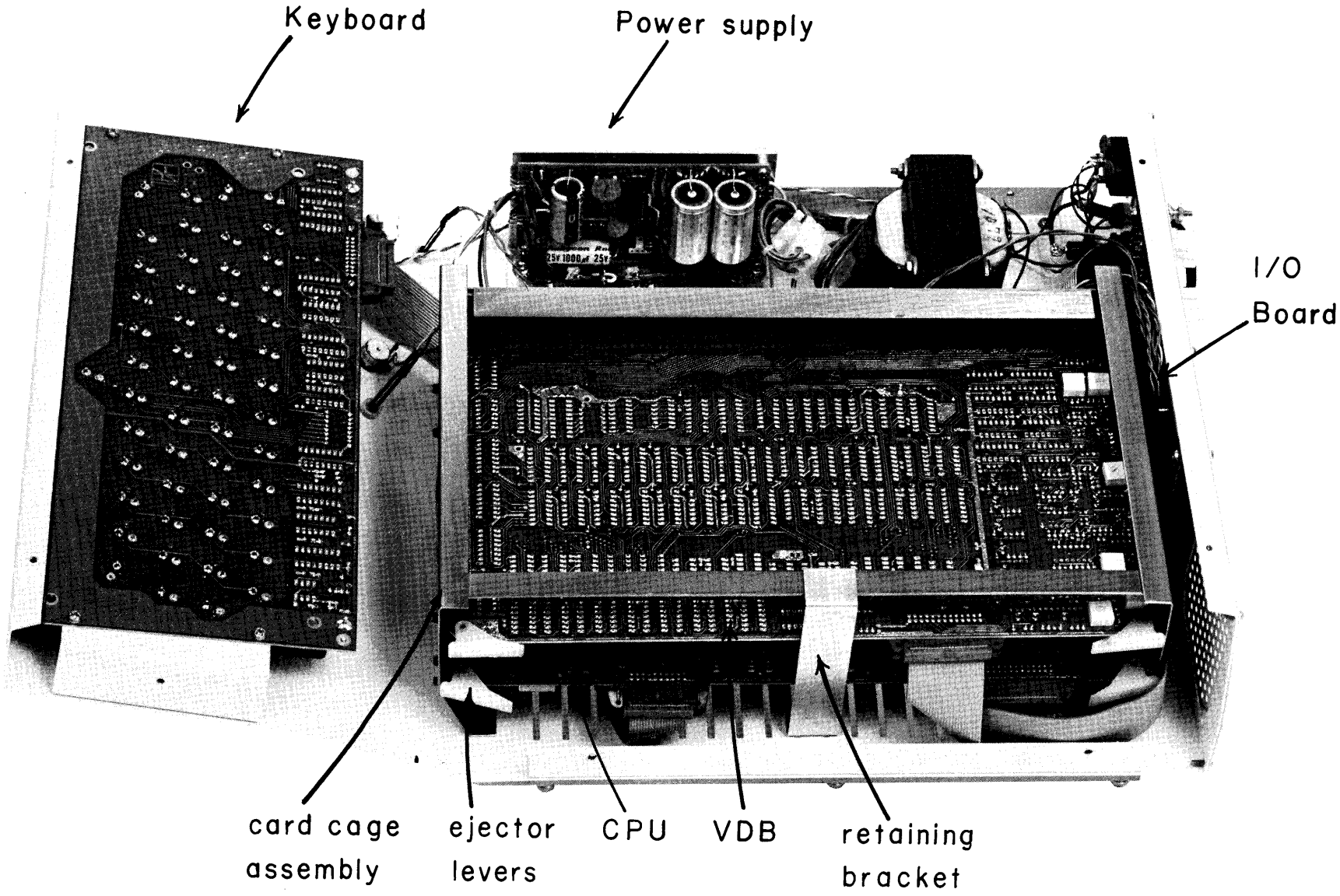


FIGURE 2.2 ASR INTERIOR -- IDENTIFICATION OF SUBASSEMBLIES

2.5 Removal of power supply module

The power supply module is fastened to the ASR chassis by four sets of 6-32 hardware. Before removing these screws and locknuts, unplug the two molex shells on the ends of the two cables attached to the power supply module (one going to the backplane, and one to the transformer).

2.6 Removal of the I/O (Input/Output) board

The card cage assembly must be removed before the I/O board can be accessed. Unplug the two 26-pin ribbon cable connectors from the I/O board, and disconnect the small 16-pin Berg connector (black plastic connector near top of board). Two wires must be unsoldered before the I/O board can be removed. The black ground wire leading from the I/O board to a solder lug on the ASR chassis must be unsoldered from this point, and the red "video" wire that feeds through the board and is then soldered to a small pad almost directly above, must also be unsoldered. Unscrew the four phillips-head screws that secure the I/O board, and then separate the board from the ASR rear panel by applying moderate pressure on the "audio-out" molex shell that protrudes through the rear panel until it pops through the panel. Do not use excessive force. When all of the shells have passed through the rear panel, slip the red wire back through the hole, freeing the I/O board.

2.7 Reassembly of ASR components in chassis

Follow the following steps in replacing any removed ASR components. In general, follow in reverse the procedure outlined in the respective section (2.1 - 2.6). The steps below are included to help ensure that proper reassembly is completed without difficulty.

1. Make certain that no cables are pinched when the bottom cover of the ASR is replaced and secured with screws.

2. Be sure to reinstall the CPU and VDB cards in the proper slots of the card cage: VDB on top, CPU on bottom (refer to Fig. 2.2). Also, be sure that cables are connected in the same manner that they were originally, with arrows on ribbon-cable plugs mating with those on the board sockets. Note that in the photographs the cables are always installed so that the ribbon wires protrude from the lower edge of the plug when viewed as shown in Fig. 2.2. Make sure that both boards are securely seated in their respective backplane edge connectors before installing the retaining bracket. Refer to Fig. 2.3 for details of ribbon cables.

3. Install all ribbon cable plugs on the I/O board and keyboard, and route them under and around the area to

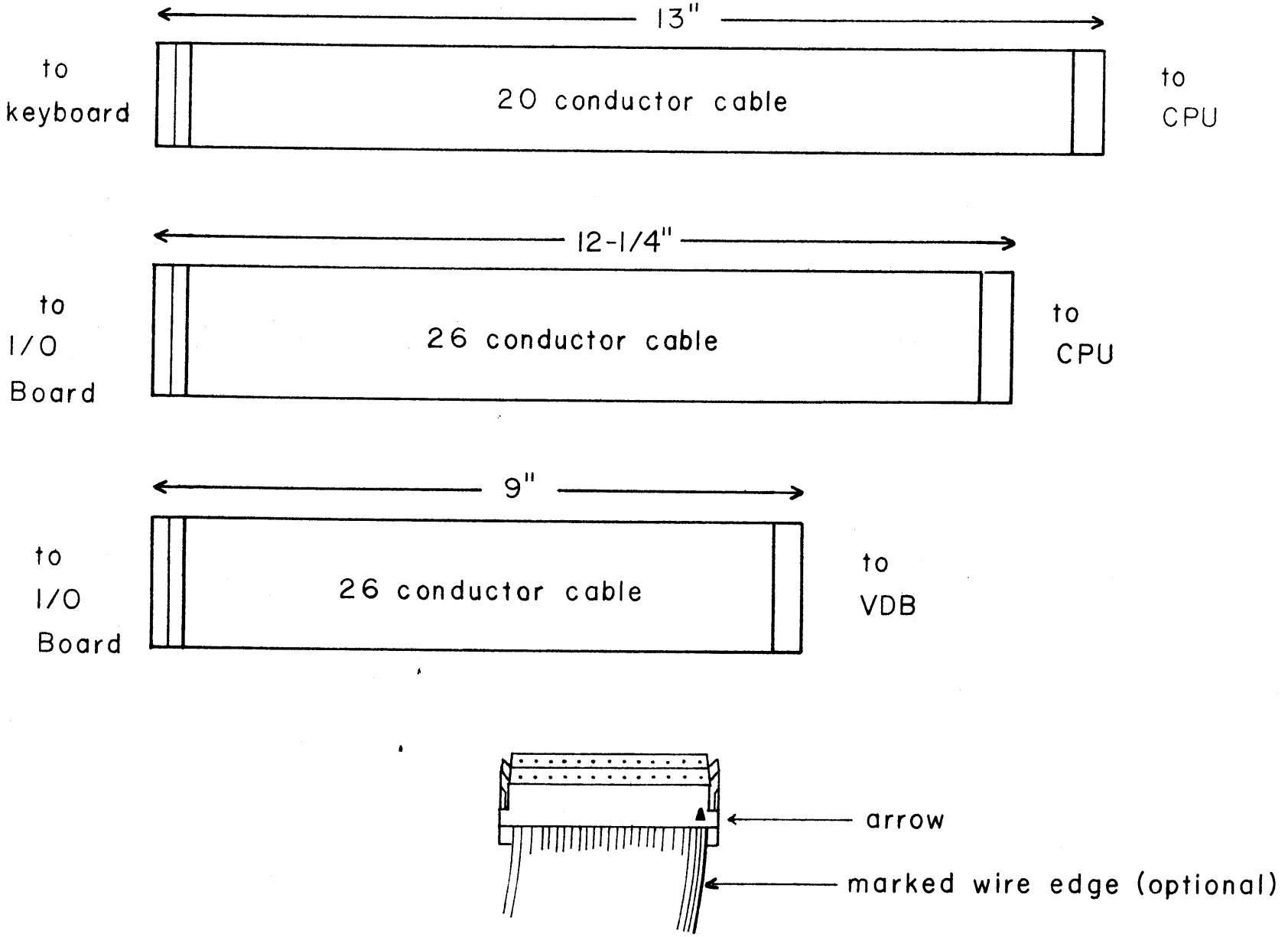


FIGURE 2.3 ASR CABLES AND CONNECTORS USED BETWEEN SUBASSEMBLIES

be occupied by the card cage assembly. Set the card cage in place, and start the four screws into the Pem nuts on the cage. Do not tighten the screws before ensuring that none of the ribbon cables are caught between the card cage bottom and the ASR chassis. Remember to reconnect the molex cable shell to the mating plug on the power supply module.

4. When the keyboard is reinstalled in the ASR chassis, the screws should not be tightened until it has been determined that all keyswitch buttons clear the chassis top without rubbing or binding on the edges of the metal cutout when depressed.

5. Be sure that both sets of molex-connector cables are plugged together after the power supply module is reinstalled in the ASR chassis.

6. When reinstalling the I/O board, feed the red video wire through the board hole marked "VO", insert the stripped end into the small pad just above that hole, and solder the connection. Also, solder the black ground wire back to the ASR chassis terminal lug it was removed from. Push the molex shells through the holes on the rear panel until they all "snap" into place, allowing the I/O board spacers to contact the rear panel. Secure with screws, and be sure to reconnect the proper ribbon cables, as indicated in Fig. 2.4. Also, be sure to plug the Berg connector into its socket on the I/O board, making sure that it is oriented properly--with the blue and purple wires at the end closest to the open side of the card cage.

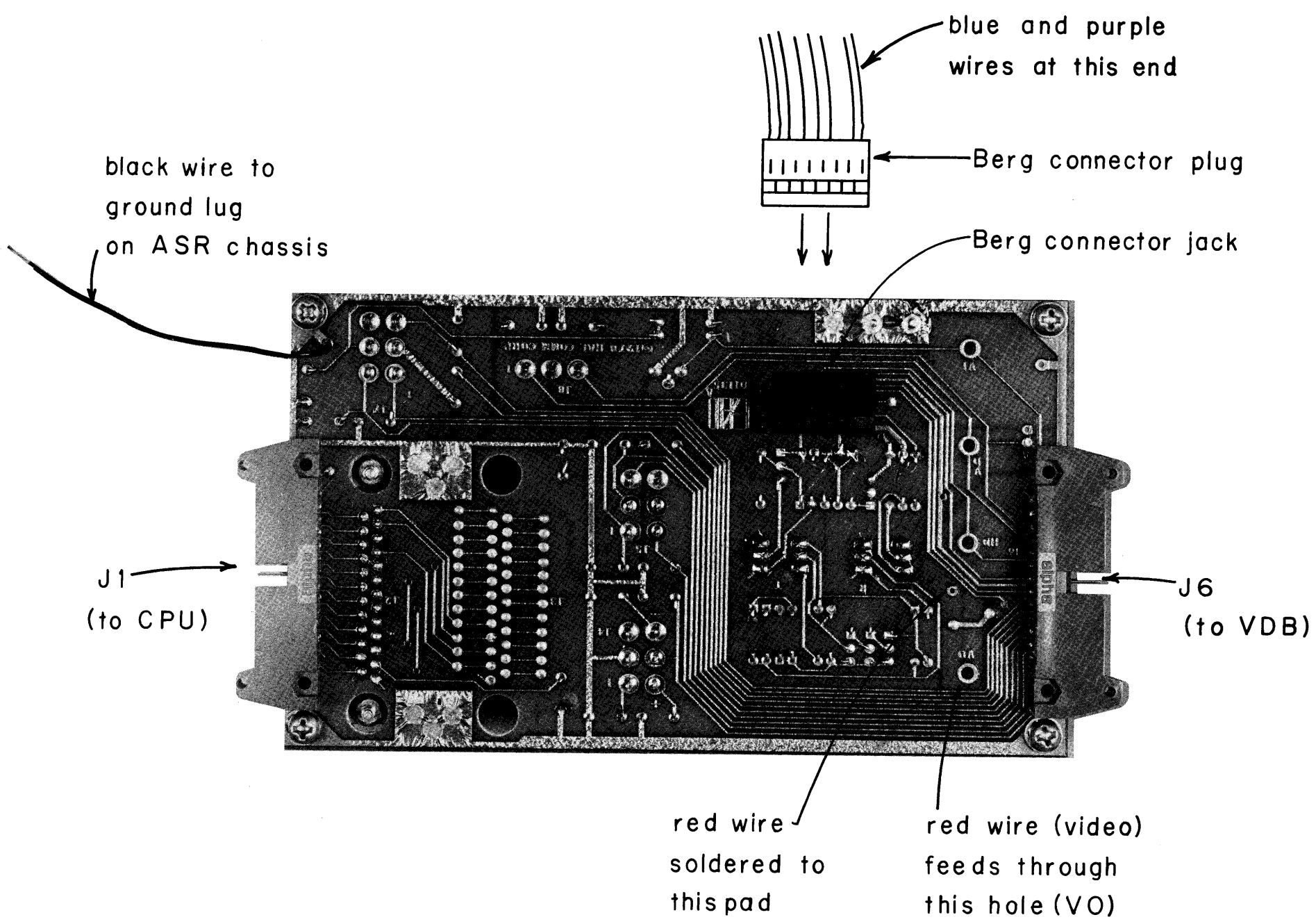


FIGURE 2.4 ASR I/O BOARD

3. I/O SPECIFICATIONS AND LIMITATIONS

Before making any connections to the DS3100 ASR, other than standard RTTY or CW interfacing as outlined in the Owner's manual, review the following specifications.

```
*********************************
*            CAUTION!           *
*                               *
*   IMPROPER CONNECTIONS MADE   *
*   TO ASR I/O PORTS MAY CAUSE  *
*   DAMAGE TO INTERNAL PARTS.   *
*********************************
```

Input/Output Data: (See Fig. 3.1)

Loop current input (J4-pins 4,6)

200 V maximum

120 mA maximum

RS-232 voltage input and output (J4-pins 1,3)

Mark: -5 to -15 VDC

Space: +5 to +15 VDC

Morse audio input (J7-pin 1): 10 V RMS maximum; 0.5 to 1.0 V P-P optimum.

Morse keying outputs (J8-pins 1,3): Transistor switches to ground, keying negative (grid-block) and positive (cathode) voltage circuits simultaneously. ± 150 VDC; 150 mA maximums.

KY lines (J5-pins 1-4) and KOS output (J4-pin 5): Transistor switches to ground, keying positive voltage circuits. +200 VDC; 100 mA maximums.

Retransmit data output (J5-pin 6): RS-232 compatable signal (± 12 V). Ten-unit ASCII code; 110-300 baud (rate adjustable).

Modem Connector: For use in connecting DS3100 ASR to RS-232 Modems. See Fig. 3.1 for pinout.

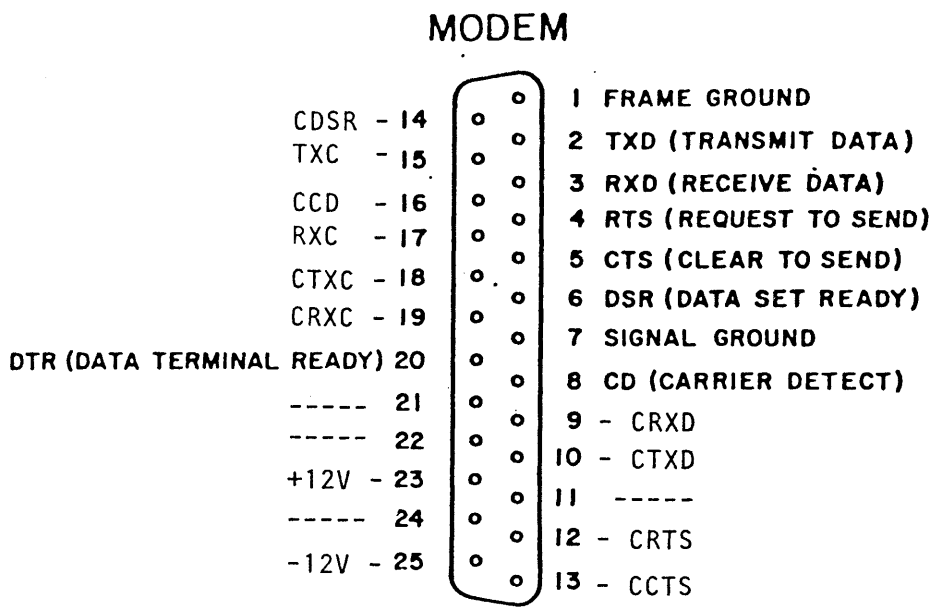
1. Frame ground - Safety ground connection to DS3100 chassis.

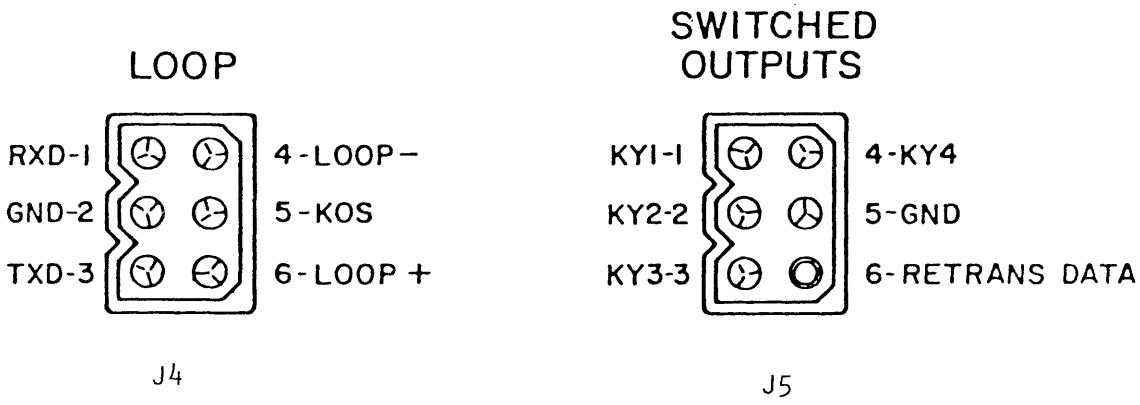
2. Transmit data - RS-232 compatible output from DS3100.

3. Receive data - RS-232 compatible input to DS3100.

4. Request to send - same as KOS-on and XMIT ACTIVE conditions.

5. Clear to send - internally set on when modem not connected; but over-ridden by modem when connected.





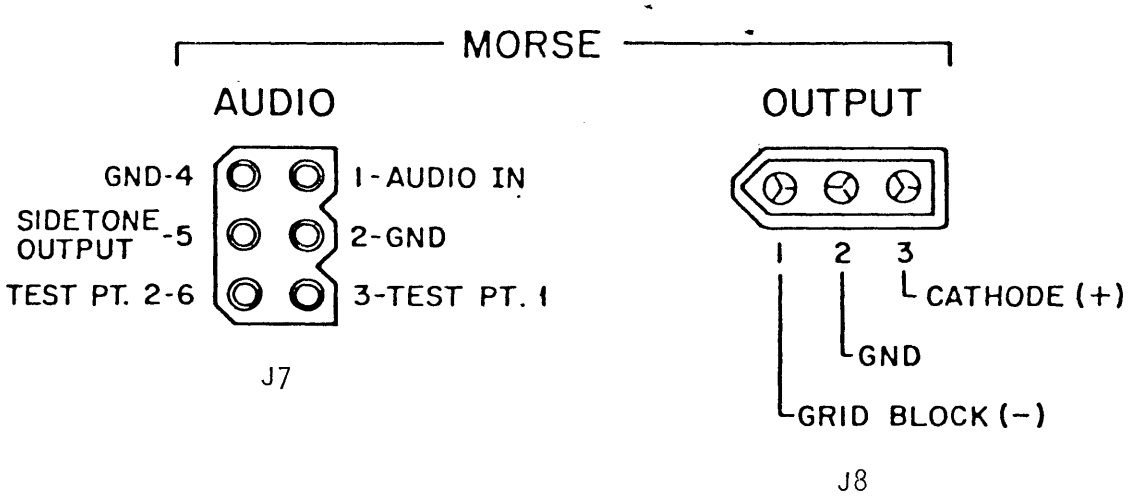


FIGURE 3.1 ASR I/O CONNECTIONS ON REAR PANEL

6. Data set ready - not required for DS3100 operation.

7. Signal ground - Ground return for all data and control signal circuits.

8. Carrier detect - Not required for DS3100 operation.

9 through 19 - Internal signals, not to be connected externally.

20. Data terminal ready - Always set on by DS3100 (high output).

21 and 22 - Internal signals.

23. +12 volt line - For reference use only: not to be connected externally except for measurement.

24. Internal signal.

25. -12 volt line - For reference use only: not be to connected externally except for measurement.

Always check wiring of modem connectors before connecting to the ASR modem jack (J2), as improper connections can cause damage to internal components.

4. TROUBLESHOOTING PROCEDURES FOR THE DS3100 ASR

As explained in the introduction to this manual, it is important for the operator to rule out "cockpit error" as a possible problem before trying to troubleshoot the ASR. In the event that your DS3100 ASR develops a malfunction, the first step to take toward getting the unit repaired is to carefully note all of the symptoms of the problem. This suggests that a logic-based flow chart should be used to determine as closely as possible what portions of the circuitry are working, and at what point there seems to be a "breakdown" in system operation. This section contains sufficient information to allow the technician to verify proper operation of portions of the ASR, and through simple circuit tracing and the process of elimination narrow down the anomaly to one section of the ASR circuitry.

4.1 Initial Connector Check

```
**************************
*      IMPORTANT!        *
*                        *
* ALWAYS UNPLUG EQUIPMENT *
* BEFORE OPENING CABINET. *
*                        *
**************************
```

The first thing that you should do if a problem occurs is open the ASR cabinet (see section 2) and check to see that all connectors are in place. This includes both ends of each of the ribbon cables, the Berg connector on the I/O board, and the power supply molex connectors. Also, verify that the CPU and VDB cards are firmly seated in the card-cage edge connectors by pulling them partially out and then pushing each one firmly back into place. Inspect the ASR interior visually for any loose hardware or dangling wires.

4.2 Returning Equipment

The following flow chart indicates specific subassemblies that should be returned to the factory when problems are encountered in ASR operation.[1] Always obtain prior authorization from the factory before sending any equipment (complete unit, or any subassemblies) back for repair. Refer to section 4 of the ASR Owner's Manual if any difficulties are experienced with the DS3100. Part 4.3 specifically covers repair and return procedures. IMPORTANT: Any ASR problem that is suspected to be the result of lightning damage may involve a large number of components on more than one subassembly. The entire DS3100 ASR -- both keyboard section and monitor -- should be returned to the factory for servicing if lightning damage is suspected.

4.3 Using The Flow Chart

The chart in Fig. 4.1 generally flows from left to right and top to bottom. A key provides identification of symbols and abbreviations used

[1] For units purchased from a HAL distributor, all references to "the factory", when used in context with returning equipment or getting technical assistance or replacement parts, should be interpreted as "the distributor where purchased."

in the chart. In most cases this diagram should narrow down ASR problems to a specific subassembly, eleiminating the necessity of returning the entire unit. However, some malfunctions cannot be isolated in this fashion. In these cases, where pc-board circuit tracing or other specialized troubleshooting techniques are required to affect repairs, the customer should NOT attempt to repair the ASR, or do troubleshooting beyond the scope of that indicated in the flow chart. Any damage that is determined by the factory to be the result of unauthorized troubleshooting will not be repaired under warranty, and may void the warranty.

4.4 Troubleshooting Guide

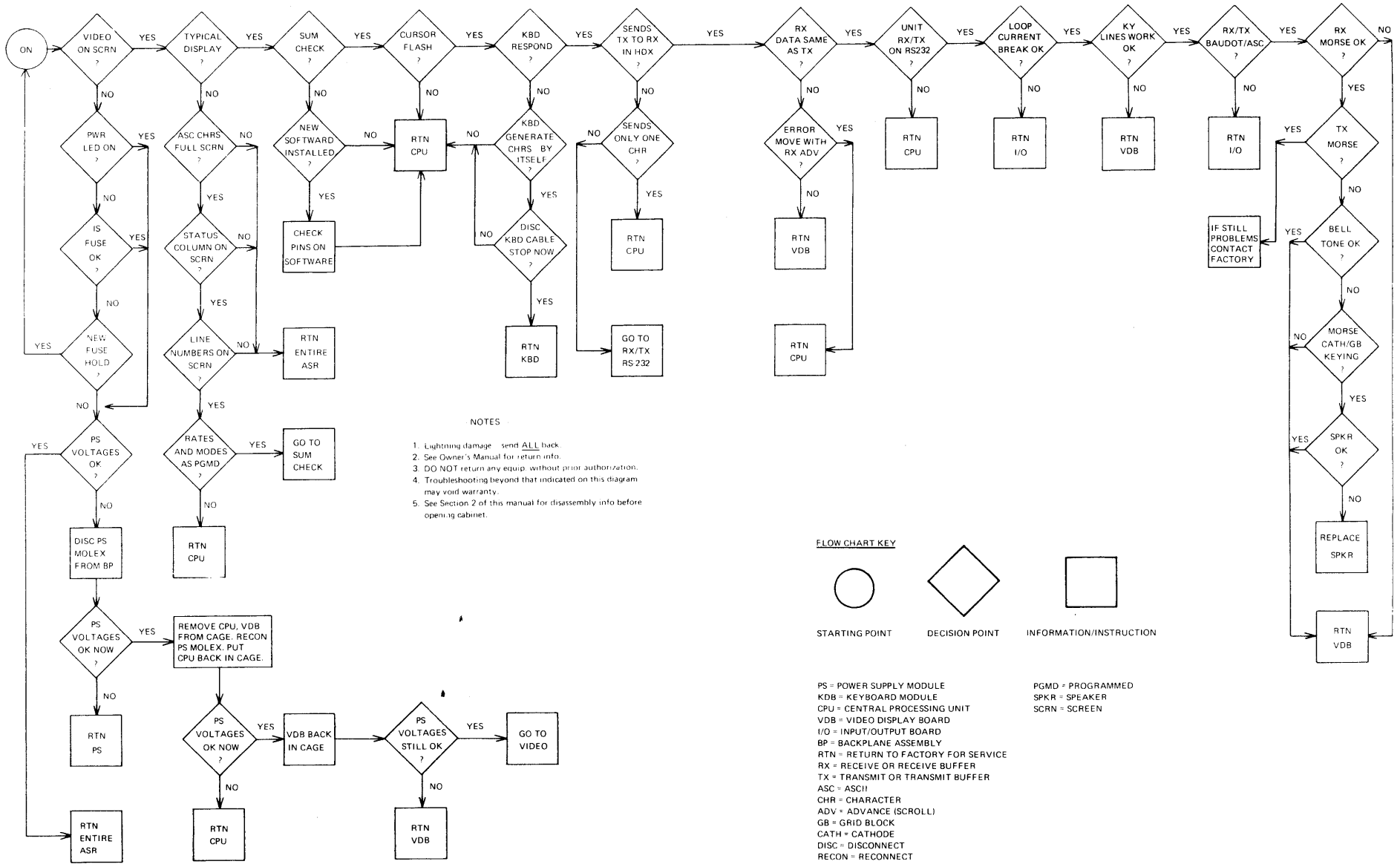
The following text is provided to supplement the information contained in the flow chart. Each vertical flow section -- where a problem is indicated, causing a branch-off from the main flow -- is explained in sequence. Until you become familiar with Fig. 4.1, use this text in conjunction with the flow chart when doing troubleshooting.

1. Video On Screen?

If no video appears on the DV3000 screen, there are several obvious causes that should be checked out before starting down this branch. Is the power cord plugged into the ASR? Is the DV3000 power cord (from ASR) plugged into the monitor? Is the contrast control on the rear panel of the DV3000 set at the proper level? After these things have been checked, continue with the decisions on this branch of the flow chart. If a bad fuse is replaced and continues to blow, DO NOT keep replacing. Especially, do not replace with a fuse that has a higher rating than stated in the Owner's Manual. Power supply voltages should be checked next.

```
**********************************
*                                *
*          CAUTION!              *
*                                *
*  LETHAL VOLTAGES ARE EXPOSED   *
*  IN REAR SECTION OF ASR NEAR   *
*  POWER TRANSFORMER AND FUSE.   *
*                                *
**********************************
```

The plus and minus 12-volt supplies can be tested on modem-connector pins 23 and 25 respectively without removing the bottom cover. The +5V supply should be tested at pin 3 on the molex connector going to the backplane assembly (red wire). Refer to section 2 (assembly/ disassembly) before attempting any troubleshooting INSIDE the ASR cabinet. The regulator circuits in the ASR power supply are designed to "shut down" when excessive current is drawn. A short circuit or defective component on one of the circuit boards could cause this to happen. Verify proper power supply operation by disconnecting the power supply molex connector and testing the power supply outputs with no load attached. By the process of elimination, the power-hungry area can be isolated. This is done by testing voltages with individual boards connected.



NOTES

1. Lightning damage - send ALL back.
2. See Owner's Manual for return info.
3. DO NOT return any equip. without prior authorization.
4. Troubleshooting beyond that indicated on this diagram may void warranty.
5. See Section 2 of this manual for disassembly info before opening cabinet.

FLOW CHART KEY

STARTING POINT — DECISION POINT — INFORMATION/INSTRUCTION

PS = POWER SUPPLY MODULE
KDB = KEYBOARD MODULE
CPU = CENTRAL PROCESSING UNIT
VDB = VIDEO DISPLAY BOARD
I/O = INPUT/OUTPUT BOARD
BP = BACKPLANE ASSEMBLY
RTN = RETURN TO FACTORY FOR SERVICE
RX = RECEIVE OR RECEIVE BUFFER
TX = TRANSMIT OR TRANSMIT BUFFER
ASC = ASCII
CHR = CHARACTER
ADV = ADVANCE (SCROLL)
GB = GRID BLOCK
CATH = CATHODE
DISC = DISCONNECT
RECON = RECONNECT
PGMD = PROGRAMMED
SPKR = SPEAKER
SCRN = SCREEN

FIGURE 4.1 TROUBLESHOOTING FLOW CHART FOR DS3100 ASR

2. Typical Display?

The ASR video screen should display the video in a certain order when power is first applied to the keyboard section. Initially the entire screen is filled with random ASCII characters (garbage) and then quickly cleared from top to bottom. The status column is then displayed, followed by the line numbers, in quick succession. If any of these things doesn't happen, the entire ASR base section should be returned. The video monitor (DV3000) is probably okay if the raster is visible on the screen when the contrast control is advanced. EAROM operation can be checked by verifying that all operating modes and rates, non-volatile here-is messages, WRU message, and special option character are all as they were programmed. Consult the Owner's Manual for information on any of these features if you are not familiar with them.

3. Sum Check?

The CPU does a sum check and generates a decimal point on the video display between the two numerals in the version number if the check verifies that the software is good. Any other character may be displayed instead of the decimal point if the software sum check fails. If a new version of software has been installed, you should check to see that all of the IC pins are in the socket holes and not bent underneath the IC. If all pins appear to be making good contact with socket pins, and the sum check still fails, return the CPU board to the factory for service.

4. Cursor Flash?

The flashing cursors on the ASR video screen are a continuing indication that the program is running properly. The cursor is flashed in response to processor interrupts generated by the programmable interval timer. Thus, the flashing cursor verifies proper execution of the program interrupt service routine. No cursor flash would indicate a problem on the CPU board, which should be returned for service.

5. Keyboard Respond?

The keyboard should respond to key presses, with the typed information being displayed in the transmit buffer regardless of the operating mode or code being used as long as the split-screen display mode is selected. If the keyboard doesn't respond to key presses, but instead generates characters by itself, check to see if this stops when the keyboard cable is disconnected from the CPU. The outcome will determine the faulty subassembly.

6. Sends TX to RX in HDX?

This decision point determines whether the ASR operates properly when text is typed into the transmit buffer and sent. The keyboard echo feature that functions when the terminal is in half-duplex mode duplicates all transmit text into the receive buffer so that the operator can review past transmissions. (Note that the split-screen display mode must be selected for both TX and RX text to be visible simultaneously.) Failure of the keyboard echo, where only one character is echoed, indicates a problem on the CPU, which should be returned for service. Complete

keyboard echo failure (no characters echoed) does not, by itself, indicate any specific subassembly as the problem area. Thus, the trouble-shooting jumps to the RX/TX RS-232 decision point.

7. RX Data Same As TX?

An error in dynamic- or static-RAM memory can cause a faulty character to be displayed at one or more video locations on the screen. If an error occurs, this branch of the chart determines which memory area is at fault. If the error (improper character) moves up and down as the receive text is scrolled by using the RX-advance feature (FN-ADV-R or SHIFT-FN-ADV-R) then CPU dynamic RAM is most likely the culprit. An error that stays at the same video location when RX text is scrolled up and down would indicate a problem in static RAM on the VDB. In either case, the indicated subassembly should be returned to the factory for service.

8. Unit RX/TX on RS-232?

This decision point provides a "closed-circuit" test of the system, independent of the loop keying interface. Connect the EIA output to the EIA input by jumpering modem-connector pin 2 to pin 3 and pin 4 to pin 5. With the ASR in full-duplex mode, compose a message in the transmit buffer and send it (FN XMIT). The message should go out one character at a time and be received by the ASR through the jumper between RS-232-OUT and RS-232-IN. Each received letter should appear as "bright" video, just as if received from another station. Failure of this test indicates a bad CPU.

9. Loop Current Break?

If the ASR passes the previous test (RS-232 RX/TX) but will not key the current loop, and/or will not receive via the loop, the problem is most likely on the I/O board.

10. KY Lines Work OK?

If the KY lines don't operate (transistor doesn't switch to ground) when activated using the FN-KY# sequence the VDB board is most likely the problem area.

11. RX/TX Baudot/ASCII?

If the ASR could not be tested for RX/TX on RS-232, or if a loop test is preferred, connect the ASR to a suitable demodulator/tone keyer (ST6000) and connect the tone keyer audio output to the demodulator input. With the ASR in full-duplex mode, transmit a message from the transmit buffer. The text should be received, and displayed as "bright" text in the receive buffer. Alternatively, the ASR can be connected to any transmitting and receiving equipment that it is to be used with and tested through "on-the-air" transmission and reception (using separate TX and RX).

12. RX Morse OK?

The next decision point verifies reception and display of incoming Morse. Be sure that the signal is properly tuned, and that the CW-Detect LED flashes in unison with the received code elements (dots and dashes). When the "threshold" control on the front panel of the ASR is

set to approximately the center of its range, an incoming Morse signal of about 800 Hz should cause the detect LED to flash if the input signal is of sufficient strength. If the CW-Detect LED does not flash but copy is achieved on the video screen, then the CW-Detect LED is probably defective. If the incoming Morse text is not displayed on the screen even though the CW-Detect LED flashes, then the receive program should be reset by the FN-CLR sequence (see Owner's Manual). If a reset does not cause display of the Morse text, then the VDB is probably at fault and should be returned for service.

13. TX Morse?

During CW transmissions, the ASR generates a sidetone through the BELL-ON signal on the VDB. This signal controls an audio oscillator connected to the speaker. If no sidetone is present during attempted Morse transmissions, check to see that the volume control (on rear panel of ASR) is turned up. If no sidetone is present and the CW keying outputs (cathode and grid-block) do not function (check with ohmmeter at jack on rear panel) then the VDB is the likely problem area. An absence of sidetone accompanied by good CW-keying outputs points to a defective speaker.

4.4 Difficulties

If you complete the flow chart tests and still can't determine which specific subassembly you should return for servicing, contact the factory for technical assistance. In most cases, if the difficulty cannot be determined through the use of Fig. 4.1 and the troubleshooting text you will need to return the entire ASR to the factory for service. In any case, be sure that you obtain proper return authorization from the factory before sending anything back for service.

5. ADJUSTMENTS AND OPTIONS

The following are adjustments that can be made and options that can be selected or implemented by the DS3100 ASR operator. Read all of this information carefully before attempting to make an adjustment or select an option on the ASR, as physical damage or improper ASR operation may result from changing the wrong jumper or turning the wrong potentiometer.

```
*****************************
*        CAUTION!           *
*                           *
* DISCONNECT AND TURN OFF   *
* POWER BEFORE OPENING ASR. *
*                           *
*****************************
```

5.1 Sidetone Adjustments *

Sidetone volume can be adjusted by turning the potentiometer provided on the rear panel. A small-bladed standard screwdriver should be used to make this adjustment.

Sidetone frequency is also adjustable, although not externally. If the frequency of the sidetone must be changed, open the ASR base section as described in section 2 of this manual. The sidetone-frequency potentiometer is located on the VDB, at the back edge of the board as shown in Fig. 5.1. Turning the frequency potentiometer (pot "T" on Fig. 5.2) clockwise will increase the sidetone frequency, while counterclockwise rotation will decrease sidetone frequency. If a specific frequency is required, attach a frequency counter to the sidetone output (pin 5 on J7 -- see Fig. 3.1) and monitor during adjustments. Hold down the FN-Break keys to generate a continuous sidetone output.

5.2 Retransmit Data Rate Adjustment *

The rate of serial output from the retransmit-data port on the ASR is adjustable from approximately 110 Baud to 300 Baud, and is set at the frequency of the retrans-data clock. The adjustment potentiometer for the retrans-data clock is adjacent to the sidetone osc. adjustment pot described above (see Fig. 5.2, pot "R"). The retrans-data clock should be set so that the frequency is equal to the desired Baud rate. Attach a frequency counter probe to pin 2 of the 74LS165 (see Fig. 5.2) and measure the clock rate while adjusting pot "R". The retrans-clock is set at the factory for 300 Hz/300 Baud. CAUTION: BE SURE THAT THE COUNTER PROBE DOES NOT SLIP OFF OF THE TEST POINT, OR SHORT AGAINST OTHER PINS.

5.3 Microprocessor Clock Adjustment

A crystal-controlled oscillator provides the clock signal to the Z-80 microprocessor in the DS3100 ASR. This oscillator is quite stable and should not require adjustment. An adjustment procedure is included here in the event that the oscillator drifts off frequency, or the crystal

* With MSO option installed, these adjustments cannot be made until all boards are removed from card cage and placed in standard ASR configuration. To do this, turn off power, remove all three boards, and put VDB in top of card cage, as shown in Fig. 2.2. Then restore power and make adjustments. When finished, return boards to their original positions in card cage.

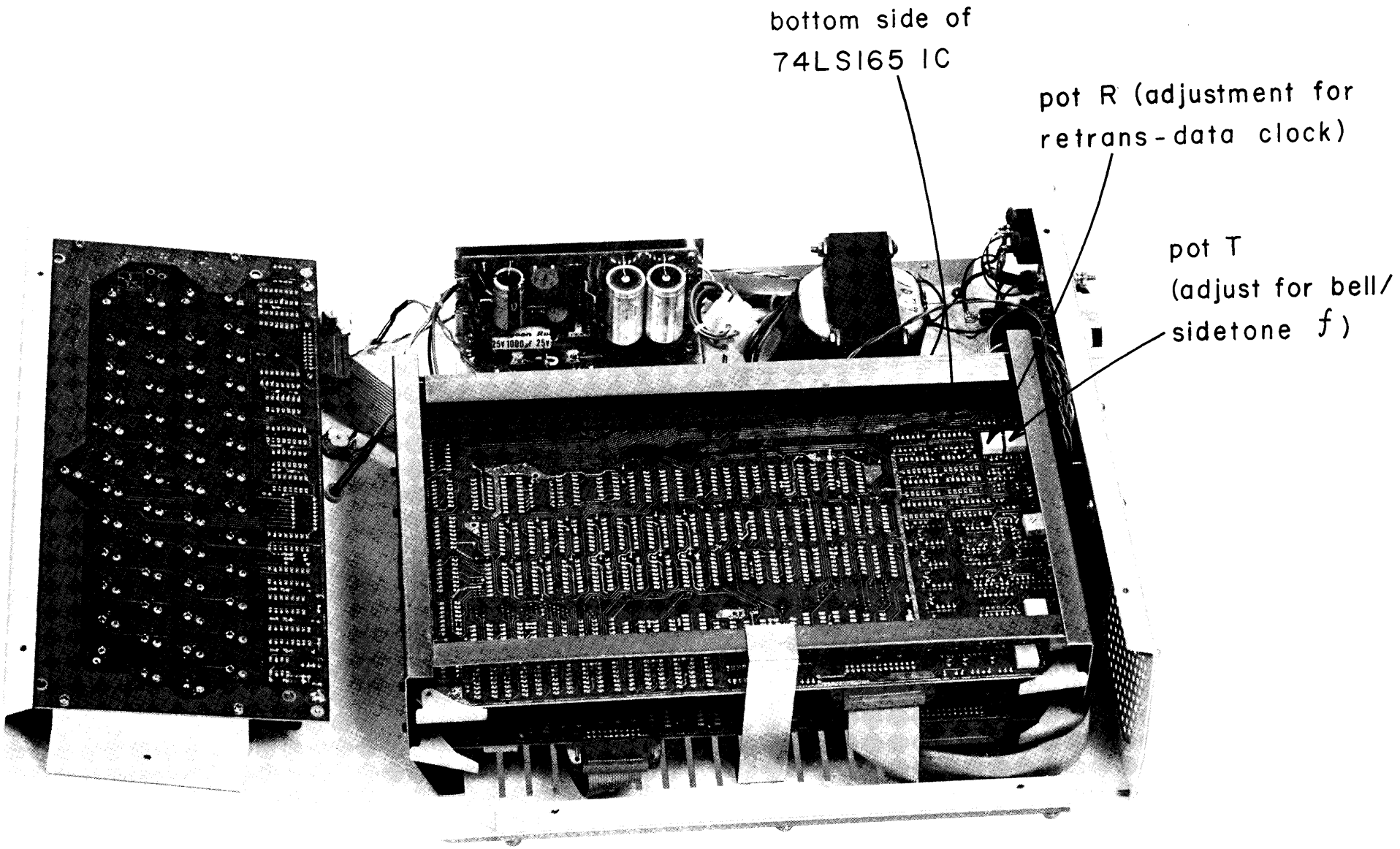


FIGURE 5.1 LOCATION OF ADJUSTMENTS ON VDB

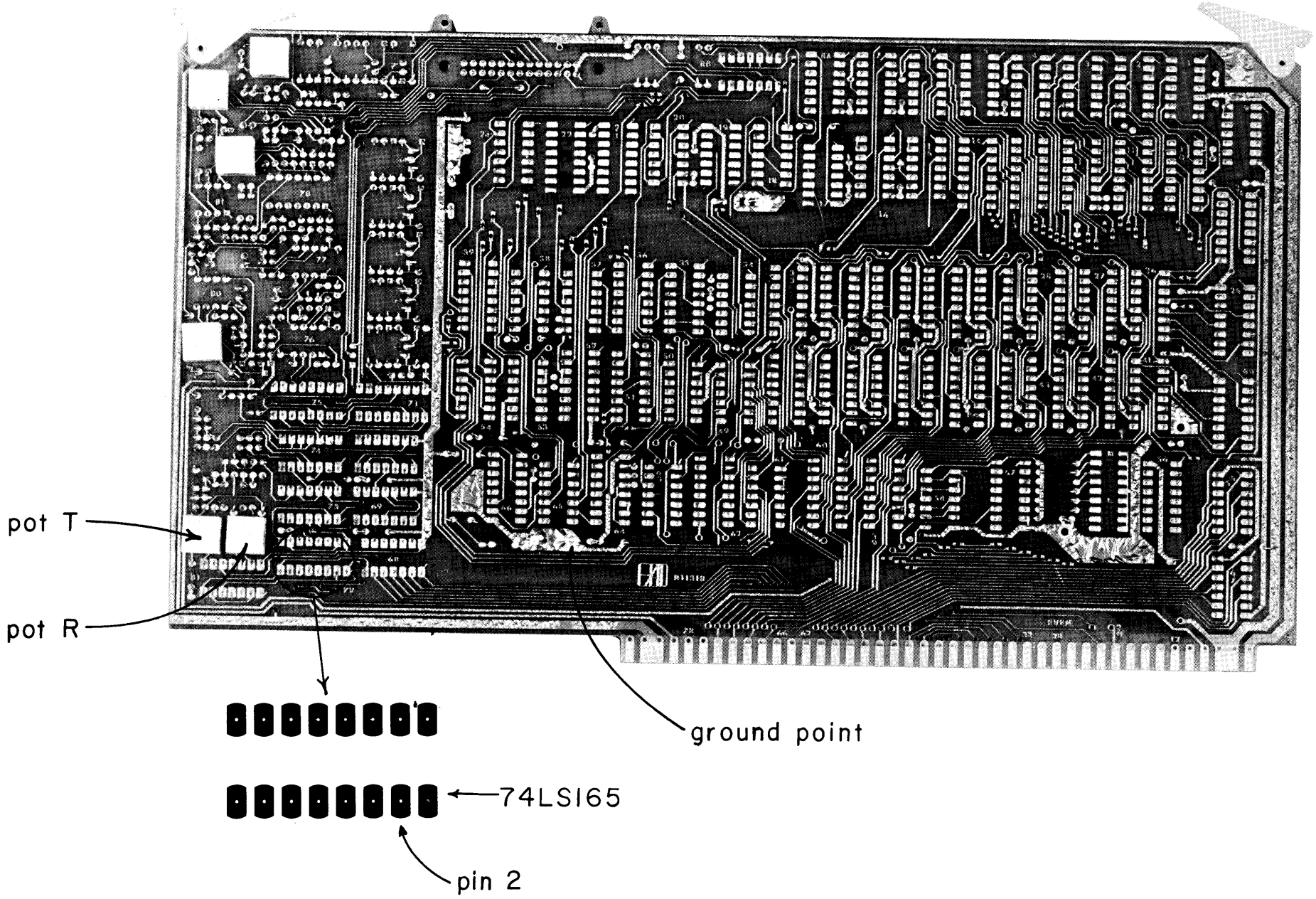


FIGURE 5.2 CLOSE-UP VIEW OF VDB ADJUSTMENTS/TEST POINTS

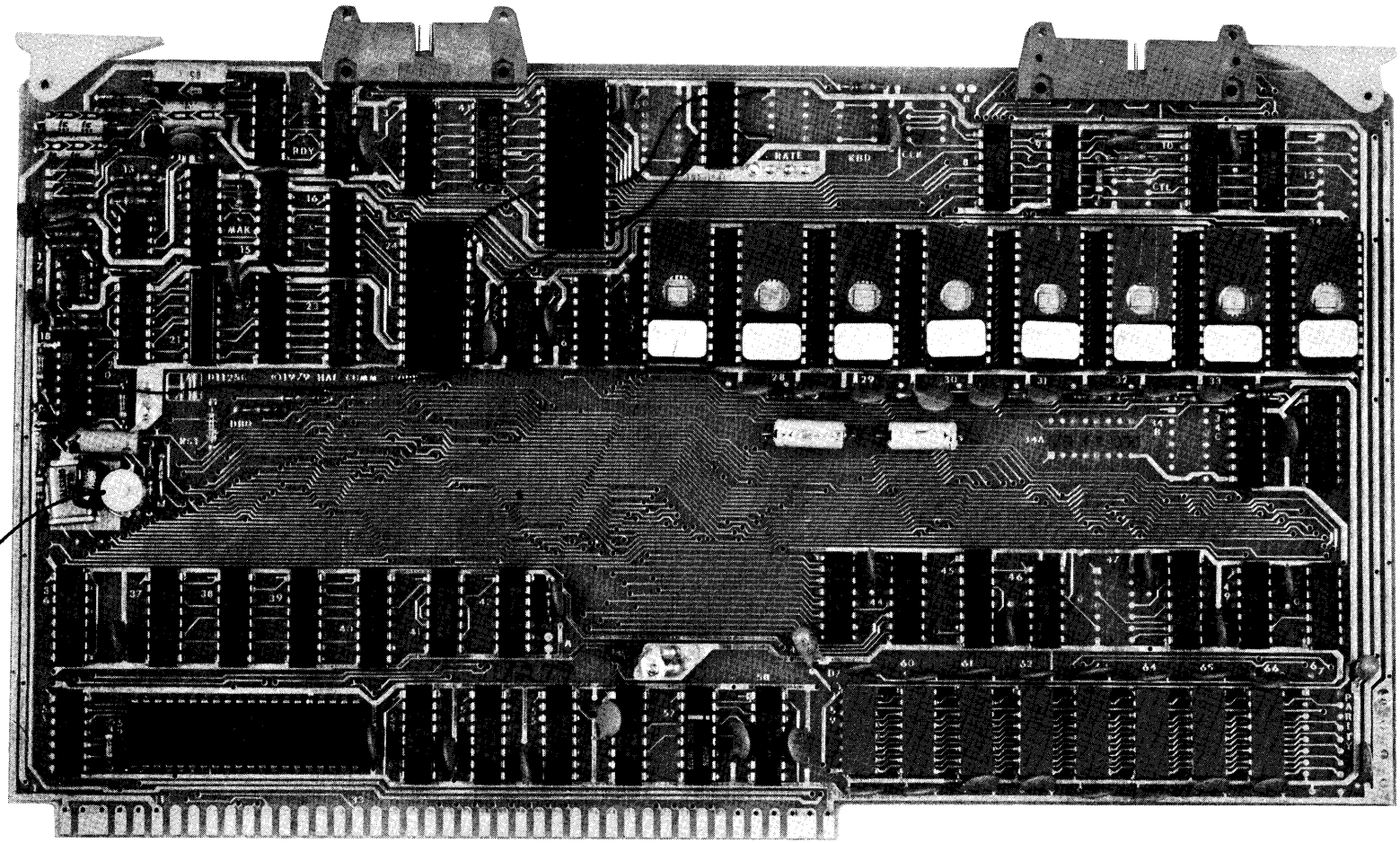


FIGURE 5.3 LOCATION OF CPU CLOCK ADJUSTMENT

is replaced. Fig. 5.3 shows the location of the crystal and trimmer capacitor on the component side of the CPU board. Use an extender board[1] to connect the CPU board to the backplane while out of the card cage. The keyboard and I/O cables won't reach with the CPU on the extender board; however, the CPU should still come up in the proper state when power is first applied. Connect a high-impedance counter probe to pin 6 of the 8224 IC located near the crystal. The frequency at this point should measure 2000 kHz when the unit is completely warmed up. If the frequency is set when the board is cold, it should be set for 2000.1 kHz (100 Hz high) to compensate for drift. IMPORTANT: BE CAREFUL NOT TO TOUCH ANY OTHER IC PINS WITH THE PROBE TIP WHEN PERFORMING THE ABOVE MEASUREMENT AND ADJUSTMENT.

5.4 Modification for Operation with 50-Hz Line Frequency

The DS3100 ASR can be operated at 110-V/220-V and 60-Hz/50-Hz. Operating voltages are selected by changing the transformer wiring, as described in the Owner's Manual, section 3.5 (pages 55-57). Operation on 50-Hz line frequency requires two changes on the VDB: a different crystal frequency, and a jumper change. Fig. 5.4 shows the location of the crystal and "A" jumper. Unsolder the crystal, pry it loose from the board and replace with new crystal obtained from HAL factory. (60-Hz crystal should be 14.1925 MHz; 50-Hz crystal should be 13.9776 MHz.) Jumper "A" should be connected between the upper two holes (closest to the letter A) for 60-Hz operation, and between the lower two holes for 50-Hz operation.

5.5 Software Option Selection

Section 2.6.6 of the Owner's Manual describes the selection of special options via the programming of the special-option character in the EAROM. The table in Fig. 5.5 provides a quick reference guide for selection of the proper special-option character for the desired combination of ASR options. See Table 4 on page 39 of the ASR Owner's Manual for a listing of the display symbols used for ASCII code.

[1]Extender boards for the DS3100 ASR are available from HAL,(part #915-3103) for $50.00 each.

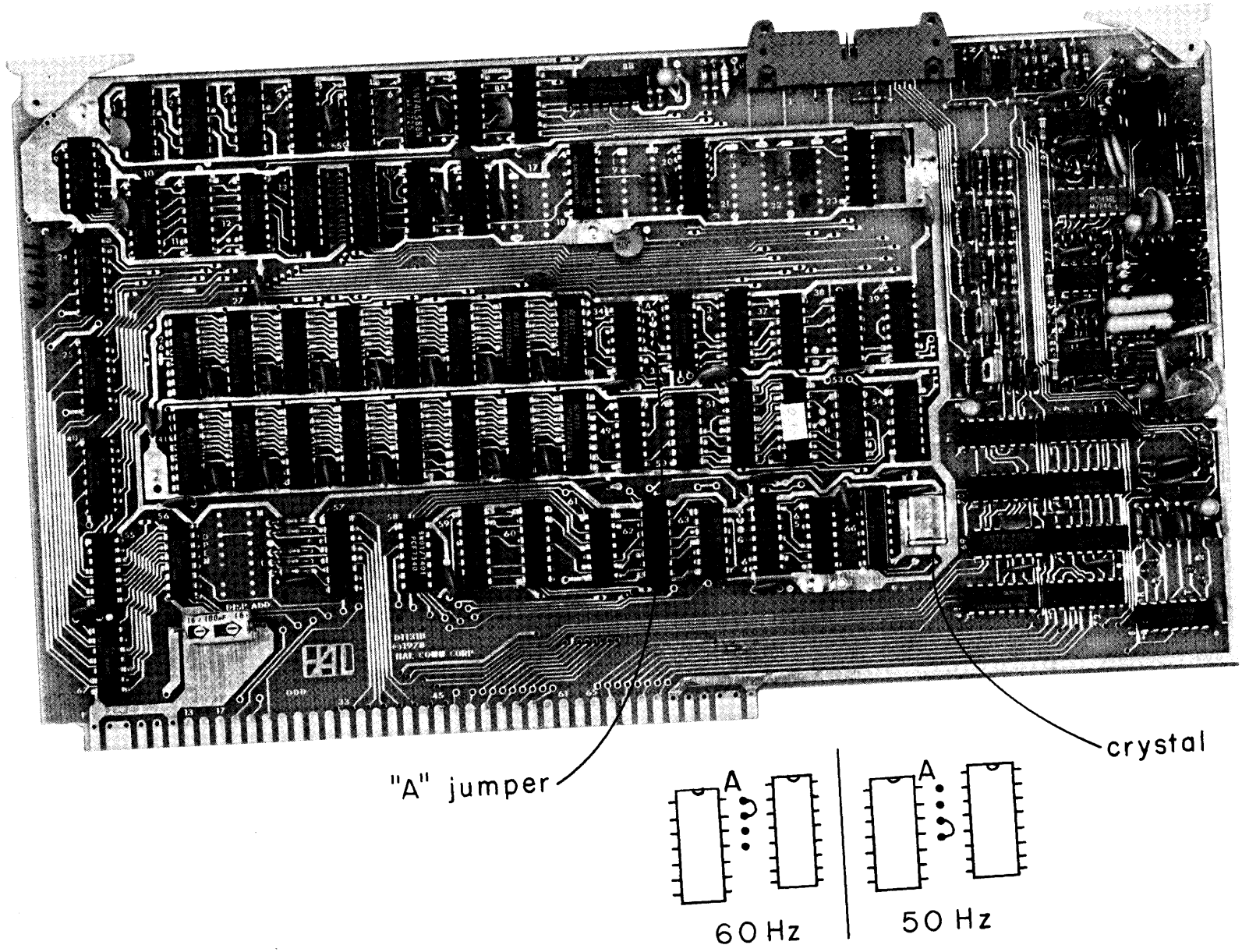


FIGURE 5.4 50-HZ/60-HZ MODIFICATION ON VDB

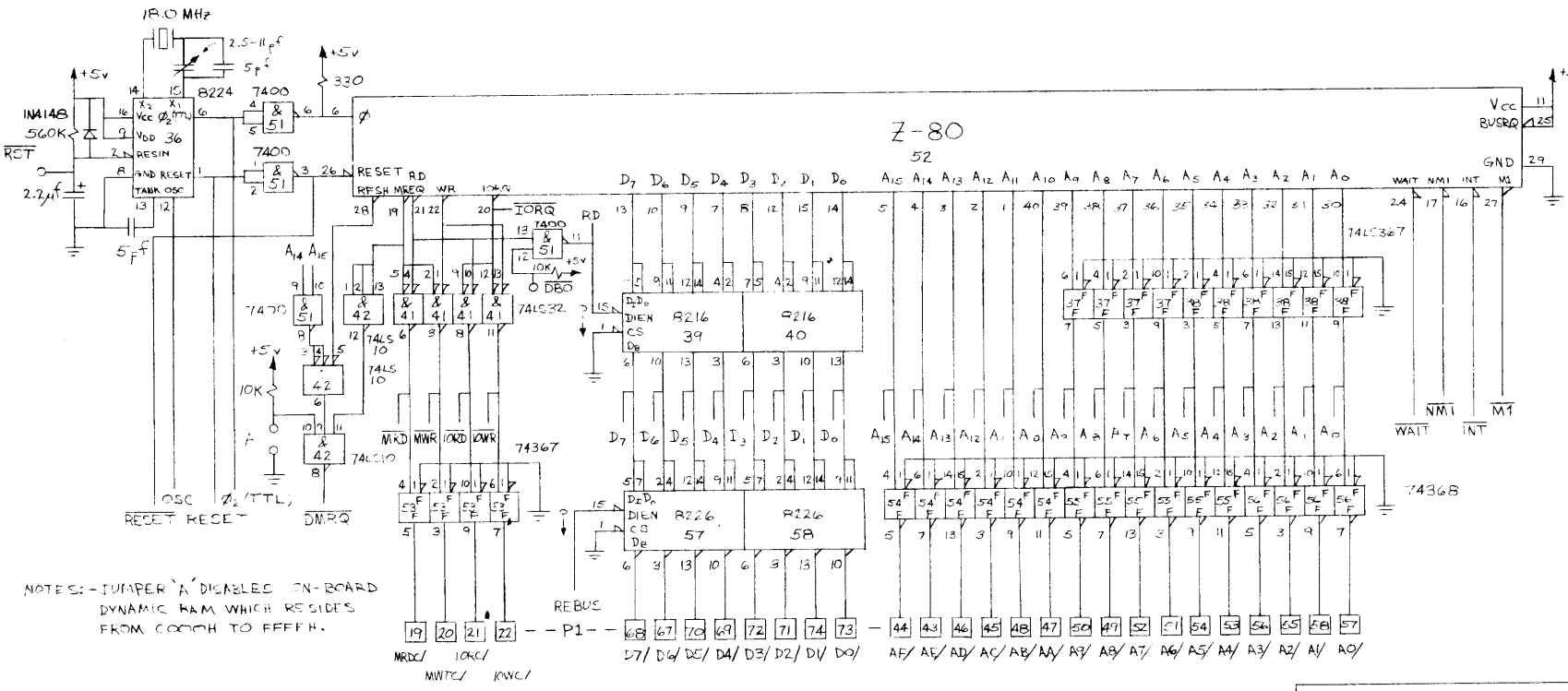
COMBINATION OF OPTIONS				PARITY DISABLED		PARITY ENABLED	
TX LINE	BAUDOT SET	ASC FDX NEW LINE	TX DELAY	BIT 8 = SPACE	BIT 8 = MARK	EVEN PARITY	ODD PARITY
72 CHR	USA BAUDOT	CR/LF	DEL ON	SHIFT-CTRL-P (NUL)	CTRL-A (SOH)	CTRL-B (STX)	CTRL-C (ETX)
69 CHR	USA BAUDOT	CR/LF	DEL ON	SPACE BAR (SPACE)	SHIFT-1 (!)	SHIFT-2 (")	SHIFT-3 (#)
72 CHR	CCITT #2	CR/LF	DEL ON	CTRL-P (DLE)	CTRL-Q (DC1)	CTRL-R (DC2)	CTRL-S (DC3)
69 CHR	CCITT #2	CR/LF	DEL ON	Ø (ZERO)	1 (ONE)	2 (TWO)	3 (THREE)
72 CHR	USA BAUDOT	CR/LF	DEL OFF	CTRL-D (EOT)	CTRL-E (WRU)	CTRL-F (ACK)	CTRL-G (BELL)
69 CHR	USA BAUDOT	CR/LF	DEL OFF	SHIFT-4 ($)	SHIFT-5 (%)	SHIFT-6 (&)	SHIFT-7 (')
72 CHR	CCITT #2	CR/LF	DEL OFF	CTRL-T (DC4)	CTRL-U (NAK)	CTRL-V (SYN)	CTRL-W (ETB)
69 CHR	CCITT #2	CR/LF	DEL OFF	4 (FOUR)	5 (FIVE)	6 (SIX)	7 (SEVEN)
72 CHR	USA BAUDOT	CR	DEL ON	CTRL-H (BS)	CTRL-I (HT)	CTRL-J (LF)	CTRL-K (VT)
69 CHR	USA BAUDOT	CR	DEL ON	SHIFT-8 (L. PAREN)	SHIFT-9 (R. PAREN)	SHIFT-: (*)	SHIFT-; (+)
72 CHR	CCITT #2	CR	DEL ON	CTRL-X (CAN)	CTRL-Y (EM)	CTRL-Z (SUB)	ESCAPE (ESC)
69 CHR	CCITT #2	CR	DEL ON	8 (EIGHT)	9 (NINE)	: (COLON)	; (SEMICOLON)
72 CHR	USA BAUDOT	CR	DEL OFF	CTRL-L (FF)	CTRL-M (RTN)	CTRL-N (SO)	CTRL-O (SI)
69 CHR	USA BAUDOT	CR	DEL OFF	, (COMMA)	- (HYPHEN)	. (PERIOD)	/ (SLASH)
72 CHR	CCITT #2	CR	DEL OFF	SHIFT-CTRL-L (FS)	SHIFT-CTRL-M (GS)	SHIFT-CTRL-N (RS)	SHIFT-CTRL-O (US)
69 CHR	CCITT #2	CR	DEL OFF	CTRL-, (L. CAROT)	SHIFT-HYPHEN (=)	CTRL-. (R. CAROT)	SHIFT-/ (?)

FIGURE 5.5 SPECIAL-OPTION CHARACTER SELECTION CHART

Note:

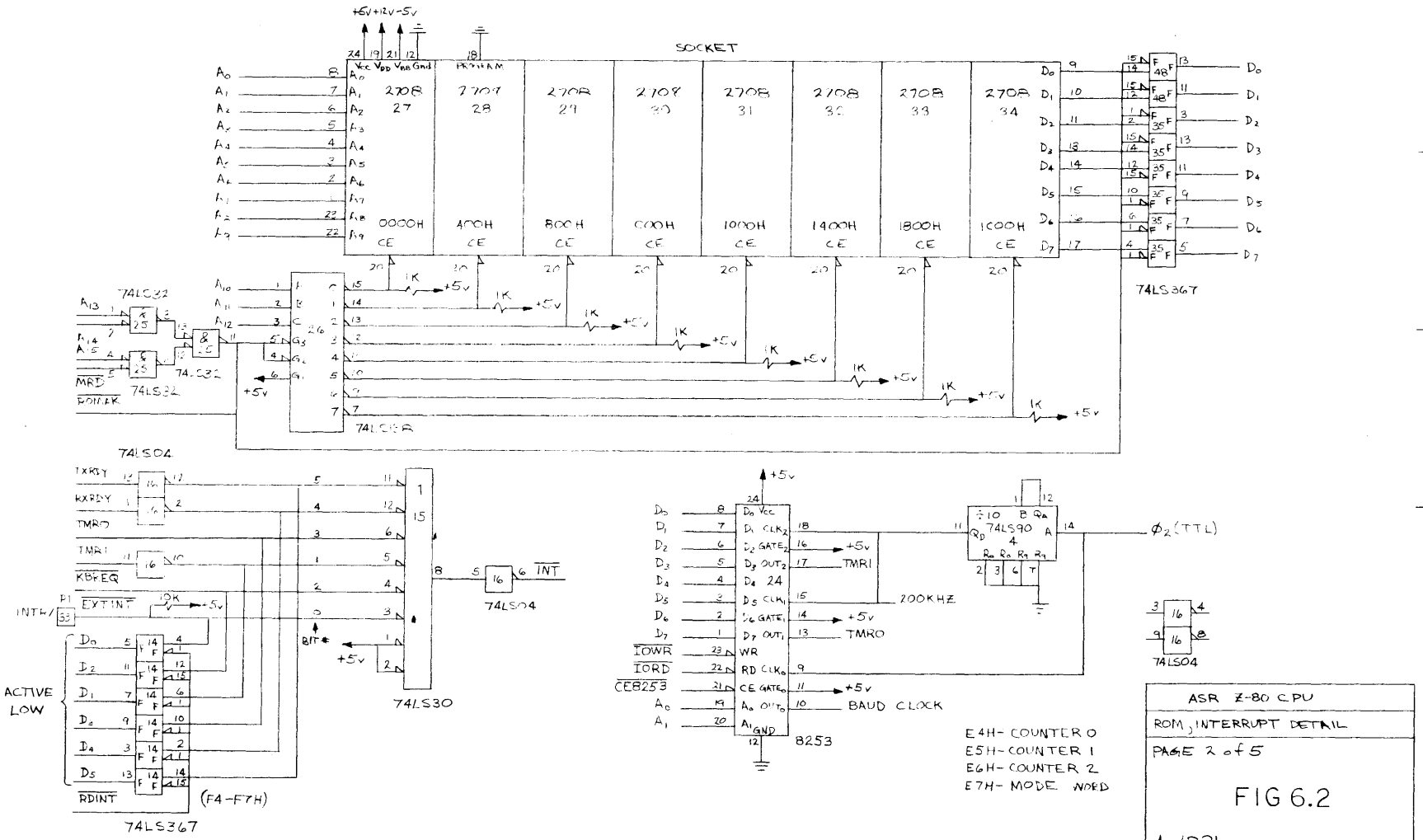
The special-option-character programming for DS3100 ASRs containing the MSO-3100 option is somewhat different. Check sections 3.3 and 4.4 in the MSO-3100 manual for information on the differences in SOC programming for DS3100s containing MSO-3100 Message Storage Option boards.

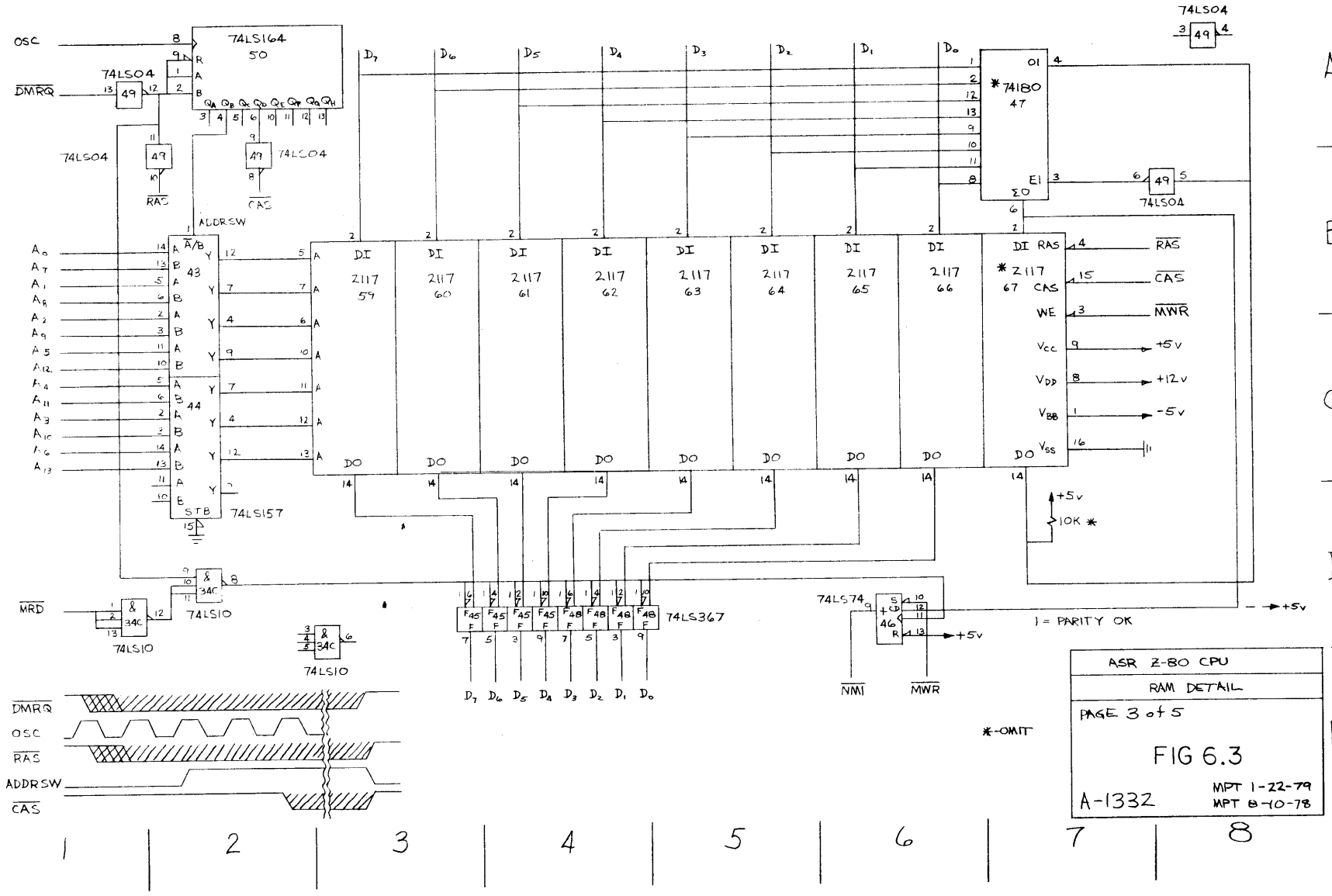
6. ILLUSTRATIONS - TABLE OF CONTENTS

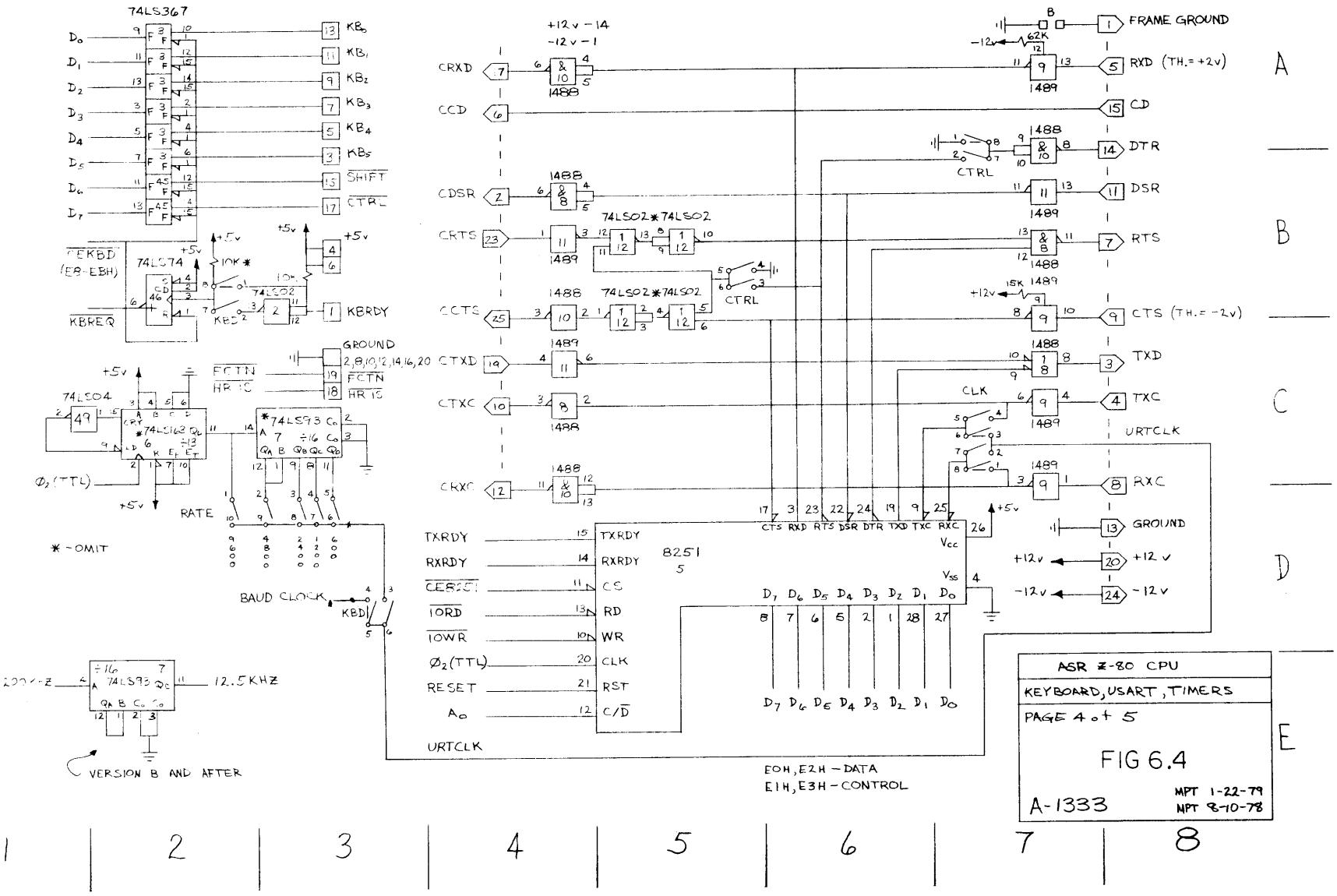


NOTES:- JUMPER 'A' DISABLES ON-BOARD DYNAMIC RAM WHICH RESIDES FROM C000H TO FFFFH.

ASR Z-80 CPU
CPU DETAIL
PAGE 1 of 5
FIG 6.1
A-1330 MPT 1-22-79 MPT 8-10-78


+5V +12V -5V
SOCKET
2708 27
2708 28
2708 29
2708 30
2708 31
2708 32
2708 33
2708 34
0000H CE
0400H CE
0800H CE
0C00H CE
1000H CE
1400H CE
1800H CE
1C00H CE
74LS32
74LS04
74LS367
74LS138
MRD
ROMAK
1K
+5V
TXRDY
RXRDY
TMRO
TMR1
KBREQ
INTR/
EXTINT
10K
RDINT
(F4-F7H)
ACTIVE LOW
74LS30
INT
74LS90
200KHZ
TMR1
TMRO
IOWR
IORD
CE8253
BAUD CLOCK
8253
E4H- COUNTER 0
E5H- COUNTER 1
E6H- COUNTER 2
E7H- MODE WORD
ASR Z-80 CPU
ROM, INTERRUPT DETAIL
PAGE 2 of 5
FIG 6.2
A-1331
MPT 8-10-78


OSC
DMRQ
74LS164
50
74LS04
RAS
CAS
ADDRSW
A/B
43
44
STB
74LS157
DI
2117
59
60
61
62
63
64
65
66
67
DO
74180
47
74LS04
RAS
CAS
MWR
WE
Vcc
VDD
VBB
VSS
+5v
+12v
-5v
10K *
MRD
74LS10
74LS367
74LS74
46
1 = PARITY OK
NMI
MWR
*-OMIT
ASR Z-80 CPU
RAM DETAIL
PAGE 3 of 5
FIG 6.3
A-1332
MPT 1-22-79
MPT 8-10-78



ASR Z-80 CPU

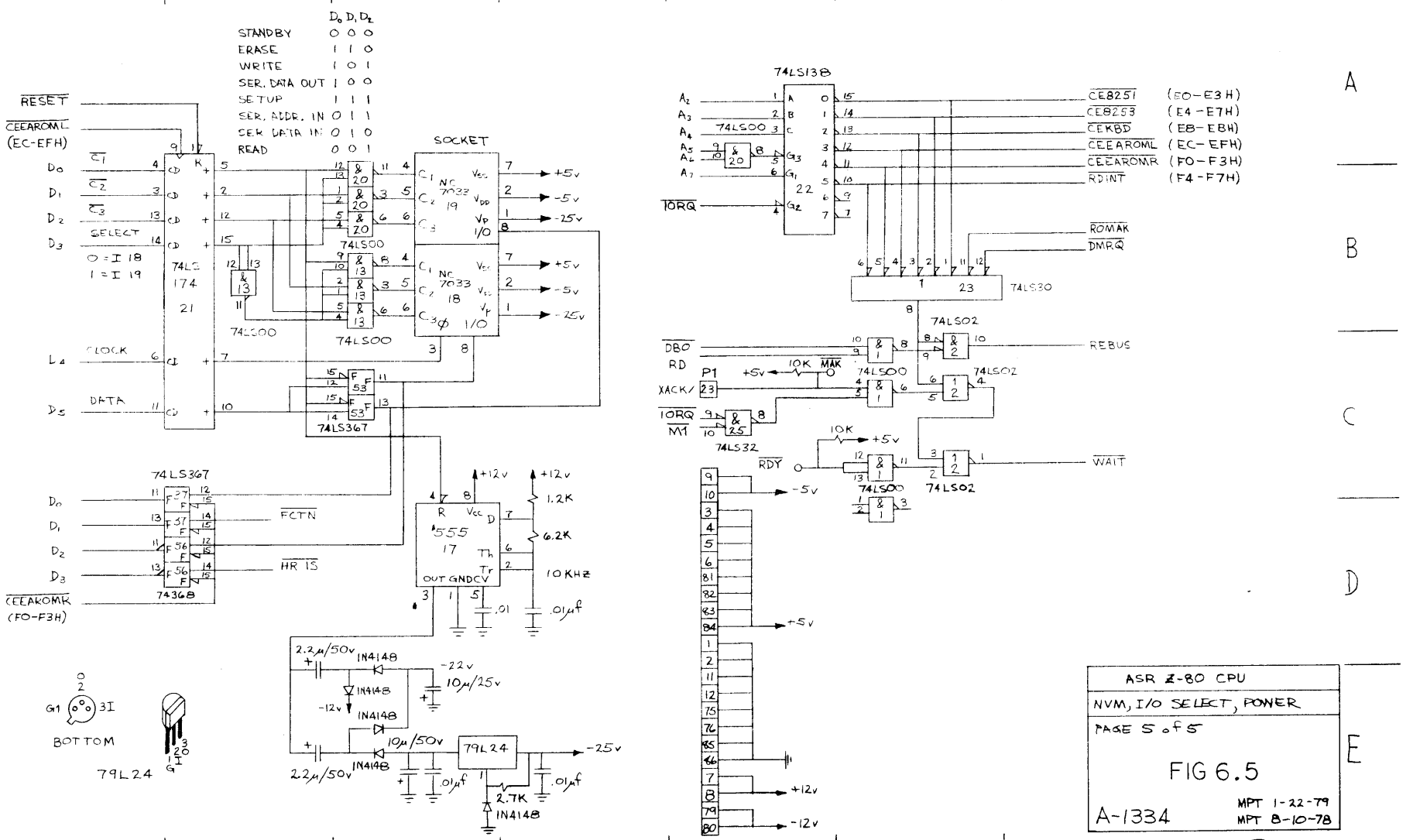
KEYBOARD, USART, TIMERS

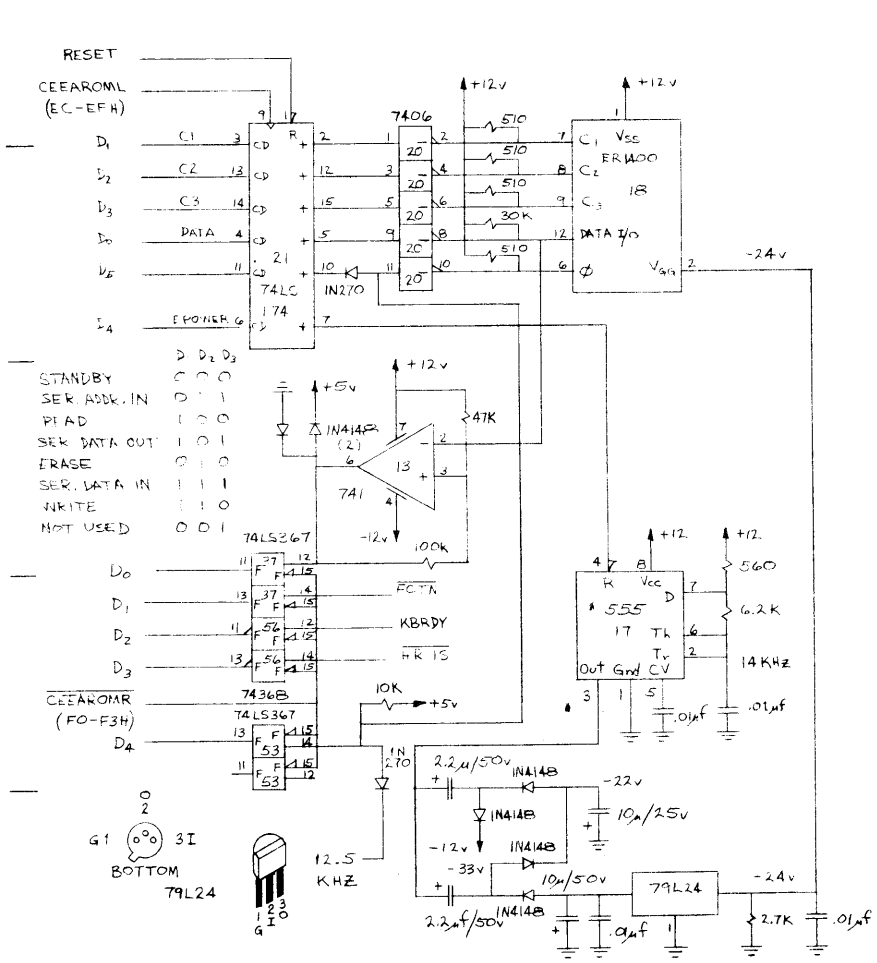
PAGE 4 of 5

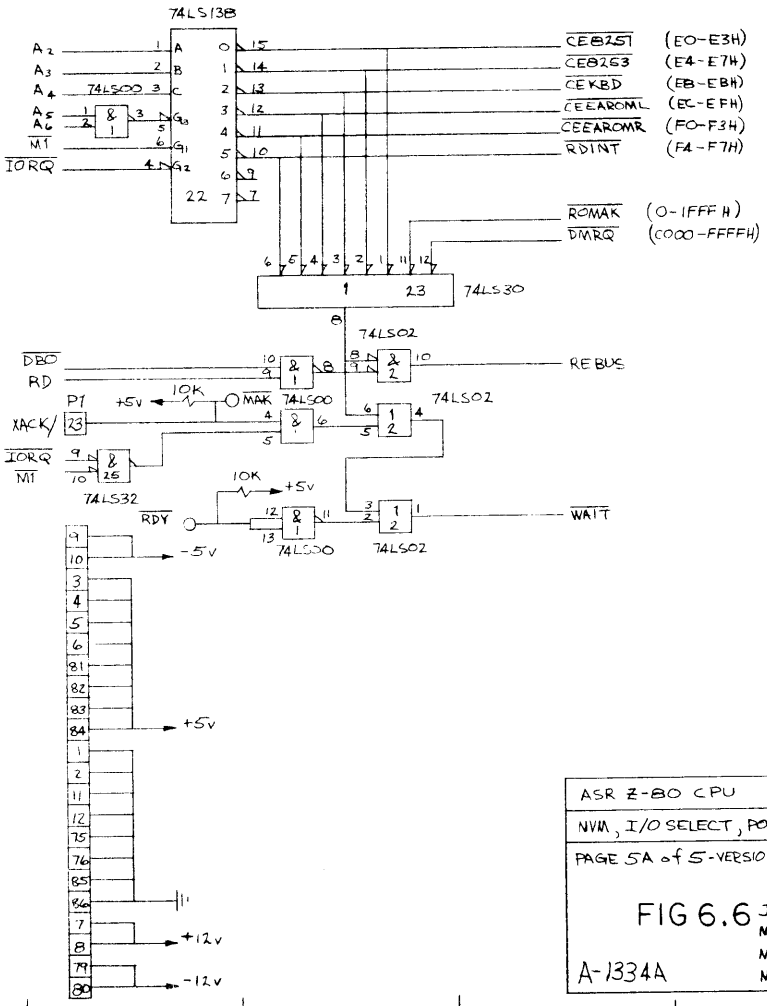
FIG 6.4

A-1333

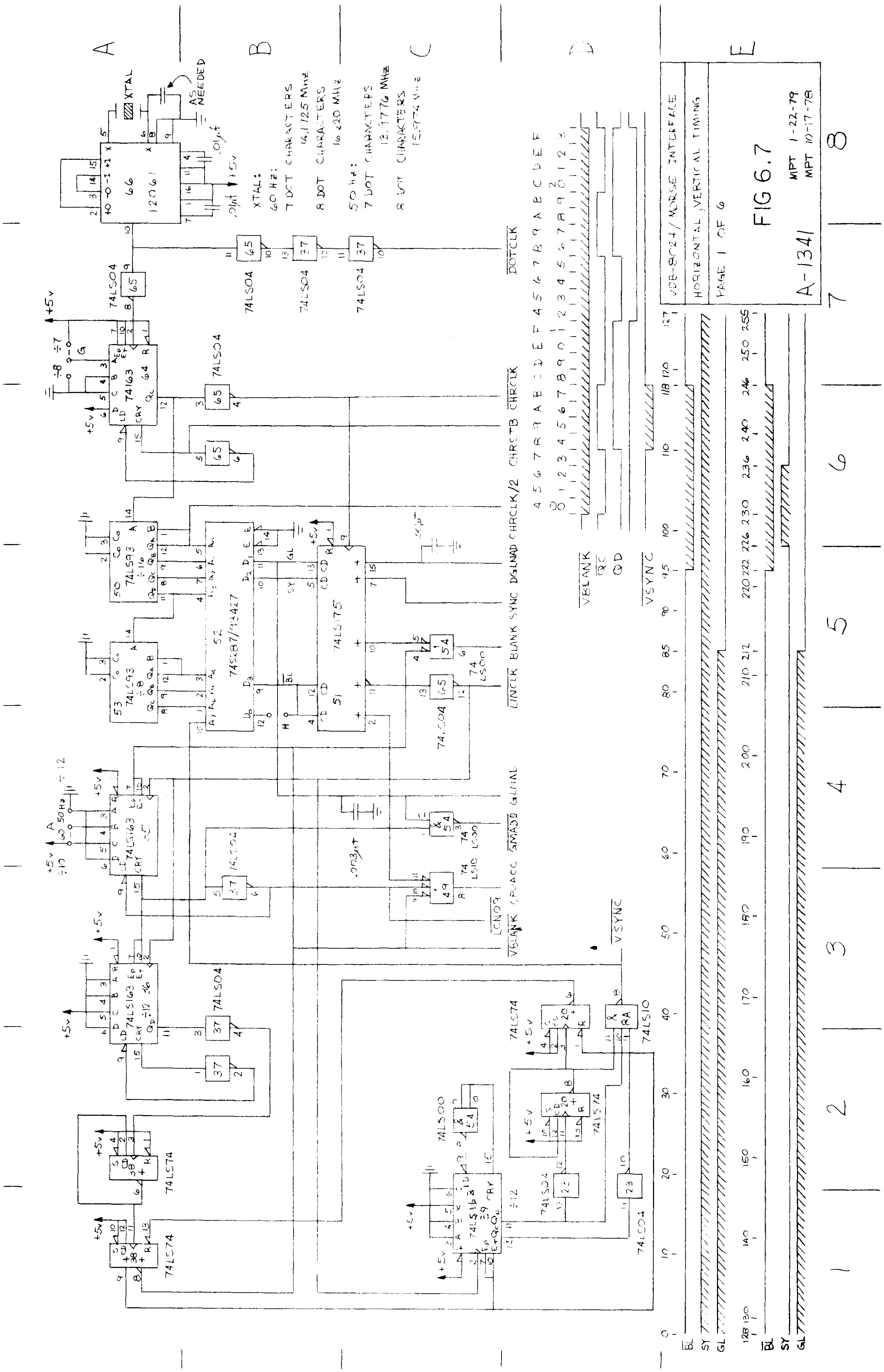
MPT 1-22-79
MPT 8-10-78

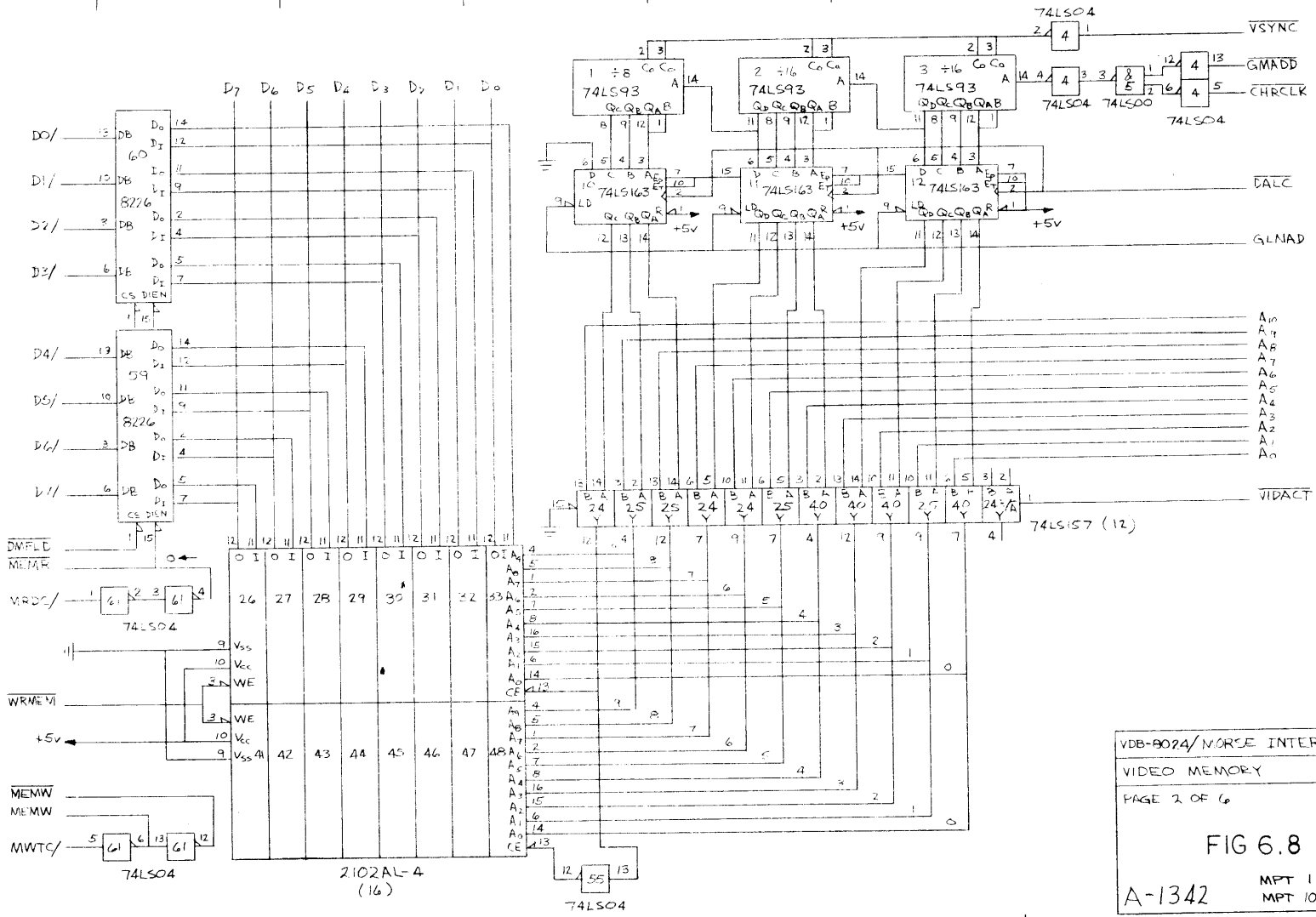

D0 D1 D2
STANDBY 0 0 0
ERASE 1 1 0
WRITE 1 0 1
SER. DATA OUT 1 0 0
SETUP 1 1 1
SER. ADDR. IN 0 1 1
SER DATA IN 0 1 0
READ 0 0 1
RESET
CEEAROML
(EC-EFH)
SELECT
O = I 18
I = I 19
74LS 174
CLOCK
DATA
SOCKET
74LS00
74LS367
74LS368
CEEAROMR
(F0-F3H)
FCTN
HR IS
555
10KHZ
.01µf
2.2µ/50v
IN4148
-22v
10µ/25v
-12v
79L24
2.7K
BOTTOM
74LS138
CE8251 (E0-E3H)
CE8253 (E4-E7H)
CEKBD (E8-EBH)
CEEAROML (EC-EFH)
CEEAROMR (F0-F3H)
RDINT (F4-F7H)
IORQ
ROMAK
DMRQ
74LS30
74LS02
DBO
RD
XACK
M1
P1
10K
MAK
REBUS
RDY
WAIT
ASR Z-80 CPU
NVM, I/O SELECT, POWER
PAGE 5 of 5
FIG 6.5
A-1334
MPT 1-22-79
MPT 8-10-78





ASR Z-80 CPU
NVM, I/O SELECT, POWER
PAGE 5A of 5 - VERSION B + AFTER
FIG 6.6 JB 12-18-79 MPT 3-19-79 MPT 1-22-79 MPT 8-10-78
A-1334A


VDB-8024/MORSE INTERFACE
HORIZONTAL VERTICAL TIMING
PAGE 1 OF 6
FIG 6.7
A-1341
XTAL:
60 Hz:
7 DOT CHARACTERS 14.1125 MHz
8 DOT CHARACTERS 16.020 MHz
50 Hz:
7 DOT CHARACTERS 13.3776 MHz
8 DOT CHARACTERS 15.974 MHz
AS NEEDED
DOTCLK
CHRCLK
CHRSTB
VBLANK
VSYNC
74LS04
74LS163
74LS74
74LS93
74LS175
74LS10
74LS00

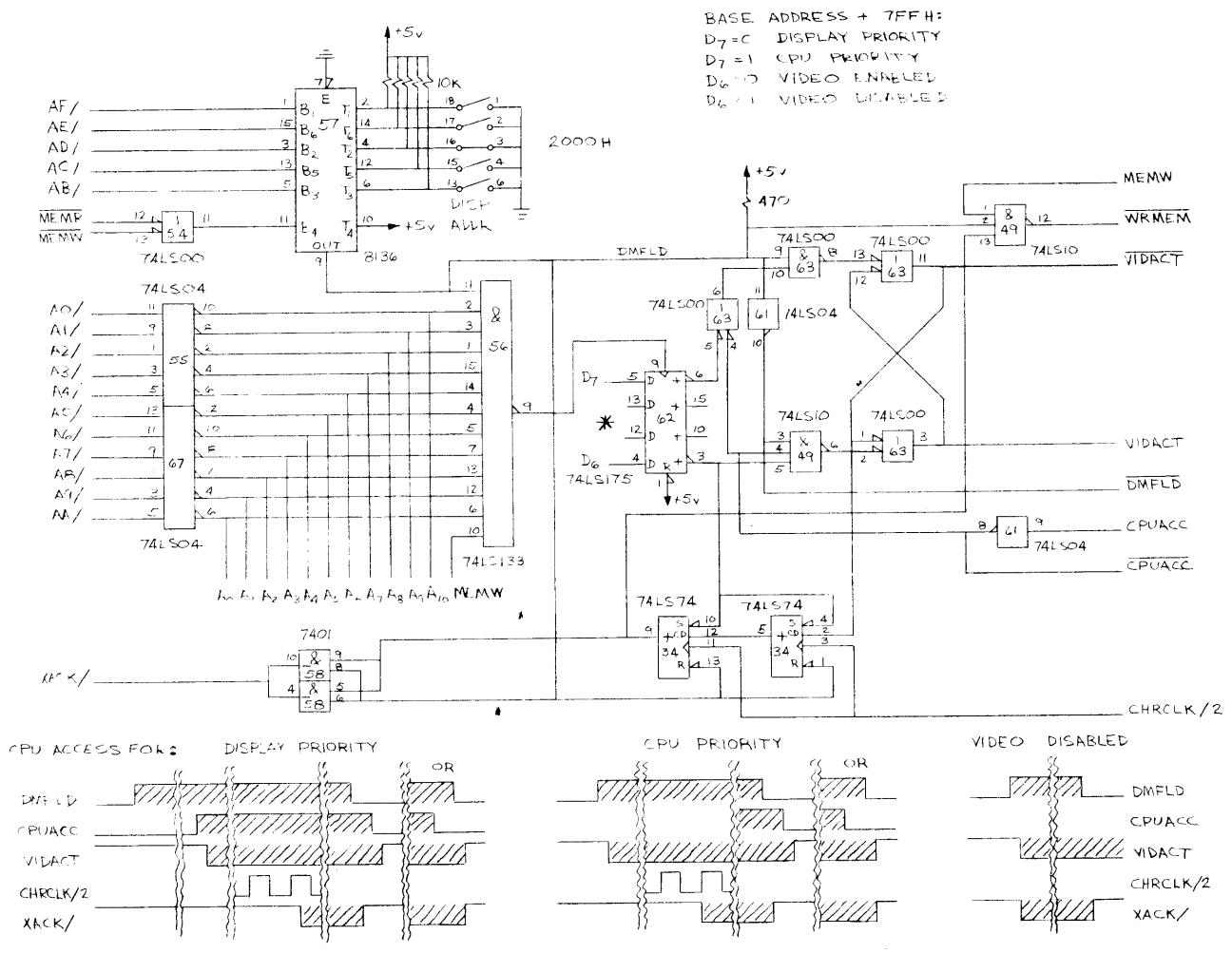


VDB-8024/MORSE INTERFACE
VIDEO MEMORY
PAGE 2 OF 6

FIG 6.8

A-1342

MPT 1-22-79
MPT 10-20-78



74LS04 74LS04 74LS86 74LS00 74LS74 74LS10

ADDITIONAL UNUSED ARRAYS ARE IN I24 + I62

* THIS PART DELETED ON LATER PRODUCTION MODELS. PIN 1 JUMPERED TO PIN 3; PIN 16 CONNECTED THROUGH 10kΩ TO PIN 6.

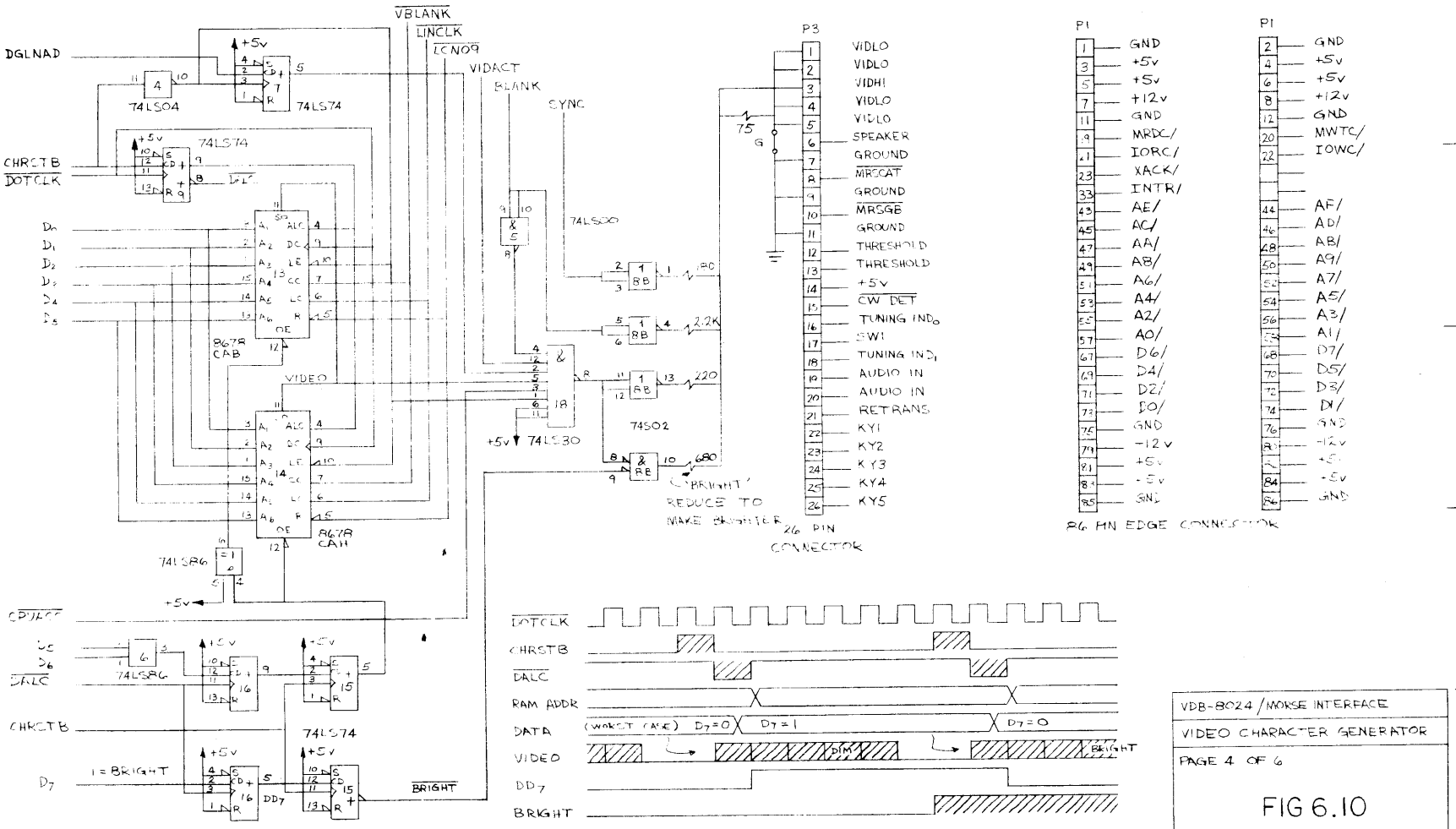
VDB-8024/MORSE INTERFACE
CPU ACCESS ARBITRATER
PAGE 3 OF 6

FIG 6.9

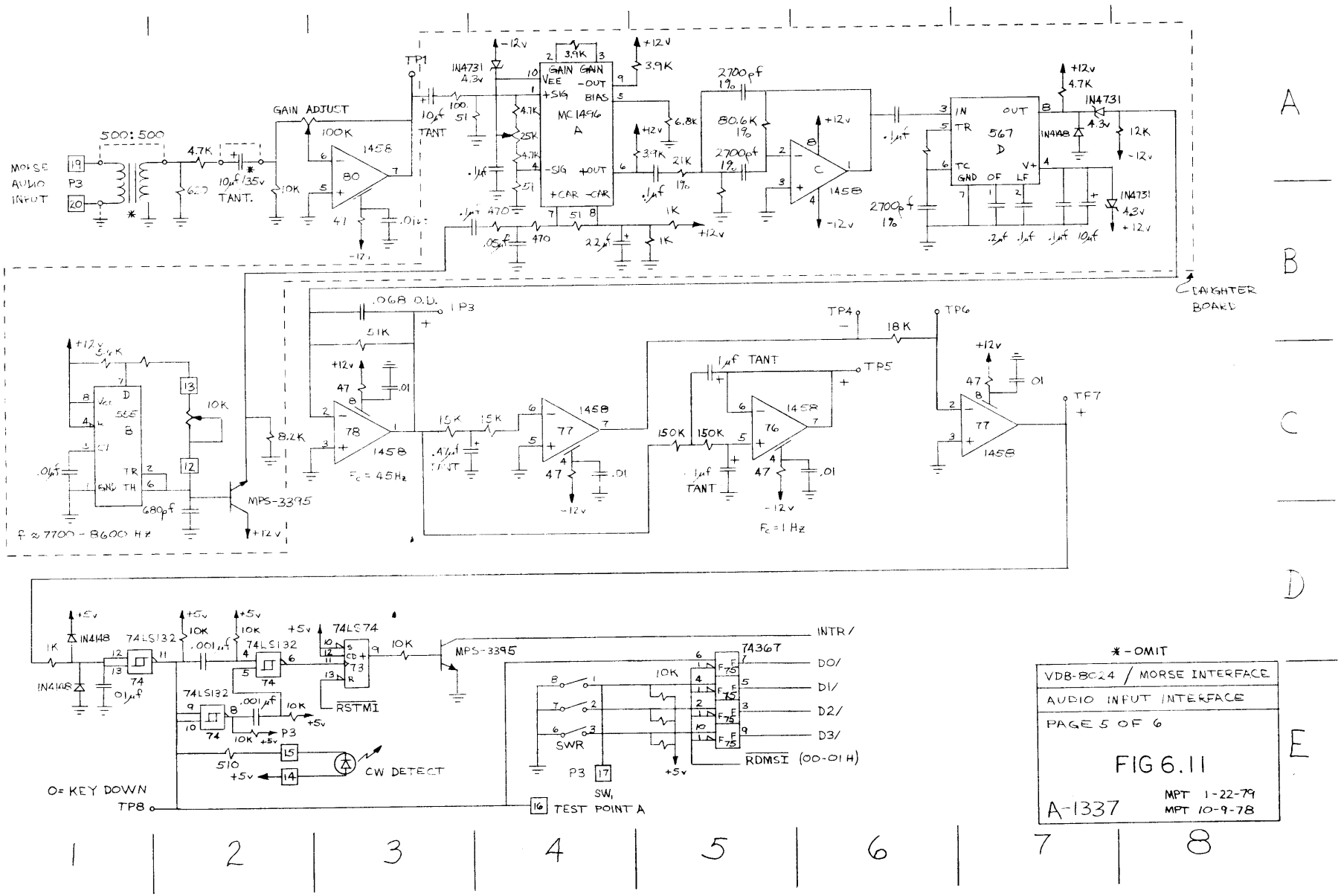
JB 12-18-79
MPT 1-22-79
MPT 10-16-78

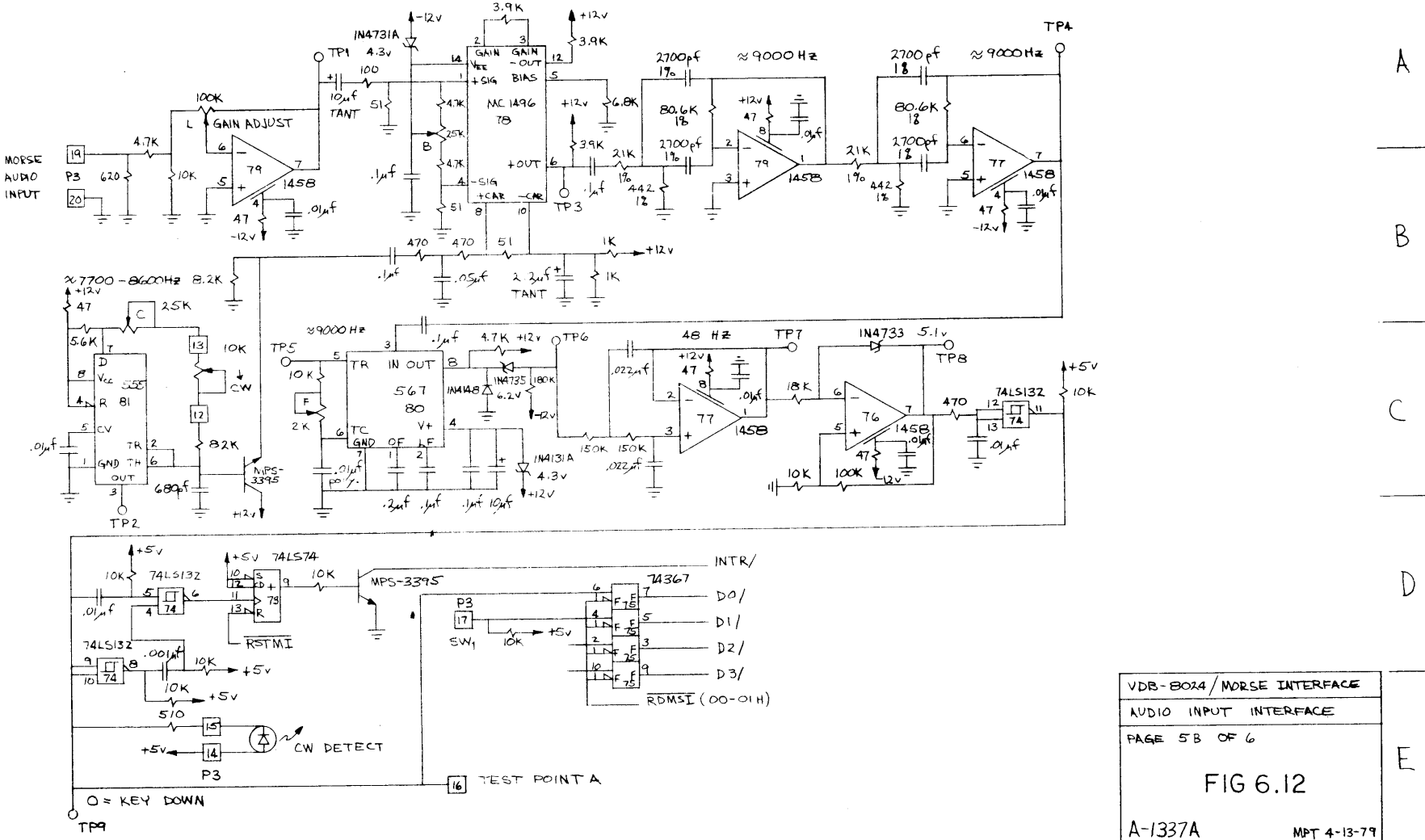
A-1343

48

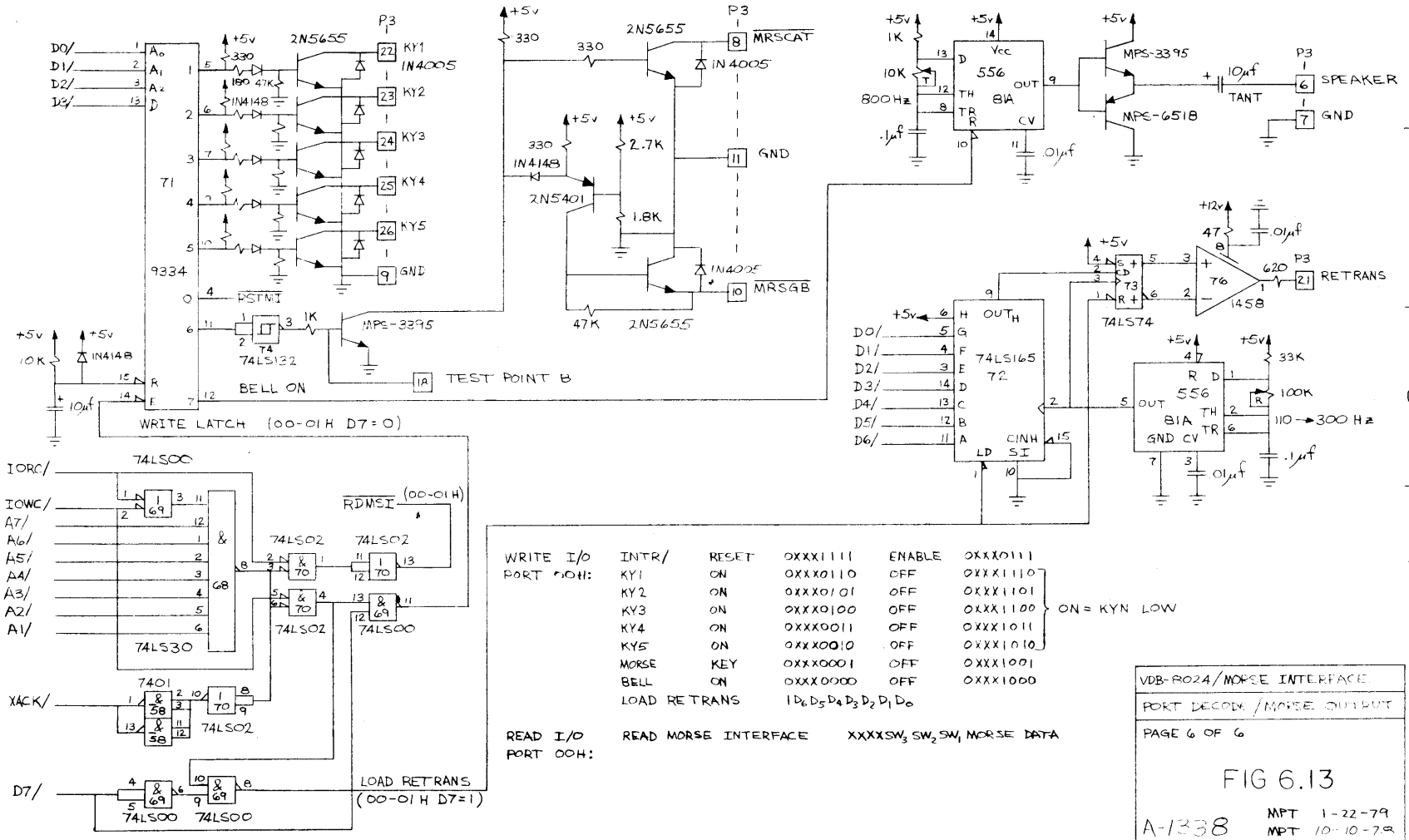


VDB-8024 / MORSE INTERFACE
VIDEO CHARACTER GENERATOR
PAGE 4 OF 6
FIG 6.10
A-1344 MPT 1-22-79 MPT 10-16-78


MORSE AUDIO INPUT
P3
19
20
500:500
4.7K
10μf/35v TANT.
GAIN ADJUST
100K
10K
1458
80
41
.01μf
TP1
10μf TANT
100.
51
IN4731 4.3v
MC1496 A
GAIN VEE +SIG -SIG +CAR -CAR GAIN -OUT BIAS +OUT -OUT
3.9K
25K
.1μf
470
.05μf
22μf
1K
6.8K
3.9K
2700pf 1%
80.6K 1%
1458 C
2700pf 1%
.1μf
567 D
IN GND TR TC OF LF OUT V+ LF
IN4148
12K
.2μf
10μf
DAUGHTER BOARD
.068 O.D.
TP3
51K
47
78
77
76
15K
.47μf TANT
150K
1μf TANT
18K
TP4
TP5
TP6
TP7
F_c = 45Hz
F_c = 1Hz
555 B
.01μf
680pf
MPS-3395
f ≈ 7700 - 8600 Hz
74LS132
74LS74
74
73
RSTMI
CW DETECT
510
O= KEY DOWN
TP8
74367
INTR/
DO/
D1/
D2/
D3/
RDMSI (00-01 H)
SWR
SW1
TEST POINT A
16
17
* - OMIT
VDB-8024 / MORSE INTERFACE
AUDIO INPUT INTERFACE
PAGE 5 OF 6
FIG 6.11
A-1337
MPT 1-22-79
MPT 10-9-78



VDB-8024 / MORSE INTERFACE
AUDIO INPUT INTERFACE
PAGE 5B OF 6
FIG 6.12
A-1337A MPT 4-13-79



WRITE I/O PORT 00H:	INTR/	RESET	0XXX1111	ENABLE	0XXX0111
	KY1	ON	0XXX0110	OFF	0XXX1110
	KY2	ON	0XXX0101	OFF	0XXX1101
	KY3	ON	0XXX0100	OFF	0XXX1100
	KY4	ON	0XXX0011	OFF	0XXX1011
	KY5	ON	0XXX0010	OFF	0XXX1010
	MORSE	KEY	0XXX0001	OFF	0XXX1001
	BELL	ON	0XXX0000	OFF	0XXX1000
	LOAD RETRANS		$1D_6D_5D_4D_3D_2D_1D_0$		

ON = KYN LOW

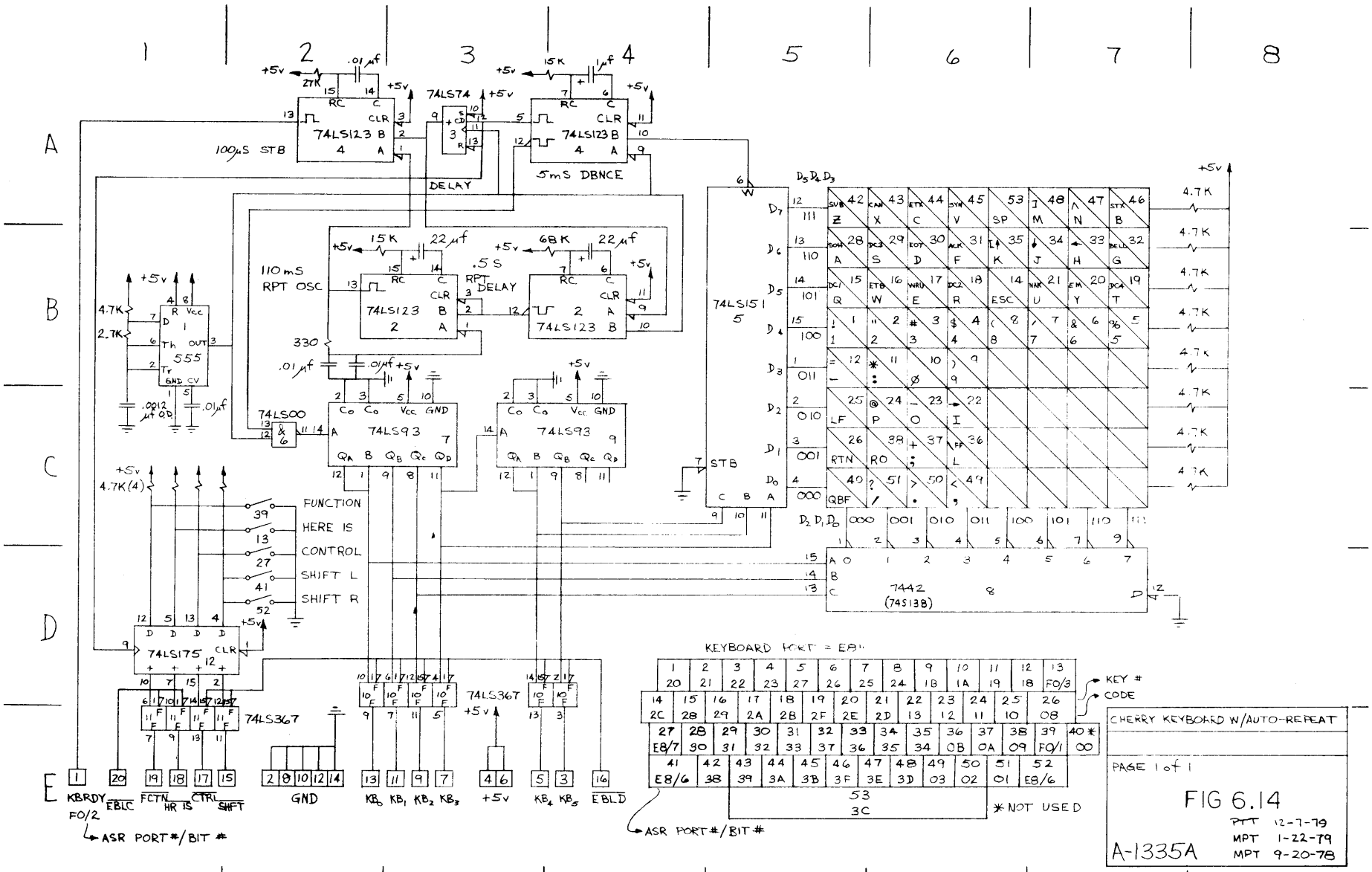
READ I/O PORT 00H: READ MORSE INTERFACE XXXXSW$_3$ SW$_2$ SW$_1$ MORSE DATA

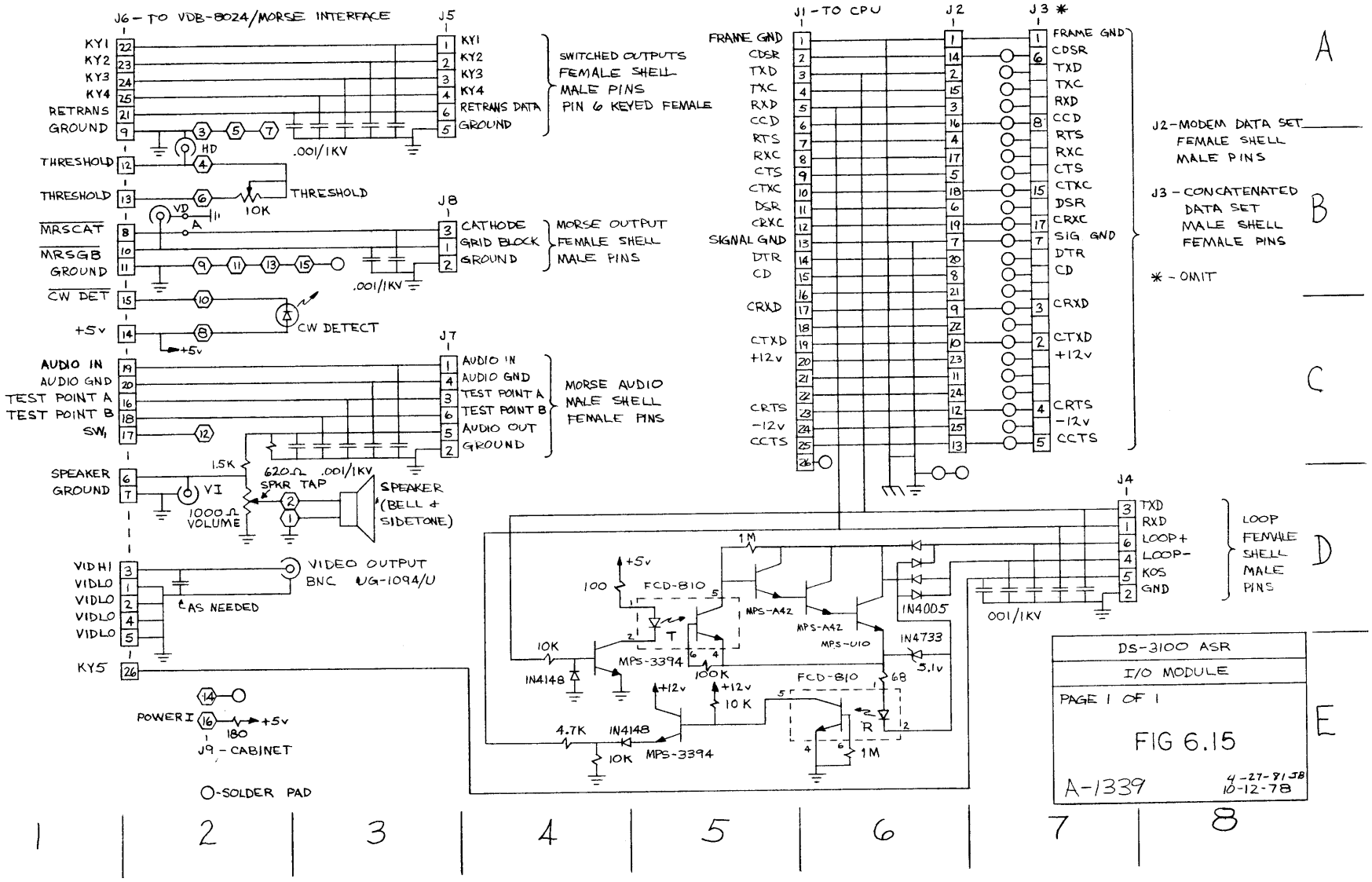
VDB-8024/MORSE INTERFACE
PORT DECODE/MORSE OUTPUT
PAGE 6 OF 6

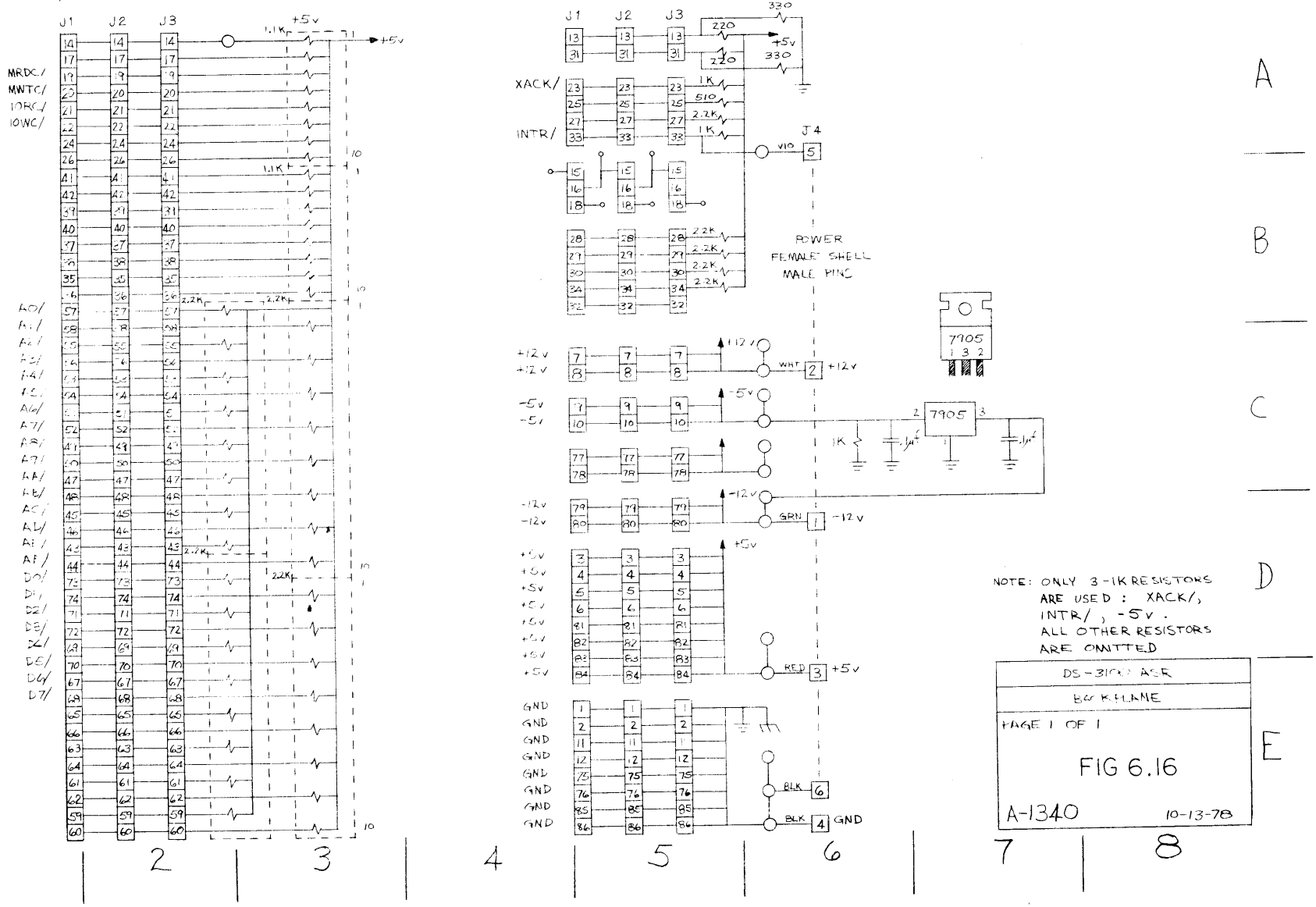
FIG 6.13

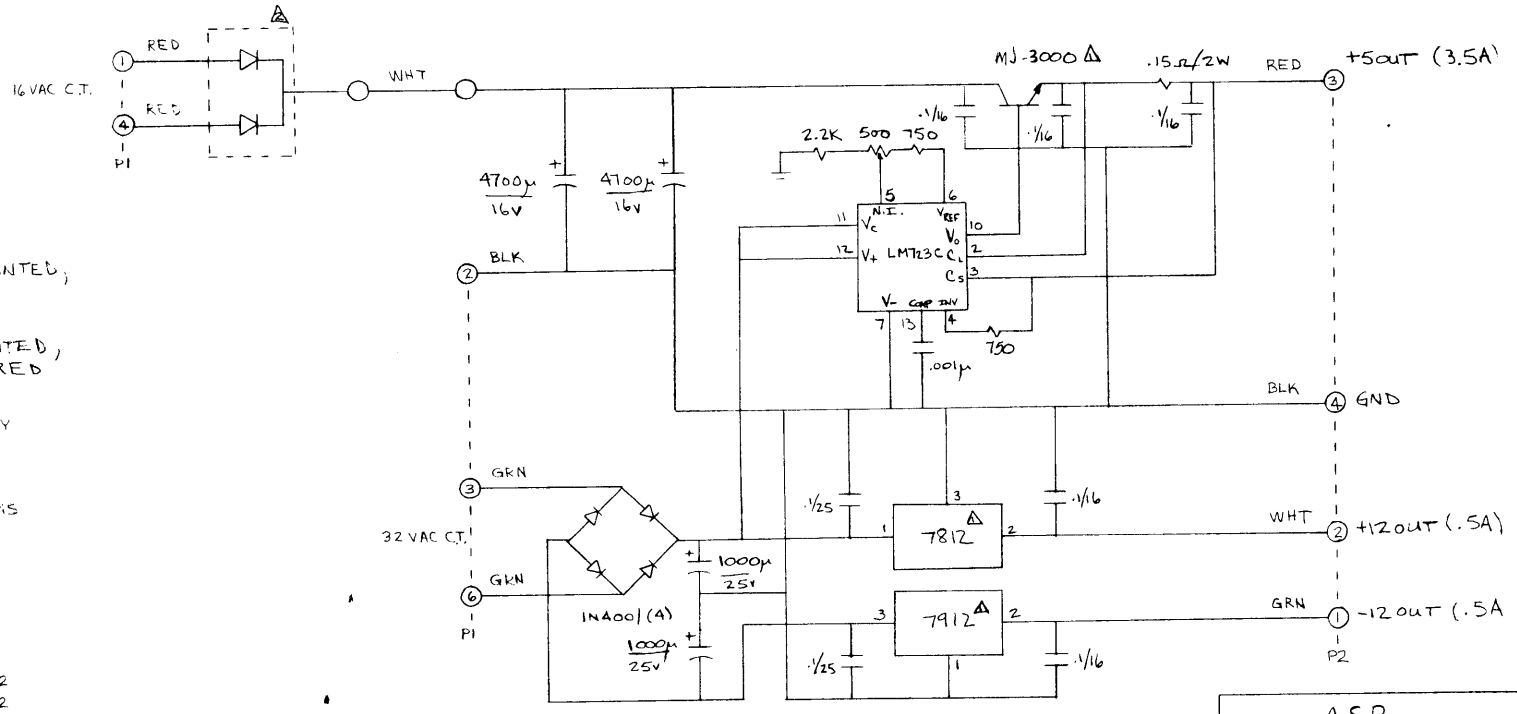
A-1338

MPT 1-22-79
MPT 10-10-79


100μS STB
DELAY
5mS DBNCE
110mS RPT OSC
RPT DELAY
.5 S
74LS123 B
74LS174
74LS00
74LS93
74LS175
74LS367
74LS368
74LS151
555
7442 (74S138)
FUNCTION
HERE IS
CONTROL
SHIFT L
SHIFT R
STB
KEYBOARD PORT = EB₁₆
KEY #
CODE
* NOT USED
KBRDY
FCTN
CTRL
SHIFT
GND
ASR PORT#/BIT #
CHERRY KEYBOARD W/AUTO-REPEAT
PAGE 1 of 1
FIG 6.14
A-1335A
PTT 12-7-79
MPT 1-22-79
MPT 9-20-78


J6 - TO VDB-8024/MORSE INTERFACE
J5
KY1
KY2
KY3
KY4
RETRANS
GROUND
SWITCHED OUTPUTS
FEMALE SHELL
MALE PINS
PIN 6 KEYED FEMALE
RETRANS DATA
HD
.001/1KV
THRESHOLD
10K
VD
J8
CATHODE
GRID BLOCK
MORSE OUTPUT
FEMALE SHELL
MALE PINS
MRSCAT
MRSGB
CW DET
CW DETECT
+5v
J7
AUDIO IN
AUDIO GND
TEST POINT A
TEST POINT B
SW1
MORSE AUDIO
MALE SHELL
FEMALE PINS
1.5K
620Ω
SPKR TAP
SPEAKER
(BELL & SIDETONE)
VI
1000Ω VOLUME
VIDEO OUTPUT
BNC UG-1094/U
VIDHI
VIDLO
AS NEEDED
KY5
POWER I
180
J9 - CABINET
O-SOLDER PAD
J1 - TO CPU
J2
J3 *
FRAME GND
CDSR
TXD
TXC
RXD
CCD
RTS
RXC
CTS
CTXC
DSR
CRXC
SIGNAL GND
DTR
CD
CRXD
CTXD
+12v
CRTS
-12v
CCTS
J2 - MODEM DATA SET
FEMALE SHELL
MALE PINS
J3 - CONCATENATED DATA SET
MALE SHELL
FEMALE PINS
* - OMIT
J4
LOOP+
LOOP-
KOS
LOOP FEMALE SHELL MALE PINS
1M
+5v
100
FCD-810
MPS-A42
MPS-U10
IN4005
IN4733
5.1v
T
MPS-3394
IN4148
100K
10K
68
R
4.7K
001/1KV
DS-3100 ASR
I/O MODULE
PAGE 1 OF 1
FIG 6.15
A-1339
4-27-81 JB
10-12-78


J1
J2
J3
J4
+5v
MRDC/
MWTC/
IORC/
IOWC/
1.1K
2.2K
XACK/
INTR/
330
220
510
1K
VIO
POWER
FEMALE SHELL
MALE PINS
+12v
-5v
-12v
WHT
GRN
RED
BLK
GND
7905
NOTE: ONLY 3-1K RESISTORS ARE USED : XACK/, INTR/ , -5v . ALL OTHER RESISTORS ARE OMITTED
DS-3100 ASR
BOK FLAME
PAGE 1 OF 1
FIG 6.16
A-1340
10-13-78

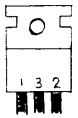


Δ FRAME MOUNTED, P.C. WIRED.

Δ FRAME MOUNTED, FRAME WIRED

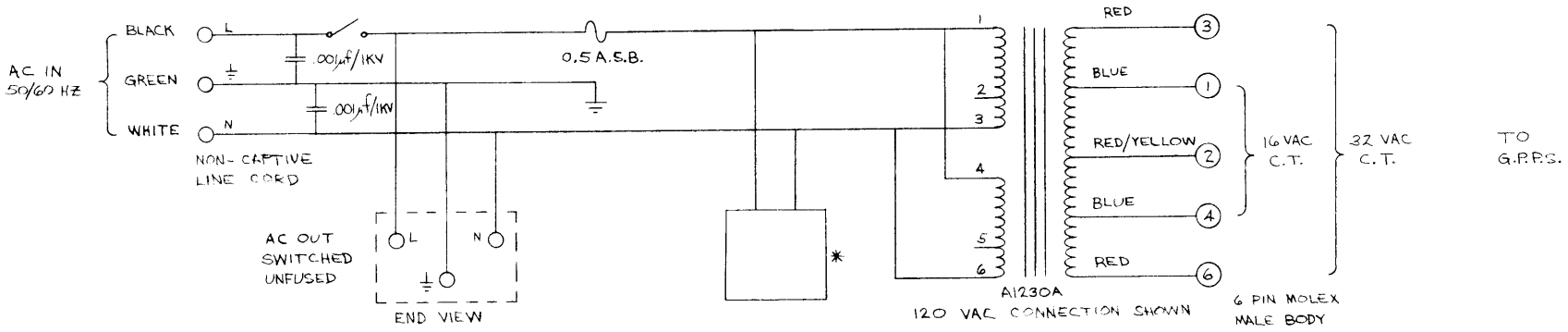
P1 = 6 PIN MOLEX
FEMALE BODY
MALE PINS

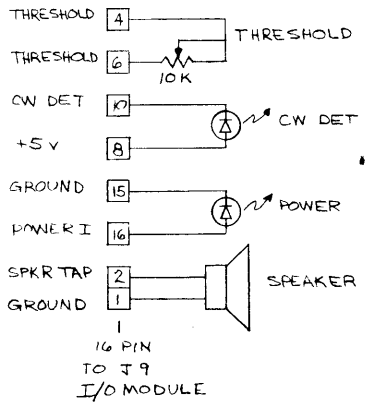
P2 = 6 PIN MOLE
MALE BODY
FEMALE PINS



U G R - 7812
G U R - 7912

ASR
POWER SUPPLY
FIG 6.17
P.T.T. 02/12/77 A1261





TRANSFORMER CONNECTIONS

VAC	JUMPER	POWER
100	1-4, 2-5	1, 5
120	1-4, 3-6	1, 6
200	2-4	1, 5
240	3-4	1, 6

*-OMIT

DS-3100 ASR
CABINET WIRING
PAGE 1 OF 1
FIG 6.18
A-1345 12-1-78

FIGURE 6.19 ASR - BASE AND MONITOR SECTIONS TOGETHER

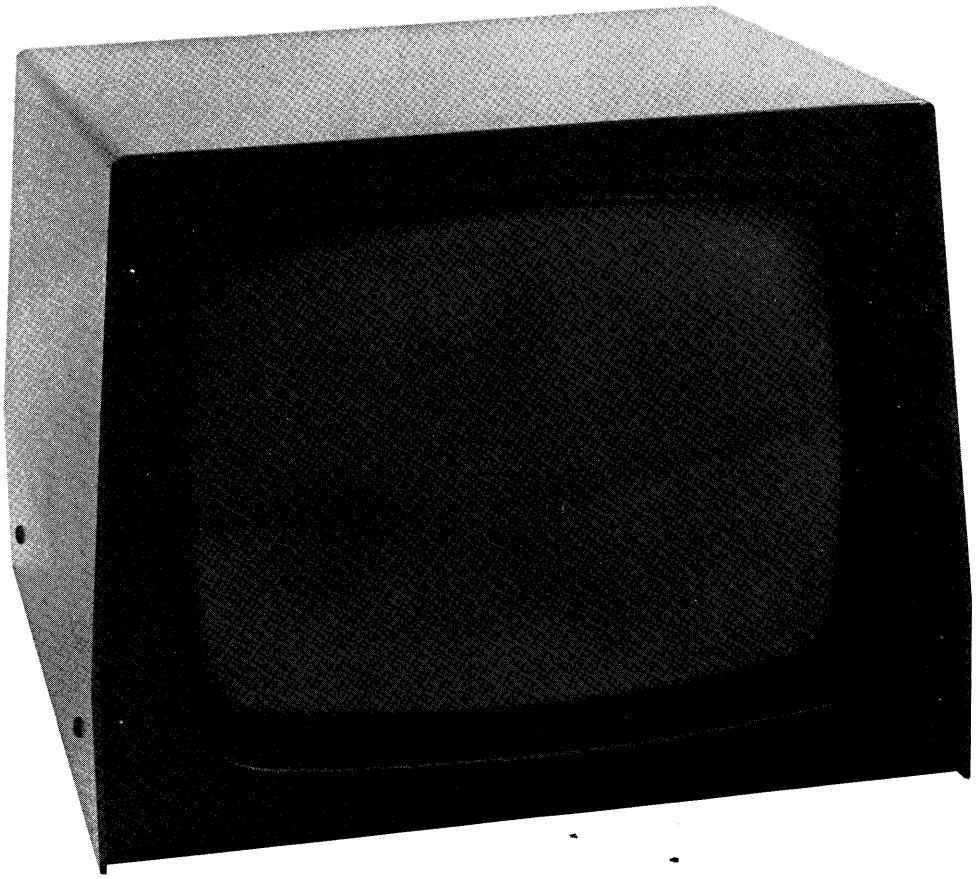


FIGURE 6.20 ASR - MONITOR SECTION DETACHED FROM BASE

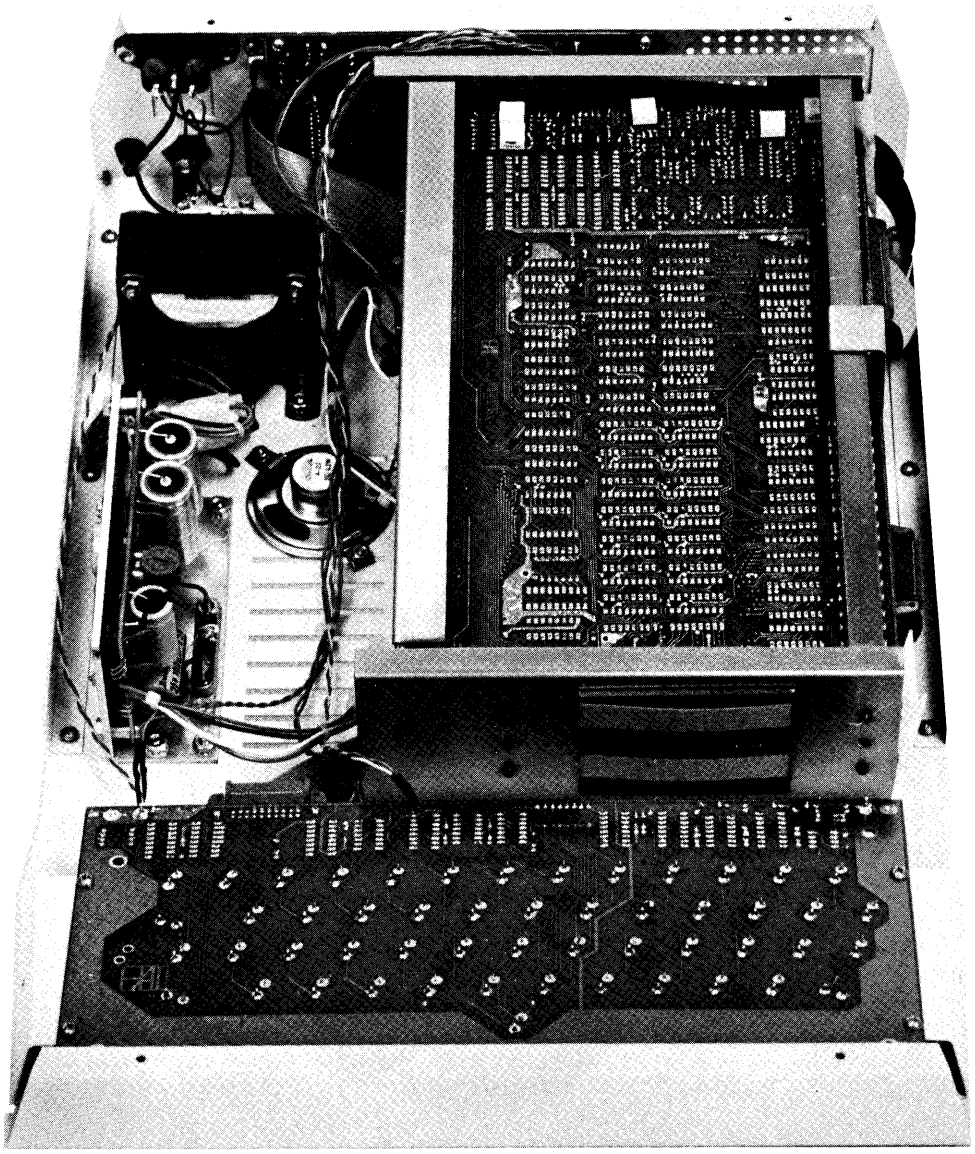


FIGURE 6.21 ASR - INTERIOR VIEW OF ASR BASE SECTION

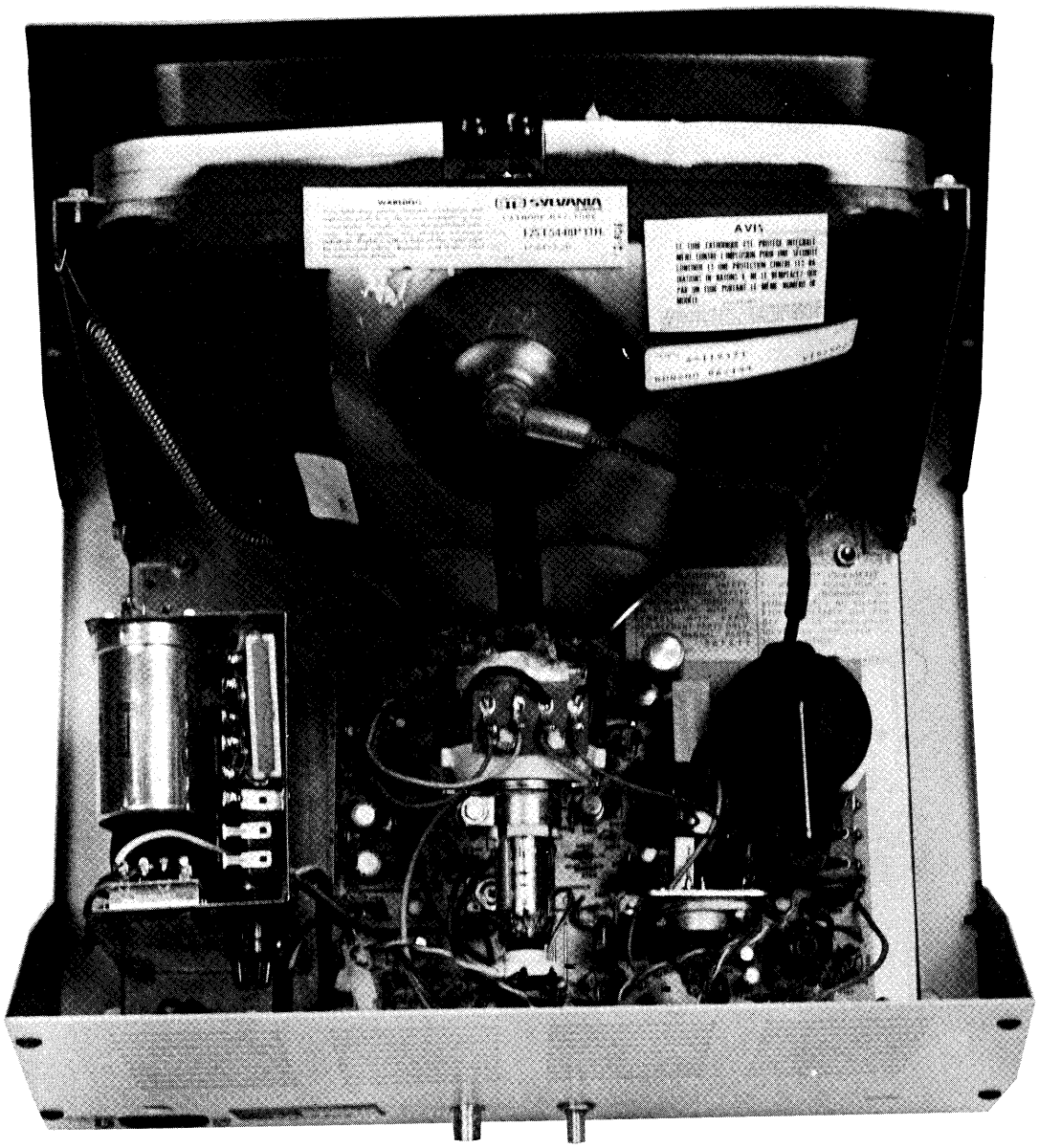


FIGURE 6.22 ASR - INTERIOR VIEW OF MONITOR SECTION

FIGURE 6.23 ASR - COMPONENT SIDE OF KEYBOARD

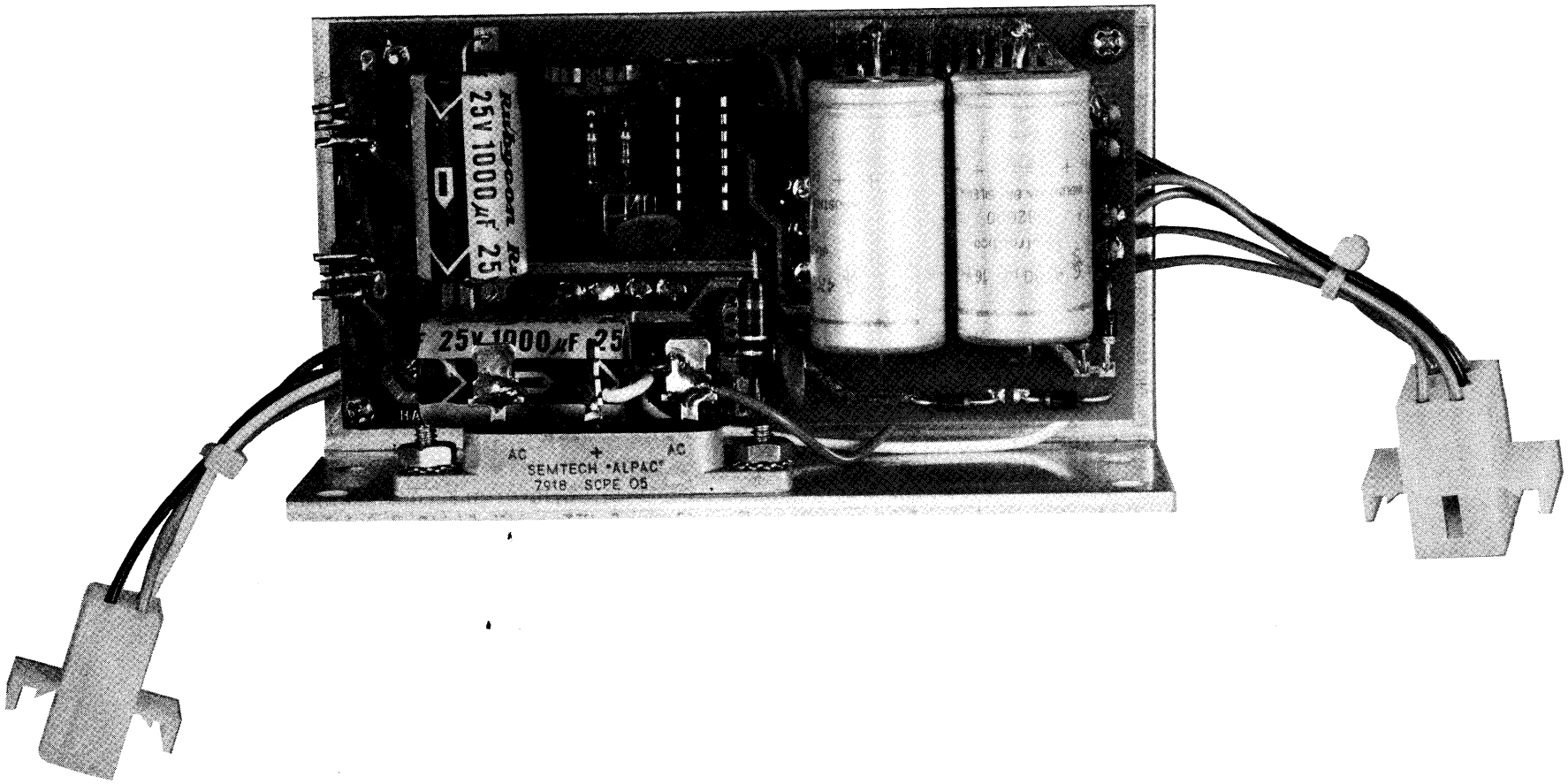


FIGURE 6.24 ASR - POWER SUPPLY MODULE

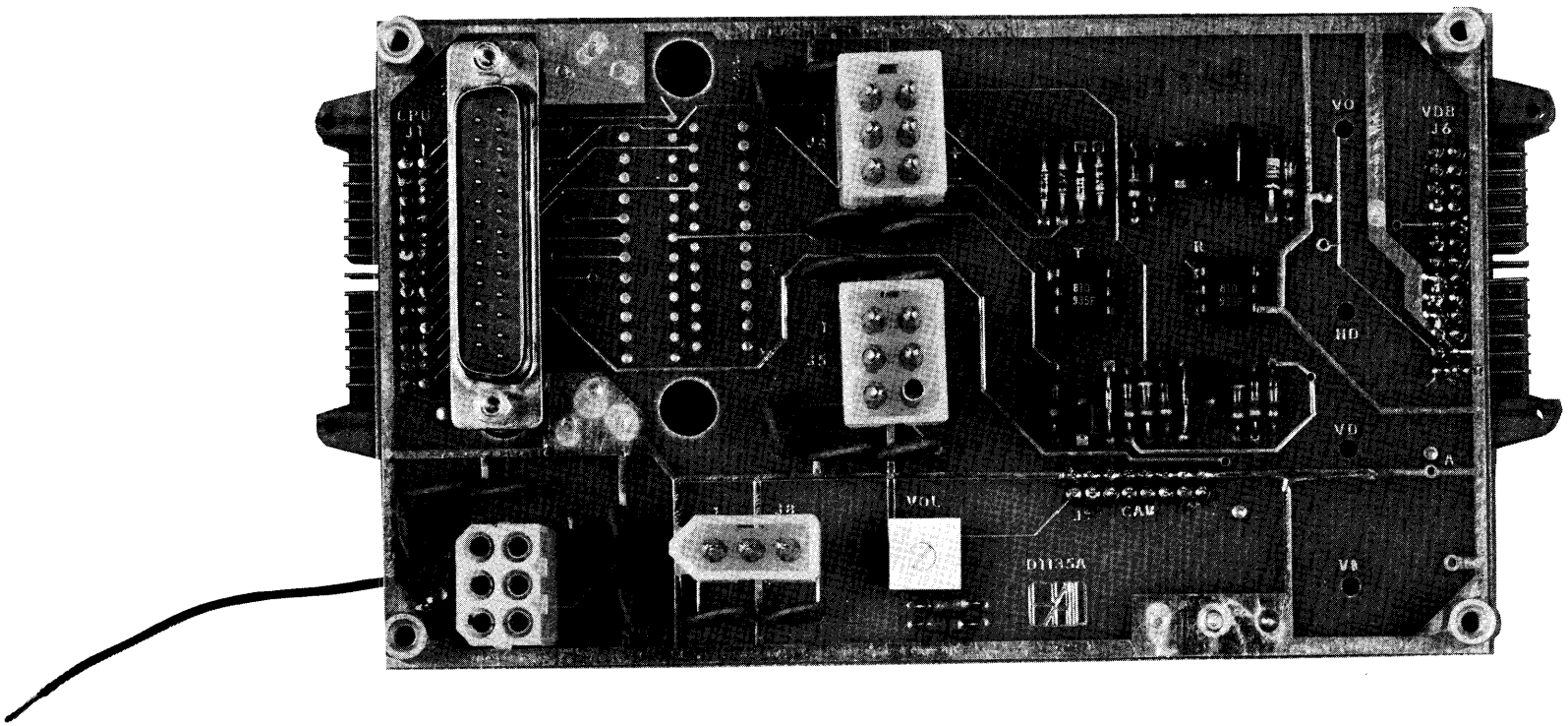


FIGURE 6.25 ASR - COMPONENT SIDE OF I/O BOARD

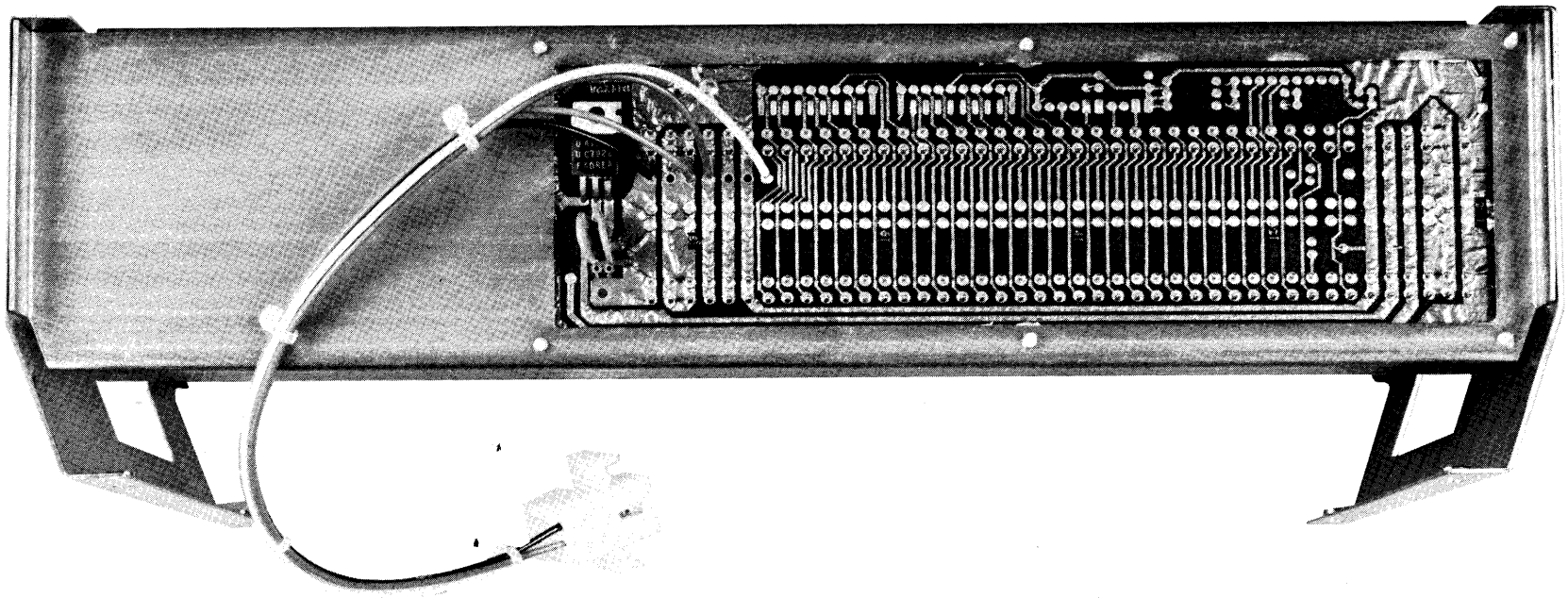


FIGURE 6.26 ASR - CARD CAGE ASSEMBLY/BACKPLANE