INSTRUCTION MANUAL

MODEL 703

CODE CONVERTER

November 1972

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ERRATA SHEET
MODEL 703

REFERENCE	CORRECTION
Page 4-13, Paragraph 4.3.4.4	Figure reference should be "Figure 6-1, Sheet 3" not "Figure 1, sheet 3". ECN 2502 1-4-77 PTM

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Model 703

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Figures 6-3 and 7-2.	Track has been cut between Z28-9 and Z31-13 to reduce the OSR stop bit length from 2 units to 1 unit. ECN 1261 12/6/72
Figure 6-3, Sheet 3	Z36-A output incorrectly labeled pin 2, should be labeled pin 6. ECN 1269 1/5/73
Figure 7-2, Parts List	Change manufacturers name of item 58 from Intel to National Semiconductor. ECN 1275 1/24/73

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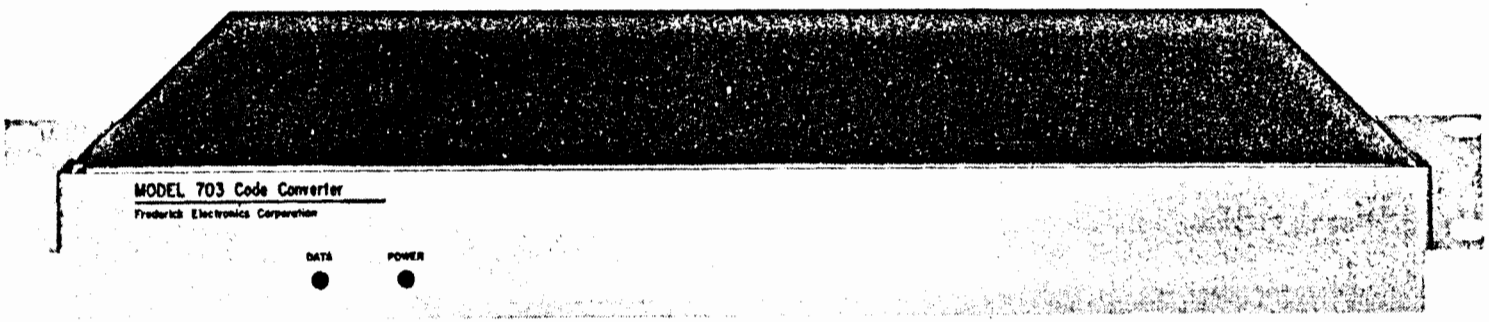


Figure 1-1. Model 703 Code Converter

SECTION I

INTRODUCTION

1.1 PURPOSE OF EQUIPMENT

The Model 703 is designed to operate as an on-line converter for translating 5-level start-stop code to an equivalent 8-level start-stop code.

The primary application for the 703 is as a computer code interface where 5-level baudot information must be converted to 8-level ASCII code. The 703 is also useful for interfacing a 5-level international or domestic communications channel to 8-level R.O. Office Equipment, in interoffice communications networks.

Character conversions are a 1 for 1 format requiring the output character time to always be equal to or less than the input character time.

Input signals to the Model 703 are isolated and gated to an input register via an input isolator and under the control of an input time base.

When a complete character is detected, the register applies the parallel 5-level character bits to a ROM (Read Only Memory), where it is decoded to activate the ROM storage positions. The ROM performs the actual format conversion, generating eight bits which are stored in a 1-character buffer. The conversion process is a 1 in/1 out character operation. Converted characters are presented to an output shift register buffer. The rate at which the output shift register releases data to the output driver is controlled by an output time base. There are two types of output signals available: a polar logic level EIA RS-232-C driver and high level neutral dry loop contacts.

Utilizing a master crystal oscillator and programmable input and output time base dividers, the 703 can operate at rates between 37.5 and 2400 baud.

1.2 PHYSICAL DESCRIPTION

The Code Converter is a completely solid-state device, packaged on a single printed circuit board. Access to the board is provided thru a removable top cover. The board tray is designed

to be mounted in the kneewell of a teleprinter or in a standard 19-inch equipment rack depending on the requirements of the customer.

The tray dimensions including the rear panel connectors are 16 inches wide (19 inches for rack mounting), 1-3/4 inches high, and 10 inches deep.

NOTE

Special mounting ears are attached for mounting in a 19-inch equipment rack.

All front and rear panel lettering is silk screened and the chassis is clear anodized.

1.3 SPECIFICATIONS

A list of specifications for the Model 703 is shown in Table 1-1.

Table 1-1. Specifications, Model 703

Input Signal	Accepts 5-level start-stop telegraph code with a stop pulse length of one unit or longer.
Input Circuit	Accepts 20 to 60 ma neutral, or 5 to 60 ma polar telegraph loops. Input impedance less than 100 ohms.
Input Rate	Selectable from 37.5 to 2400 baud.
Output Rate	Character time must be equal to or shorter than input character time.
Output Distortion	Less than 3% over complete range.
Output Signal	8-level start-stop telegraph code with a stop pulse length of two units.
Output Rate	Selectable from 37.5 to 2400 baud.
Output Circuits	Low Level: EIA RS-232-C polar logic level. High Level: Dry contacts of a neutral high level keyer suitable for keying 10 to 100 ma loops.

Table 1-1. (cont.)

Temperature Range	0°C to 55°C
Humidity Range	5% to 95%
Power Requirements	115/230 vac (±10%) 47/420 Hz universal ac power; approximately 18 watts.
Weight	Approximately 6 pounds (2.7 kg.)
Dimensions	Height: 1-3/4 inches (4.4 cm.) Width: 16 inches (40.6 cm.) Depth: 10 inches (25.4 cm.)

SECTION II

INSTALLATION

2.1 GENERAL

This section contains instructions for unpacking, mounting, programming of selectable characteristics, and connection of all necessary signal lines. Each 703 is programmed to match the users specifications and tested for correct operation prior to shipment from the factory. In the event that the unit does not operate properly, refer to the troubleshooting procedures discussed in Section V.

2.2 UNPACKING AND INSPECTION

Open the shipping container being careful not to puncture the container with sharp/metallic objects which may damage the contents. Remove the packing and the unit(s) from the container. Inspect the unit(s) for damage. If any damage is observed as the result of shipping, file a written claim with the shipping agency and forward a copy of this claim to:

Frederick Electronics Corporation
Hayward Road, Post Office Box 502
Frederick, Maryland 21701

If repacking for storage or reshipment is anticipated, replace the packing material and store the containers for later use.

2.3 POWER REQUIREMENTS

WARNING

VOLTAGES AS HIGH AS 230 VAC ARE HAZARDOUS TO LIFE. Exercise extreme caution when working in the power areas.

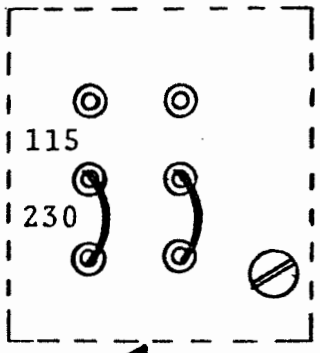
The Model 703 is shipped from the factory ready to operate directly from a nominal 115 vac, 47 to 420 Hz, 18 watt (maximum) power source unless the user has specified 230 vac at time of purchase (unit will have 230 vac label attached to chassis). Power is connected by plugging the power cord into a standard

three-prong ac outlet. The input is fused by F1 prior to application to the power supply.

CAUTION

Power transformer T1 must be correctly jumpered before unit can operate from a 230 vac source.

To wire the unit for 230 vac (or 115 vac), remove the screws securing the top cover to the chassis, and rewire T1 as shown in Figure 2-1.



Remove screw and protective cover to gain access to jumpers.

1. Remove jumper wires from "115" eyelets.
2. Install two new wire jumpers in "230" eyelets and solder. One half inch lengths of #22 wire make suitable jumpers.

Figure 2-1. Power Supply Jumper Connections

2.4 MOUNTING

The Model 703 is designed to be mounted in either the kneewell of a conventional teleprinter terminal or in a standard 19-inch equipment rack. The unit is normally shipped with special L-shaped rack mounting brackets which are attached to each side of the chassis with three screws to adapt the 703 for mounting in either a standard 19-inch rack or a kneewell location.

When the 703 is installed in the kneewell of a teleprinter, the special mounting ears are rotated to permit vertical attachment to the teleprinter chassis. When arranged for rack mounting the ears are mounted to secure the unit horizontally in the 19-inch rack.

NOTE

For rack mounting the front of the 703 protrudes 3-inches to the front of the rack.

2.5 SIGNAL CONNECTIONS

All input/output signal connections are provided at a 12-pin Molex connector located on the rear panel of the 703. Molex connector assembling information is provided in Figures 2-2 and 2-3. The connector and list of pin connections are shown in Figure 2-4.

CAUTION

To prevent keyer damage, ascertain that neutral loop circuit conforms to following requirements.

The loop keyer output connections are not polarity sensitive, but external current limiting must be used to limit current to a level below 100 milliamperes (maximum). When driving an inductive load (e.g., loops containing selector magnets, etc.), appropriate resistor-capacitor arc suppression must be connected across the output to limit voltage spikes across the keyer transistor switch.

2.6 OPERATIONAL PROGRAMMING

The Model 703 is programmed at the factory to match the users specifications. If the specifications are incomplete or if the programming requires changing at a later time, the eyelet positions shown on Figure 7-2 may require rewiring as indicated.

To install a wire jumper, cut and bend a short piece of #22 wire (approx. ½ inch) to a U-shape and insert between the designated eyelet pair. Solder each jumper and clip excess lead lengths.

The more complex input and output baud rate selection jumpering is discussed in 2.6.1.

Step 1. Strip about 1/8-inch of insulation from end of lead wire. Wire gauge range: #20 through #24 stranded conductor.

Step 2. Select appropriate pin type and lay lead wire in connector pin valley so that end of insulation is centered at notch between tabs.

Step 3. Using long nose or chain nose pliers, fold down one tab over exposed conductor wires.

Step 4. Fold down opposite tab over conductor wires.

Step 5. Solder crimped conductor to pin. Do not let solder flow towards pin tip. Avoid melting wire insulation.

Step 6. After pin has cooled, fold down a clamp tab over wire insulation.

Step 7. Fold down the remaining tab over wire insulation to complete pin assembly.

Figure 2-2. Connector Pin Assembly

As shown above, the complete cable plug is formed by inserting the lead wire and pin assemblies into the proper holes in the rear of the nylon connector body. A small screwdriver blade or similar tool may be used to assure full pin seating by placing the tool along the wire and pressing end-wise on the shoulder formed by tabs wrapped around the wire insulation. Proper seating obtains when the barbs on the pin sides have expanded beyond the hole diameter as viewed from the mating side of the connector plug.

Removal of pins from the connector body for replacement or wiring alterations may be facilitated by the tool listed below. The tool works by collapsing the retaining barbs on a pin so that it may be pulled out.

A hand operated crimping tool is available and may be desirable whenever large numbers of connections are required.

The following items are manufactured by:

Molex Products Company
5224 Katrine Ave.
Downers Grove, Ill. 60515

Removal tool	Part Numbers:	HT-1010-2B
Hand crimping tool		HT-1031-C

Figure 2-3. Connector Assembly

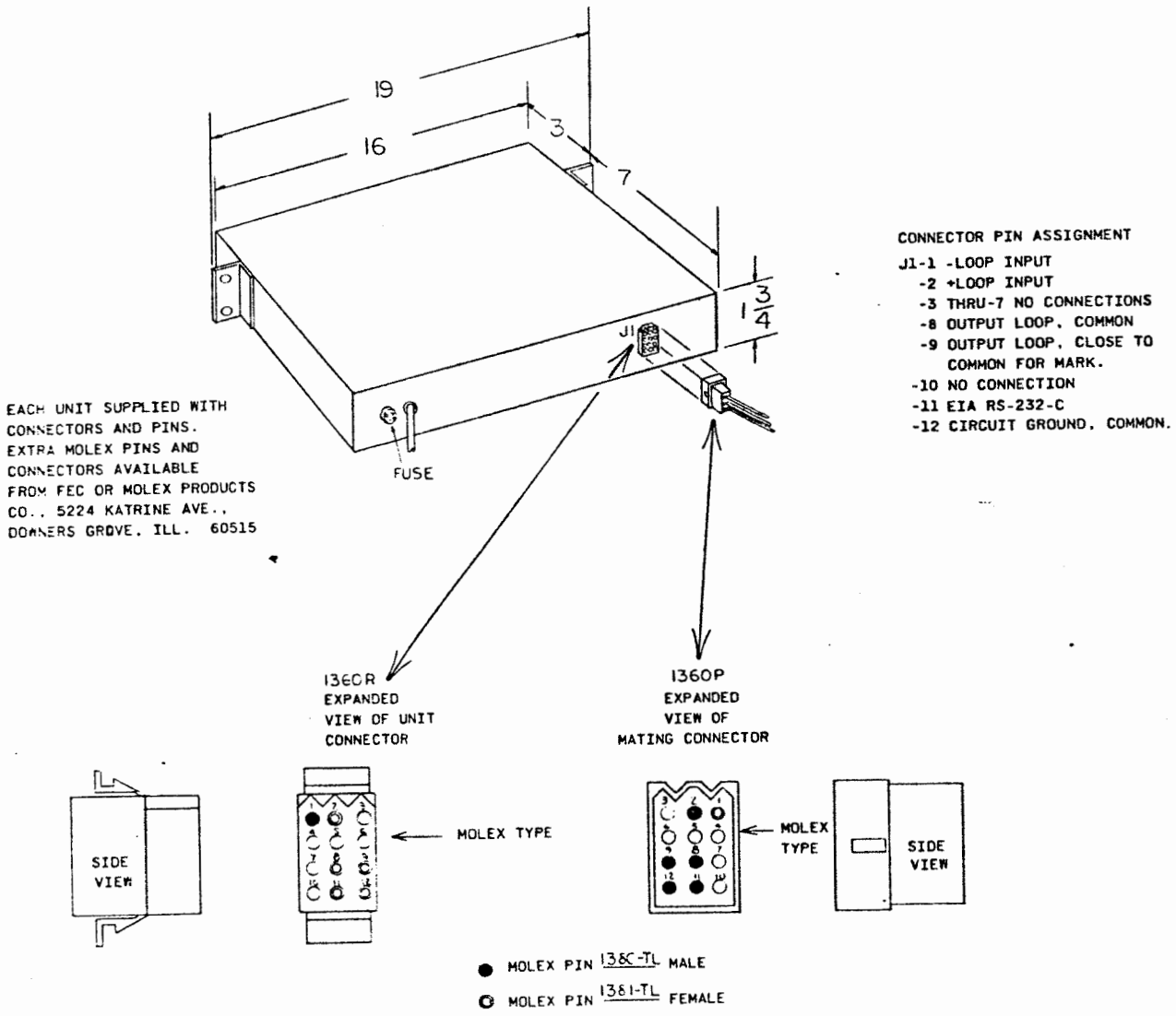


Figure 2-4. Installation Connections
C2642A

2.6.1 INPUT/OUTPUT RATE SELECTION

The Model 703 is capable of handling data at speeds up to 2400 baud. Baud rates are programmed by installing jumpers on board N01082 as shown in Figure 7-2. Each unit is shipped from the factory with the input and output time bases wired for customer specified baud rates.

Each time base circuit essentially contains an input clock selector circuit (384 kHz or 38.4 kHz), a 9-stage binary counter, and a ÷2 output clock flip-flop. Jumper positions on the board connect a binary 1 from selected counter stage outputs to permit integer divisions of the master clock. The time base counter output is programmable from 1 thru 511.

An additional jumper designated "X10" is also provided on the N01082 board for each time base to multiply the programmed baud rate by a factor of 10. These jumper points should be used when the operating rate exceeds approximately 600 baud.

The division factor (binary number) related to a specific baud rate is found from the formula:

$$\text{Division Factor} = \frac{38{,}400 \text{ Hz}}{\text{Required Baud Rate}} \times \tfrac{1}{2}$$

or

$$\text{Division Factor (X10)} = \frac{384{,}000 \text{ Hz}}{\text{Required Baud Rate}} \times \tfrac{1}{2}$$

Once the division factor is calculated, the hole-pairs can be jumpered. An example of this is shown for a required baud rate of 110.

1. Determine the division factor:

$$\text{Division Factor} = \frac{38{,}400 \text{ Hz}}{110} \times 1/2 = \frac{19{,}200}{110} = 174\tfrac{1}{11}$$

Since the time base circuitry division factors are integers, a fractional quotient must be increased or decreased to produce a valid division factor. In this case it is decreased to 174.

2. Since the quotient in Step 1 is the sum of two or more binary division factors, determine the hole-pairs to jumper as follows:

   a. Select the largest labeled binary division factor less than 174; the factor is 128 and the subtracted result is 46.
   b. Repeat step a. for the number 46; the factor is 32 and the result is 14.
   c. Repeat step a. for the number 14; the factor is 8 and the result is 6.
   d. Repeat step a. for the number 6; the factor is 4 and the result is 2, also a factor.

   Thus, the desired division factors are 128, 32, 8, 4, and 2.

3. Cut and bend five short pieces of #22 wire (approx. ½ inch) to a U-shape and insert a jumper between each selected hole-pair in the universal speed chip. Solder jumpers and clip excess lead lengths.

4. Apply power to 703 and ascertain that characters are being read thru correctly.

Table 2-1 identifies the hole pairs to be jumpered for some commonly used baud rates.

Table 2-1. Frequency Counter Jumpers For Common Baud Rates

Baud Rate	Speed Chip Jumpers
37.5	All positions
45.45	2, 4, 32, 128, & 256
50	128 & 256
74.2	1, 2, & 256
75	1 & 256
110	2, 4, 8, 32, & 128
150	128
1200 (X10)	128 & 32

SECTION III

OPERATION

3.1 GENERAL

The 703 contains two indicators lamps:

1. A POWER on indicator.
2. A DATA indicator to monitor the passage of DATA at the output.

No other indicators/controls are provided because the Model 703 code conversion operation is fully automatic. Before placing the 703 in operation ascertain that it is correctly installed as discussed in Section II.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section explains the functional operation of the Model 703 in sufficient detail to permit a trained electronics technician to understand the theory of each circuit.

4.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the Model 703 is shown in Figure 4-1. The Input Level Interface converts serial 5-level start-stop character inputs from a loop circuit to 0 to +5 vdc signals for application to an Input Shift Register. The leading edge of the Start bit of each character initiates each Register operation by starting an Input Time Base.

The Time Base, in turn, loads the Register at mid bit and then shifts forward each character bit one-half bit later. The Time Base receives both a 384 kHz and a 38.4 kHz clock input from a Master Crystal Oscillator. A programmable counter in the Time Base reduces the selected clock to the desired operating baud rate.

When the complete character is positioned in the Register, control gates generate a Strobe pulse which enables a Letters/Figures decoder in the Code Converter and a Transfer pulse which reads the converted 8-level character bits into an Output Shift Register. Special "L" and "F" jumpers from the Code Converter decoders normally inhibit generation of the Transfer pulse whenever the incoming 5-level character is a Letters or Figures character. If the "L" and "F" jumpers are not installed the equivalent control characters will be read from the 703.

As the character is transferred into the Output Shift Register, it will also start an Output Time Base if the Register is empty. If the Register is not empty, the Time Base will complete its current cycle and restart immediately. The Output Time Base is identical to the Input Time Base and also receives clock inputs from the Master Crystal Oscillator.

Functionally, the conversion operation is initiated when a complete character is detected in the Input Register. The Code Converter, consisting of a ROM (Read Only Memory) storage

module, performs the actual translation to eight character bits which are simultaneously read into the Output Register 1-character buffer. Thus, the conversion process is a 1 in/1 out character translation, requiring that the time of a complete output character (including start and stop bits) be shorter than the time of an input character.

When the complete 8-level character is shifted serially out of the Register, an empty detector not only stops the Output Time Base, it also clamps the Register signal output to mark.

The 8-level serial characters generated by the Output Register drive an Output EIA Driver, and Output Neutral Loop Keyer, and a DATA lamp. The DATA lamp is turned on when the output is mark.

4.3 DETAILED DESCRIPTION

4.3.1 MASTER OSCILLATOR

The master oscillator provides accurate timing signals to both the Input and Output Register Time Base circuits. The oscillator, shown in Figure 6-1 consists of crystal oscillator stages Z4-A/Z4-B and ÷10 counter Z2 located on board N01082.

The frequency of the two-stage oscillator is controlled by a 384 kHz series-resonant crystal Y1. The combination of digital inverters Z4-A/Z4-B and Y1 results in an output which approximates a square wave signal. The output is isolated by Z4-C and Z3-A before application to ÷10 counter Z2 producing both 384 kHz and 38.4 kHz signals for use by the Input/Output Register Time Base circuits.

4.3.2 INPUT SHIFT REGISTER

The input shift register converts incoming serial 5-level characters from the data circuit to parallel information bits. Each 5-level character is simultaneously converted to parallel 8-level information bits by the Code Converter and transferred to the Output Shift Register. The input register includes the following basic circuits:

1. Input Level Interface
2. Input Time Base
3. Shift Register And Control

All of the circuits are contained on board N01082 and are illustrated in Figure 6-1.

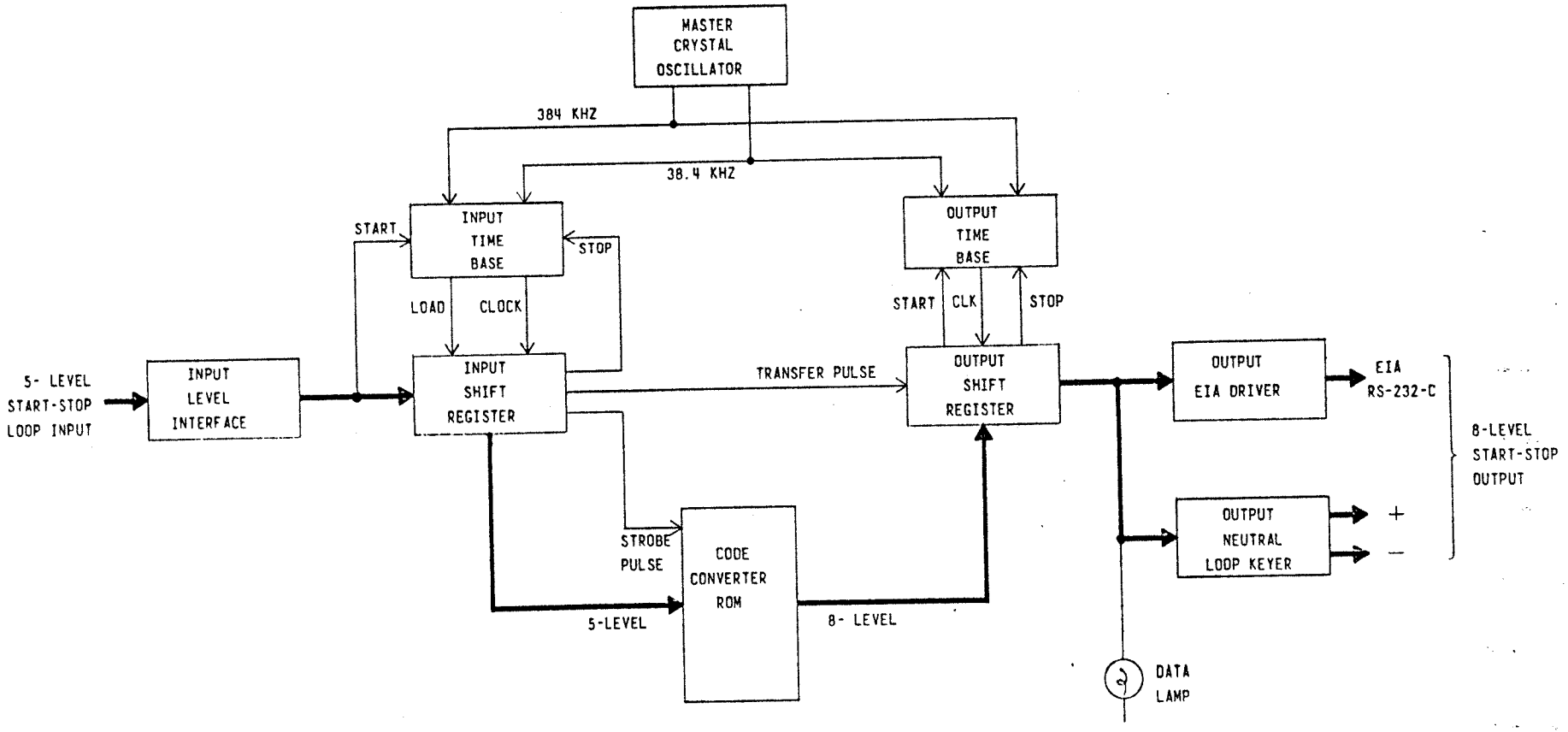


Figure 4-1. Functional Block Diagram
C2725

4.3.2.1 INPUT LEVEL INTERFACE. The input level interface converts neutral or polar, 20 to 60 ma loop circuit signals to 0-5 volt logic level signals for application to the Input Time Base and the Input Shift Register.

The high level input isolator consists of level gate Q4, photo isolator module Z5, and threshold detector Q5/Z11-C. External loop connections are attached to J1 pin 1 (-) and pin 2 (+) as shown in Figure 6-1.

The isolator will accept standard 20-60 ma/130 vdc neutral or polar loop connections. A wire jumper must be installed in the appropriate eyelet position ("20" or "60") to establish the switching threshold for neutral input loops. Neither eyelet pair is jumpered for polar loop inputs.

NOTE

External current limiting must be provided to prevent the current from exceeding 100 ma. Reverse voltage connections will not damage the isolator because of CR6.

Input mark current gates on Q4 which applies a positive level to photo isolator Z5. This positive level turns on Z5, generating a positive voltage at pin 4. The positive output turns on threshold detector Q5 producing a 0-volt mark output. During a space input, Q4 turns off and the photo isolator removes the positive level at pin 4 which switches the output of Q5 to a +5 volt space output.

Inverter Z11-C provides hysteresis feedback to the input of Q5 to provide positive switching and to reduce the effects of noise on the input loop.

The 0-volt mark output from Q5 drives the A_I input of the Shift Register while the inverted output from Z11-C (0-volt space) is used to drive the input of the Time Base.

4.3.2.2 INPUT TIME BASE. The time base circuit produces a series of clock pulses at the input signal baud rate to shift each character into the shift register.

The time base, shown in Figure 6-1 consists of the following circuits:

1. Start-stop flip-flop Z6-B
2. Input clock selection gates Z3-B (384 kHz) and Z3-D (38.4 kHz)

3. 9-stage frequency counter Z1, Z7, and Z6-A
4. Division selector jumper positions and gate Z8-B
5. Counter reset flip-flop Z9-C/Z9-D and reset gate Z9-A
6. ÷2 output clock flip-flop Z13-B
7. Load flip-flop Z13-A
8. Stop gate Z11-A
9. False start reset counter Z12

The ÷10 divider and the two clock control gates permit selection of either a 384 kHz (Z3-B) or a 38.4 kHz (Z3-D) input to the frequency counters thus permitting the upper baud rate limit to be expanded by a factor of 10. The counter is normally operated with Z3-D enabled below 600 baud and Z3-B enabled above 600 baud. Gate Z3-D is enabled by leaving jumpers out of the eyelets designated "X10" on N01082.

During the time between incoming characters, the time base is held in the reset state by start-stop flip-flop Z6-B. With the start-stop flip-flop reset, the LL0 Q output of Z6-B holds output flip-flop Z13-B and the frequency counter stages reset (via gate Z9-A), and holds the Input Shift Register modules in the clear state. The LL1 $\overline{Q}$ output from Z6-B also holds false start counter Z12 reset.

Time Base operation is initiated at the beginning of each character because the leading edge of the character start pulse from Z11-C clocks start-stop flip-flop Z6-B to a LL1 Q output. This releases the reset level from output clock flip-flop Z13-B and the frequency counter stages and removes the clear level from the Input Shift Register.

With the reset level removed from gate Z9-A, the frequency counter begins dividing the 38.4 kHz or 384 kHz clock from gate Z3-B or Z3-D. As the divider counts the clock input, selected binary outputs are ANDed by jumpers on board N01082 producing a high node input level to Z8-B when the desired division factor (binary number) is reached. (Refer to Section II for speed wiring information.) The divider modules are connected in series to produce a 9-stage divider that permits selection of division factors up to 2^9 (factors of 1 to 511). The binary number selected is determined by the jumper arrangement on the board and directly selects the division factor of the counter. For example, if a factor of 174 (i.e., 110 baud) is desired, a binary 174 (10101110) is programmed into the board eyelets.

NOTE

A jumper is installed for each binary 1.

The LL0 output from Z8-B sets flip-flop Z9-C/Z9-D which, in turn, enables reset gate Z9-A. The resultant LL1 from Z9-A returns the counter to reset and clocks Z13-B to the opposite state. After a short duration, the opposite phase (LL1) of the clock drive (i.e., 384 kHz or 38.4 kHz) signal resets flip-flop Z9-C/Z9-D via Z11-D. Thus, the frequency counter begins a new countdown sequence coincident with the next LL0 input clock transition.

The counter reset pulse output, after inversion by Z9-B, clocks Z13-B to a LL0 $\overline{Q}$ state coincident with mid bit of the character start pulse producing a half of a clock cycle. This LL0 level does not advance the register, but it does clock load flip-flop Z13-A to a LL1 Q state which enables the preset (P_E) input to Shift Register module Z10, loading the character start bit into stage A_I (none of the remaining preset inputs are used). The preset pulse is removed 2.9 or 29 microseconds later when the 384 kHz or 38.4 kHz clock resets Z9-C/Z9-D as discussed above.

One-half clock time later as the divider again resets, the reset pulse switches clock flip-flop Z13-B to a LL1 $\overline{Q}$ state producing the first shift level to the Shift Register. Clock generation continues until the five character information bits are loaded into the register, causing the register to reset the start-stop flip-flop by enabling stop gate Z11-A.

Since the dividers are connected in series, a total division factor of 2^9 can be programmed by jumpering the counter. Detailed wiring information is provided in Section II.

In addition to advancing the shift register, the output clock signal from Z13-B also advances false start reset counter Z12. Inverter Z11-B monitors the D_0 output of Z12 to detect a binary count of 8. In the event that the Time Base is not reset by the register or is inadvertently started by a noise pulse on the input line, Z11-B will reset the start-stop flip-flop after 8 clock transitions.

4.3.2.3 INPUT SHIFT REGISTER AND CONTROL. The shift register, shown in Figure 6-1, converts the 5-level serial characters to parallel form for translation to 8-level characters and generates conversion/transfer timing for the Code Converter Output Shift Register. The register circuitry includes 7-bit shift register Z10, Z14-A, and Z14-B; transfer gate Z15-B; strobe gate Z16-A; and a delay flip-flop Z37-A.

Register operation is initiated by the Time Base start-stop flip-flop at the beginning of each incoming serial character. Each character bit, beginning with the start bit, is loaded into the A_I stage of Z10 at mid bit by the preset pulse from the Time Base. One-half bit time later each bit is advanced to the next stage by the LL1 clock output from the Time Base.

When the character start bit (space) advances to stage Z14-A (5th clock pulse), the Q output of Z14-A switches to LL1 enabling one input to both the transfer gate Z15-B and the strobe gate Z16-A. At this time because the register stages were initially cleared to the mark state, the $\overline{Q}$ output of Z14-B is LL1 enabling an additional input to Z15-B.

A timing input, utilized as an enabling pulse for both gates, is generated when the trailing edge of the register preset pulse sets delay flip-flop Z37-A to a LL1 Q state. Several microseconds (2.9 or 29) later the selected Time Base clock signal (i.e., 384 kHz or 38.4 kHz) resets Z37-A, removing the enabling pulse. A delay in enabling the gates allows time for the ROM module in the Code Converter circuits to convert the input bits to an equivalent 8-level output. This delay also times the strobe gate output to enable decoders in the Code Converter in order to detect the presence of a Letters or a Figures input character. Detection of the Letters/Figures character can be used to inhibit generation of a transfer pulse from the Input Shift Register. The transfer gate, Z15-B, is inhibited during Letters/Figures characters by the "L" and "F" eyelet positions as long as jumper wires are installed because there are no 8-level character equivalents required for the Letters/Figures characters. If neither character is detected by the Code Converter or if the jumpers are not installed, transfer gate Z15-B is also enabled by the delay pulse from Z37-A. The generated transfer pulse reads the converted 8-level character from the Code Converter into a buffer register in the Output Shift Register.

In addition to producing a level to control the transfer gate, a decoded Letters or Figures character also sets a flip-flop in the Code Converter causing the Converter to begin producing the correct 8-level output characters from the upper or lower case 5-level input characters.

The next shift register clock pulse (6th) shifts the start pulse to stage Z14-B disabling the transfer gate (so next preset pulse cannot enable it) and enabling one input to Time Base stop gate Z11-A. One-half clock time later, the preset pulse enables Z11-A generating a short duration LL0 pulse which resets the Time Base start-stop flip-flop (Z6-B) to the clear state (LL1 $\overline{Q}$/LL0 Q).

This action causes the shift register and Time Base circuits to be returned to a reset or clear state until the beginning of the next character.

4.3.3 CODE CONVERTER

The code converter accesses the contents of a programmed Read Only Memory (ROM) module with the binary number produced by the 5-level character bits to generate the eight character bits of the equivalent 8-level characters. Since 5-level code utilizes a Letters or Figures character to generate alpha and numeric characters and the 8-level code requires no such control characters, correct interpretation of the 5-level code is provided by generating a sixth input bit to the ROM controlled by recognition of a Letters or Figures character. This sixth bit, referred to here as a LTRS/FIGS case bit, is stored in the selected binary state until the opposite control character is detected in order to permit the incoming 5-bit characters to access the correct memory positions in the ROM module.

The code converter, shown in Figure 6-2, consists of a 63-position ROM module Z17, letters decoder gate Z36-B, figures decoder gate Z23-A, letters/ figure storage flip-flop Z16-C/Z16-D, and several signal inverters. The character bits 1 thru 5 from the Input Shift Register are applied to binary address inputs designated A5 thru A1, respectively; these A_5 thru A_1 designations match bits 1 thru 5 as shown in ROM Truth Table, Figure 4-2.

NOTE

The actual binary input/output levels levels are inverted from normal so that a 1 or mark bit is a LL0 level.

Referring to the truth table, notice that output bits 5, 6, and 7 are 1, 0, 0 when the 5-level character is Figures and the outputs are 1, 1, 1 when the character is Letters. To detect a Figures control character the Figures decoder gate Z23-A samples the inverted bit 5 output of Z17 because it is LL1 and the direct bit 6 and 7 outputs because they are LL0 from the ROM. Conversly because all three bits are LL0, the Letters decoder gate Z36-B looks for the complement of Figures by sampling only the inverted bit 6 and 7 outputs of Z17. Neither gate is enabled until all of the character bits are read into the correct stages of the Input Shift Register because of the LL1 Strobe input generated by gate Z16-A as discussed previously.

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT						OUTPUT									
	BAUDOT SYMBOL	ASCII SYMBOL	BAUDOT						ASCII									
			CASE	1	2	3	4	5	b_1	b_2	b_3	b_4	b_5	b_6	b_7	EP
0	BLANK	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	T	T	0	0	0	0	0	1	0	0	1	0	1	0	1	1
2	CR	CR	0	0	0	0	1	0	1	0	1	1	0	0	0	1
3	O	O	0	0	0	0	1	1	1	1	1	1	0	0	1	1
4	SPACE	SPACE	0	0	0	1	0	0	0	0	0	0	0	1	0	1
5	H	H	0	0	0	1	0	1	0	0	0	1	0	0	1	0
6	N	N	0	0	0	1	1	0	0	1	1	1	0	0	1	0
7	M	M	0	0	0	1	1	1	1	0	1	1	0	0	1	0
8	LF	LF	0	0	1	0	0	0	0	1	0	1	0	0	0	0
9	L	L	0	0	1	0	0	1	0	0	1	1	0	0	1	1
10	R	R	0	0	1	0	1	0	0	1	0	0	1	0	1	1
11	G	G	0	0	1	0	1	1	1	1	1	0	0	0	1	0
12	I	I	0	0	1	1	0	0	1	0	0	1	0	0	1	1
13	P	P	0	0	1	1	0	1	0	0	0	0	1	0	1	0
14	C	C	0	0	1	1	1	0	1	1	0	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	1	0	1	0	1	0
16	E	E	0	1	0	0	0	0	1	0	1	0	0	0	1	1
17	Z	Z	0	1	0	0	0	1	0	1	0	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	0	1	0	0	0	1	0
19	B	B	0	1	0	0	1	1	0	1	0	0	0	0	1	0
20	S	S	0	1	0	1	0	0	1	1	0	0	1	0	1	0
21	Y	Y	0	1	0	1	0	1	1	0	0	1	1	0	1	0
22	F	F	0	1	0	1	1	0	0	1	1	0	0	0	1	1
23	X	X	0	1	0	1	1	1	0	0	0	1	1	0	1	1
24	A	A	0	1	1	0	0	0	1	0	0	0	0	0	1	0
25	W	W	0	1	1	0	0	1	1	1	1	0	1	0	1	1
26	J	J	0	1	1	0	1	0	0	1	0	1	0	0	1	1
27	UPPER	IS1/CAN	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	1	0	1	0	1	0	1	0
29	Q	Q	0	1	1	1	0	1	1	0	0	0	1	0	1	1
30	K	K	0	1	1	1	1	0	1	1	0	1	1	0	1	0
31	LOWER	DELETE	0	1	1	1	1	1	1	1	1	1	1	1	1	1
32	BLANK	NULL	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33	5	5	1	0	0	0	0	1	1	0	1	0	1	0	0	0
34	CR	CR	1	0	0	0	1	0	1	0	1	1	0	0	0	1
35	9	9	1	0	0	0	1	1	1	0	0	1	1	1	0	0
36	SPACE	SPACE	1	0	0	1	0	0	0	0	0	0	0	1	0	1
37	#/£S/S	BS/FE	1	0	0	1	0	1	0	0	0	1	0	0	0	1
38	•	•	1	0	0	1	1	0	0	0	1	1	0	1	0	1
39	-	-	1	0	0	1	1	1	0	1	1	1	0	1	0	0
40	LF	LF	1	0	1	0	0	0	0	1	0	1	0	0	0	0
41	)	)	1	0	1	0	0	1	1	0	0	1	0	1	0	1
42	4	4	1	0	1	0	1	0	0	0	1	0	1	1	0	1
43	&	&	1	0	1	0	1	1	0	1	1	0	0	1	0	1
44	8	8	1	0	1	1	0	0	0	0	0	1	1	1	0	1
45	0	0	1	0	1	1	0	1	0	0	0	0	1	1	0	0
46	:	:	1	0	1	1	1	0	0	1	0	1	1	1	0	0
47	;	;	1	0	1	1	1	1	1	1	0	1	1	1	0	1
48	3	3	1	1	0	0	0	0	1	1	0	0	1	1	0	0
49	"	"	1	1	0	0	0	1	0	1	0	0	0	1	0	0
50	$	$	1	1	0	0	1	0	0	0	1	0	0	1	0	0
51	?	?	1	1	0	0	1	1	1	1	1	1	1	1	0	0
52	BELL	BELL	1	1	0	1	0	0	1	1	1	0	0	0	0	1
53	6	6	1	1	0	1	0	1	0	1	1	0	1	0	0	0
54	!	!	1	1	0	1	1	0	1	1	1	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	1	1	1	0	1	0	0
56	-	-	1	1	1	0	0	0	1	0	1	1	0	1	0	1
57	2	2	1	1	1	0	0	1	0	1	0	0	1	1	0	0
58	*	*	1	1	1	0	1	0	1	1	1	0	0	1	0	0
59	UPPER	CAN	1	1	1	0	1	1	0	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	1	1	0	1	1	0	1
61	1	1	1	1	1	1	0	1	1	0	0	0	1	1	0	1
62	(	(	1	1	1	1	1	0	0	0	0	1	0	1	0	0
63	LOWER	DELETE	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LEGEND

EP - EVEN PARITY
LF - LINE FEED
CR - CARRIAGE RETURN
CAN - CANCEL
IS1 - INFORMATION SEPARATOR-1
S/S - STOP/START
BS - BACK SPACE
1=LLO=MK
0=LLT=SP

ROM Truth Table

If either decoder gate is activated by the ROM output, the resultant LL0 pulse sets flip-flop Z16-C/Z16-D to the respective state (i.e., Figures = LL1 from Z16-D and Letters = LL1 from Z16-C) and inhibits the output of transfer gate Z15-B (if the "L" and "F" jumpers are installed) in the Input Shift Register as discussed previously.

The letters/figures storage flip-flop output is inverted and used to control the A_6 (CASE) input to ROM module Z17 thus, accessing that portion of the ROM storage containing the programmed Letters or Figures equivalent 8-level characters. At the same time output bits produced by Z17 during a Letters or Figures character are never read from the 703 if the "L" and "F" jumpers are installed because they are not transferred to the Output Shift Register.

Two jumper options are provided in the code converter circuit. The first is a set of jumper eyelets designated "FIGS". When jumpered, this option locks the letters/figures flip-flop and, consequently, the ROM in the "Figures only" state by clamping input bit A_6 to 1. Thus, all incoming characters produce equivalent upper case 8-level outputs.

The second option permits the eighth 8-level bit generated by the 703 to be strapped for continuous mark or to be controlled by the parity output stored in the ROM for each character. Three eyelets are provided; a single jumper is installed between the pair designated "M" for continuous mark or the pair designated "P" to select the ROM parity output.

The 8 output bits are transferred to a 1-character buffer register in the Output Shift Register coincident with the Transfer pulse generated by the Input Shift Register.

4.3.4 OUTPUT SHIFT REGISTER

The output shift register circuits produce serial start-stop characters from the 8-level parallel bits generated by the ROM storage. The Output Shift Register consists of the following basic circuits:

1. Buffer Register
2. Output Time Base
3. Output Shift Register And Control
4. Output Interface Circuits

All of the circuits are contained on board N01082 and are illustrated in Figure 6-3.

4.3.4.1 BUFFER REGISTER. The buffer register stores the 8-bit outputs from the ROM and signals to the Time Base that a new character is waiting. The buffer consists of 4-bit latches Z24/Z25 and character ready flip-flop Z22-A shown in Figure 6-3.

In operation, the Transfer pulse generated by the Input Shift Register simultaneously loads the character bits into the buffer stages and clocks the character ready flip-flop to a $\overline{Q}$ LL1 or Character Ready state. However, the character ready flip-flop will be set only if the previous character has been loaded from the buffer to the Output Register (this operation will be discussed with the Time Base).

4.3.4.2 OUTPUT TIME BASE. The output Time Base, shown on Figure 6-3, consists of load control gate Z27-D; load flip-flop Z18-A; start-stop flip-flop Z18-B; clock selection gates Z30-A (384 kHz) and Z30-B (38.4 kHz); 9-stage frequency counter Z20, Z29, and Z28-A; division selection jumper positions and associated gate Z19-A counter reset flip-flop Z21-A/Z21-B; reset gate Z21-C; and output clock flip-flop Z22-B.

The Time Base produces a series of clock pulses for the Output Register at the selected outgoing baud rate (normally 110 baud) each time a new character is read into the Register from the Buffer. The Output Time Base operates functionally the same as the Input Time Base; therefore, only the load and start-stop control operations will be discussed.

With the start-stop flip-flop Z18-B initially in the reset state, the Q output holds the output clock flip-flop Z22-B reset, enables gate Z21-C which holds the frequency counter stages reset, and resets counter reset flip-flop Z21-A/Z21-B. The Q output of Z18-B also holds the Output Shift Register in the clear state.

At the same time, the $\overline{Q}$ output of Z18-B enables one input to load gate Z27-D. Thus, when a character is transferred from the ROM to the Buffer, the resultant $\overline{Q}$ LL1 output from character ready flip-flop Z22-A produces a LL0 output from gate Z27-D. This output, in turn, enables NOR gate Z27-C which removes a reset input from load flip-flop Z18-A. The next LL0 clock input to the Time Base (i.e., 384 kHz or 38.4 kHz) sets flip-flop Z18-A to a Q LL1 (load) state, which transfers the waiting character from the Buffer to the Output Shift Register stages. Simultaneously, the $\overline{Q}$ LL0 output clocks start-stop Z18-B to the start state, resets the character ready flip-flop, and enables gate Z27-C preventing immediate reset of load flip-flop Z18-A as the character ready flip-flop is reset. Thus, the next LL0 clock cycle (i.e., 384 kHz or 38.4 kHz clock) resets Z18-A assuring generation of a reliable load pulse to the Register stages.

Once the start-stop flip-flop is set to start, the Time Base begins generating clock pulses which, in turn, begin shifting the character bits out of the Register. In addition, the $\overline{Q}$ LL0 output holds the load flip-flop reset via gate Z27-D until the Time Base is reset. When the Register is empty, gate Z31-B resets the time base start-stop flip-flop.

The Time Base remains in this state until the next character is transferred from the Code Converter. Although the 703 requires that the output character time be shorter than the input character time, the two signals are asynchronous, thus the Buffer may have a character waiting when the Register reads empty. In these instances, the character ready signal will restart the Time Base immediately.

4.3.4.3 SHIFT REGISTER AND CONTROL. The output shift register and control adds Start and Stop bits to the parallel 8 information bits and shifts them serially from the 703 to form 8-level start-stop characters at the baud rate selected by the Time Base.

The register and control, shown on Figure 6-3, consists of 10-stage shift register Z33-Z34, register empty detector gates Z32, output data gate Z31-A, and stop bit flip-flop Z28-B and associated stop gate Z31-B.

The preset (P_E) input loads a character from the Buffer Register each time the Time Base load flip-flop Z18-A is set. At the same time, the A input to Z34 inserts a mark (stop) bit at the end of the character bits and the E input to Z33 inserts a space (start) bit at the beginning of the character. Prior to this time the register has been in the clear state, causing the output of empty gate Z32 to hold the data gate Z31-A in mark. When loaded, this level is removed permitting the E output of Z33 to control Z31-A.

The first clock pulse is generated one bit time after loading and begins shifting the character out of the register. As the bits are shifted out (LL0 = mark), the S_I input to Z34 loads the register to an all space or clear state. Thus, when the mark stop bit reaches stage E of Z33, not only is the output of Z31-A driven to mark, the empty gate is also enabled. The empty gate, in turn, holds Z31-A in mark, releases a reset clamp from stop flip-flop Z28-B, and enables one input to stop gate Z31-B. However, until the mark stop bit reads out of the register, the E output holds Z31-B disabled. One clock time later, the E output switches to space (LL1) enabling the input to Z31-B and the J input to Z28-B. Thus, the next clock pulse (2 bit

times after the beginning of stop pulse), switches Z28-B to a Q LL1 state which activates Z31-B resetting the Time Base start-stop flip-flop. Thus, data gate Z31-A produces a mark output until a new parallel-to-serial character conversion is initiated by the Time Base.

4.3.4.4 OUTPUT INTERFACE CIRCUITS. The output interface circuits, shown on Figure 6-3, consist of polar logic level driver Z26, isolated neutral loop keyer circuit Q1 thru Q3 and a front panel DATA lamp. All three circuits are driven directly from data gate Z31-A with the input to the isolated keyer inverted by Z27-A.

The polar logic level driver Z26 is a single operational amplifier with a preset switching threshold designed to convert 0 (space) to +5 vdc (mark) inputs to ±10 vdc signals conforming to EIA Standard RS-232-C specifications (-mark). The +5 vdc mark input to Z26 also turns on DATA lamp CR42, a Light Emitting Diode (LED).

The isolated neutral keyer is comprised of voltage-keyed oscillator Q2-Q3, isolation capacitors C10-C11, full-wave bridge rectifier CR11 thru CR14, filter C9-R12 and loop switching transistor Q1 and associated voltage bridge circuit CR7 thru CR10.

The Q2-Q3 oscillator is a complementary RC multivbrator controlled by elements C12 and C13. The oscillator is keyed on when Z27-A switches a +5 vdc across the oscillator by grounding the common side of the oscillator. The oscillator free-runs at approximately 750 kHz until the input is removed. The oscillator output is coupled by C10 and C11 to the CR11 thru CR14 bridge rectifier. Elements C9 and R12 filter the rectifier output, which turns on transistor switch Q1. Current flows thru the CR7 thru CR10 bridge circuit into the transmission loop, so the keyer module is not polarity sensitive.

CAUTION

External limiting is required to inhibit loop current from exceeding 100 ma, and external filtering across the loop is required for inductive loops.

4.3.5 POWER SUPPLY

The power supply consists of a ±10.7 vdc zener regulated section and a +5 vdc series-regulated section located on board N01082 as shown in Figure 6-2. The input windings to primary transformer T1 can be selected for 115 vac or 230 vac by jumpering "115/230" eyelet positions on board N01082 to the desired position. No primary power switch is provided on the 703.

NOTE

Unless otherwise specified, the Model 703 is wired for 115 vac.

The ±10.7 vdc section consists of full-wave rectifier CR1 thru CR4; +10.7 vdc filter C1-C26-R36, zener CR38 and diode CR39; and -10.7 vdc filter C2-C27-R37, zener CR40 and diode CR41. The zener regulated ±12 vdc outputs are supplied only to the ROM circuits in the Code Converter. Unregulated ±12 vdc is used by the output logic level driver.

The +5 vdc section consists of full-wave rectifier module CR5, series regulator Q6-Q7, and reference voltage operational amplifier Z35. The operational amplifier is internally referenced to +5 vdc at one input (pin 3) and monitors the +5 vdc output at the othe. input (pin 6) in order to control the conduction of series regulator Q6. Thus, as the +5 vdc output attempts to increase, Z35 reduces the conduction of Q7 which, in turn, reduces the conduction of Q6 increasing the series impedance. The opposite action occurs if the +5 vdc drops below the reference voltage.

SECTION V

MAINTENANCE

5.1 GENERAL

The maintenance information in this section will help assigned technicians troubleshoot the 703. Service technicians should possess a thorough understanding of solid-state integrated circuits and a background in TTY techniques before attempting to repair a defective unit. In addition, the technician will need an understanding of the circuit theory, and the related programming which might change the operating characteristics.

A discussion of the circuit theory is contained in Section IV and programming is discussed in Section II. Schematic and part location drawings are contained in Sections VI and VII, respectively.

WARNING

THE POWER SUPPLY AREAS MAY CONTAIN VOLTAGES AS HIGH AS 230 VAC. These voltages are always hazardous to life. Exercise extreme caution when working in these areas.

5.2 PREVENTIVE MAINTENANCE

Since the 703 is a solid-state low-power device, preventive maintenance is not recommended. Internal component inspection and cleaning is not recommended except during corrective maintenance. However, in locations with extreme environmental conditions, such as sand, dust, and/or large variations in humidity the unit may require frequent cleaning. Use a soft non-abrasive cloth or a medium bristle paint brush to clean the dirt.

CAUTION

Do not use harsh cleaning solvents.

5.3 CORRECTIVE MAINTENANCE

If the technican thoroughly understands the operation of the 703, malfunctions in its operation should be readily apparent by monitoring the input versus output traffic. Corrective maintenance involves observation of these malfunctions to localize a trouble to a specific malfunction.

5.3.1 REQUIRED TEST EQUIPMENT

The test equipment or its equivalent required to repair the 703 is listed in Table 5-1.

No special tools other than those normally contained in an electronic toolbox are required.

Table 5-1. Required Test Equipment

EQUIPMENT	MANUFACTURER
Oscilloscope	Tektronix 453
5-Level Teleprinter	Teletype Corp. 32
8-Level Teleprinter	Teletype Corp. 33
5-Level Message Generator	Frederick Electronics 1306A

5.3.2 TROUBLESHOOTING

Tables provided in this Section along with other suggested procedures, should help the service technician isolate a trouble to a specific circuit. Figure 7-2 shows the location of the components on the circuit board.

Begin troubleshooting by placing the test equipment in a convenient location for easy access to the 703. Remove the top cover to permit access to printed circuit board N01082.

Inspect the board components for obvious defects such as cracked or burned resistors, swollen capacitors, etc. as indicated in Table 5-2.

Follow visual inspection by measuring the Power Supply voltages at C1, C2 and C3 with an oscilloscope. With a nominal 115 vac or 230 vac input, the dc voltages should be as follows:

POINT	VOLTAGE
+ Side C2	Ground
+ Side C3	+5 vdc ±1%
+ Side C1	+12 vdc ±10%
- Side C2	-12 vdc ±10%

If the visual and voltage checks do not reveal the trouble, connect the test equipment as shown in Figure 5-1 and then proceed by checking the test points in Table 5-3. After a trouble is isolated to a general area, use the schematic diagrams in Section VI and an oscilloscope to locate the exact trouble.

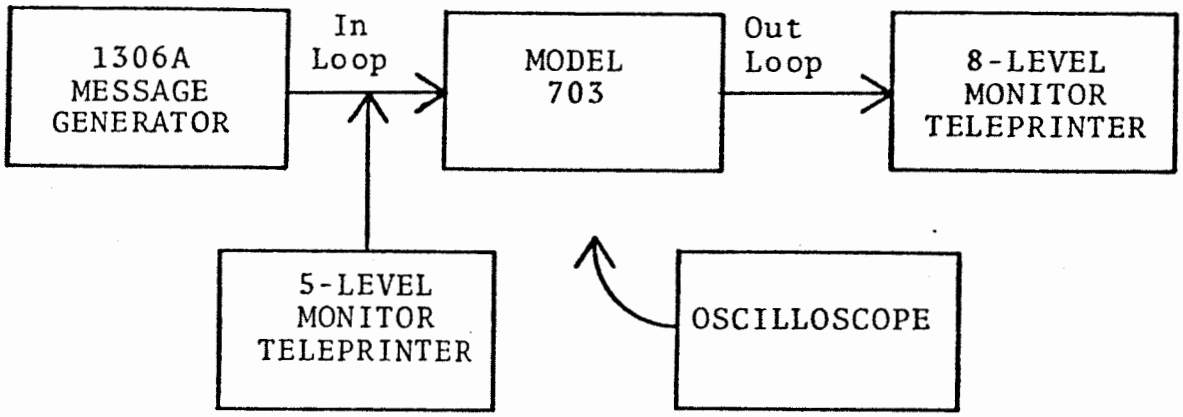


Figure 5-1. Test Equipment Connections

5.4 REPAIR

The Model 703 is designed for ease of subassembly removal and installation and will pose no problems for an experienced technician. Replacement of component parts is also routine. However, exercise caution not to damage or bend the pins of ROM module Z17 if removal is required; do not remove Z17 unless absolutely necessary.

Table 5-2. General Inspection Procedures

COMPONENT	CONDITION	CAUSE	CORRECTION
Resistors	Discolored, swollen, or cracked Cracked or broken	Overheated due to overload Improper handling	Locate and correct overload condition. Replace resistor.
Capacitors	Leakage, bulging, split case, or broken end seals	Physical damage or dielectric breakdown due to high voltage or improper handling	Check for high voltage condition and repair. Replace capacitor.
Transformers	Discolored insulation or windings, leakage	Overheated due to current overload	Locate and correct overload. Replace transformer if destroyed.
Connectors and jacks	Bent pins, charred insulation, marred threads, moisture, dirt, or grease	Improper handling	Straighten pins, clean or replace part.
Switches and controls	Broken, worn, bent, or dirty	Rough handling or normal wear	Clean, straighten, or replace.
Indicator lamps	Broken Burnt out	Rough handling, excessive current, or normal wear	Replace lamp.
Wiring and cables	Cut or frayed insulation, broken wires or connections	Improper handling	Repair or replace.
Solder connections	Loose or corroded connections, cold solder joints	Improper soldering	Clean and resolder.

Table 5-3. Trouble Isolation Chart

SYMPTOM	PROBABLE CAUSE	REMEDY
1. Incoming traffic not reading thru 703 to output.		
a. No signal at TP2.	a. Input Level Interface	a. Check loop circuit connections to 703. Check for 20/60 ma jumper with neutral loops. Repair Interface circuit.
b. No clock at TP1.	b. Master Oscillator or clock selector gates	b. Check 384 kHz output of oscillator. If present and "X10" jumper is removed, check for 38.4 kHz output at pin 12 of Z2/ pin 11 of Z3-D.
c. No register load pulse at TP5 but clock at TP4.	c. Load flip-flop Z13-A	c. Repair Z13-A.
d. No baud rate clock at TP4. NOTE If clock is present at TP4 but frequency is incorrect, check counter programming in Section II.	d. Input Time Base	d. Check for reset pulse at pin 3 of Z9-A. If present repair Z13-B. If not present check operation of counter and reset flip-flop.

Table 3. (cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
e. No transfer pulse at TP6.	e. Input Shift Register Transfer flip-flop Delay flip-flop	e. Check pin 5 of Z14-A to see if start bit is being read into register (i.e., switches to LL1 after 5 clock pulses). Check pin 5 of Z37-A to see if delay flip-flop is operating on trailing edge of Load pulse (TP5). Check transfer gate, especially "L" and "F" inputs from Code Converter.
f. TP8 not switching to LL0 when transfer pulse occurs at TP6.	f. Character Ready flip-flop	f. If TP9 is LL0, repair Z22-A.
g. No character bits present at buffer input pins 2 thru 7 of Z24/Z25.	g. Code Converter	g. Check bit inputs to pins 1, 2, 3, 20, and 21 of ROM Z17 from Input Shift Register. If present check output pins 4 thru 11 of Z17 for data bits.
h. Normal signals at TP8, TP9, and time base start-stop flip-flop is switching to LL1 at TP10, but no output at TP11. NOTE If clock is present at TP11 but frequency is incorrect, check counter programming in Section II.	h. Output Time Base counter or output flip-flop	h. Check for counter reset pulse at pin 8 of Z21-C. If present repair Z22-B. If not present check counter and reset flip-flop.

Table 5-3. (cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
i. Clock present at TP11 but no data at TP12.	i. Output Shift Register or Data Gate	i. If pin 10 of Z33 from register shows data transitions, repair gate Z31-A. If pin 10 is resting LL0, repair shift register.
2. Certain characters are being printed incorrectly on monitor.	a. ROM (Read Only Memory)	a. Apply repetitive incorrect character input to 703 and check for correct bit outputs from Input Shift Register using Table 4-2 (or appropriate coding chart). Sync oscilloscope externally to transfer pulse (TP6) to sample bit levels at correct time.
	b. Input Shift Register	b. If input bits are correct, check output bits from ROM by referring to Table 4-2. Sync oscilloscope externally to TP6 to sample bit levels.
	c. Output Shift Register	c. If ROM bits are correct, check input bits to Output Shift Register from Buffer Register using Table 4-2. Sync oscilloscope externally to Character Ready pulse (TP8) to check transfer of bits into Buffer and to load pulse (TP9) to check transfer of bits to Shift Register.
3. Data not present at Logic Level output but DATA lamp shows data.	a. Logic Level driver	a. Repair driver.

Table 5-3. (cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
4. Data not present at neutral loop output but DATA lamp shows data.	a. Neutral keyer	a. Check for data at pin 3 of Z27-A. If present, check for correct keyer connections to output loop. If connected correctly, repair neutral keyer.

SECTION VI

SCHEMATIC DIAGRAMS

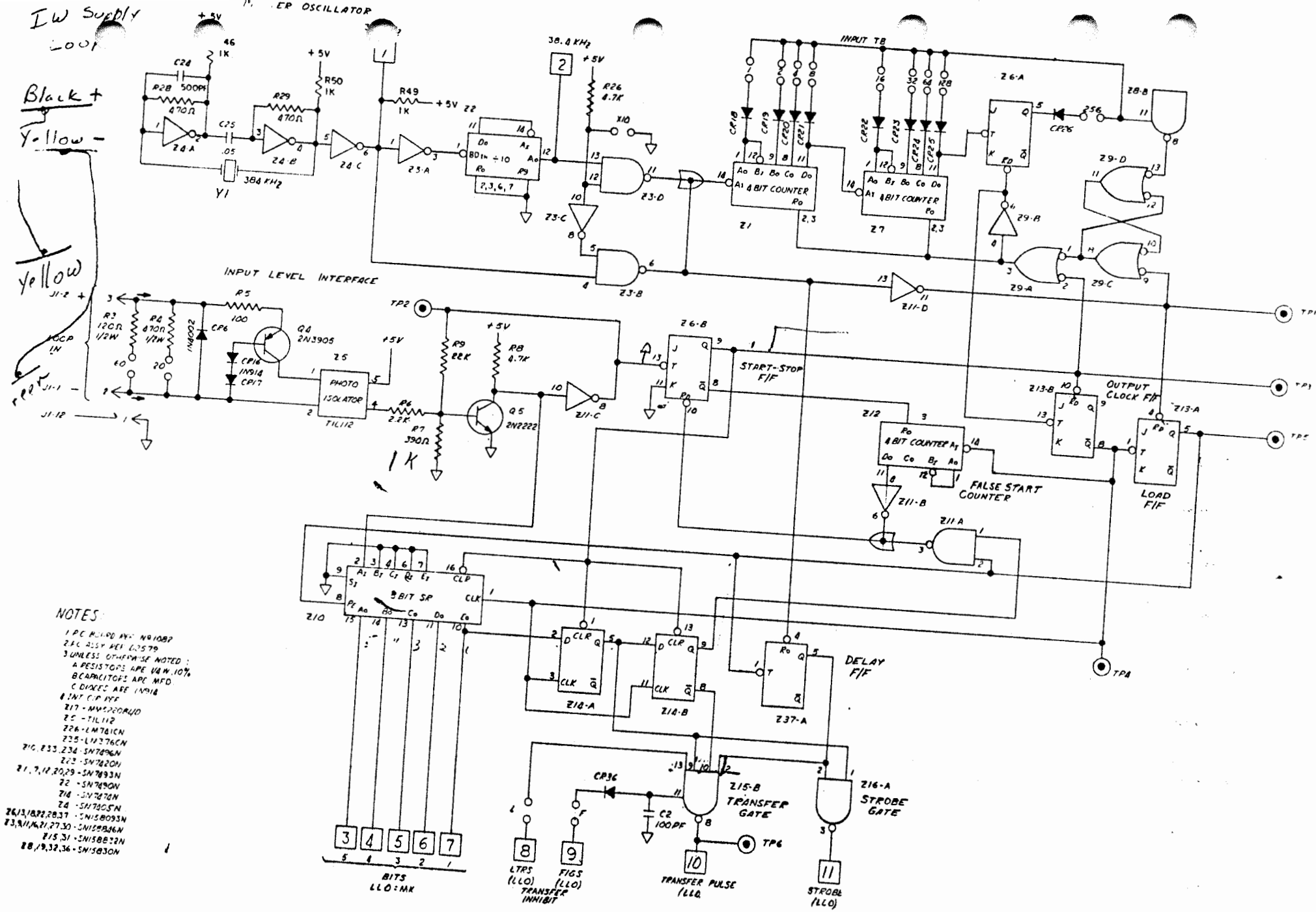


Figure 6-1. Input Shift Register Schematic Diagram
D2578A, Sheet 1

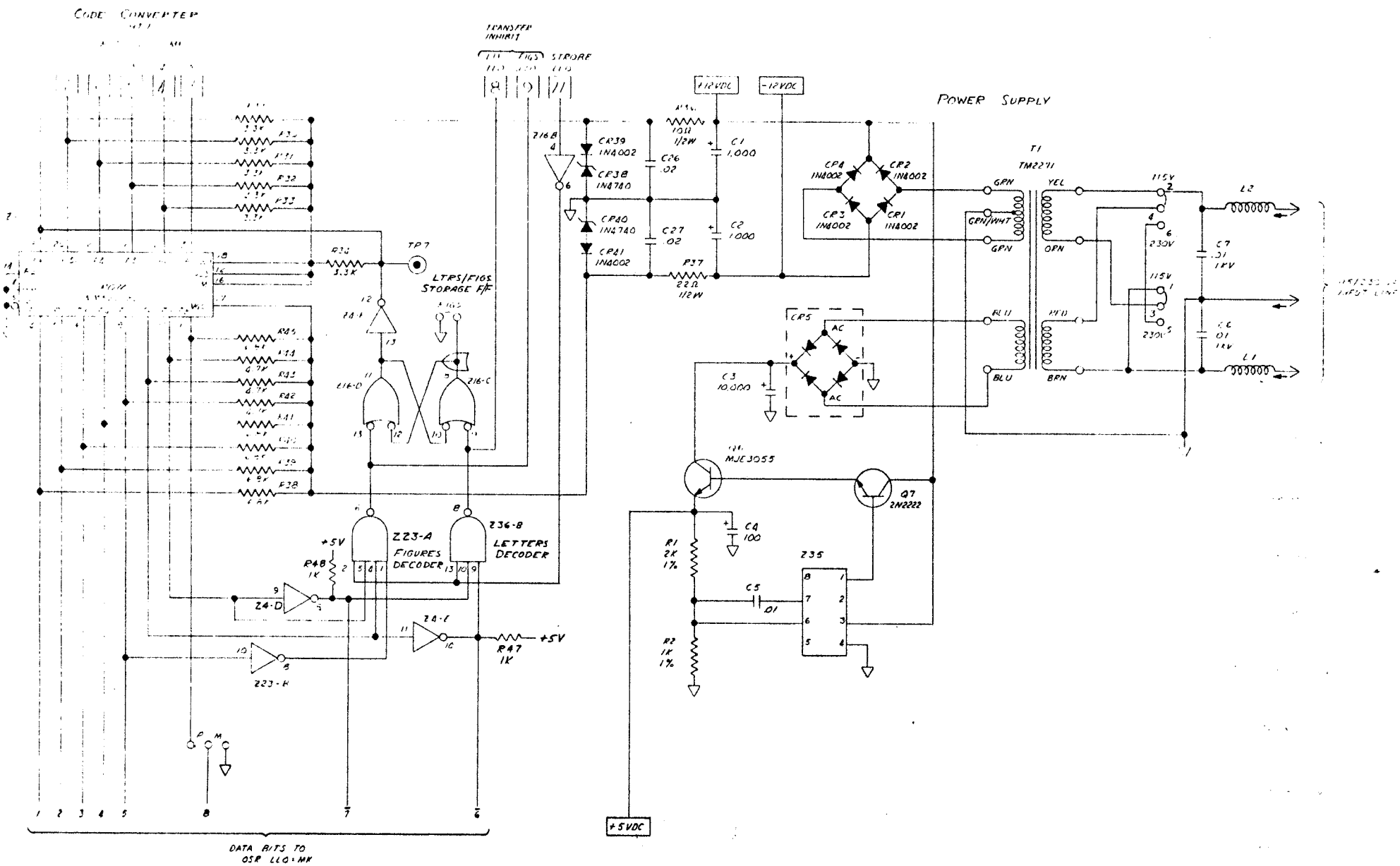


Figure 6-2. Code Converter And Power Supply Schematic Diagram
D2578A, Sheet 2

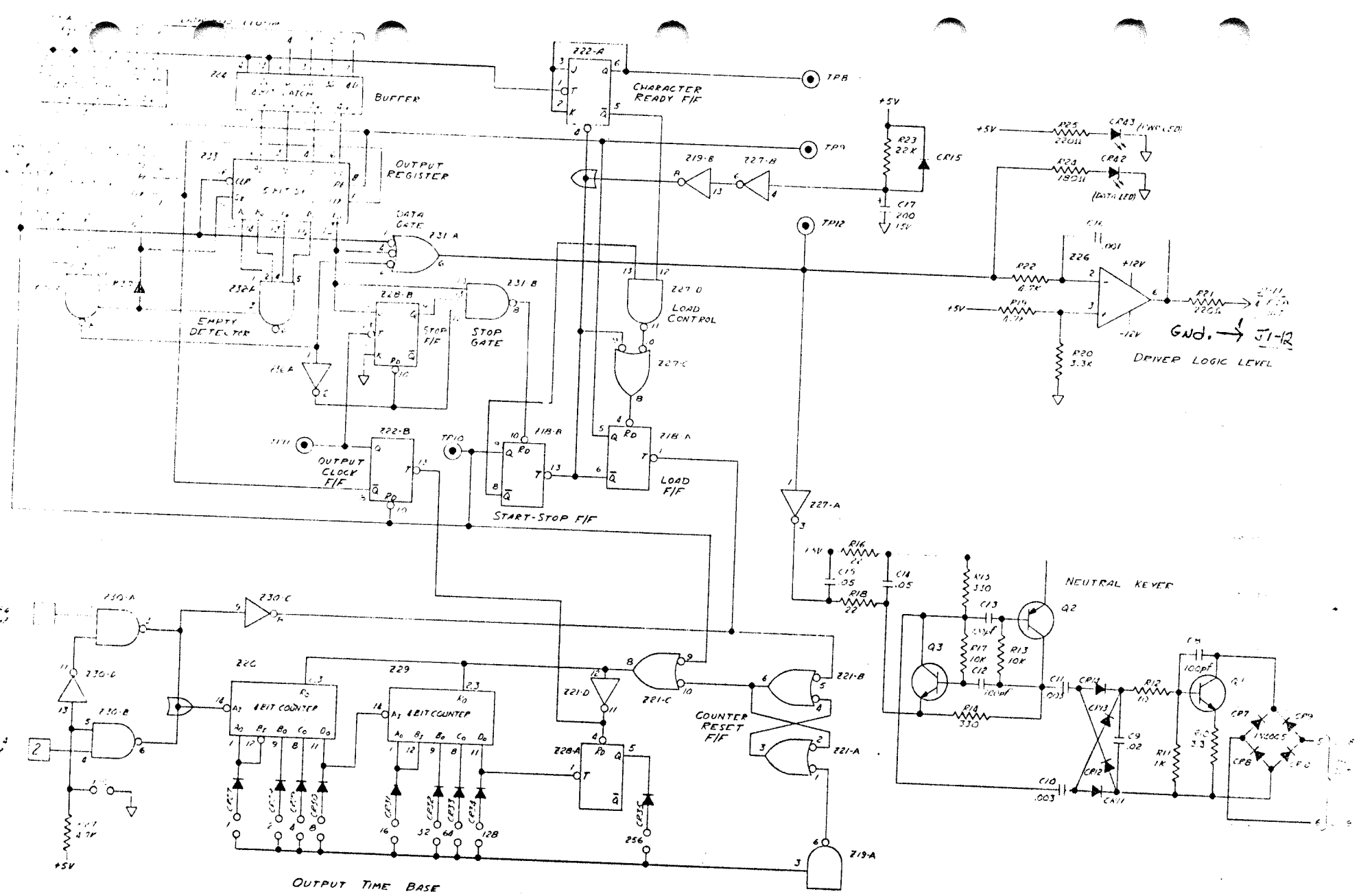
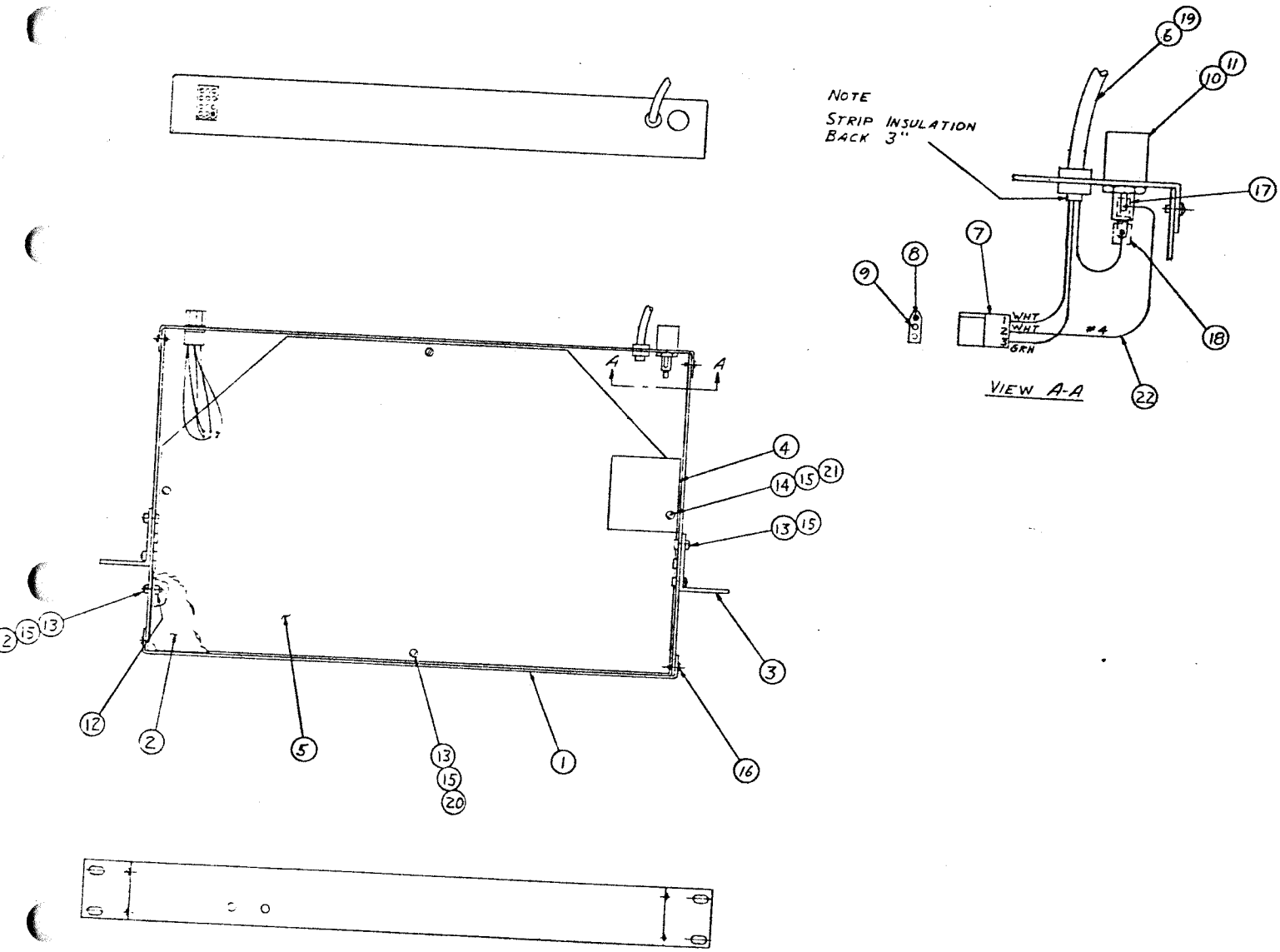


Figure 6-3. Output Shift Register Schematic Diagram
D2578A, Sheet 3

SECTION VII

PART REPLACEMENT DRAWINGS



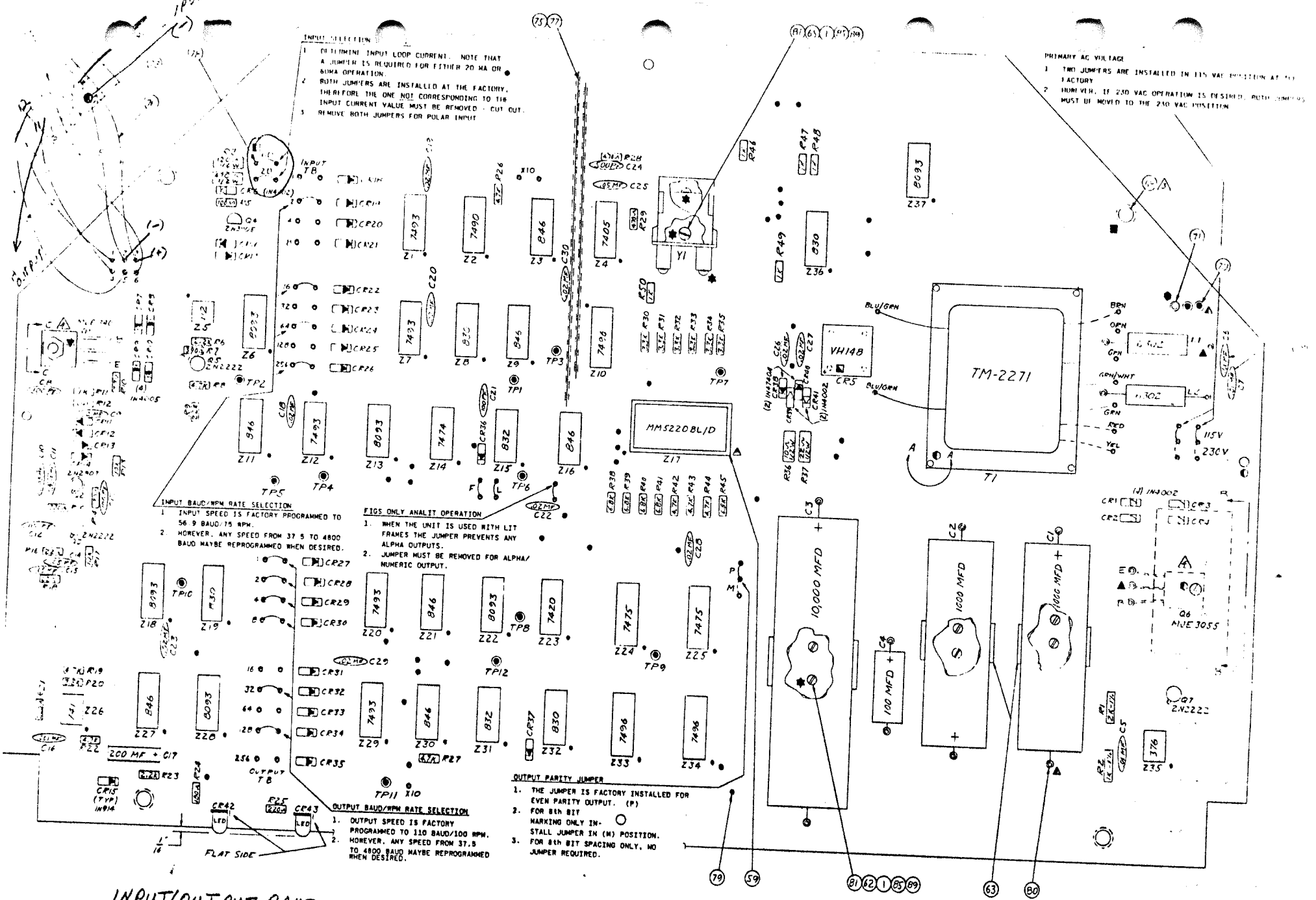
NOTES

1. BOARD MASTER IS B1853
2. CHASSIS SILK SCREENS ARE T0074 & T0075
3. ITEMS 23, 24, & 25 ARE SUPPLIED AS LOOSE EQUIPMENT AND WILL BE SHIPPED AS SUCH.

Figure 7-1. Model 703 Assembly
D2581

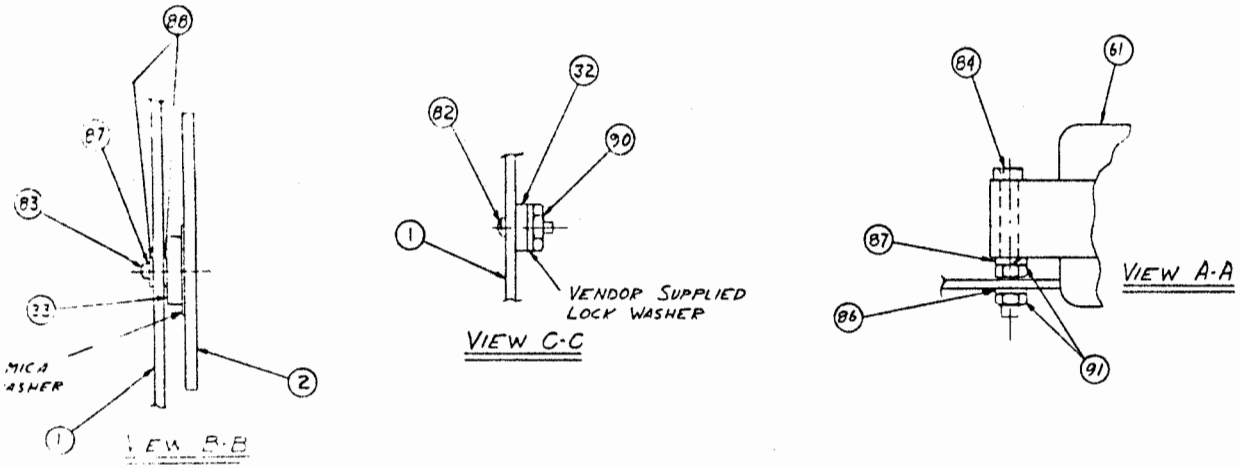
ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT PART NO	FINISH	FINISH SPEC	CKT SYM
25 (△3)	5	1380TL	TERMINAL MALE	MOLEX				
24 (△3)	1	1381TL	TERMINAL FEMALE	MOLEX				
23 (△3)	1	1360P	RECEPTACLE	MOLEX				
22	A/R		WIRE, 16 GA WHT	ALPHA				
21	1	1247-15	STANDOFF	CTC				
20	4	1246-11	STANDOFF	CTC				
19	A/R	17237	LINE CORD	BELDEN				
18	A/R	RNF100-1/4	HEAT SHRINKABLE TUBING	RAYCLAD				
17	A/R	RNF100-1/8	HEAT SHRINKABLE TUBING	RAYCLAD				
16	8	AD42H	RIVET	US				
15	13		WASHER, NO.6 INT TOOTH	SST				
14	1		SCREW NO.6-32 x 1 BH	SST				
13	11		SCREW NO.6-32 x 5/16 BH	SST				
12	12	6-32 x .050	PLUG NUT	LAM.SESS				
11	1	342004	FUSE HOLDER	LIT-FUSE				
10	1	313.5	FUSE, 1/2 A. SLO-BLO	LIT-FUSE				
9	2	1561-TL8	TERMINAL, FEMALE	MOLEX				
8	1	1560-TL8	TERMINAL, MALE	MOLEX				
7	1	1625-3R1	RECEPTACLE	MOLEX				
6	1	5-P4	STRAIN RELIEF	HEYCO				
5	1	D2579	ASSY P.C. BOARD	FEC				
4	1	B1868	P/S COVER	↓				
3	2	B1852	BRACKET, MTG.	⋮				
2	1	C2615	COVER	↑				
1	1	D2528	CHASSIS	FEC				

Figure 7-1. Parts List



INPUT/OUTPUT BAUD STRAPS:
110 BAUD = STRAPS IN: 2, 4, 8, 32, 128
300 BAUD = STRAPS IN: 64 only

Figure 7-2. Code Converter P.C. Board Assembly D2579B



NOTES

1. SCHEMATIC REF D2578
2. UNLESS OTHERWISE SPECIFIED DRILL ALL MOUNTING HOLES NO.55 (.052) AND INSTALL 46410 GRIPLETS.
   ALL I.C.'S ARE NO.70 (.028) DR.
   - ✱ NO.38 (.101) DR - 10 PLACES
   - ▼ NO.30 (.128) DR - 1 PLACE
   - ▲ NO.60 (.040) DR - AS REQUIRED FOR ITEM 59
   - ■ NO.11 (.191) DR - 4 PLACES
   - ◥ NO.55 (.052) DR - ✱ PLACES (NO GRIPLETS)
   - ▮ NO.55 (.052) DR - AS REQUIRED FOR ITEM 78
   - ▲ NO.49 (.073) DR - 15 PLACES
   - ◢ NO.52 (.063) DR - 14 PLACES
   - ● NO.43 (.089) DR - 1 PLACE
   - ◐ 5/32 (.156) DR - 9 PLACES
3. DO NOT SOLDER STANDOFFS TO BOARD.
4. INSTALL ITEM 32 WITH GOLD PLATING DOWN AND ITEM 33 WITH GOLD PLATING FACING ITEM 2.

ITEM	REQD	PART NO.	DESCRIPTION	MFR
94				
93				
92	1	DD-501	CAPACITOR 500PF, 1KV	CRL
91	8		NUT HEX NO.6-32 x 1/4 AF	SST
90	1		NUT HEX NO.4-40 x 1/4 AF	↓
89	7		NUT HEX NO.2-56	
88	2		WASHER NO.6 x 1/64 THK FL	
87	5		↓ NO.6 SPLIT LOCK	
86	4		↓ NO.6 INT TOOTH	
85	7		WASHER NO.2 SPLIT LOCK	
84	4		SCREW NO.6-32 x 1" BH	
83	1		↓ NO.6-32 x 3/8" BH	
82	1		↓ NO.4-40 x 3/8" BH	↓
81	7		SCREW NO.2-56 x 3/16 BH	SST
80	12	47042	GRIPLET	BERG
79	A/R	46410	GRIPLET	BERG
78	A/R	S-6064	EYELET	US
77	A/R		TUBING, NAT	ALPHA
76	A/R		WIRE, 24 GA WHT	ALPHA
75	A/R		WIRE, 22 GA SOLID	ALPHA
74	5	1381TL	TERMINAL FEMALE	MOLEX
73	1	1380TL	TERMINAL MALE	MOLEX
72	1	1360R	CONNECTOR	MOLEX
71	1	M93-102ET	STAKE PIN FEMALE	B.CHAIN
70	14	R62-3ET	STAKE PIN MALE	B.CHAIN
3 69	4	1246-11	STANDOFF	CTC
68	2	521-9165	LED DIODE	DIALCO
67	2	6302	CHOKE	MILLER
66	1	D2400-89	CRYSTAL, 384 KHz	FEC
65	1	8000-AG3	SOCKET, CRYSTAL	AUGAT

ITEM	REQD	PART NO	DESCRIPTION	MFR
64	2	SN7475N	INT CIR	TI
63	2	6018-63A	CLAMP CAPACITOR	AUGAT
62	1	6020-28A	CLAMP CAPACITOR	AUGAT
61	1	TM2271	TRANSFORMER	TRANS-INF
60	1	VH148	RECTIFIER	VARO
59	1	IC246-S2	SOCKET	ROBINSON
58	1	MM5220BL/D	INT CIR (ROM)	INTEL
57	1	TIL112	↓	TI
56	1	LM741CN		NAT
55	1	LM376CN		NAT
54	3	SN7496N		TI
53	1	20N		↓
52	5	93N		
51	1	90N		
50	1	74N		
49	1	SN7405N		
48	6	SN158093N		
47	7	846N		
46	2	832N	↓	↓
45	4	SN1583ON	INT CIR	TI
44	1	39D109G010J4	CAPACITOR 10.000MFD 10V	SPRAGUE
43	2	39D108G025GL4	↓ 1.000MFD 25V	SPRAGUE
42	1	MTP207M015P1C	200MFD 15V	MALLORY
41	1	TE1162	100MFD 15V	SPRAGUE
40	3	5855Y5U503Z	.05MFD 25V	ERIE
39	11	5835Y5U203Z	.02MFD 25V	ERIE
38	2	5HK-S10	.01MFD 1KV	SPRAGUE
37	1	5835Y5U103Z	.01MFD 25V	ERIE
36	2	DD302	.003MFD 1KV	CRL
35	1	801X5F102K	.001MFD 1KV	ERIE
34	4	DD101	CAPACITOR 100PF 1KV	CRL
4 33	1	MJE3055	TRANSISTOR	MOT
4 32	1	MJE340	↓	MOT
31	1	2N3905		MOT
30	1	2N2907	↓	MOT
29	3	2N2222	TRANSISTOR	NAT
28	2	1N4740A	DIODE, ZENER	MOT
27	4	1N4005	↓	MOT
26	7	1N4002	↓	MOT
25	27	1N914	DIODE	GE
24	1	RC20GF471K	RESISTOR 470Ω 1/2W 10%	AB
23	1	121K	120Ω ↓ ↓	↓
22	1	220K	22Ω ↓ ↓	↓
21	1	RC20GF100K	10Ω 1/2W 10%	AB
20	1	RN60D2001F	2K 1/4W 1%	CORNING
19	1	RN60D1001F	1K 1/4W 1%	CORNING
18	1	RC07GF223K	22K 1/4W 10%	AB
17	1	391K	390Ω ↓ ↓	↓
16	2	103K	10K	
15	5	682K	6.8K	
14	9	472K	4.7K	
13	7	332K	3.3K	
12	2	222K	2.2K	
11	6	102K	1K	
10	2	471K	470Ω	
9	2	331K	330Ω	
8	2	221K	220Ω	
7	1	181K	180Ω	
6	1	101K	100Ω	
5	2	220K	22Ω	
4	1	100K	10Ω ↓ ↓	↓
3	1	RC07GF3R3K	RESISTOR 3.3Ω 1/4W 10%	AB
2	1	B1832	HEAT SINK	FEC
1	1	ND1082A	PC BOARD	FEC
ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR

Figure 7-2. Parts List