

INSTRUCTION MANUAL

DOVETRON MPC-1000CR/T MARK II

REGENERATIVE TEMPEST

RTTY TERMINAL UNIT

E SERIES

MULTIPATH CORRECTION

SIGNAL REGENERATION - SPEED CONVERSION

THE CONTENTS OF THIS MANUAL AND THE ATTACHED PRINTS ARE PROPRIETARY TO DOVETRON AND ARE PROVIDED FOR THE USER'S CONVENIENCE ONLY. NO PERMISSION, EXPRESSED OR IMPLIED, IS GIVEN FOR COMMERCIAL EXPLOITATION OF THE CONTENTS OF THIS MANUAL AND/OR THE ATTACHED PRINTS AND DRAWINGS.

DOVETRON † 627 Fremont Avenue
So. Pasadena, California, 91030
† P O Box 267 †† 213-682-3705 †

CONTENTS

MPC-1000CR/T MARK II REGENERATIVE RTTY TERMINAL UNIT

<u>SECTION</u>	<u>PAGE</u>
DESCRIPTION	1
DOCUMENTATION	2
TSR-200D SIGNAL REGENERATION ASSEMBLY	2
DUAL CRYSTAL-CONTROLLED CLOCK	4
BILATERAL STEERING CIRCUIT	6
UART PROGRAMMING	6
UART OPTIONS	7
TEST POINTS	8
TEMPEST MAIN BOARD	9
MAIN BOARD JUMPERS	10
POWER/LOGIC CABLE	11
MAIN BOARD TO BBP-100 CONNECTIONS	12
OPERATION	13
OTHER VARIATIONS	13
DATA OUTPUT INFORMATION	14
EXTERNAL TUNING INDICATOR (J9-J10)	15
DUAL DIVERSITY OPERATION (J11-J12)	15
STORAGE	16
RESHIPMENT	17
PARTS LIST ADDENDUM	18

* * *

MPC-1000CR/T MARK II TEMPEST REGENERATIVE

RTTY TERMINAL UNIT

DESCRIPTION

The MPC-1000CR/T Mark II Tempest RTTY Terminal Unit is a variation of the MPC-1000T Tempest unit (complete with BBP-100 Binary Bit Processor and SSD-100 Solid State Cross Display) to which a Dovetron TSR-200D Signal Regeneration assembly (Dovetron P/N 75172, Rev 2) has been added to provide signal regeneration and speed conversion, which significantly reduces error rate.

In addition, the MPC-1000CR/T (II) contains four additional BNC coaxial connectors on the rear panel.

Two of these connectors permit interconnecting two or more MPC-1000CR/T (II) units for Dual Diversity operation.

The second pair of BNC connectors provides for the use of an external oscilloscope, which may be used as an external or remote tuning indicator and/or for signal analysis.

The instruction manual for the MPC-1000CR/T (II) consists of the MPC-1000T manual (Issue 3, July 1982) and this section, which details the TSR-200D Signal Regeneration assembly.

In case of conflict between the CR/T and T sections of this manual, the information provided in this section takes precedence.

DOCUMENTATION

Eight prints are supplied with the MPC-1000CR/T Mark II:

- 1) 75100 Assembly, Main Board, E-Series (MPC-1000).
- 2) 75103 Schematic, Main Board, E-Series (MPC-1000).
- 3) 75103CR/T Schematic Addendum, E-Series, Mark II.
- 4) 75164 Schematic, TSR-200D Signal Regenerator.
- 5) 75171 Assembly, TSR-200D Signal Regenerator.
- 6) 75192 Assembly, BBP-100 Binary Bit Processor.
- 7) 75195 Schematic, BBP-100 Binary Bit Processor.
- 8) 75307 Assembly/Schematic, SSD-100 Display Board.

TSR-200D REGENERATION ASSEMBLY

The MPC-1000CR/T (II) contains a standard Dovetron TSR-200D assembly, Dovetron P/N 75172, Rev 2. (See Paragraph 3 below.)

The Signal Regeneration section of the TSR-200D regenerates the incoming signal to a bias distortion of less than 0.5%, significantly improving the error rate on weak signals and on signals that have been smeared by multipath distortion, i.e., apparent pulse stretching.

When installed in an MPC-1000CR/T (II), the 12 ohm resistor (essentially a jumper) on the TSR-200D board is moved from location R55 to location R54, which bypasses an inverter section of Z3 (pins 8, 9 and 10).

This inverter section normally is used to invert an EIA input

(Mark-negative, Space-positive) to a TTL configuration (Mark-high, Space-low), compatible with the TSR's input.

When used in a CR/T Tempest unit, this inversion is not necessary, since it is anticipated that polar inputs will conform to MIL STD 188C (Mark-positive, Space-negative).

If an EIA (RS 232C) polar input is to be used, remove R54 and replace R55 with a jumper or a 12 ohm resistor.

Since the front panel of the MPC-1000CR/T contains a REGEN ON-OFF switch, the REGEN ON-OFF slide switch S4 on the TSR-200D should always be left in the ON (forward) position.

The speed conversion (SPEED CONVERT) switch S5 will normally also be left in the ON (forward) position, but may be set to the OFF position, depending on the operator's requirements.

Signal Regeneration and Speed Conversion are accomplished by an Intersil IM6402 CMOS UART (Universal Asynchronous Receiver-Transmitter) 40 pin integrated circuit.

This UART is a dual chip. One half is a serial-parallel converter and the other half is a parallel-serial converter.

When used in Half Duplex operation, both the incoming and outgoing signals are processed thru the UART. Since the TSR-200D is a Half Duplex device, it must be switched between Transmit and Receive by the front panel Send-Receive switch or by the

rear panel remote LOCK line.

Although both sides of this UART are programmed simultaneously by the UART Program Switch S3, they have separate clock input ports. When a single clock is used at both ports, straight-thru regeneration is achieved, i.e., no change in baud rate.

If the Speed Conversion Switch S5 is set to ON, the two sides of the UART can be clocked at different baud rates, providing up/down Speed Conversion.

Since the UART contains only a single character of Memory, the Output Clock (Loop) should always be set as fast or faster than the Input Clock to prevent character over-runs.

Speed Conversion is convenient if the local teleprinter is set for 100 WPM, because the front panel switch may be used to select slower incoming baud rates, which will be up-converted by the UART to 100 WPM. The UART in this mode of operation is an effective electronic gear shift.

DUAL CRYSTAL-CONTROLLED CLOCK

The Dual Clock circuitry consists of a CMOS oscillator (Z1) and a very low frequency crystal (60.000KHz), whose output is divided by two identical frequency dividers: Z7/Z8 and Z9/Z10.

When the Speed Convert switch (S5) on the TSR-200D assembly is OFF, both sides of the UART regenerator are driven by the output of Clock 1 Divider, which is controlled by the front panel

Signal Speed select switch.

If this switch is set to 75 baud, an incoming signal will be processed thru the UART at 75 baud.

If the Speed Convert switch is set to ON, the Signal Speed switch will select the input baud rate (baud rate of the incoming signal) and the 8-pole DIP switch (S2) will select the baud rate at which the regenerated signal will be clocked out of the UART and sent to the local teleprinter.

This output clock may be programmed for baud rates from 37.5 baud to 3750 baud. Poles 1 thru 4 represent the Most Significant Digit (MSD) and Poles 5 thru 8 represent the Least Significant Digit (LSD). The BCD weight of each switch pole is etched on the PC board just below the switch.

Assuming that the local teleprinter is geared for 100 WPM (74.2 or 75 baud operation), S2 must be programmed for 75 Baud operation, i.e., S2 set for a BCD number of 50.

To determine the proper divisor number for a baud rate, use the following formulae:

- 1) BAUD RATE X 16 = CLOCK FREQUENCY (HZ).
- 2) 60,000/CLOCK FREQUENCY = DIVISOR.

Example: 75 Baud X 16 = 1200 Hz. $\frac{60,000}{1200} = 50.$

Therefore, if S2 is programmed with a divisor (BCD number) 50, the frequency dividers of Clock 2 will divide the 60.000 KHz

oscillator signal down to 1200 Hz, and the UART will output the regenerated signal at 75 Bauds.

BILATERAL STEERING CIRCUIT

When used in the Half-Duplex mode, the two clocks are inverted when the terminal unit is switched between Receive and Send, which permits effective Speed Conversion of both incoming and outgoing signals. If the UART is up-converting in Receive, it will be down-converting in Send.

This switching of Input and Output ports of the UART and the automatic inversion of the two clocks is accomplished by the Bilateral Steering Circuit, which consists of Z3, Z4, Z5 and Z6.

UART PROGRAMMING

The UART may be programmed for various code levels and functions.

Assuming that the MPC-1000CR is to be used for Radio TTY communications with the 5 level Baudot (Murray) code, program the UART via the 8-pole DIP switch at S3:

<u>SWITCH POLE</u>	<u>FUNCTION</u>	<u>MODE</u>	<u>SWITCH POSITION</u>
8	EPS	ZERO	LEFT
7	SBR	NO	LEFT
6	NB1	ZERO	LEFT
5	NB2	ZERO	LEFT
4	TSB	ONE	LEFT
3	ASBS	OFF	RIGHT
2	PARITY	NO	LEFT
1	FSK	EIA	LEFT

If other coding is desired, the UART may be re-programmed per the coding charts on the TSR-200D Schematic Print 75164.

UART OPTIONS

STOP BIT REQUIRED (SBR): Normally it is best to leave this function in the NO position. There is no reason to force the UART to dump a good character just because the Stop Bit was not detected on the incoming signal. Since all languages are highly redundant in structure, it is always better to print a character, even if it is wrong. The precise Stop Bit generated at the end of each regenerated character will prevent the local teleprinter from losing signal synchronization.

TOTAL STOP BITS (TSB): The UART offers the option of attaching a 1.0 or 1.5 Character Unit stop bit to the end of the regenerated character. Selecting a 1.0 CU stop bit guarantees no character over-runs with Baudot teleprinters operating with 7.0, 7.42 and 7.5 CU coding.

PARITY & EPS: Baudot Coding does not require Parity, so Pole 2 of the UART Program Switch should be set to NO (LEFT). With Parity set to NO, ESP has no function, so Pole 8 can be left in either position.

AUTOMATIC STOP BIT SELECT (ASBS): With TSB (above) set for a 1.0 CU, and ASBS set to ON, the TSR-200D will Receive with a single stop bit added to each character (1.0 CU), but will TRANSMIT with a 1.5 CU Stop Bit on the end of each character.

TEST POINTS

Seven Test Points have been provided on the TSR-200D assembly to assist in rapid signal tracing and trouble shooting:

TP-1: CRYSTAL OSCILLATOR OUTPUT

The oscillator circuit is comprised of a Statek quartz crystal, sealed in a gold-plated TO-5 type can and a CMOS 14007 DIP package. It is not unusual for this type of oscillator to take up to four seconds to start oscillating after initial turn-on. The nominal frequency of this crystal is 60.000 KHz \pm 0.05%.

TP-2: CLOCK 1 OUTPUT

The frequency at TP-2 is the 60 KHz clock divided by the Signal Speed Select dividers (Z7 and Z8). If the Signal Speed switch (S1) is set for a division of 82 (45.45 Baud), the output frequency will be $60,000/82 = 732$ Hz.

TP-3: CLOCK 2 OUTPUT

The frequency at TP-3 is the 60 KHz clock divided by the Loop Speed Select dividers (Z9 and Z10). If the Loop Speed Switch (S2) is set for a division of 50 (74.2/75 Baud), the output frequency will be $60,000/50 = 1200$ Hz.

TP-4: UART INPUT CLOCK

The frequency at TP-4 is the Input Clock to the UART at the output of the bilateral steering section. In Receive, it is Clock 1 and in Transmit, it is Clock 2.

TP-5: UART OUTPUT CLOCK

The frequency at TP-5 is the Output Clock to the UART at the output of the bilateral steering section. In Receive, it is Clock 2 and in Transmit, it is Clock 1.

TP-6: UART DATA INPUT

This test point is the same as Pin 20 on the UART, which is the DATA INPUT port. In Receive, it contains the unregenerated signal from Q6 (loop driver) in the MPC, and in Transmit, it contains the unregenerated signal as originated at the local teleprinter, TD, etc.

TP-7: UART DATA OUTPUT

This test point is the same as Pin 25 on the UART, which is the DATA OUTPUT port. In Receive, it contains the regenerated (and possibly speed-converted) data signal that is routed to the high level keyers. In Transmit, it contains the regenerated signal as generated by the local teleprinter.

TEMPEST MAIN BOARD

When the MPC-1000T is configured as an MPC-1000CR/T (II) with

a TSR-200D assembly, the main board is slightly modified at the time of production.

These modifications consist of:

- 1) Removing the white/brown wire between E-Point 00 and the Standby section of front panel switch S7.
- 2) Removal of jumper between points B and C in middle-center of the main board.
- 3) Removal of the blue wire between the E-56 (mainboard) and E-56 on the BBP-100 Binary Bit Processor board.
- 4) Installation of two jumper wires on the main board of the MPC-1000CR/T.
- 5) Installation of a power/logic cable that interconnects the TSR-200D Regeneration Assembly with the mainboard.

MPC-1000CR/T MAINBOARD JUMPERS

- 1) Remove the buss-bar jumper between B and C (See item number 2 above).
- 2) Remove the white/Brown wire between the Standby switch (S7) and E-Point 00.
- 3) Install a six inch brown/white wire between the Standby switch (S7) and Point C.
- 4) Install a green wire between E-Point E35 on the main

board and the center lug of the front panel REGEN ON-OFF switch.

- 5) Install a TSR-200D Power/Logic cable, P/N CA9130.

TSR-200D POWER/LOGIC CABLE INSTALLATION

Install the CA9130 cable to the following mainboard locations:

- 1) Brown wire to the lower lug of the front panel REGEN ON-OFF switch.
- 2) Red wire to E-Point E46 in left front corner of mainboard. This is system ground.
- 3) Orange wire: Cut off. Do not use.
- 4) Yellow wire to the $\emptyset\emptyset$ E-Point in the right front corner of the mainboard. Two $\emptyset\emptyset$ points are available and either is acceptable.
- 5) Green wire: Cut off. Do not use.
- 6) Blue wire is connected to the anode of the CR54 location in the right front of the mainboard. Diode CR54 is not installed on the board. When making this connection be sure to select the anode location, which is to the far right of the diode location.
- 7) Violet wire is installed on the mainboard at a location just to the left of the center line of the mainboard.

This location is the upper right-most location of a three-hole pattern that is located just to the right of a transistor (Q5) location. This location can be easily identified in that it has a trace that runs to the right to a feed-thru hole just to the left of an empty transistor location at Q7.

- 8) Gray wire: Cut off. Do not use.
- 9) White wire: Cut off. Do not use.
- 10) Black wire: Cut off. Do not use.
- 11) White/brown wire is installed in the -V location just to the right of op-amp location Z19 in left front part of mainboard. This is the -15 volt regulated line.
- 12) White/red wire is installed in the +V location just right of op-amp location Z19 in the left front part of mainboard. This is the +15 volt regulated line.
- 13) White/orange wire: Cut off. Do not use.
- 14) White/yellow wire: Cut off. Do not use.

MAINBOARD TO BBP-100 CONNECTION

Connect a violet wire between the upper lug of the front panel REGEN ON-OFF switch and TP17 on the BBP-100 Binary Bit Processor board. This location (TP17) is located in the right-front of

the BBP board and just to the left of Op-amp 71. This location (TP17) is the same as E56 on the BBP board, but is more conveniently located for this installation.

OPERATION

The TSR-200D Regeneration Assembly is a Half-Duplex device. When operated in Half-Duplex mode, both incoming and outgoing signals are regenerated (and speed converted if necessary), depending on the location of the front panel REC-SEND switch S7. (NOTE: On the MPC-1000T, S7 is designated as ON-STANDBY. On the MPC-1000CR/T (II), S7 is designated as RECEIVE-SEND, inferring the Half-Duplex role of the TSR-200D assembly.)

When operating in Full-Duplex, switch S7 is normally left in the REC (Receive) position and the AFSK tone keyer in the MPC-1000CR/T (II) is driven directly by the MIL STD 188C Polar Input at the rear panel. In Full-Duplex operation, the polar input signals are not regenerated or speed converted by the TSR-200D.

In Half-Duplex, with the S7 switch in SEND, the polar input signals are regenerated and speed converted thru the TSR-200D assembly.

OTHER VARIATIONS

The Mark and Space VFO potentiometers (R145A and R147A) have been replaced with 2500 ohm units (which replace the 2000 ohm

units in the MPC-1000T), and permit the MPC-1000CR/T to tune input frequencies from 1000 Hz to 3000 Hz.

The front panel calibration markings of the Mark and Space VFOs have been changed to reflect this expanded range of input tones.

All other specifications of the MPC-1000T apply to the MPC-1000CR/T Mark II RTTY Terminal Unit.

CAUTION - HIGH VOLTAGE

The EMI-RFI filter in the MPC-1000T and MPC-1000CR/T "charges" in normal operation and can provide a stored voltage when the unit is turned off and the power cord is disconnected. When servicing the Tempest Series terminal units, it is a good idea to alleviate this shock hazard by discharging both sides of the EMI-RFI filter to ground at the filter outputs A and C. Point B is chassis ground.

DATA OUTPUT INFORMATION

The MPC-1000T TEMPEST terminal unit provides simultaneous MIL STD 188C and EIA RS232C FSK outputs.

The MPC-1000CR/T (II) TEMPEST terminal unit provides simultaneous MIL and EIA outputs ONLY when operated in the REGEN OFF mode.

Pole 1 of the UART Program Switch (S3) on the TSR-200D Assembly establishes the regenerating mode of the terminal unit.

When Pole 1 is set for MIL, the MIL FSK output is regenerated

if the front panel REGEN ON-OFF switch is in the ON position.
The selected Signal Sense is automatically maintained when the
REGEN switch is moved between ON and OFF.

For regenerated EIA operation, Pole 1 must be set to the EIA position and Signal Sense must be manually reversed by the front panel NORMAL-REVERSE switch when switching between REGEN ON and REGEN OFF.

In other words, REGENERATED MIL and EIA FSK outputs are not available simultaneously and are dependent upon the setting of Pole 1 of the UART Program Switch (S3) on the TSR-200D Regeneration assembly.

EXTERNAL TUNING INDICATOR

The output of the buffer amplifiers (Z13 and Z21) on the mainboard is available at the rear panel connectors J9 and J10, and may be used to drive either an external dual-trace oscilloscope for signal analysis, or an external/remote tuning display. These output lines are isolated by 100K resistors (R37 and R62) on the mainboard, which provide a good degree of voltage isolation between the external device and the terminal unit.

DUAL DIVERSITY OPERATION

Two or more MPC-1000CR/T (II) Terminal Units may be interconnected for dual diversity operation by jumpering the External Diversity connectors (J11-Space and J12-Mark) together, MARK to

MARK, and SPACE to SPACE.

All Diversity combining is accomplished within the interconnected terminal units and an external diversity combiner is not required.

When operating in the Diversity mode, the interconnected terminal units are operated with their Mode switches in the MS position. Switching any terminal unit to the DIV OFF position, disconnects the diversity cables of that terminal unit, permitting it to be operated independently of the other(s).

STORAGE

As shipped by Dovetron, the MPC-1000CR/T (II) is sealed within a plastic bag and supported within the shipping container by shock-absorbing plastic end caps. The detachable power cable is also sealed within this plastic bag. Both the connector on the power cable and on the rear panel of the terminal unit are protected by separate plastic caps. The Instruction manual and prints are sealed in a separate plastic bag, and then enclosed in a large heavy duty paper envelope to protect the plastic bag from tears and abrasion. Storage in this manner will protect the terminal unit from deterioration for periods as long as five years.

If the plastic bags have been opened, they can be resealed with a bag sealer or taped tightly closed.

RESHIPMENT

The shipping carton for the MPC-1000CR/T (II) has been carefully designed to protect the terminal unit and its accessories from damage during shipment. This carton and its associated packing materials should be used to reship the terminal unit.

If the original shipping carton is not available, be sure to carefully pack each unit SEPARATELY, using suitable cushioning material where necessary. Very special attention should be given to providing enough packing material around controls, connectors, and other protrusions from the terminal unit. Rigid cardboard should be placed at the corners of the equipment to protect against denting and bending.

When returning a unit for repair, ship via either AIR PARCEL POST or UPS BLUE (AIR) to:

DOVETRON, INC.
627 Fremont Avenue
South Pasadena, CA 91030
U.S.A.

PARTS LIST ADDENDUM

MPC-1000CR/T MARK II

Added to Mainboard:

1 each	Cable, Power/Logic	CA9130	Circuit Assy
--------	--------------------	--------	--------------

Added to Front Panel:

1 each	Switch, Speed	5P9958	C.T.S.
1 each	Knob, Small	S1647	Kurz-Kasch
1 each	Cable, Speed, Short	CA9131-01	Circuit Assy
1 each	Switch, Toggle, DPDT	MTA-206N	Alco

Added to Rear Panel:

4 each	Connectors, BNC (J9-J12)	31-221	Amphenol
--------	--------------------------	--------	----------

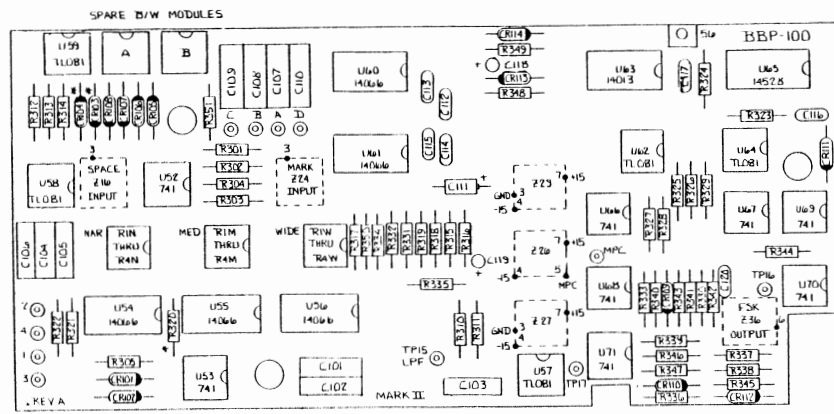
TSR-200D Signal Regeneration Assembly

(Dovetron P/N 75171-2)

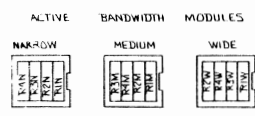
1	1	P. C. Board, TSR-200D	75172-2	Dovetron
2	C3, C4	Capacitor, 5 Pfd	CM06	Elmenco
3	C7	Capacitor, .001 Mfd	Ceramic	Dilectron
4	C1	Capacitor, 0.01 Mfd	Ceramic	Dilectron
5	C2, 5, 6, 8, 9	Capacitor, 10 Mfd, 35Vdc	Tantalum	I.T.T.
6	CR2-7, 8, 9, 11, 12, 13	Diode, Silicon, Power	1N4007	Motorola
7	CR1, 10	Diode, Zener, 5.1V	1N751A	Motorola
8	Q1	Transistor, NPN, Sil	2N2219A	Motorola
9	R35, 54	Resistor, 1/4W, 5% C.F.	12 ohms	R-Ohm
10	R30, 33, 44, 48, 56	Resistor, 1/4W, 5% C.F.	100K	R-Ohm

13	R43	Resistor, 1/4W, 5% C.F.	2K	R-Ohm
14	R36	Resistor, 1/4W, 5% C.F.	4.7K	R-Ohm
15	R1-16, 20, 28, 31, 32, 34, 39, 40, 41, 45-47, 49, 50	Resistor, 1/4W, 5% C.F.	10K	R-Ohm
16	R21	Resistor, 1/4W, 5% C.F.	150K	R-Ohm
17	R18	Resistor, 1/4W, 5% C.F.	330K	R-Ohm
18	R19	Resistor, 1/4W, 5% C.F.	470K	R-Ohm
19	R17	Resistor, 1/4W, 5% C.F.	22Meg	R-Ohm
20	R22-26	Resistor, 1/4W, 5% C.F.	910 Ω	R-Ohm
21	Z11	I.C., CMOS	14000	Motorola
22	Z3-6, 12	I.C., CMOS	14011	R.C.A.
23	Z7-10	I.C., CMOS	14522	Motorola
24	Z1	I.C., CMOS	CD4007AE	R.C.A.
25	Z2	I.C., UART, CMOS	IM6402	Intersil
26	S4, S5	Switch, P.C. DPDT	C56206L2	Switchcraft
27	S2, S3	Switch, 8PST, DIP	SL1008	Cont. Sw.
28	Y1	Crystal, 60.0000KHz	SX-1V60KHz	Statek
29	R53	Pot, P.C. Horizontal, 250K	3355U-1	Bourns
30	R51	Pot, P.C. Horizontal, 5MEG	3355U-1	Bourns
31	Z13	I.C., Op-Amp, 8 pin, minidip	μ A741	Signetics

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	UPDATE TO MARK II	8-8-80	P&C



CONSULT PRINT 75195 FOR RESISTOR VALUES OF THE SELECTABLE BANDWIDTH MODULES REGARDING THE VARIOUS BAND RATES.



QTY	W	CA	DESCRIPTION	VALUES	VALUES	VALUES	VALUES	VALUES	VALUES
36	1	CA-08PF-11	24, 24, 24, 27	29, 30	HEADER, 5 PIN				CIRC. ASSY.
35	5	CA-08P-11			BANDWIDTH MODULES				CIRC. ASSY.
51	8	u741	U52, 53	66-71	INTEGRATED CIRCUIT				TEX. INST.
33	1	1452B	U65						MOTOROLA
32	5	TLO81	U57-59, 62, 64						TEX. INST.
31	5	14066	U54-56, 60, 61						MOTOROLA
30	1	14083	U63		INTEGRATED CIRCUIT				MOTOROLA
29									
28									
27	5	METAL FILM	R312, 313, 325	326, 331	RESISTOR, 20K, 1%				DALE
26	2	CARB CLAMP	R317, 350						TRW
25	2	CARB FILM	R 327, 338		150 K				R-OHM
24	3		R323, 324, 351*		100K				
23	4		R315, 316, 318	319, 349, 347	47 K				
22	1		R332		4.7K				
21	17		R305, 311, 314	320*, 321, 322	20K				
			327-330, 335	336, 333, 340					
			342, 344, 351						
20	8		R301-304	333, 341, 345	5K				
			346						
19	1		R354		1K				
18	3	CARB FILM	R310, 348, 349		RESISTOR 470Ω, 14W, 5%				R-OHM
17									
16									
15									
14	10	1N514B	CR101, 102, 105, 112		DIODE, SIGNAL, SIL.				IRC
13	2	1N755A	CR113, 114		DIODE, ZENER, 7.5V				ITT
12									
11									
10	3	MYLAR	C101, 103, 104		CAPACITOR, 4700μF				PLESSEY
9	1	MICA	C106		2400μF				C.D.
8	1		C105		2000μF				C.D.
7	1		C102		390μF				C.D.
6	2	TANTALUM	C118, 119		10μF/16V				ITT-TAP
5	1	TANTALUM	C 111		1.0μF				SPRAGUE
4	4	MYLAR	C107-110		0.1μF				PLESSEY
3	7	CER DISC	C112-117, 120		CAPACITOR, 0.01μF				DIELECTRON
2									
1	1	75195	BBP-100		BOARD				DOVETRON
ITEM	QTY	PART NO.	REF DES	DESCRIPTION	REC MANUFACTURER				

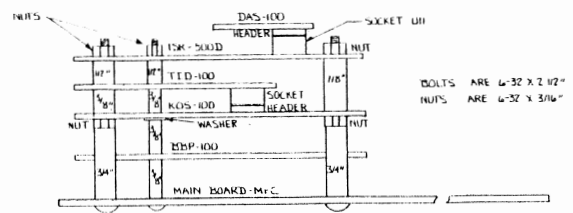
MECHANICAL INSTALLATION OF BBP 100
IN KOS-EQUIPPED MPC-1000R

MPC-1000T BANDWIDTH MODULES			
LOCATION	BAND RATE	WPM	RESISTANCE
NARROW	50.0	67	750K
MEDIUM	75.0	100	510K
WIDE	150.0	200	240K
A	95.45	60	820K
B	110	100	ASCII 330K

STANDARD BANDWIDTH MODULES			
LOCATION	BAND RATE	WPM	RESISTANCE
NARROW	45.45	60	820K
MEDIUM	50.0	67	750K
WIDE	75.0	100	510K
A	95.88	75	680K
B	110	100	ASCII 530K

NOTE: IN MPC-1000T TEMPEST UNITS ONLY, CONNECT BBP-56 TO BLUE WIRE INSTALLED IN E56 ON MAINBOARD.

NOTE: THE INVERTED FSK OUTPUT OF U71 AT BBP-56 IS NOT USED. U71 MAY BE CONSIDERED AS A SPARE OP-AMP AND THE INVERTED FSK OUTPUT MAY BE UTILIZED FOR OTHER APPLICATIONS.



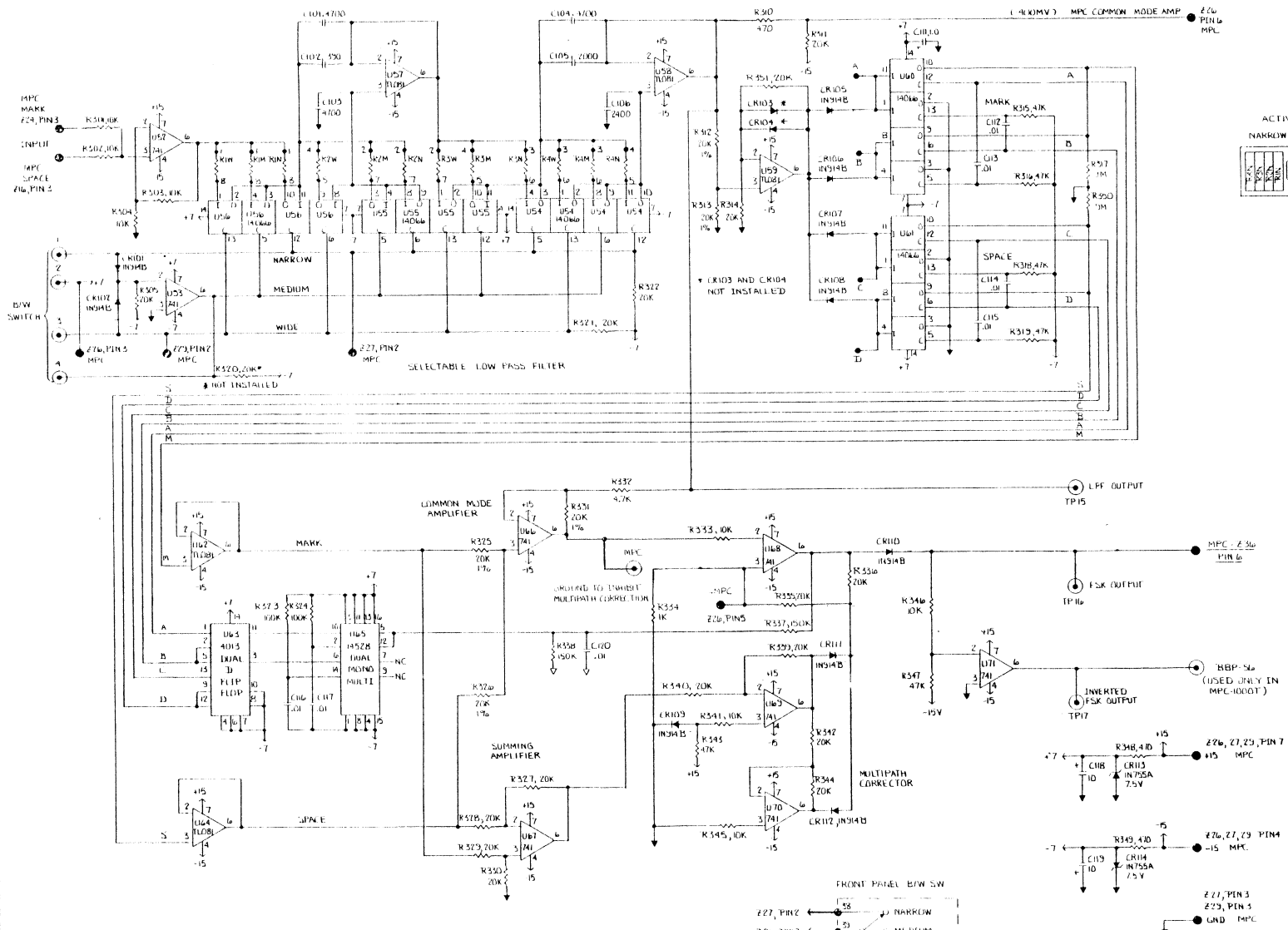
NOTE: TOP COVER OF DAS-100 IS NOT INSTALLED. SEE NOTE 2 ON PRINT 75174.

MARK II

THIS DOCUMENT CONTAINS PROPRIETARY AND CONFIDENTIAL INFORMATION, WHICH SHALL NOT BE REPRODUCED OR TRANSMITTED TO OTHERS OR TO OTHER DOCUMENTS, IN WHOLE OR IN PART, OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION FROM DOVETRON, INC.

PARTS LIST		ASSEMBLY - BBP-100	
ITEM	QTY	SCALE	SIZE
		2:1	D
			75192 A
		DO NOT SCALE DRAWING SHEET 1 OF 1	

REV.	DESCRIPTION	DATE	APPROVED
A	UPDATE TO MARK II	8-8-80	[Signature]



LOW PASS FILTER SELECTION GUIDE

BAUD RATE = BANDWIDTH

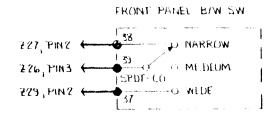
BAUD RATE	RESISTANCE	COLOR CODE	MARK	MODELS
45.45	820K	BRN-RED-YEL	X	X
50.00	750K	RED-GRN-YEL	X	Y
56.25	680K	BLU-GRN-YEL	X	X
64.00	510K	GRN-BRN-YEL	X	X
75.00	510K	GRN-BRN-YEL	X	X
100.0	300K	GRN-BLU-YEL	X	X
110.0	330K	GRN-GRN-YEL	X	X
150.0	240K	RED-YEL-YEL	X	X
200.0	150K	BRN-GRN-YEL	X	X
300.0	62K	BLU-RED-GRN	X	X

MPC SERIES TERMINAL UNITS ARE NORMALLY SUPPLIED WITH CHANNEL FILTERS. FOR 45.45 TO 75.0 BAUD OPERATIONS, THE MPC-1000T TERMPST IS NORMALLY SUPPLIED WITH 150 BAUD CHANNEL FILTERS.

WHEN BBP-100 IS INSTALLED IN MPC-1000T TERMPST, REPLACE CR27 WITH A JUMPER, CONNECT BBP-56 TO MPC-56, JUMPER MPC-B TO MPC-C UNDER CRT SHIELD.

- NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS.
 2. ALL CAPACITORS ARE μF.
 3. ● TEST POINTS & E POINTS.
 4. ● SOCKET PIN IN HEADER TO INTERCONNECT TO MPC SERIES MAIN BOARD.
 5. ✖ COMPONENTS NOT INSTALLED.

THIS DOCUMENT CONTAINS PROPRIETARY AND CONFIDENTIAL INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSMITTED TO OTHERS OR TO OTHER DOCUMENTS, IN WHOLE OR IN PART, OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION FROM LOVETRON, INC.



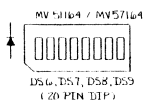
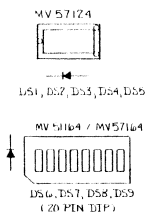
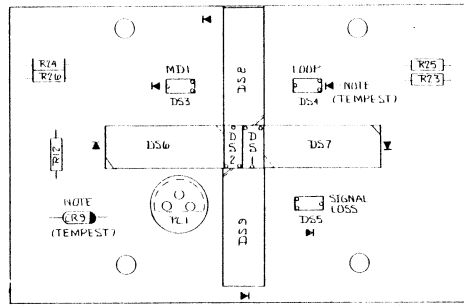
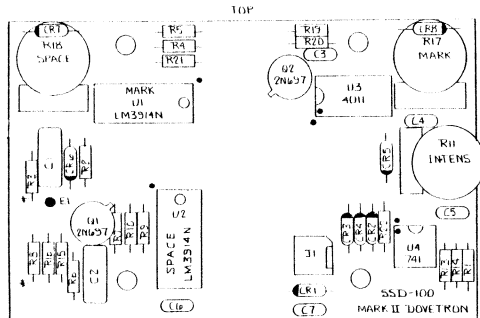
MARK II

DESIGNED BY	DATE	SIZE	DRAWING NO.
APPROVED BY	DATE	SCALE	REV.
		BBP-100 BINARY BIT PROCESSOR SCHEMATIC	
DO NOT SCALE DRAWING		SHEET 1 OF 1	

- TEMPEST -

NOTE: REVERSE POLARITY OF DS4 (LOOP LED) AND INSTALL 150HMCR27 IN PLACE OF CR9 FOR USE IN MPC-1000T.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



COMPONENTS - SSD-100K RETROFIT KIT

QTY	PART NO.	DESCRIPTION	REVISIONS	DATE	APPROVED
11	4	HHS 85021	SPACER, 1/32 X 1/2 INCH		HHS SMITH
10	1	LM-V8	CLAMP, CABLE, NYLON		ICD-RALLY
9	1	KMW-401	WASHER, FLAT NO. 4		WALDOM
8	2	CARB FILM	MPC R222		BEYSCHLAG
7	1	TLOB1CP	OP-AMP, 8 PIN MINI DIP		TEX. INST.
6	1	CARB FILM	MPC-R114		BEYSCHLAG
5	8	HHS-9291	NUT, 1/32 X 3/16 INCH		DOVETRON
4	4		BOLT, 1/32 X 1 1/2 INCH		DOVETRON
3	1	S08P82-246-10-012	E TA CODING		C.A.
2	1	75203	SSD BEZEL WITH OPTICAL FILTER		DOVETRON
1	1	75305	SSD-100		DOVETRON

COMPONENTS - SSD100 ASSEMBLY

QTY	PART NO.	DESCRIPTION	REVISIONS	DATE	APPROVED	
30	5	MV57124	DS1, 2, 3, 4, 5		GEN. INST.	
25	4	MV57164 / MV57164	DS 6, 7, 8, 9		GEN. INST.	
28	4	IN514B	CR5, 6, 7, 8		DIODE, SIGNAL	
27	4	IN4007	CR1, 2, 3, 4		DIODE, POWER	
26	5	S-LFS-B	SOCKET, TRANSISTOR		TRW	
25	2	2N697 2N2219A	Q1, Q2		TRANSISTOR	
24	4	CA-105-TSD	SOCKET, DIP, 20PIN		C.A.	
23	1	u741	U4		INTEGRATED CIRCUIT	
22	1	14011	U3		INTEGRATED CIRCUIT	
21	2	LM3394N	U1, U2		INTEGRATED CIRCUIT	
20	5	02S1-10NW	SOCKET, SIP, 2 PIN		C.A.	
19	1	VT8411	PC1		PHOTOCELL	
18	1	09-010-1183			FILTER, EMI (TEMPEST)	
17	3	5355U-1	R11, 17, 18		POT, 500K	
16	1	IN751A	CR9		DIODE, ZENER, 5.1VDC	
15	2	CARB FILM	R3, R8		RESISTOR, TBD	
14	2		R1, 6		1M, 1/4W, 5%	
13	3		R3, 23, 24		30K	
12	2		R25, 26		20K	
11	5		R12, 14, 15		4.7K	
10	2		R9, 10		7.5K	
9	2		R2, 7		2.7K	
8	1		R16		2K	
7	4		R4, 9, 19, 20		1K	
6	3	CARB FILM	R21, 22, 27		RESISTOR, 150, 1/4W, 5%	
5						
4	2	MYLAR	C1, C2		CAPACITOR, .050 uF	
3	3	GER DISC	C3, C4, C5		CAPACITOR, .01 uF	
2	2	GER DISC	C6, C7		CAPACITOR, 270 pF	
1	1	75305			P.C. BOARD	
ITEM QTY	PART NO.	REF DES.	DESCRIPTION	REVISIONS	DATE	APPROVED

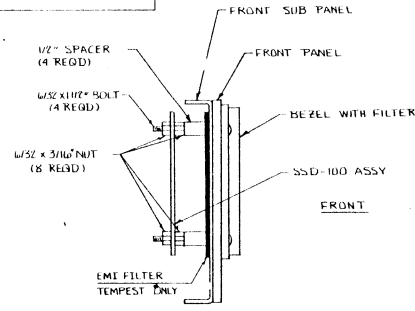
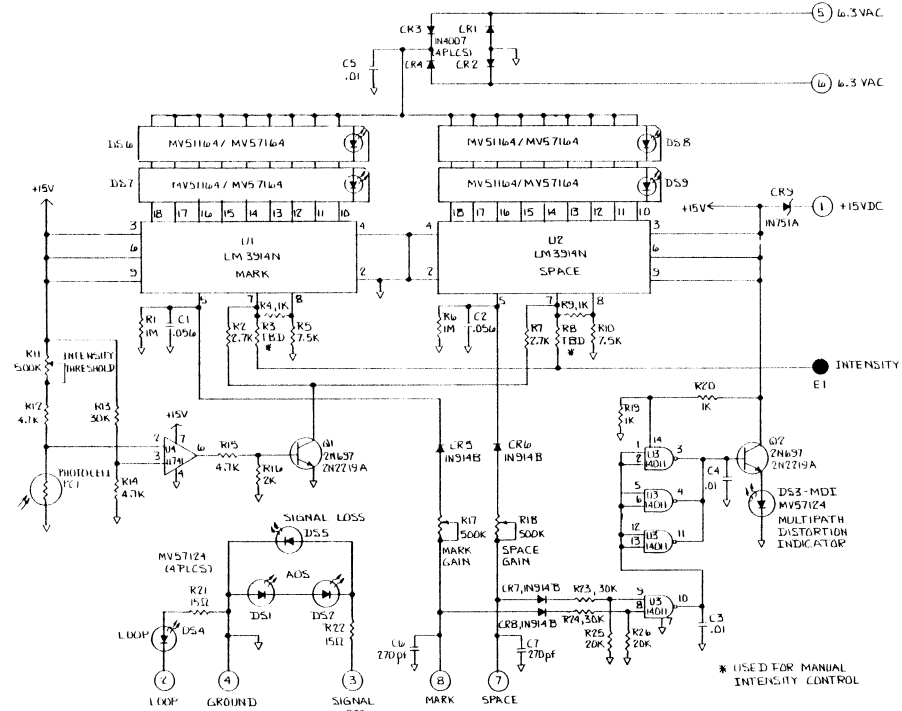


TABLE INSTALLATION IN MPC SERIES

QTY	PART NO.	DESCRIPTION
31		MPC MAIN BOARD LOCATION
1		MPC +V AT TP9
2		MPC JUMPER LOCATION C- REMOVE R176
3		JUNCTION OF R214 & R215- R214 NOT INSTALLED
4		MPC GROUND AT TP8
5		CRT FILAMENT E-POINT PIN I
6		CRT FILAMENT E-POINT PIN II
7		SPACE CHANNEL INPUT TO C64 (REMOVED)
8		MARK CHANNEL INPUT TO C63 (REMOVED)

NOTE: TO RETROFIT LRT WITH SSD-100K:
 1. REMOVE CR45, CR46, C63 & C64.
 2. CHANGE R14 TO 150K, 1/4W, 5%.
 3. CHANGE R37 TO TLOB1CP OP-AMP.
 4. CHANGE R176 & R222 TO 100K, 1/4W, 5%. CONSULT INSTALLATION INSTRUCTIONS FOR WIRING CHANGES ON MAIN BOARD.
 5. CONSULT SSD-100 CALIBRATION PROCEDURE FOR ADJUSTMENT OF MVS GAIN & INTENSITY THRESHOLD CONTROL.



* USED FOR MANUAL INTENSITY CONTROL

MARK II

THIS DOCUMENT CONTAINS PROPRIETARY AND CONFIDENTIAL INFORMATION, WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHERS OR TO OTHER DOCUMENTS IN WHOLE OR IN PART, OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION FROM DOVETRON, INC.

US PAT NO. 4,729,698

PARTS LIST			
DATE	14-72	SCALE	2:1
APPROVALS	DATE	SIZE	D
DESIGNED	DATE	DRAWING NO.	75307
CHECKED	DATE	D3 NOT SCALE DRAWING	SHEET 1 OF 1