PTTI RELATING TO THE VERDIN COMMUNICATIONS SYSTEM

by

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Abstract

VERDIN is the Navy's VLF system to replace the present FSK modulation on our VLF and on some of our LF broadcasts. The first installations are starting this week with completion planned for 1975.

The frequency range of VERDIN is between 14 and 60 kilohertz. VERDIN operates in one, two, or four 50-baud channel modes. VERDIN has a number of modulation types, CW and FSK which will be used for compatibility with our present broadcast during the period of conversion to the VERDIN system; compatible shift keying (CSK), which can be detected either for phase or frequency and minimum shift keying (MSK) which is the primary mode of modulation in the VERDIN system.

The block diagram of the transmit system (Figure 1) is simplified to show components of the VERDIN system. The control unit is the interface with the outside world. It sends messages in and out of a stored program processor which is a special purpose digital computer with a 4k, 3-microsecond memory. The rubidium frequency and time standard controls both the frequency and the time within the control unit. Comprising the receiver terminal are the stored program processor, the demodulator, a radio receiver, and a frequency/time standard (Figure 2). The radio receiver can be used as a general purpose VLF receiver or it can be used with the demodulator for detecting the MSK.

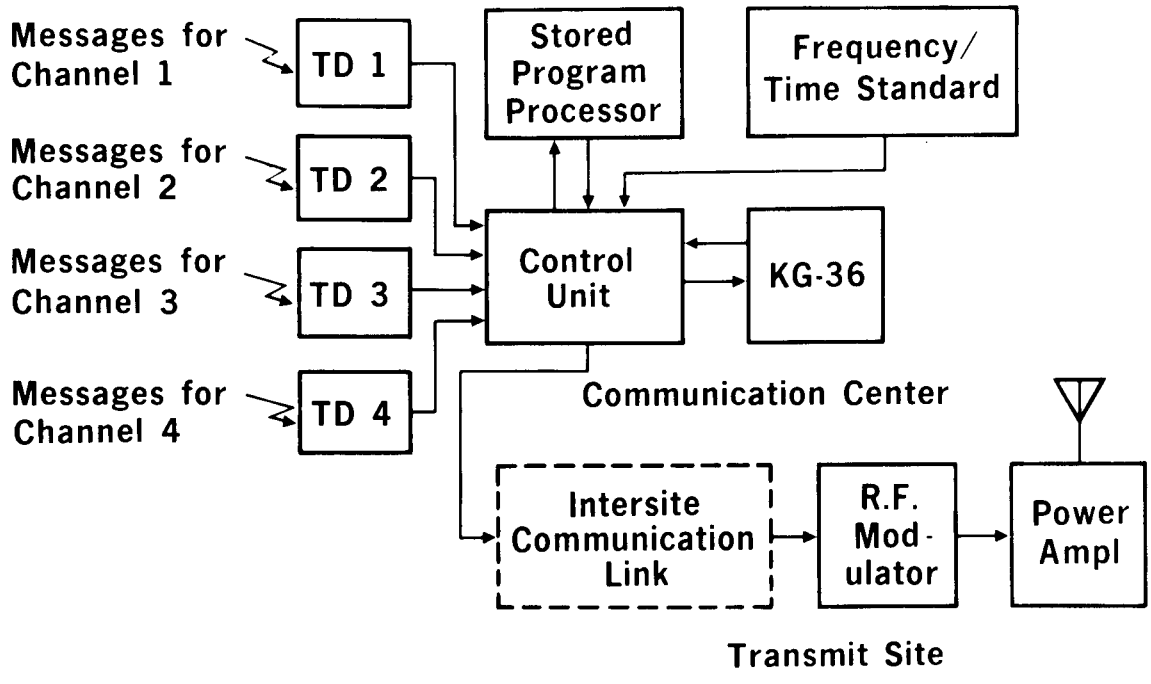

Figure 1. TRANSMIT SUBSYSTEM

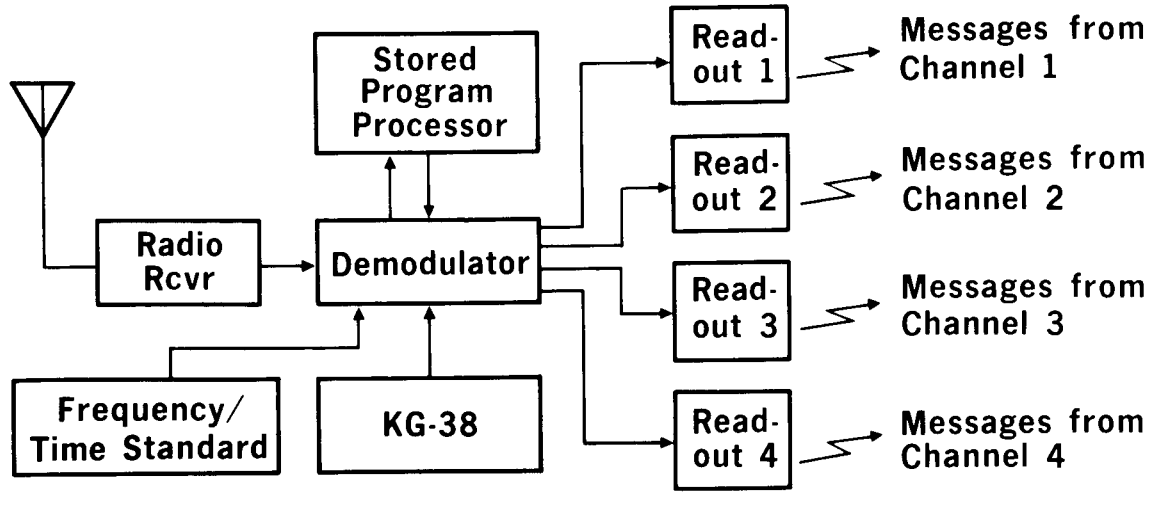

Figure 2. RECEIVE SUBSYSTEM

The stored program processor is used for synchronization and conversion of the output to a standard 7.0 low-level teletype code. Decryption is also done in the receiver terminal within the stored program processor. Again, the frequency and time standard provides accurate time within the system.

One of the main problems in a synchronous system, such as VERDIN, is synchronizing in a reasonable time. There is a tradeoff in system cost and complexity between searching for the signal over a large time uncertainty and maintaining time accurately. Figure 3 shows the cost relationship to increasing processor logic speed; as you increase the cycle time of your processor the cost curve increases fairly rapidly. If we did not have a time standard in VERDIN, we would have to search a time uncertainty of approximately $\pm$ 1 second. This would make the VERDIN system economically unfeasible and a decision was made to include a frequency and time standard in the system.

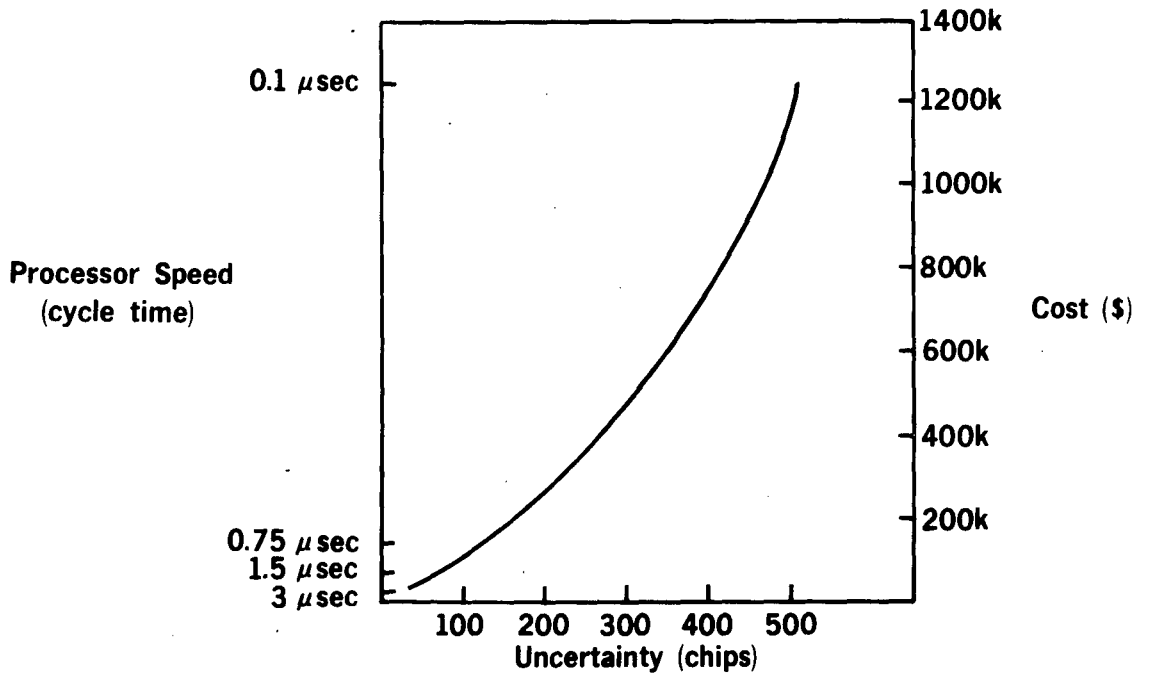

Figure 3. TIME UNCERTAINTY COSTS

In looking at the standards that were available, none were found to fit the VERDIN system very well. For the initial installations we were forced to select that which fit best into the system; however, in follow-on installations we plan to change the time standard to a design that is better integrated into the system. Figure 4 shows a comparison of the time standard that will be used in the initial and follow-on installations.

	INITIAL INSTALLATION	FOLLOW-ON INSTALLATION
Reference Cell	Rubidium	Cesium
Dimensions	H 5.22 in. W 17.0 in. D 16.0 in.	H 5.25 in. W 17.0 in. D 21.0 in.
Weight	44 lb + 10 lb standby battery	45 lb + 10 lb standby battery
Power	74 W (ac)* 50 W (dc) *with trickle charge into standby battery	90 W (ac)* 60 W (dc) *with trickle charge into standby battery
Standby Power	30 min int battery	30 min int battery
Clock	Mechanical	Electronic
Time Code	None	20-bit serial BCD

Outputs	Front	Rear	Front	Rear
5 MHz	1	4	1	4
1 MHz	1	1	1	1
100 kHz	1	1	1	1
1 pps	1	0	1	0
1 ppm	0	4	0	4

Figure 4. VERDIN FREQUENCY/TIME STANDARD CHARACTERISTICS

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