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TECHNICAL MANUAL

for

TEST SET, TELEGRAPH AN/UGM-8B(V)

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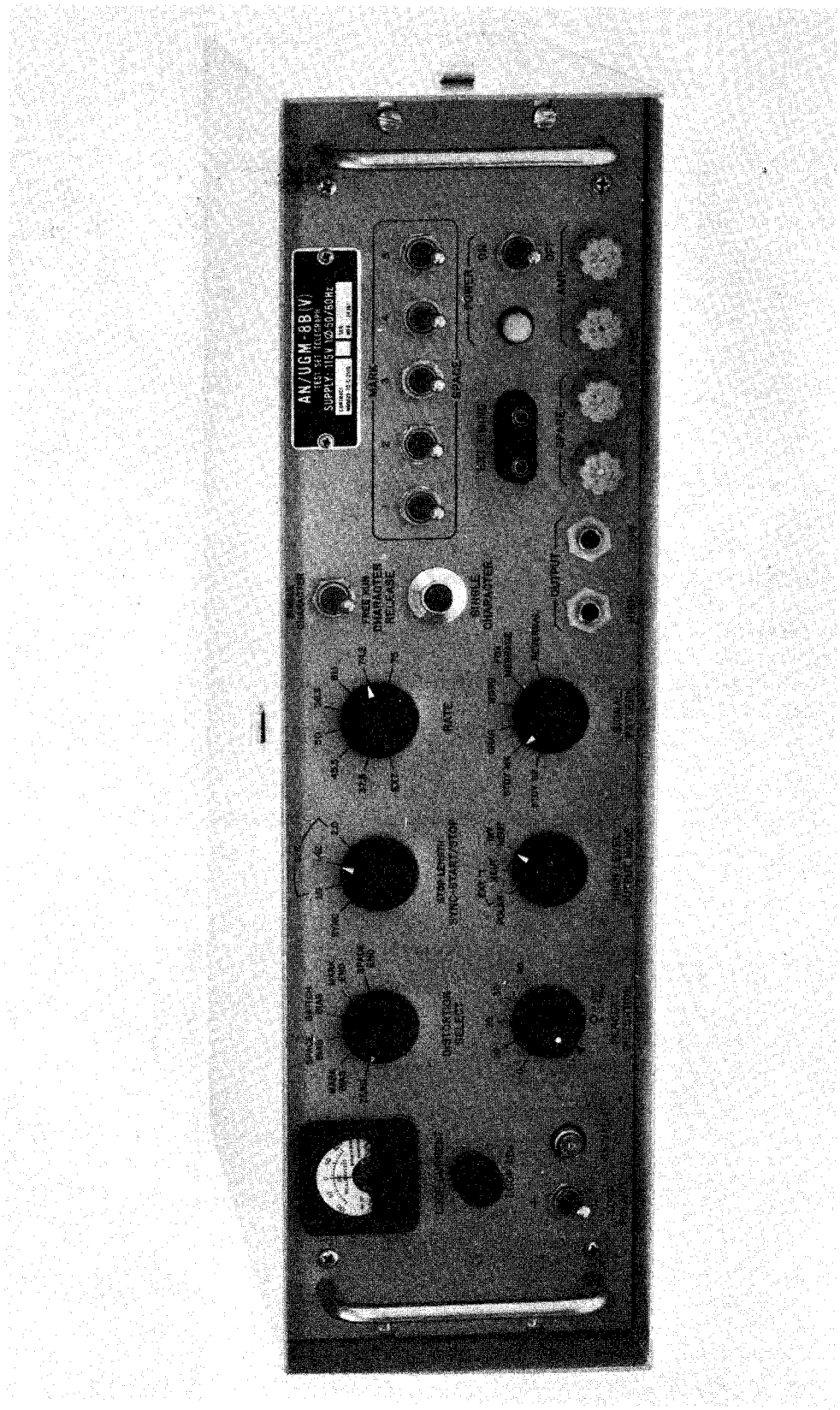


Figure 1-1. Test Set, Telegraph AN/UGM-8B(V)

SECTION 1

GENERAL INFORMATION

1-1. SCOPE

a. This technical manual contains the operation and service instructions with parts list for Test Set, Telegraph AN/UGM-8B(V), which will hereinafter, be referred to as the signal generator, is manufactured by TM Systems, Inc., Bridgeport, CT under Contract N00126-72-C-1551.

b. This technical manual is in effect upon receipt. Extracts from this publication may be taken to facilitate the preparation of other Department of Defense publications.

c. The unit contains either of three fox message assembly component boards as listed below:

Serial No.	P/N	Reference Symbol
A1 - A107	36021120	1A1A1A12
B1 - B270	36021220	1A1A1A12-1
D1 - D122	36021120-2	1A1A1A12-2

1-2. FUNCTIONAL DESCRIPTION

The signal generator provides individual teletype signals comprised of steady mark, steady space, dot cycles (reversals), selected character (repeated), fox message, and a single telegraph word composed of any six selectable characters. These test signals are available at the discretion of the operator by manipulation of front panel controls and a rear mounted programmable board. Controlled amounts and types of distortion may be introduced, also at the discretion of the operator.

1-3. PHYSICAL DESCRIPTION

a. The signal generator is supplied either as a portable unit in a carrying case or without a case for installation in a 19-inch rack. The signal generator aluminum drip-proof combination case has four rubber bumper feet on the bottom, and four dimpled feet on the rear. An access door on the rear of the case is used for connecting power cables. The combination case includes a removable front cover that has provisions for mounting the detachable power cable. A carrying handle is attached to the cover.

b. Internal circuits are constructed on plug-in printed wiring boards and wired-in printed boards. The plug-in boards are interconnected through a harness board to the wired boards and circuits through harness assemblies.

1-4. REFERENCE DATA

Reference data for the signal generator are listed in Table 1-1.

1-5. EQUIPMENT SUPPLIED

Table 1-2 lists equipment supplied with the signal generator.

1-6. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

Table 1-3 lists equipment required for various functions but not supplied with the signal generator.

TABLE 1-1. REFERENCE DATA

ITEM	DESCRIPTION
Output Test Patterns	1. Standard "FOX" message with 5-letter programmable field for station call letters. A 6th letter is factory programmed for a figure command and may be reprogrammed for an additional call letter. Message configured for 5-unit ITA No. 2 Code (American version). 2. Steady mark 3. Steady space 4. Reversals 5. Selected repetitive character 6. Teletype word, 6 characters
Modulation Rates	External: 37.5 to 2400 baud. Internal: 37.5, 45.5, 50, 56.8, 61.12, 74.2, and 75 baud (±1%).
Modes	Synchronous and 5 level code Start/Stop
Stop Pulse Lengths	1.0, 1.42, and 2.0
Character Release Modes	1. Free running 2. Single character, manual release
Distortion Types	1. Marking bias 2. Spacing bias 3. Switching Bias 4. Marking end 5. Spacing end
Distortion Accuracy	Zero to 49 percent in 1 percent steps at all rates.

TABLE 1-1. REFERENCE DATA (cont)

ITEM	DESCRIPTION
Automatic Carriage Return/line feed	Provides automatic carriage return and line feed after 72 characters when generating a selected character or a teletype word in start/stop mode.
Output Modes	Polar: Internal low level ±6 volts (positive mark) Neutral: Isolated electronic switch (closed for mark) Internal loop supply 20 or 60 milliamperes (ma) nominally 130 volts ±10 percent. External neutral loop supply: 300 volts maximum, 20 or 60 ma. External polar supply : ±130 volts maximum, 20 or 60 ma.
Output Jacks	HIGH LEVEL OUTPUT: JJ104 per MIL-J-641, Schematic J1. Tip is signal line, sleeve is signal ground. LOW LEVEL OUTPUT: Type JJ-103, per MIL J-641/3A, Schematic J2. Tip is signal line and sleeve is signal ground.
External Timing Input	Connects square wave ±6 volts at 200 x desired baud rate to EXT TIMING terminals.

TABLE 1-2. EQUIPMENT SUPPLIED

QTY PER EQUIP	NOMENCLATURE		OVERALL DIMENSIONS			VOLUME (CU. FT)	WEIGHT (LB)
	NAME	DESIGNATION	HEIGHT	WIDTH	DEPTH		
1	Test Set, Telegraph	AN/UGM-8B(V)	5 1/4	19	14 5/8	0.7	17
1	Case		6 9/16	20 1/8	16	1.1	10
2	Technical Manual	NAVSHIPS 0967-378-4010	11	8 1/2	---	---	---

TABLE 1-3. EQUIPMENTS AND PUBLICATIONS REQUIRED BUT NOT SUPPLIED

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Teleprinter	AN/UCC-48	Troubleshooting and maintenance procedures.	----------
1	AC Voltmeter	AN/USM-143	Maintenance procedures.	0 - 300 vac, all: 3%
1	Multimeter	AN/PSM-4	Troubleshooting and maintenance procedures.	0 - 1000 vdc, all: 3% 0 - 500 ma all: 3%
1	Counter	AN/USM-245	Maintenance procedures.	10 Hz - 1.2 MHz, all 1 count
1	Oscilloscope	AN/USM-117	Troubleshooting and maintenance procedures.	DC-5MHz
1	Square Wave Generator	Hewlett Packard Model 211B or equal	Troubleshooting and maintenance procedures.	1 Hz - 1 MHz 0 - +30 volts, 600 ohms
-	Loop Power Supplies		Troubleshooting and maintenance procedures.	0 - 130 vdc, 60 ma
1	Signal Analyzer	TS-2936/AN-USM329	Troubleshooting and maintenance procedures.	2% accuracy

SECTION 2

INSTALLATION

2-1. UNPACKING

No special procedures are required to unpack the signal generator.

2-2. SITE SELECTION AND INSTALLATION

The signal generator when supplied in the case, is a portable unit of test equipment and requires no special siting or installation. When the unit is supplied without a case, a 19-inch rack must be provided for mounting. The overall dimensions of the unit are shown in figures 2-1 and 2-2, in and out of the case, respectively.

2-3. POWER REQUIREMENTS

The test set requires a source of single-phase 115-volt 50-60 Hz power. Maximum Power consumption is 25 watts, operating on external current loops.

2-4. INSPECTION AND ADJUSTMENT

a. VISUAL INSPECTION. Visually inspect the signal generator for obvious signs of damage that may have occurred during shipment. Remove the signal generator from its case, by unscrewing the four front panel screws and the rear chassis holding screws, and check that all plug-in cards and components are securely in place.

b. CALL LETTER PROGRAMMING. The signal generator contains provisions for incorporating station call letters into the fox message. Provisions are made for six letters: the first five are supplied blank (spaces) and must be programmed by the operator while the sixth is prewired at the factory to provide a FIGURES command. Refer to paragraph 4-2h, then program the station call letters as follows:

(1) Remove component board 1A1A13 from the signal generator.

(2) Refer to figure 3-2 for 5-unit alphabet and figures 4-6 and 4-6A for strapping data.

(3) Connect a wire between two terminals where marks are required. Leave terminals blank where spaces are required.

(4) Replace component board 1A1A13, checking that it is securely in place.

c. WORD PROGRAMMING. The signal generator contains provisions for generating a programmable six-character word. The word board is located at the rear of the unit and is accessible through a rear panel. Plugs are provided for programming the board. Program the desired word as follows:

(1) Open rear panel to expose board, and remove cover plate.

(2) Refer to figure 3-2 for 5-unit code and figures 4-7 and 4-8 for strapping positions.

(3) Arrange plugs to provide the required marks and spaces to implement the desired word.

(4) Replace cover plate.

d. MARK POLARITY. The mark polarity in external polar operation is defined by the polar battery installation. For both internal and external neutral operation, a mark is indicated by current flow and a space by no current flow. The polarity of the output jack may be reversed by use of the front panel LOOP POLARITY switch.

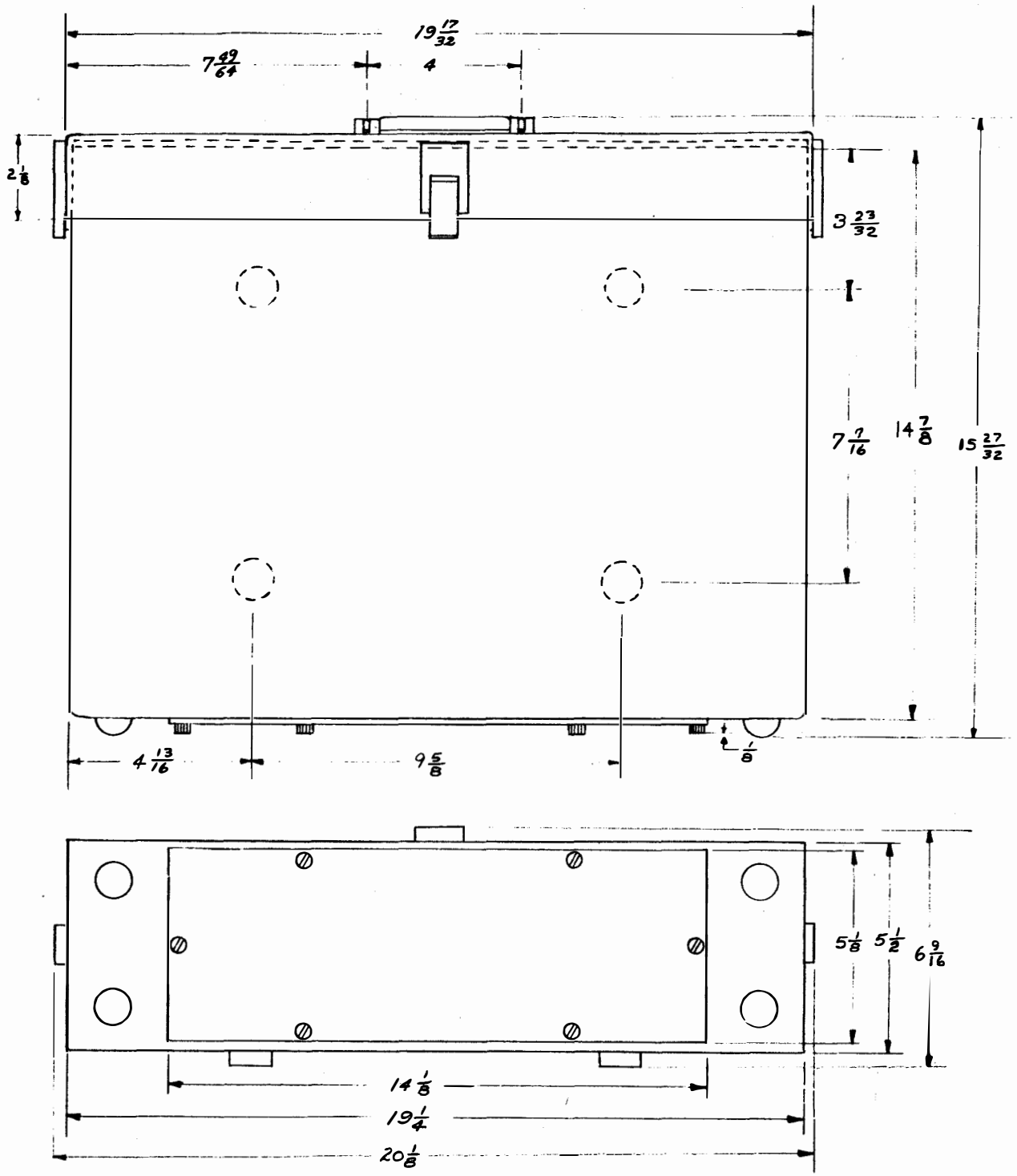


Figure 2-1. Case for Test Set, Telegraph AN/UGM-8B(V)

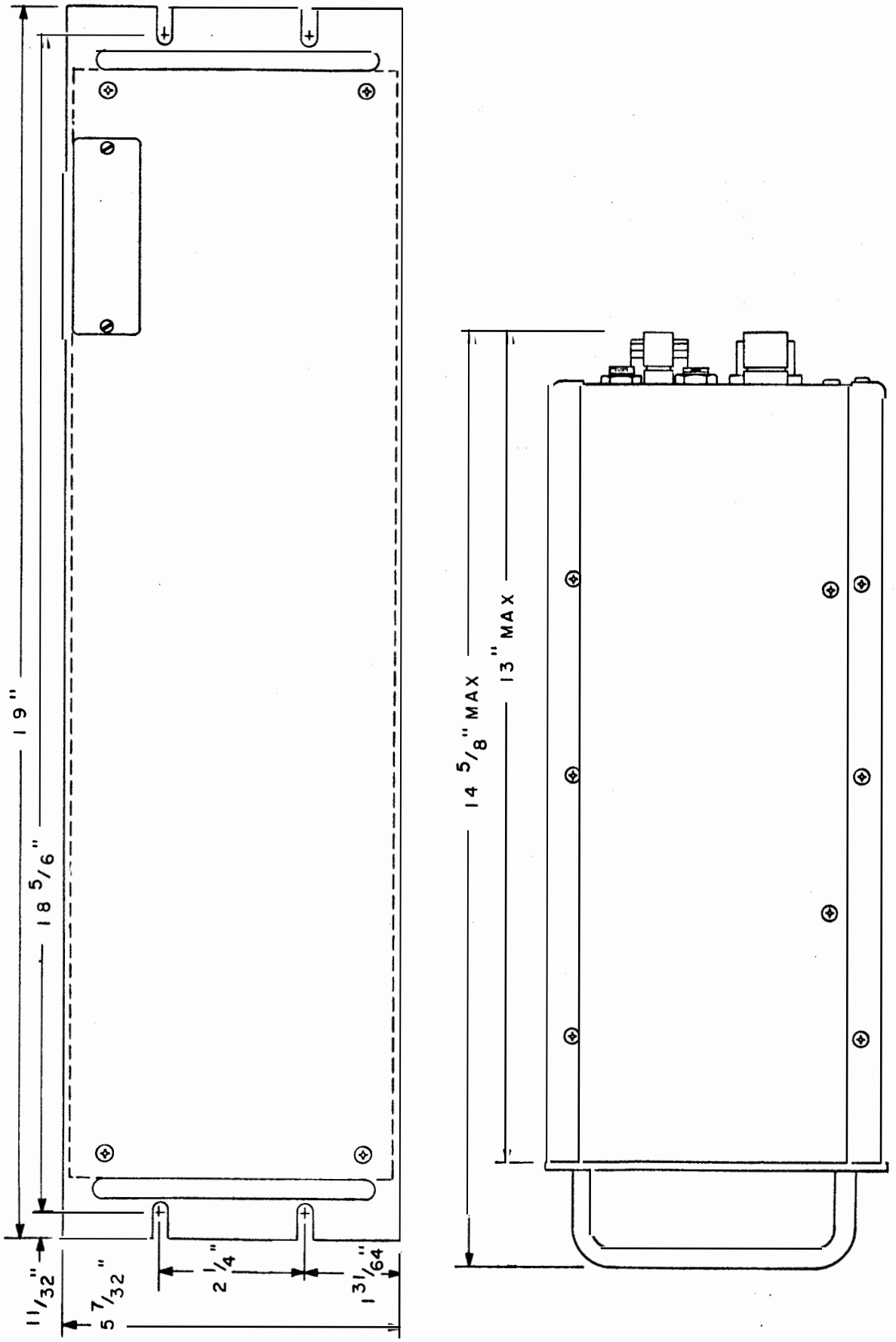


Figure 2-2. Test Set, Telegraph AN/UGM-8B(V) Installation Data

SECTION 3

OPERATION

3-1. FUNCTIONAL OPERATION

The signal generator provides a controlled telegraph test signal that is required to troubleshoot telegraph and data terminals together with associated equipment.

3-2. OPERATOR AND TECHNICIAN REFERENCE DATA

Definitions and examples of telegraph distortion and telegraphic alphabets are included for reference. Figure 3-1 shows the various types of distortion on a standard 5-level start/stop signal. The distortion errors shown are all approximately 25 percent. Figure 3-2 shows the 5-level International Telegraph Alphabet Number 2 (American Version).

3-3. CONTROLS, INDICATORS, AND JACKS.

The controls and indicators on the front and rear panels are shown in Figure 3-3 and listed in Table 3-1. An (R) in Table 3-1 represents the rear panel location of the control, indicator, or jack.

3-4. POWER TURN-ON

Power is applied to the generator by operating the POWER switch (12, Figure 3-3) to its ON position. Check that POWER lamp (13) lights when the switch is set to its ON position.

3-5. OPERATING PROCEDURES.

The operation of the signal generator is dependent on the type of signal desired. The signal is determined by the setting of the signal generator front panel controls. The front panel controls, and their functional relationship to the output signal, are shown in Figure 3-4. The diagram is divided into four selective functions that make up the output signal. These are:

1 Select signal pattern

2 Select signal characteristics

3 Select distortion

4 Select output

NOTE

The implied sequence and left-to-right flow shown in figure 3-4 is for illustrative purposes only. It does not represent signal flow. The controls may be set in any sequence desired by the operator.

a. SELECTION OF SIGNAL PATTERN. The SIGNAL PATTERN switch (21, figure 3-3) selects the type of signal pattern. As shown in figure 3-4, selection of steady space (STDY SP) or steady mark (STDY MK) signal routes these signals direct to the output circuit. Selection of CHARACTER involves the MARK/SPACE switches (7 through 11, figure 3-3) which must be set to the desired mark-space arrangement for the desired character. The WORD position provides a programmed word as determined by the operator through the rear mounted word matrix programming board. The FOX MESSAGE position selects the fox message signal pattern. The REVERSALS position selects the mark-to-space reversal pattern.

b. SELECTION OF SIGNAL CHARACTERISTICS. Four switches are involved in setting the general characteristics of the output signal: The RATE switch (4), the SYNC-START/STOP (Stop Length) switch (3), and the CHARACTER RELEASE switch (5) with the associated SINGLE CHARACTER switch (6). The RATE switch sets the baud

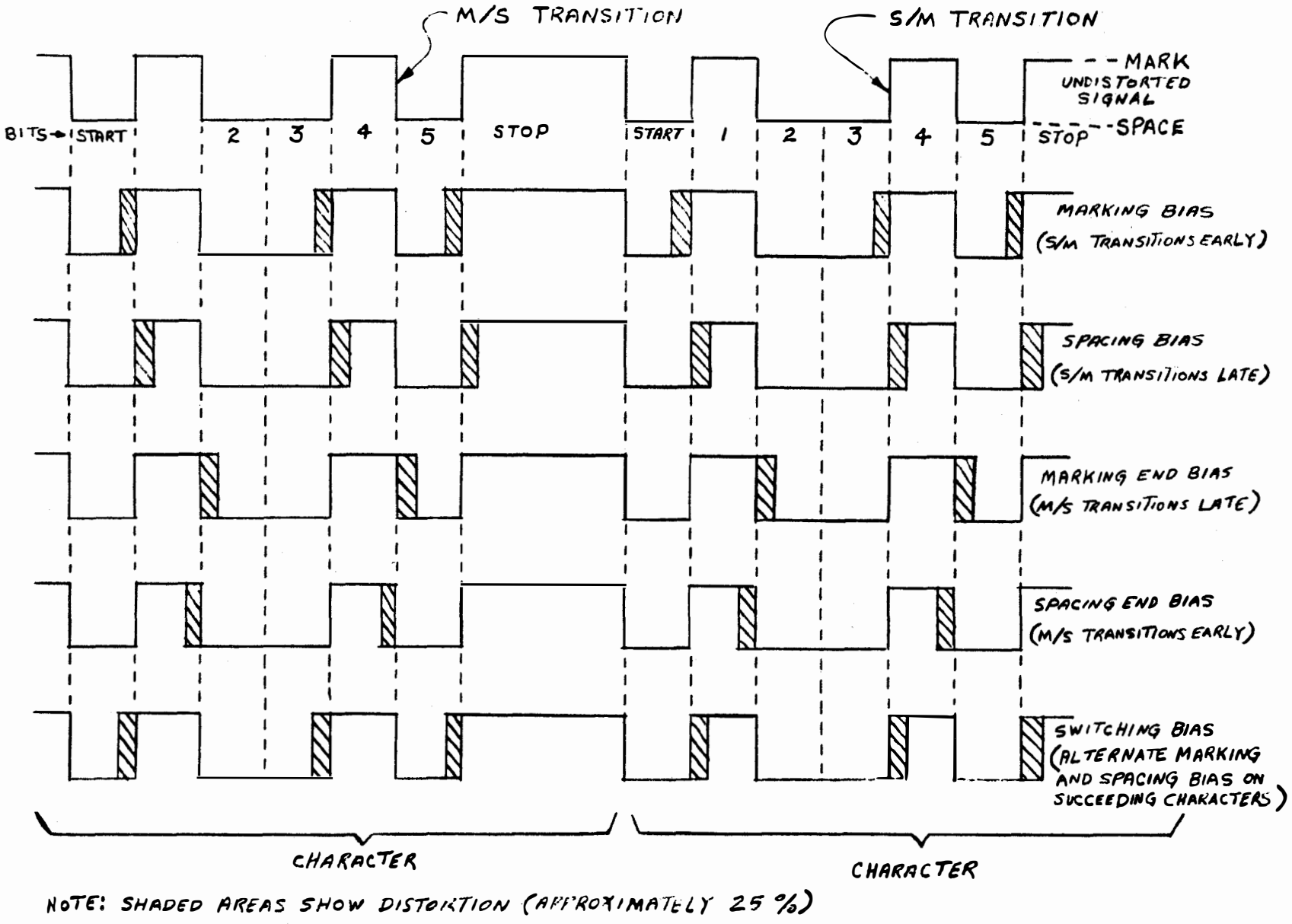


Figure 3-1. Examples of Telegraphic Distortion

CHARACTERS		WEATHER SYMBOLS	CODE SIGNAL						
LOWER CASE	UPPER CASE	UPPER CASE	START	1	2	3	4	5	STOP
A	–	↑		●	●				●
B	?	⊕		●			●	●	●
C	:	○			●	●	●		●
D	$	↗		●			●		●
E	3	3		●					●
F	!	→		●		●	●		●
G	&	↘			●		●	●	●
H	STOP	↓				●		●	●
I	8	8			●	●			●
J	'	↙		●	●		●		●
K	(	←		●	●	●	●		●
L	)	↖			●			●	●
M	.	.				●	●	●	●
N	,	⊕				●	●		●
O	9	9					●	●	●
P	0	0			●	●		●	●
Q	1	1		●	●	●		●	●
R	4	4			●		●		●
S	BELL	BELL		●		●			●
T	5	5						●	●
U	7	7		●	●	●			●
V	;	Ø			●	●	●	●	●
W	2	2		●	●			●	●
X	/	/		●		●	●	●	●
Y	6	6		●		●		●	●
Z	"	+		●				●	●
BLANK		–							●
SPACE						●			●
CARRIAGE RETURN							●		●
LINE FEED					●				●
FIGURES				●	●		●	●	●
LETTERS				●	●	●	●	●	●

NOTES
1. ● EQUAL MARKING PULSES
2. UPPER CASE H MAY BE STOP OR #

Figure 3-2. International Telegraph Alphabet No. 2, American Version

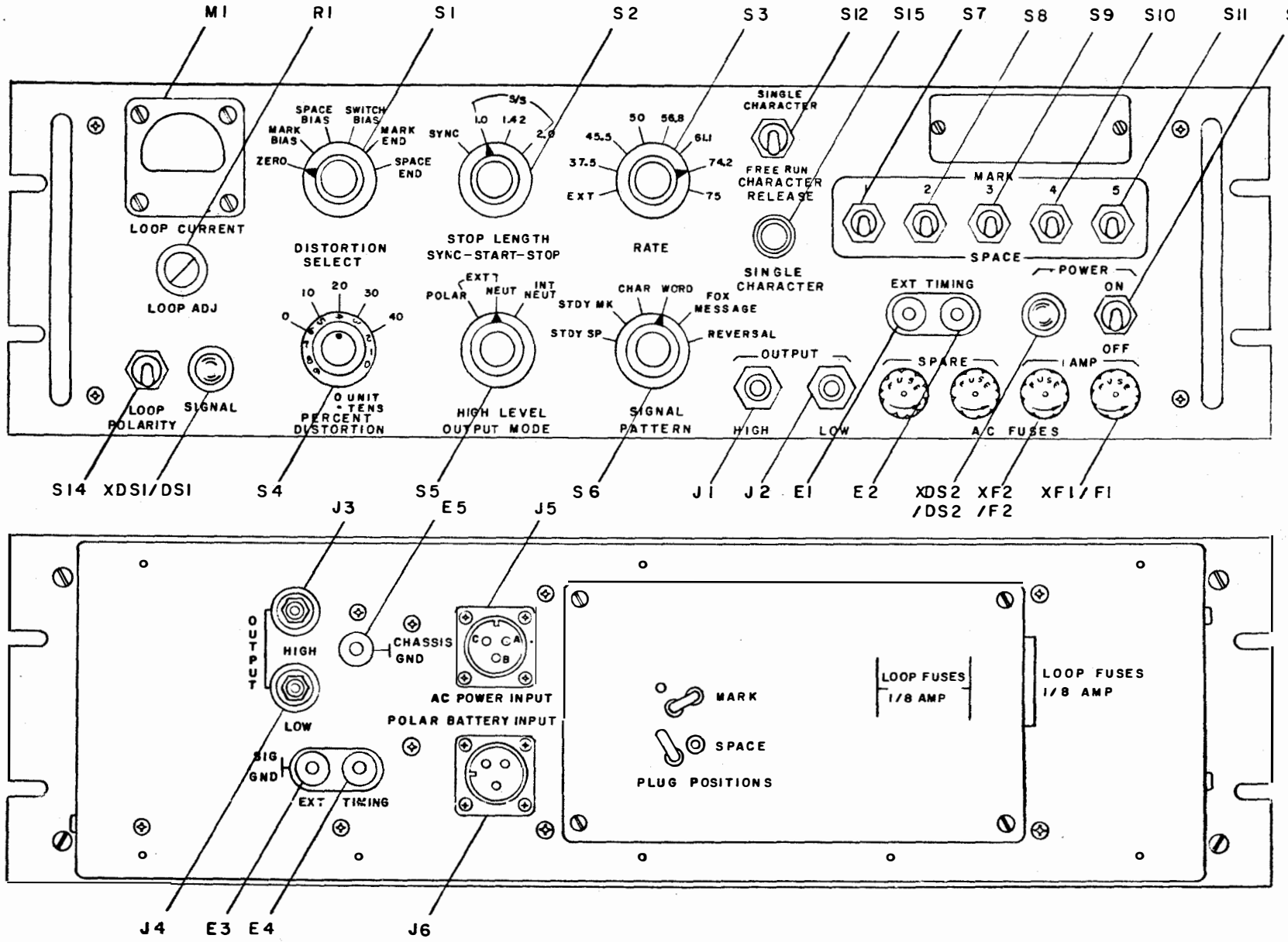


Figure 3-3. Signal Generator Controls and Indicators

TABLE 3-1. SIGNAL GENERATOR CONTROLS AND INDICATORS

FIGURE 3-3 INDEX NO.	CONTROL OR INDICATOR	FUNCTION
1	LOOP CURRENT meter	Indicates loop current in milli-amperes (ma.) (100-0-100).
1A	LOOP ADJ control	Adjusts loop current within approx-imately 70 ma range.
2	DISTORTION SELECT switch	Selects type of distortion to be applied to the output signal.
3	STOP LENGTH SYNC-START/STOP switch	Selects synchronous or start/stop mode. Also selects stop length in start/stop mode.
4	RATE switch	Selects internal baud rate from 37.5 to 75 baud or external timing.
5	CHARACTER RELEASE switch	Selects character release operating mode. In SINGLE CHARACTER position, the output is released as as single characters, each time the SINGLE CHARACTER pushbutton switch (6) is pressed. In FREE RUN position, the output signal is continuous.
6	SINGLE CHARACTER pushbutton switch	Operates in conjunction with CHAR-ACTER RELEASE switch set to SINGLE CHARACTER position.
7	MARK/SPACE 1 switch	One of a set of 5 switches. Sets first digit to either mark (up) or space (down).
8	MARK/SPACE 2 switch	Sets second digit to mark or space.
9	MARK/SPACE 3 switch	Sets third digit to mark or space.
10	MARK/SPACE 4 switch	Sets fourth digit to mark or space.
11	MARK/SPACE 5 switch	Sets fifth digit to mark or space.
12	POWER switch	AC power switch for input power.
13	POWER indicator lamp	Illuminates when ac power is applied to the pattern generator.

TABLE 3-1. SIGNAL GENERATOR CONTROLS AND INDICATORS (cont)

FIGURE 3-3 INDEX NO.	CONTROL OR INDICATOR	FUNCTION
14	AC FUSES, 1 AMP	Fuses ac line
15	AC FUSES, 1 AMP	Fuses ac line
16, 17	AC FUSES SPARE	These are spare fuses for 14 and 15.
18	EXT TIMING binding posts	Input terminals for external timing signal.
19	OUTPUT-LOW level jack	Connector for low level signals; parallel with rear panel jack.
20	OUTPUT-HIGH level jack	Connector for high level signals; parallel with rear panel jack.
21	SIGNAL PATTERN switch	Selects type of output signal. In STDY/SP, the output consists of a continuous space signal. In STDY MK, the output consists of a continuous mark signal. In CHAR, the output consists of a 5-unit character selected on the MARK/SPACE switches. In WORD, the output consists of a work programmed on the work matrix board. In FOX MESSAGE, the output consists of the 80-character fox message. In REVERSALS the output consists of alternate marks and spaces.
22	HIGH LEVEL OUTPUT MODE switch	Selects high level output mode. EXT POLAR position permits use of external batteries connected at rear of unit (29) and sets up loop for polar operation. EXT NEUT position sets up loop for dry contact operation. INT NEUT position provide loop current from internal loop supply.
23	PERCENT DISTORTION switch	Selects percent distortion in output test signal in units and tens levels of percent.

TABLE 3-1. SIGNAL GENERATOR CONTROLS AND INDICATORS (cont)

FIGURE 3-3 INDEX NO.	CONTROL OR INDICATOR	FUNCTION
24	SIGNAL lamp	Glows steadily for steady mark, remains extinguished for steady space, or blinks for keyed signal.
25	LOOP POLARITY switch	Selects jack polarity for output loop operation. For INT NEUT operation + position provides a positive polarity on the output jack tip, with respect to the sleeve. For EXT POLAR + position, common battery terminal is connected to output jack sleeve.
26, 26A(R)	OUTPUT jacks	Permits connection to either HIGH or LOW output level; parallel with front panel jacks.
27 (R)	EXT TIMING terminals	Input connection for external timing signals parallel with front panel terminals.
28 (R)	AC POWER INPUT connector	Input receptacle for external power application.
29 (R)	POLAR BATTERY INPUT	Input receptacle for polar battery power.
30,31(R)	Programming Jumpers	Jumpers for programming a desired word. Typical jumper positions are shown, 30 represents the jumper position for providing a space while 31 represents the jumper position for providing a mark.
32(R)	LOOP FUSES 1/8 AMP	Fuses for the loop keying relay, in the circuit on both internal and external loops.
33 (R)	CHASSIS GND	Ground terminal.

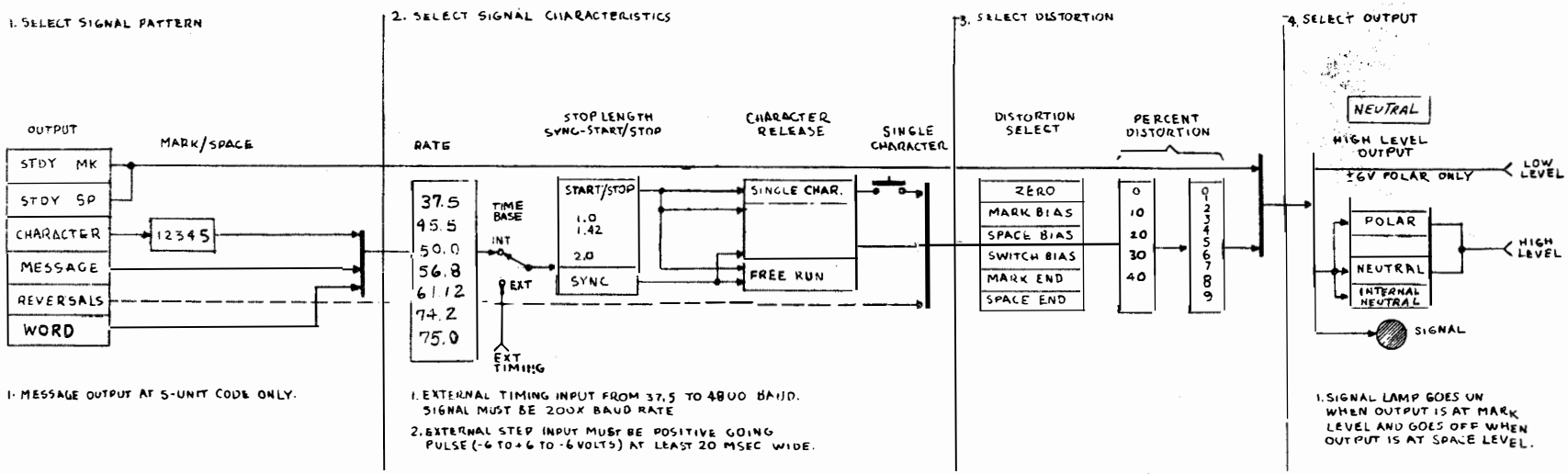


Figure 3-4. Signal Generator Functional Block Diagram

rate of the signal, by selecting either the internal timing generator or an external timing signal connected to the EXT TIMING terminals. The SYNC-START/STOP (Stop Length) switch selects either synchronous or start/stop operation with three options on the stop length. The CHARACTER RELEASE switch provides two options on the method of signal transmission:

(1) In the SINGLE CHAR position, a start/stop signal is released one character at a time when the SINGLE CHARACTER switch is pressed.

(2) In the FREE RUN position, the signal (synchronous and start/stop) is continuous.

c. SELECTION OF DISTORTION. The amount and type of distortion are selected on two switches. The DISTORTION SELECT switch (2) selects one of five types of distortion: mark-bias, space bias, switch bias, mark end, and space end. Refer to figure 3-1 for examples of these types of distortion. The distortion is selected on the PERCENT DISTORTION concentric switch (23) which sets the amount in tens and unit.

d. SELECTION OF OUTPUT CIRCUIT. The signal generator provides both high and low level outputs. The LOW LEVEL jack (19 and 26) provides a low-level polar output at ±6 volts established by an internal power supply. This jack and the correesponding jack at the rear of the signal generator should be used for low-level polar output connections. For high-level polar and neutral signals, the HIGH LEVEL jack (20 and 26A) should be used. With the HIGH LEVEL OUTPUT MODE switch (22) in the EXT POLAR position, the output signal available at the HIGH LEVEL jack is a polar signal derived from external batteries up to ±130 volts 20 or 60 ma. The same signal is also available at the corresponding high level jack (26A) at the rear of the signal generator. With the HIGH LEVEL OUTPUT MODE switch in the INT NEUT position, the output signal drives an internal electronic switch (closed for mark) keying an internal 130V supply connected to the HIGH LEVEL jack. This jack and the corresponding jack at the rear of the signal generator should be used for all neutral outputs and high level polar outputs. With the HIGH LEVEL OUTPUT MODE switch in the EXT NEUT position, the output signal available at the HIGH LEVEL jack is the dry contact keying of an external neutral loop voltage of up to 300 volts, 20 or 60 ma.

(1) The SIGNAL lamp (24), shown in the output circuit, goes on whenever the output of the signal generator is at the mark level and goes off whenever the signal is at the space level. Hence, for a steady mark signal, the lamp glows steadily. For a steady space signal, the lamp remains off. And, for keying signals, the lamp blinks on and off.

3-6. OPERATING PRECAUTIONS

The following operating precaution and warning are provided for use by the operator. The external timing signal must be a square wave with a frequency 200 times the desired baud rate and an amplitude of ±6 volts.

WARNING

To prevent a shock hazard, observe the following precautions when connecting the signal generator to the signal loop.

INTERNAL NEUTRAL AND POLAR OUTPUTS: Connect test cable to signal loop before connecting test cable to signal generator (generator provides loop voltage).

EXTERNAL NEUTRAL OUTPUTS: Connect test cable to signal generator before connecting test cable to signal loop (station provides loop voltage).

3-7. OPERATOR'S MAINTENANCE

Maintenance required by the operator is limited to replacement of the lamps and fuses in the signal generator.

SECTION 4

TROUBLE SHOOTING

4-1. LOGICAL TROUBLESHOOTING

This section contains information to aid in quickly and efficiently determining the cause of equipment malfunction. The information is given in order of over-all troubleshooting technique, operational data, and troubleshooting data.

a. SYMPTOM REGOGNITION. - This is the first step in the troubleshooting procedure and is based on complete knowledge and understanding of the equipment operating characteristics. All equipment troubles are not necessarily the direct result of component failure. Therefore, a trouble in an equipment is not always easy to recognize since all conditions of less than peak performance are not always apparent. This type of equipment trouble is usually discovered while accomplishing preventive maintenance procedures. It is important that the "not so apparent" troubles, as well as the apparent troubles, be recognized.

b. SYMPTOM ELABORATION. - After an equipment trouble has been recognized, all the available aids designed into the equipment should be used to elaborate, further, on the original trouble symptom. Use of front-panel controls and other built-in indicating or testing aids should provide better identification of the original trouble symptoms. Also, checking or otherwise manipulating the operating controls may eliminate the trouble.

c. LISTING PROBABLE FAULTY FUNCTION. - The next step in logical trouble shooting is to formulate a number of logical choices as to the cause and likely location (functional section) of the trouble. The logical choices are mental decisions which are based on knowledge of the equipment operation, a full identification of the trouble symptom, and information contained in this manual. The over-all functional description and its associated block diagram should be referred to when selecting possible faulty functional sections.

d. LOCALIZING THE FAULTY FUNCTION. - For the greatest efficiency in localizing trouble, the functional sections which have been selected by the logical choice method should be tested in an order that will require the least time. This requires a mental selection to determine which section to test first. The selection should be based on a further extension of the logical choice method. If the tests do not prove that functional section to be at fault, the next section should be tested, and so on until the faulty functional section is located. As aids in this process, this manual contains a functional description and a servicing block diagram. Also, where applicable, test data are supplied to augment the functional description and servicing block diagram.

e. LOCALIZING TROUBLE TO THE CIRCUIT. - After the faulty functional section has been isolated, it is often necessary to make additional logical choices as to which group of components or component (within the functional section) is at fault. Servicing schematic diagrams for each functional section provide the information needed to bracket and then isolate the faulty component.

f. FAILURE ANALYSIS. - After the trouble has been located, but prior to performing corrective action, the procedures followed up to this point should be reviewed to determine exactly why the fault affected the equipment in the manner it did. This review is usually necessary to make certain that the fault discovered is actually the cause of the malfunction, and not just the result of the malfunction.

4-2. SIGNAL GENERATOR THEORY OF OPERATION.

a. FUNCTIONAL BLOCK DIAGRAM. - Figure 4-1 shows the functional circuits and signal flow for the signal generator. The baud rate of the signal generator output is controlled by either the internal time base generator output frequency or the frequency of an external timing signal. The RATE switch selects the output frequency of the time base generator. The internal time base generator or external source supplies a timing signal, 200 times the baud rate, to the timing control circuitry.

(1) The timing control circuit controls the mode of character release of the signal generator. The CHARACTER RELEASE switch determines the mode of operation by (a) allowing a continuous time base signal to feed the message generating circuits in FREE RUN, or (b) allowing the time base signal to feed through for the length of only one character when the SINGLE CHARACTER switch is pressed. The timing control output to the divide-by-100 counter is 100 times the baud rate.

(2) A divide-by-100 BCD counter provides a baud rate output which is used as a clock signal for the bit counter. In addition to the baud rate output, the divide-by-100 counter supplies signals to the distortion trigger circuit which generate distortion triggers for the signal processing circuit. Units and tens PERCENT DISTORTION switches select the percentage of bias or end distortion imposed on the output signal of the signal generator.

(3) The bit counter gates the outputs of a binary counter to provide separate gating signals for each bit of the characters in the message. A character advance and stop mark enable signal are also generated at the end of each character. The gating signals for each character bit provide timing for the message-generating circuits. The character advance signal of the bit counter is a clock signal for the character counter, and the stop mark enable signal starts the generation of the stop mark in the stop mark circuit.

(4) The stop mark circuit restarts the counting sequence in the signal generator at the end of the stop mark. Stop mark widths of 1.0, 1.42, and 2.0 bits can be selected by the STOP LENGTH switch, which programs the gating in the stop mark circuit to restart the counting sequence after the proper stop mark length.

(5) The stop mark circuit triggers the character reset circuit which resets the divide-by-100 and bit counters and produces the mark signal in the signal processing circuit. When in SINGLE CHARACTER mode, another signal from the stop mark circuit inhibits the timing control circuit after one character is generated. When the signal generator operates in the synchronous mode of transmission, the SYNC-START/STOP switch disables the stop mark trigger circuit so that the signal generator counting sequence is continuous.

(6) The character gates the outputs of seven flip-flops to provide matrix address signals for the Fox message and call letter matrices. The combination of the character counter signals and bit gating signals from the bit counter make up a complete address for each bit in the characters of the message. The matrices are programmed so that each character bit location address contains a mark or space as required for the particular character of the message. The signals from the matrix output gates is the message without the stop mark.

(7) The selected character generating circuit is programmed by the MARK-SPACE switches to produce a particular character. The MARK-SPACE switches cause a mark or space to occur at the bits of the character to provide the code for the particular character. The bit gating signals from the bit counter release the mark or space signal at each bit of the selected character. A selected word generating circuit is programmed by shorting straps inserted in the word card. The presence or absence of the straps cause marks and spaces to occur at the bits of the character for the word. The bit gating signals release the mark or space signal at each bit. For selected character and word signal pattern, 72 characters are

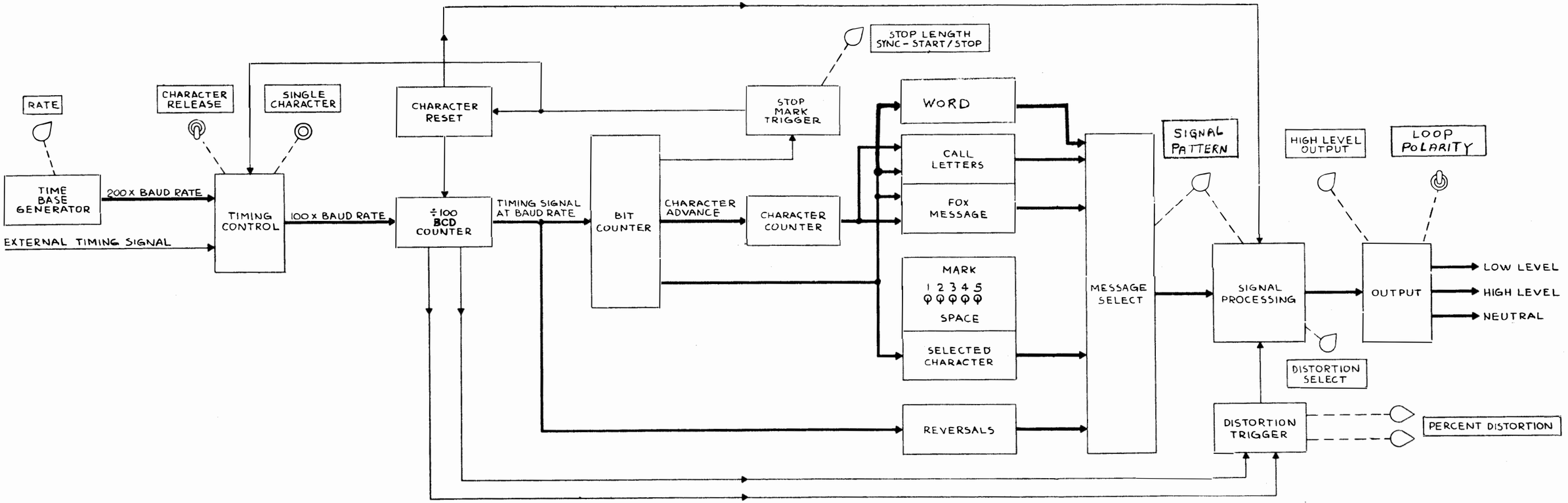


Figure 4-1. Signal Generator Functional Block Diagram

generated then two carriage returns and a line feed are produced.

(8) A reversal signal, consisting of a squarewave at half the bit rate, uses an output of the bit counter. When reversals are selected by the OUTPUT switch, the squarewave is passed to the message select circuit and the stop mark circuit is disabled so that the squarewave is continuous.

(9) The programmed word, call letter-Fox message, selected character, and reversal signals are applied to a message select circuit which permits passage of signal selected by the OUTPUT switch and applies it to the signal processing circuit. The OUTOUT switch also permits selection of a steady mark or steady space output, which is developed in the signal processing circuit.

(10) In the signal processing circuit, the message signal is gated and delayed to add the stop mark, except for synchronous transmission, and any distortion selected by the PERCENT DISTORTION switches.

(11) The output of the signal processing circuit feeds drivers in the output circuit which provide a low and high level output at the front and rear panel jacks. There is a continuous polar low level output at the LOW LEVEL OUTPUT jack. The HIGH LEVEL OUTPUT switch selects polar or neutral output for the HIGH LEVEL OUTPUT jack.

(12) SERVICING BLOCK DIAGRAM. The following paragraphs describe the operation of the signal generator in detail. The servicing block diagram for the signal generator, figure 4-11, provides a logic diagram with sufficient detail to follow signal generator operation down to the functioning of individual integrated circuits and other piece parts.

(13) On the servicing block diagram, the numbers beside the leads into the logic symbols indicate the pin numbers on the integrated circuit module. The circled numbers with arrows to points in the circuit are the numbers of waveforms in the timing diagrams of figure 4-10.

(14) The timing diagrams show signal relationships which will aid in troubleshooting as well as following the description of signal generator operation. Each waveform in the timing diagram has a number to the right of it; in the text, certain signals are identified by including their number on the timing diagram in parentheses ( ).

(15) In the text, the printed circuit cards are referred to as A2, A3, etc., omitting the 1A1 prefix. As an aid in troubleshooting, sets of signals that are fed to gating circuits are identified in the timing diagrams and on the servicing block diagrams.

(16) The signal generator uses two types of flip-flops: A J-K type and a pulse triggered. Figure 4-2 shows the internal connections within the integrated circuit, each integrated circuit module contains two J-K flip-flops of the type shown. Reference to this diagram may be helpful in understanding the switching of the flip-flops. Table 4-1 is a truth table for the J-K flip-flops.

Notes:

1. NC = No change.

2. CS = Change state.

3. Logic 0 at S_D overrides J and K inputs to provide high $\overline{Q}$ and low Q outputs.

(17) The pulse-triggered flip-flop has an ac-coupled input to both the set and clear gates, which also require a logic 0 enable input. The servicing block diagram shows the detail block diagram of these flip-flops. Table 4-2 is a truth table for the pulse-triggered flip-flops.

b. TIME BASE GENERATOR. The time base generator provides 7 internal timing signals corresponding to the 7 baud rates on the RATE switch. Additional baud rate signals can be generated by connecting an external time base generator to the EXT

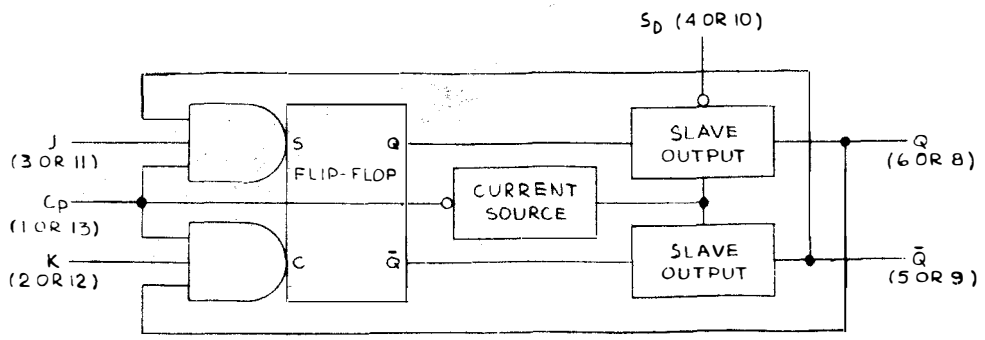


Figure 4-2. J-K Flip-Flops, Block Diagram

TABLE 4-1. TRUTH TABLE FOR J-K FLIP-FLOPS

INPUTS		OUTPUTS	
J (3 or 11)	K (2 or 12)	Q (6 or 8)	$\bar{Q}$ (5 or 9)
1	0	1	0
0	1	0	1
1	0	1	0
0	0	NC	NC
1	1	CS	CS

TIMING terminals. In external mode RATE switch also enables A4IC6N3, allowing the external timing signal from differential comparator A15IC2 to reach the timing control circuit through card connector A4-6.

(1) The internal time base generator uses crystal-controlled oscillators and an eight stage binary counter to obtain the 7 timing signals generated. Table 4-3 lists the frequencies, division ratios, and output gates for each of the 7 timing signals. The crystal-controlled oscillators on the A1 and A2 cards contain an oscillator stage, emitter follower, and driver stage. The driver output feeds through a NAND gate which somewhat squares the oscillator output in addition to gating the output to the divider on card A3. The RATE switch supplies V_{CC} to only the oscillator being used and enables its output NAND, allowing the signal to be fed to the divider on A3. The various division ratios for the oscillator signals are obtained by taking the output of various stages of the divider as well as the output of the last stage. Figure 4-10A shows the relationships of the signals in the eight stage divider.

(2) The 1.92 MHz oscillator signal (1) enters card connector A3-2 to clock the first stage of the divider. This oscillator signal is used for three of the time base generator signals. The timing signals for the 37.5 and 75 baud rates are obtained by taking the output of the eighth and seventh stages, respectively, of the divider. To obtain the 50 baud rate timing signal, the 1.92 MHz oscillator signal is divided by 192 ($2^6 \times 3$). This action is performed by resetting the last two divider stages to provide a divide-by-3 output as shown in figure 4-10. When the RATE switch is on the 50 position, A3IC5N3 supplies an S_D signal to flip-flop A3IC4F1 at every third C_P input from A3IC3F2.

(3) The 145.6 and 195.584 kHz oscillator signals enter card connector A3-14 to clock the fifth stage of the divider so that the input signal is divided by 16. The 118.72 kHz oscillator signal feeds through card connector A3-21 to clock the sixth divider stage giving an output signal divided by 8.

(4) The 181.8 kHz oscillator is used to develop the 56.8 baud rate. The oscillator output is coupled through card connector terminal A3-14 to A3IC3F1. The counter

TABLE 4-2. TRUTH TABLE FOR PULSE-TRIGGERED FLIP-FLOPS

INPUTS						OUTPUTS	
S (pin 4)	Pt_1 (pin 5)	C (pin 10)	Pt_2 pin 6)	S_D (pin 13)	C_D (pin 1)	Q (pin 3)	Q (pin 11)
1	x	x	1	1	1	NC	NC
x	1	1	x	1	1	NC	NC
0	0	1	x	1	1	1	0
0	0	x	1	1	1	1	0
1	x	0	0	1	1	0	1
x	1	0	0	1	1	0	1
0	0	0	0	1	1	Indeterminate	
x	x	x	x	0	1	1	0
x	x	x	x	1	0	0	1
x	x	x	x	0	0	1	1

TABLE 4-3. TIME BASE GENERATOR OSCILLATOR FREQUENCIES AND DIVISIONS

BAUD RATE	OSCILLATOR FREQUENCY	DIVIDED BY	OUTPUT GATE ON A3
37.5	1.92 MHz	2^8	IC5N2
45.5	145.6 kHz	2^4	IC5N2
50	1.92 MHz	$2^6 \times 3$	IC5N2
56.8	181.8 kHz	2^4	IC5N2
61.12	195.584 kHz	2^4	IC5N2
74.2	118.720 kHz	2	IC5N2
75	1.92 MHz	2	IC7N4

is clocked to produce output signal at A3IC5N2 that is divided by 16.

(5) The time base generator output signal (11) is 200 times the baud rate. This timing signal is fed to the timing control circuit through card connector A4-4.

c. TIMING CONTROL CIRCUIT. The CHARACTER RELEASE switch programs the timing control circuit on card A4 to operate in one of two modes: free run or single character. Figure 4-3 shows the circuit configuration for the various modes of operation.

(1) In the free run mode, flip-flop A4IC7 constantly enables timing signal gate A4I C6N1 because of the ground applied to the S_D input of the flip-flop by the CHARACTER RELEASE switch. This allows the internal or external time base signal to toggle flip-flop A4IC2F2 and to enable A4IC9N1 at every positive half cycle.

(2) In the single character mode, the timing control circuit provides the master timing signal (14) for the length of one character plus an extra half bit to allow for any distortion applied to the output message. Flip-flop A4IC7 enables NAND A4IC6N1, permitting the internal or external timing signal to pass.

(3) In the SINGLE CHARACTER position, the CHARACTER RELEASE switch applies a high signal to the S_D and C_D inputs of A4IC7 so that the flip-flop is controlled by the combination of three signals: an inverted positive step signal (17) from the SINGLE CHARACTER switch, $\overline{M}$ - the inverted output of the divide-by-100 counter (17), and a character end signal (18) from the stop mark circuit on card A6. When the SINGLE CHARACTER switch is pressed, a low signal is applied to A4IC7-5 (15) causing a high output at Q. This high Q (16) enables timing gate A4IC6N1 and feeds back to the set input gate, disabling it. The Q output remains high as long as no clear signal reaches the flip-flop. When the SINGLE CHARACTER switch sets flip-flop A4IC7, the $\overline{M}$ and character end signals to the clear input gate are high so that no clear signal can reach the flip-flop. The M signal goes low on every bit, but the character end signal remains high to inhibit the clear input gate. After one character is generated, the character end signal goes low to enable the clear input gate of A4IC7. However, at this point the $\overline{M}$ signal is high until half a bit later when it goes low to clear the flip-flop and disable timing tate A4IC6N1. While timing gate A4IC6N1 is enabled, the time base generator signal (11A) is divided by 2, as in the free run mode, to supply a times-100 master timing signal to the divide-by-100 counter.

d. Divide-by-100 Counter. The divide-by-100 counter is a binary coded decimal (BCD) counter consisting of two four-stage decade counters - a units and a tens in series. The units counter is on A5; the tens counter on A7. The outputs of each stage of the decade counters are gated so that the decade counters divide their input signal by 10. The counter outputs which are gated to control the count are listed in table 4-4. Figure 4-10D shows the output waveforms and timing in the two decade counters. The output of the tens counter, the M (or $\overline{M}$) signal (19), clocks the bit counter and controls switching in the timing control and signal processing circuits. The outputs of all stages of the two decade counters are supplied to the distortion trigger circuit which provides the distortion trigger for the signal processing circuit on the A8 card.

e Bit Counter. The bit counter on card A10 consists of a four stage binary counter and NAND gates which generate bit gating pulses, the stop circuit enable signal, and the character advance signal. The bit-gating pulses are produced by gating the output of the four stage counter, and are used to time the message generating circuits. The stop circuit enable signal and character advance signals occur at the end of each character to initiate stop mark generation and to clock the character counter. The following description covers bit counter operation in the start/stop mode of transmission; refer to paragraph 4-2n for differences during synchronous transmission.

(1) The bit counter operates by gating bit pulse 6, for 5-level code. This pulse

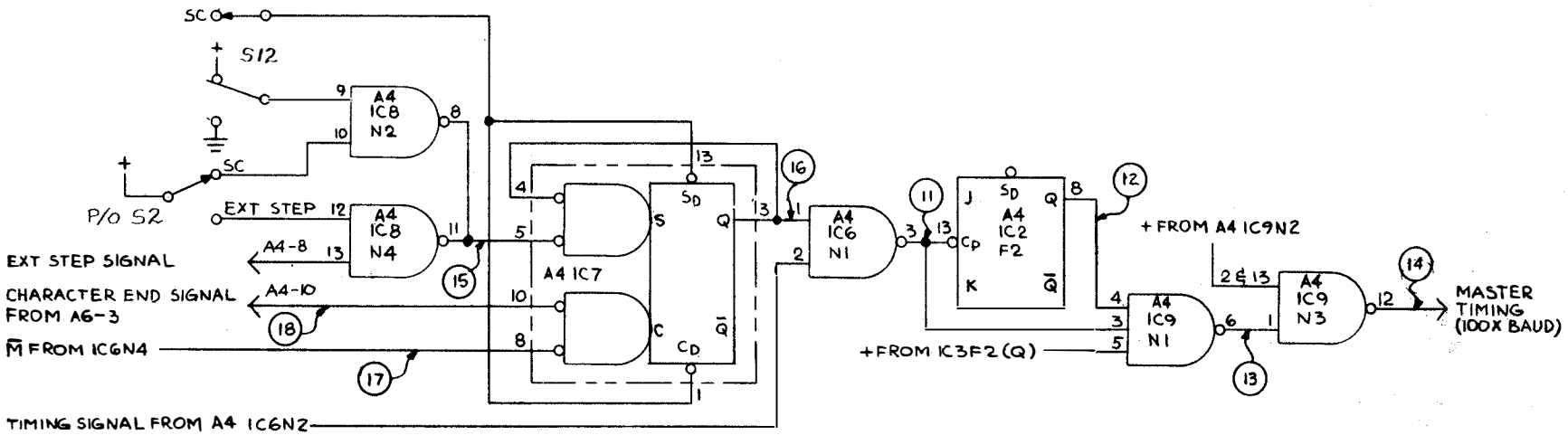


Figure 4-3. Timing Control Circuits, Simplified Schematic

TABLE 4-4. BCD COUNTER GATE INPUTS

GATE	INPUTS						
	E	$\overline{E}$	G	$\overline{G}$	H	$\overline{H}$	I
A5IC1N1		x				x	
A5IC1N2		x					x
A5IC6N1	x			x			
A5IC1N4		x					x
A5IC1N3		x				x	
A5IC6N2	x			x			
A5IC6N3						x	
A5IC6N4		x					x
	J	J	K	$\overline{K}$	L	L	M
A7IC1N1		x				x	
A7IC1N2		x					x
A7IC6N1	x			x			
A7IC1N4		x					x
A7IC1N3		x				x	
A7IC6N2	x			x			
A7IC6N3						x	
A7IC6N4		x					x

acts as the stop enable pulse and thus initiates the bit counter reset process as described below.

(2) Flip-flops A101C1F1 and A101C7F2 are connected as an up-counter, producing a normal counting sequence up to point Z as shown in figure 4-10E. The output of the divide-by-100 divider, M, which is at the bit rate, toggles the first bit counter flip-flop A10IC1F1. NANDs A10IC6N2 through A10IC5N1 receive the counter outputs required to produce the five bit gating pulses (36-40) and the stop circuit enable signal (41), as shown in figure 4-10E. Table 4-5 lists the counter signals gated by the NANDs to produce the bit gating pulses and stop circuit enable signals.

(3) NAND A10IC5N1 takes counts $\overline{AA}$, $\overline{BB}$, CC and $\overline{DD}$ to produce a pulse starting on the sixth bit. NAND A101C10N2 is enabled to pass this pulse on the sixth bit. This inhibit pulse (42) prevents subsequent clock pulses from toggling A101C1F1. As a result, at point Z (figure 4-10E) the M signal does not set A101C1F1. The inhibit pulse is inverted by A101C8N1 (42), removing the S_D signal from stop circuit flip-flops A61C4F1 and F2 and arming the inputs of A61C4F1 to allow it to toggle at the next negative transition of the M signal. The negative transition of the EE output of A61C4F1 toggles A61C4F2.

(4) At time t_9 (figure 4-10E) the inhibit pulse (42) in the bit counter is still low. At this point A61C3N3 receiving $\overline{EE}$ and FF signals enables, passing a negative transition to A61C1N3 (45). This stop mark trigger signal (45) is inverted and applied to the S_D inputs of the bit counter flip-flops, causing all four flip-flops to set at time t_9. NAND A6IC3N3 is thus inhibited, having remained enabled only long enough for its output to take effect, and the S_D inputs are removed from flip-flops A10IC1F1 through A10IC7F2. Since the inhibit pulse (42) went high when the sixth bit pulse (41) returned to a low, flip-flop A10IC1F1 is now armed to change state at time t_{10}.

(5) From time t_{10} the bit counter goes through the sequence, providing the five bit gating pulses and stop circuit enable signal. The five bit gating pulses (36-40), applied to the message and character generating circuits, are each one bit wide and correspond to successive bits in the character code. The sixth bit pulse (41) is one bit wide plus the width of the stop mark.

(6) A character advance signal is produced by inverting the stop circuit enable signal (41); this pulse occurs once each character and is used to clock the character counter. At the end of each character, the stop circuit enable signal enables the stop mark generation circuit which determines the length of the stop mark in the output message.

TABLE 4-5. BIT COUNTER GATE INPUTS

A10 GATE	INPUTS							
	AA	$\overline{AA}$	BB	$\overline{BB}$	CC	$\overline{CC}$	DD	$\overline{DD}$
IC6N2	x		x		x		x	
IC4N2		x		x		x		x
IC4N1	x			x		x		x
IC3N1		x	x			x		x
IC2N2	x		x			x		x
IC5N1		x		x	x			x
IC5N2	x			x	x			x
IC3N2		x	x		x			x
IC6N1	x		x		x			x

f. STOP MARK CIRCUIT. The stop mark circuit on A6 and A4 generates three trigger signals which produce a stop mark of either 1.0, 1.42, or 2.0 bits duration in the output message. These 3 signals are divide-by-100 and bit counter set signals, and stop and set/clear signals for the signal processing circuit. A character end signal for the timing control circuit is also generated. In synchronous operation the stop mark circuit is disabled as described in paragraph 4-2n.

(1) In the description of the bit counter, the generation of the EE and FF signals in the stop mark circuit was described in relation to the bit counter set signal. That description was for a stop mark of 2.0 bits duration. The following paragraphs describe the generation of stop mark signals for the 1.0 and 1.42, bit stop marks. Figure 4-4 is a simplified schematic of the stop mark circuit. Figure 4-10F shows the timing of the signals in the stop mark circuit. For a stop mark of 1.0 bit, A6IC7N3 is enabled and A6IC3N1 is disabled. The output of A6IC2N6, which is EE and $\overline{FF}$, is the only signal affecting the bit counter set signal (45) out of A6IC1N3. As shown in figure 4-10F, the bit counter set signal, a high, is produced after one complete cycle of the M signal - one bit. This set signal is inverted and applied to the S_D inputs of the bit counter flip-flops. The effects of the bit counter set signal were described in the section on the bit counter.

(2) Since the divide-by-100 counter produces 100 counts during each bit, triggers for a 1.42 bit stop mark are produced by gating divide-by-100 counter signals, which causes the counter to restart on the 42nd and 50th counts. By setting the divide-by-100 counter to restart, the M signal which clocks the stop mark flip-flops is set to change the outputs of flip-flops A61C4F1 and F2. Changing the outputs of A61C4F1 and F2 produces the bit counter set signal (45) and the signals for the signal processing circuit at the proper time after the last character bit. See Figure 5-12.

(3) NAND A6IC5N1 receives the J, $\overline{K}$, L, and $\overline{M}$ signals from the divide-by-100 counter, producing a low output (51) during counts 40 to 50 of the divide-by-100 counter. The inverted output of A6IC5N1 is used for only the 1.42, stop mark.

(4) When 1.42 is selected by the STOP LENGTH switch, NAND A6IC1N4 is enabled, gating the $\overline{E}$ signal of the divide-by-100 counter. The output of A6IC1N4 (52) is dot-ANDed with the signal from A61C2N2 and applied to A61C3N1, along with the output of A6IC2N6 and an enable signal from STOP LENGTH switch. As shown in figure 4-10F, the output of A6IC1N4 (52) goes high on the 41st count of the divide-by-100 counter. This signal produces a negative pulse at A6IC3N1 (54A) which fires single-shot A61C6. The output (55A) of A6IC6 sets the divide-by-100 counter, clearing flip-flop A6IC4F2. Clearing A6IC4F2 causes the Q output (56A) to go high at count 41.

(5) The divide-by-100 counter set signal from A6IC6 occurs on count 41 and is over by the time the next times-100 clock pulse is applied to the first stage of the counter. This next times-100 clock pulse clears the divide-by-100 counter so the M signal (19) goes negative on count 42. This transition of the M signal does two things: (a) sets flip-flop A4IC2F1 and (b) clears flip-flop A6IC4F1.

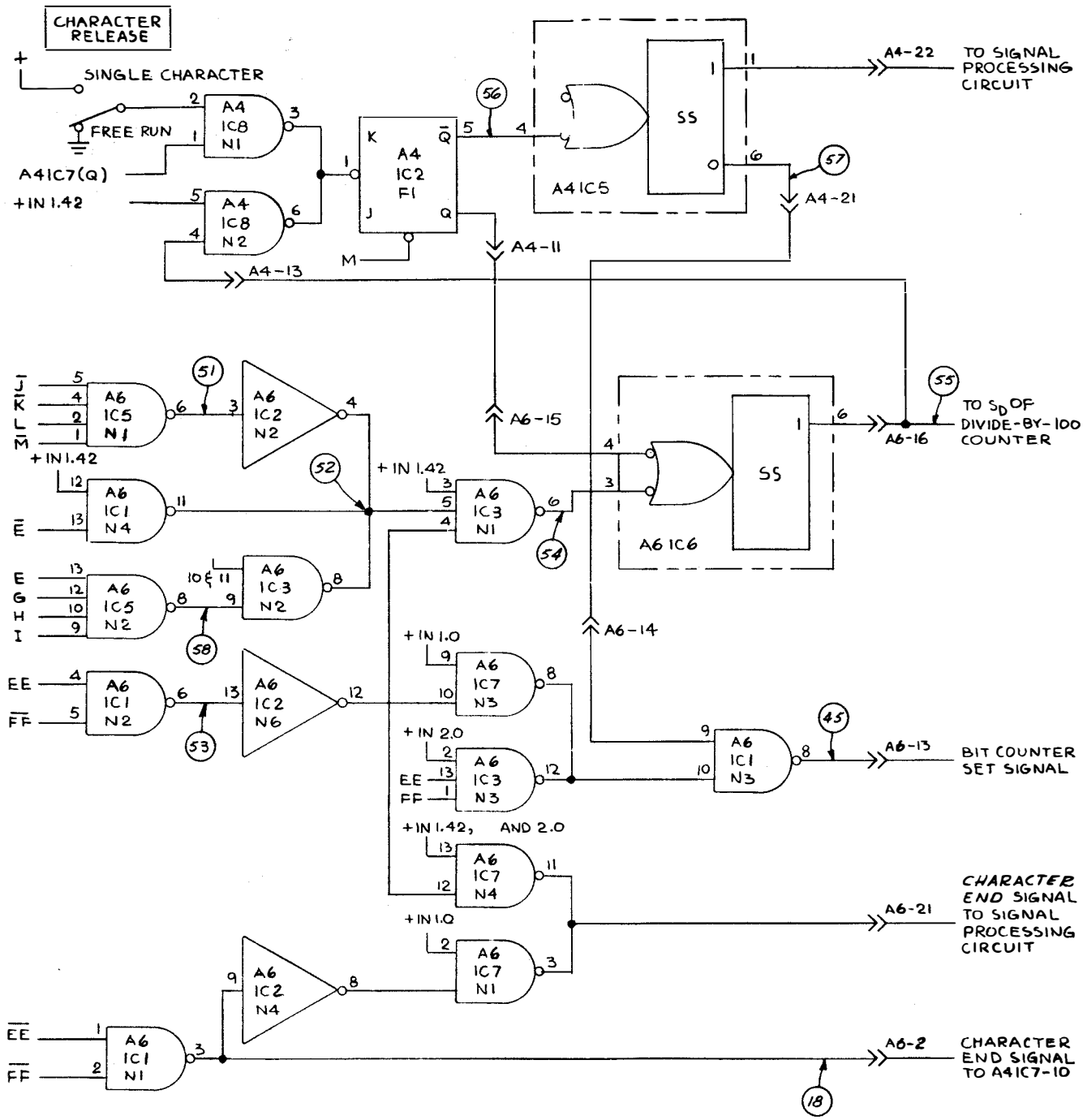


Figure 4-4. Stop Mark Generating Circuits, Simplified Schematic

(6) The M signal sets flip-flop A4IC2F1 through the S_D input on count 42. When the flip-flop is set, the $\overline{Q}$ output goes low, firing single-shot A4IC5. The negative going 0 output (57A) of A4IC5 is applied to NAND A6IC1N3. The output of A6IC1N3, the bit counter set signal, is a positive pulse on count 42. Setting the bit counter removes the stop circuit enable signal (41) is described in the section on the bit counter.

(7) Just before the stop enable signal is removed, the negative transition of the M Signal on count 42 clears A6IC4F1 so that there is a short negative pulse at the EE output. Clearing A6IC4F1 on count 42 also caused A6IC4F2 to be set.

(8) The character end signal (18), which is used by the timing control circuit in the SINGLE CHARACTER mode, is generated by NAND A6IC1N1. NAND A6IC1N1 gates the $\overline{EE}$ and $\overline{FF}$ signals to produce a negative going transition used as the single character release circuit on A4. Figure 4-10F shows that the character end signal occurs at the time the stop circuit enable signal (41) goes high, regardless of the setting on the STOP LENGTH switch.

(9) A stop signal output at A6-21, applied to the signal processing circuit on A8, uses the outputs (18 and 53) of A6IC1N1 and A6IC1N2. For the 1.0 bit stop mark, A6IC7N1 is enabled to provide a positive going transition at the end of the 1.0 bit stop mark. For 1.42, and 2.0 bit stop marks, A6IC7N4 is enabled to provide a positive transition after one bit because of the output of A6IC1N2.

g. CHARACTER COUNTER. The character counter, on A14 and A9, is clocked by the character advance signal (same as 42) from the bit counter so that it counts once for each complete cycle of the bit counter. The character counter operates in one of three modes: (1) a message mode, in which it counts 80 characters and resets, and (2) a selected character mode, or (3) word mode in which it counts 75 characters (72 character, 2 carriage returns and line feed).

(1) In the message mode the counter, made up of seven flip-flops, acts as a natural binary or chain up-counter as shown in figure 4-10G. NAND A9IC1N1 receives counter outputs JJ, $\overline{KK}$, $\overline{LL}$, and MM, A9IC3N4 inverts the resulting output (see figure 4-10H, no. 66) which is applied to NAND A14IC10N2 along with counter outputs GG, HH, and II and an enable signal from the SIGNAL PATTERN switch. The output (74) of A15IC10N2 (binary 1001111, decimal 79) is double inverted through A14IC5N1 and parallel NANDs A14IC9N6 and A14IC5N3 to become the set direct pulse (74) for the character counter flip-flops. Figure 4-10I shows the timing of the set direct pulse. The set direct pulse sets all seven counter stages on the 79th count. The 80th character advance signal toggles the first stage, clearing the character counter to begin a new counting sequence.

(2) As shown in figure 4-10I, NANDs A14IC6N2 and N3 produce pulse (84 and 86) for counts 79 through 2 and 2 through 5, respectively. The inversions of these pulses control A14IC5N2 so that there is a positive pulse output (88) from count 79 through count 5. This positive pulse is inverted (89) by A14IC9N5 and is applied to A15IC4N1 to inhibit the output of the memory unit while the output of the call letter matrix is being used.

(3) In the selected character or word mode, the character counter is changed to two counters. The first three stages are made into a divide by six counter and the next four into a divide by 12 counter. After a count of 72 characters three special characters are generated, which are two carriage returns and a line feed.

(4) The character counter generates two sets of matrix address signals: one set for the Fox message memory unit, A12IC1, and another set for the call letter matrix. Character counter outputs GG through MM (59-65) are applied directly to the memory unit inputs as part of the address for the characters of the Fox message.

(5) The call letter matrix requires separate character wide pulses for each

of its six characters. These character wide pulses (87-83) are produced by gating the outputs of the character counter as shown in figure 4-10I. When the SIGNAL PATTERN switch is in CHARACTER, NANDs A91C3N1 and N2 are disabled and provide a positive signal to the character pulse gating NANDs (A141C1, 1C2, and 1C7). By applying this constant positive signal, the gating NANDs are controlled by only the outputs of the GG, HH, and II flip-flops.

(6) For call letter generation, NANDs A91C3N1 and N2 are enabled to gate the outputs of the JJ, KK, LL, and MM flip-flops. The character pulse gating NANDs provide six successive character wide pulses to the call letter matrix with every cycle of the character counter (every 80 characters).

(7) Fox Message Generation. A memory circuit is preprogrammed to produce the Fox message. The required characters are stored at sequential addresses that require only a straight binary count input. A second, programmable, matrix produces local call letters, which are inserted into blanks left in the Fox message.

(8) The GG through MM outputs of the character counter are applied to the address inputs of memory unit A12IC1. As the count progresses, each count enters the address portion of the memory unit and produces a binary-coded character. Table 4-6 summarizes the input-output relationship of the memory unit. The first column shows the alphabet character ultimately fed into the tele-typewriter. The second column shows the count that is applied to the address portion of the unit. The third column shows the binary-coded output. The five character bits correspond to the alphabet portion of the standard five-unit start-stop teletypewriter code; for example, binary 10100 is equivalent to the letter "S".

TABLE 4-6. MEMORY UNIT BIT PATTERNS

ALPHABET CHARACTER	ADDRESS INPUTS							OUTPUTS				
	A64	A32	A16	A8	A4	A2	A1	B1	B2	B3	B4	B5
Cr	1	0	0	0	0	1	1	0	0	0	1	0
Cr	1	0	0	0	1	0	0	0	0	0	1	0
Lf	1	0	0	0	1	0	1	0	1	0	0	0
Lt	1	0	0	0	1	1	0	1	1	1	1	1
T	1	0	0	0	1	1	1	0	0	0	0	1
E	1	0	0	1	0	0	0	1	0	0	0	0
S	1	0	0	1	0	0	1	1	0	1	0	0
T	1	0	0	1	0	1	0	0	0	0	0	1
Sp	1	0	0	1	0	1	1	0	0	1	0	0
D	1	0	0	1	1	0	0	1	0	0	1	0

TABLE 4-6. MEMORY UNIT BIT PATTERNS (cont)

ALPHABET CHARACTER	ADDRESS INPUTS							OUTPUTS				
	A64	A32	A16	A8	A4	A2	A1	B1	B2	B3	B4	B5
E	1	0	0	1	1	0	1	1	0	0	0	0
Sp	1	0	0	1	1	1	0	0	0	1	0	0
↑ Programmable	1	1	1	1	1	1	1	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	0	0	0	0
	0	0	0	0	0	1	0	0	0	0	0	0
	0	0	0	0	0	1	1	0	0	0	0	0
	0	0	0	0	1	0	0	0	0	0	0	0
↓ Programmable	0	0	0	0	1	0	1	1	1	1	1	1
Sp	0	0	0	0	1	1	0	0	0	1	0	0
Sp	0	0	0	0	1	1	1	0	0	1	0	0
Sp	0	0	0	1	0	0	0	0	0	1	0	0
Sp	0	0	0	1	0	0	1	0	0	1	0	0
Lt	0	0	0	1	0	1	0	1	1	1	1	1
T	0	0	0	1	0	1	1	0	0	0	0	1
H	0	0	0	1	1	0	0	0	0	1	0	1
E	0	0	0	1	1	0	1	1	0	0	0	0
Sp	0	0	0	1	1	1	0	0	0	1	0	0
Q	0	0	0	1	1	1	1	1	1	1	0	1
U	0	0	1	0	0	0	0	1	1	1	0	0
I	0	0	1	0	0	0	1	0	1	1	0	0
C	0	0	1	0	0	1	0	0	1	1	1	0

TABLE 4-6. MEMORY UNIT BIT PATTERNS (cont)

ALPHABET CHARACTER	ADDRESS INPUTS							OUTPUTS				
	A64	A32	A16	A8	A4	A2	A1	B1	B2	B3	B4	B5
K	0	0	1	0	0	1	1	1	1	1	1	0
Sp	0	0	1	0	1	0	0	0	0	1	0	0
B	0	0	1	0	1	0	1	1	0	0	1	1
R	0	0	1	0	1	1	0	0	1	0	1	0
O	0	0	1	0	1	1	1	0	0	0	1	1
W	0	0	1	1	0	0	0	1	1	0	0	1
N	0	0	1	1	0	0	1	0	0	1	1	0
Sp	0	0	1	1	0	1	0	0	0	1	0	0
F	0	0	1	1	0	1	1	1	0	1	1	0
O	0	0	1	1	1	0	0	0	0	0	1	1
X	0	0	1	1	1	0	1	1	0	1	1	1
Sp	0	0	1	1	1	1	0	0	0	1	0	0
J	0	0	1	1	1	1	1	1	1	0	1	0
U	0	1	0	0	0	0	0	1	1	1	0	0
M	0	1	0	0	0	0	1	0	0	1	1	1
P	0	1	0	0	0	1	0	0	1	1	0	1
S	0	1	0	0	0	1	1	1	0	1	0	0
Sp	0	1	0	0	1	0	0	0	0	1	0	0
O	0	1	0	0	1	0	1	0	0	0	1	1
V	0	1	0	0	1	1	0	0	1	1	1	1
E	0	1	0	0	1	1	1	1	0	0	0	0
R	0	1	0	1	0	0	0	0	1	0	1	0

TABLE 4-6. MEMORY UNIT BIT PATTERNS (cont)

ALPHABET CHARACTER	ADDRESS INPUTS							OUTPUTS				
	A64	A32	A16	A8	A4	A2	A1	B1	B2	B3	B4	B5
Sp	0	1	0	1	0	0	1	0	0	1	0	0
T	0	1	0	1	0	1	0	0	0	0	0	1
H	0	1	0	1	0	1	1	0	0	1	0	1
E	0	1	0	1	1	0	0	1	0	0	0	0
Sp	0	1	0	1	1	0	1	0	0	1	0	0
L	0	1	0	1	1	1	0	0	1	0	0	1
A	0	1	0	1	1	1	1	1	1	0	0	0
Z	0	1	1	0	0	0	0	1	0	0	0	1
Y	0	1	1	0	0	0	1	1	0	1	0	1
Sp	0	1	1	0	0	1	0	0	0	1	0	0
D	0	1	1	0	0	1	1	1	0	0	1	0
O	0	1	1	0	1	0	0	0	0	0	1	1
G	0	1	1	0	1	0	1	0	1	0	1	1
Fg	0	1	1	0	1	1	0	1	1	0	1	1
	0	1	1	0	1	1	1	0	0	1	1	1
Sp	0	1	1	1	0	0	0	0	0	1	0	0
1	0	1	1	1	0	0	1	1	1	1	0	1
2	0	1	1	1	0	1	0	1	1	0	0	1
3	0	1	1	1	0	1	1	1	0	0	0	0
4	0	1	1	1	1	0	0	0	1	0	1	0
5	0	1	1	1	1	0	1	0	0	0	0	1
6	0	1	1	1	1	1	0	1	0	1	0	1

TABLE 4-6. MEMORY UNIT BIT PATTERNS (cont)

ALPHABET CHARACTER	ADDRESS INPUTS							OUTPUTS				
	A64	A32	A16	A8	A4	A2	A1	B1	B2	B3	B4	B5
7	0	1	1	1	1	1	1	1	1	1	0	0
8	1	0	0	0	0	0	0	0	1	1	0	0
9	1	0	0	0	0	0	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0	1	1	0	1

NOTE

Either of three fox message assemblies are used in the Signal Generator. Units with serial numbers A1 through A107 contain assembly A12 with part number 36021120. The operation of this assembly is discussed in paragraph (9a). Units with serial numbers B1 through B270 contain assembly A12 with part number 36021220. The operation of this assembly is discussed in paragraph (9b). Units with serial numbers D1 through D122 contain assembly A12 with part number 36021120-2. The operation of this assembly is discussed in paragraph (9c).

(9a) (Part Number 36021120) Address inputs develop the output bits, indicated in Table 4-6, at terminals 7 through 11 of A12IC1. Each of these discrete output signals is applied to one output of a two-input NAND gate. The marks and spaces for each character are present at pins 7 through 11 of A12IC1 for a period, the length of which is six bits plus the stop mark. Address read (A/R) pulses applied to the memory unit help maintain the memory output signal at the input of the NAND gates for the required time period. Therefore, at the proper bit time, a particular NAND gate is enabled by a bit gating pulse from the bit counter; the NAND gate then passes the output from the memory. The output signals are inverted to provide a pulse train (97) reflecting the character mark and space code as shown in figure 4-10J.

(9b) (Part Number 36021220) Address inputs develop the output bits, indicated in Table 4-6 at terminals 7 through 11 of A12JC1. Each of these discrete output signals is applied to one input of a two-input NAND gate. The marks and spaces for each character are present at pins 7 through 11 of A12IC1 for a period equal to six bits plus the stop mark. Address read (A/R) pulses applied to the memory help maintain the memory output signal at the input of the NAND gates during the required time period. Therefore, at the proper bit time, a particular NAND gate is enabled by a bit gating pulse from the bit counter; the NAND gate the passes the memory output signal to output flip-flop A12IC5. A/R pulses applied through monostables A12IC7 and A12IC6 synchronize output flip-flop A12IC5 to the memory. The resulting output signal is a pulse train that reflects the mark-space code of a character (97A) generated by the memory, which is delayed with respect to the internal timing.

(9c) (Part Number 36021120-2) Address inputs develop the output bits, indicated in

Table 4-6, at terminals 4 through 8 of A12IC1. Each of these discrete output signals is applied to one input of a two-input NAND gate. The marks and spaces for each character are present at pins 4 through 8 of A12IC1 for a period, the length of which is six bits plus the stop mark. Therefore, at the proper bit time, a particular NAND gate is enabled by a bit gating pulse from the bit counter; the NAND gate then passes the output from the memory. The output signals are inverted to provide a pulse train (97) reflecting the character mark and space code as shown in figure 4-10J.

h. CALL LETTER GENERATION. The station call letters are a part of the Fox Message output. These call letters are locally programmed on the matrix of card A13. As shown in table 4-6, the programmable characters are spaces in the memory unit A12IC1. During these characters the five call letters and a "figure" command are generated by the call letter matrix.

(1) The character counter generates six character-wide matrix address signals for the call letter matrix as described in paragraph 4-2g. A character-wide signal is applied to one of the six columns of the matrix for the length of six bits plus the stop mark length. During this time the marks and spaces for each character are present at the matrix outputs which are applied to separate NAND gates. The bit gating signals from the bit counter enable the output gates to release the bits of each character at the proper time, the same as for memory unit A12IC1.

(2) To program the five call letters on the call letter matrix (see figure 4-6), diode connections must be made between the diodes on the lines designated by numerals 1 through 5 and the vertical lines designated by letters A through F. Each terminal pair that is connected produces a mark for the position in the character location. For example, if it is desired to generate "FOX" as call letters, the letters are converted to the mark-space code. This action transcribes F to M-S-M-M-S, 0 to S-S-S-M-M, and X to M-S-M-M-M as shown in figure 3-2 and table 4-6. For each mark indicated, the respective diode terminal must be connected to the letter designated line as shown in figures 4-5 and 4-6. The call letter matrix also includes a figure command, which is factory programmed in the sixth row F.

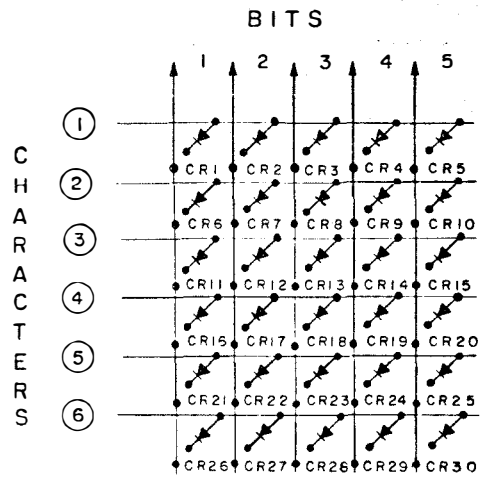


Figure 4-5. Programming Call Letter Matrix

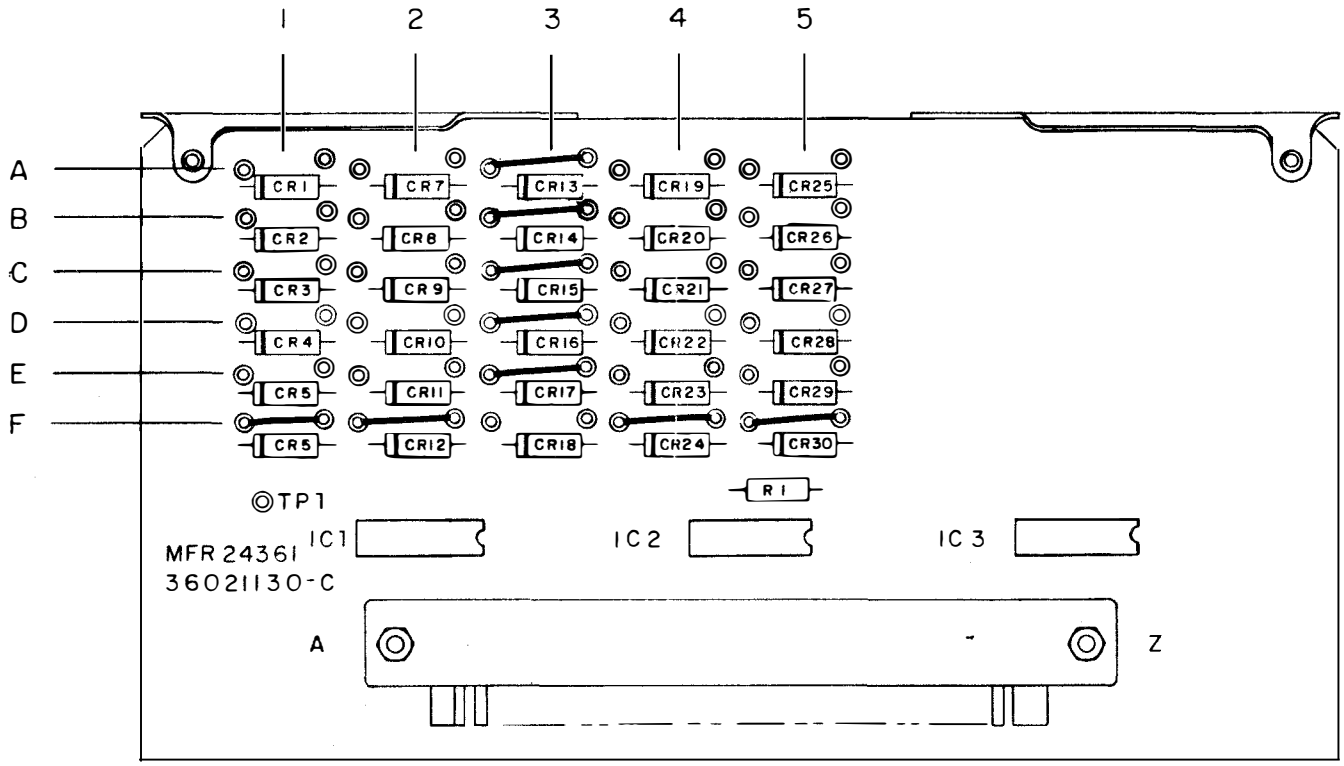
This may be reprogrammed if a sixth character is required by the call letters. The output of five call letters and the figure command is applied to message select gate A15IC4N1, which is enabled by the MESSAGE position of the OUTPUT switch.

i. SELECTED CHARACTER GENERATION. The front panel MARK-SPACE switches allow programming a character which is continuously repeated. The circuit generating the selected character is on card A12.

(1) Five NANDS on A11 are connected to one of the five MARK-SPACE switches with the five bit-gating pulses applied to the corresponding NANDs. By setting a switch to SPACE, a positive signal is applied to the corresponding NAND so that when the bit-gating pulse occurs the NAND output goes low. A positive mark is the output at A12-21 after inversion by A11IC3N1. If the switch is in MARK the corresponding NAND retains a high output during the bit-gating pulse applied to it so that a low-space-output-is at A11-21.

j. REVERSALS GENERATION. A reversal signal, consisting of a squarewave signal at half the bit rate, is provided when the OUTPUT switch is in REVERSAL. The reversal signal is taken from the AA signal (32) of the bit counter and is gated by NAND A131C2N1. The inverted AA signal from A131C2N1 is applied to message select gate A151C4N2 and passed to the signal processing circuit on A8. The OUTPUT switch also enables A101C10N1 and A61C7N2. NAND A101C10N1 gates the eight bit pulse which sets the bit counter through A61C7N2 and A61C6N3. Since the bit counter is set on an even number of counts, the AA signal is a constant squarewave.

k. WORD GENERATION. A 6-character programmed word is generated in the same manner as call letter generation, except that the format is 72 continuous characters, two carriage returns and a line feed. The word is programmed by placement of shorting bars in a word matrix board using the character code of figure 3-2. See figures 4-7 and 4-8.



NOTES:

1- FOR STRAGGING, USE APPROXIMATELY 3/4" OF AWG 22 OR 24 SOLID TINNED BUS WIRE.

2- USE STANDARD PRINTED CIRCUIT BOARD SOLDERING TECHNIQUES.

3- THIS BOARD IS NORMALLY SUPPLIED WITH ALL SPACES (NO JUMPERS).

Figure 4-6. Strapping for Call Letter Matrix Board

TABLE 4-7. PROGRAMMABLE MATRIX 1A1A13

CALL LETTER NO.	BIT NO.				
	1	2	3	4	5
1	CR1	CR7	CR13	CR19	CR25
2	CR2	CR8	CR14	CR20	CR26
3	CR3	CR9	CR15	CR21	CR27
4	CR4	CR10	CR16	CR22	CR28
5	CR5	CR11	CR17	CR23	CR29
6	CR6	CR12	CR18	CR24	CR30

1. DISTORTION TRIGGER GENERATION. The output signal of the signal generator can contain distortion in amounts from 1 to 49 percent. The following description covers the triggers that eventually cause the bias or end distortion, whereas the process of generating distortion in the output signal is covered later in paragraph 4-2m.

(1) The divide-by-100 BCD counter consists of a units counter and a tens counter. Each of these has an associated one out of ten decoder. The tens decoder produces sequential triggers representing 0 through 40, which are ten times as wide as the units triggers. Figure 4-10K shows the waveforms for the 10 units triggers.

(2) The PERCENT DISTORTION switches, one for units and one for tens, select the proper count into the B/D converter by inhibiting one or the other of complementary count outputs. NAND A51C4Na receives the desired units count and produces downcounted logic 0 triggers (98). The COUNTER OUTPUTS are also inverted and applied to NAND A5IC4N2, producing up- counted logic 0 triggers (99). The tens section works similarly. Figure 4-9 shows the gating used to obtain the distortion triggers.

m. SIGNAL PROCESSING CIRCUIT. Up to this point, all the signal components-- the coded message, the stop mark trigger, and the distortion triggers -- exist independently. Card A8 brings together these components and processes them to produce the desired signal configuration. Basically, the output signal is processed to have no distortion, or either bias or end distortion; since the circuitry is used slightly differently when distortion is generated, the following paragraphs explain what happens when the various percentages of bias distortion are selected.

(1) Bias Distortion. Bias distortion affects the leading edge of the mark character bits. It is "mark bias", if the leading edge occurs before it should; or, it is "space bias", if the leading edge occurs after it should. Mark bias distortion is discussed first.

(2) With the DISTORTION SELECT switch set to MARK BIAS, a logic 1 is applied to the K input of flip-flop A8IC4F1. The input to NAND A8IC1N2 is a logic 0, producing a logic 1 output. The $\overline{Q}$ output is a logic 1 and enables NAND A8IC8N2; its Q output is a logic 0, inhibiting NAND A8IC8N1.

(3) The other inputs to NAND A81C8N2 are the units and tens down-count distortion triggers (106) and the times-100 timing signal (16). Assuming a setting of 20 percent distortion, the output of A81C8N2 appears as waveform 100A figure 4-10L. This is applied to one of the set inputs to flip-flop

A81C5. (Flip-flop A81C5 has been cleared at the C_D input by the character reset trigger from A4-22 applied through NAND A81C9N2; N2 is enabled by Vcc through resistor A8R2). The other input results as follows. The message -- the character R is chosen here as an example because it begins with a mark bit followed by a space bit -- is dot-ORed with the $\overline{M}$ signal and is applied to NAND A81C3N2 (NAND A81C3N2 is enabled by V_{CC} applied through resistor A8R2; A81C3N1 is inhibited by a ground from the MARK BIAS position of the DISTORTION SELECT switch.) The A81C3N2 output is inverted by inverter A81C2N1, applying a logic 1 to arm the K input to flip-flop A81C4F2 at time t_1. At the same time, the $\overline{M}$ signal fires single-shot A81C6, producing a trigger that toggles A81C4F2 to the clear state. Thus, its Q output goes to logic 0 to arm the set input to A81C5. When distortion trigger occurs at time t_2, A81C5 sets. At time t_3, the A81C3N2 output (102A) is at logic 1, arming the J input to A81C4F2; thus the flip-flop sets at time t_3 with the A81C6 single-shot output (103). The $\overline{Q}$ output of A81C4F2 is therefore logic 0, NANDing with the logic 0 transition of the M signal (21) at time t_4. This clears flip-flop A81C5 at time t_4. With the DISTORTION SELECT switch set to MARK BIAS, NAND A81C9N1 is inhibited, and NAND A81C9N4 is enabled. NAND A81C9N4 takes the $\overline{Q}$ output of A81C5 and inverts it, producing the equivalent of the Q output which is sent to output circuit.

(4) When the DISTORTION SELECT switch is set to SPACE BIAS, the J input to flip-flop A81C4F1 is armed, permitting the stop circuit signal to toggle A8IC4F1 to the set state. The logic 1 output at Q then arms NAND A81C8N1, while the logic 0 output at $\overline{Q}$ inhibits NAND A81C8N2. Thus, the up-count distortion triggers (107) are passed instead of the down-count triggers (106). These triggers provide a pulse at the set input gate of flip-flop A81C5 to set the flip-flop, the results are the same as those described for mark bias, except that the mark bit begins 20 percent later than it would with no space bias distortion.

(5) When the DISTORTION SELECT switch is in SWITCH BIAS, both the J and K input gates of flip-flop A81C4F1 are armed so that the flip-flop is toggled by the stop circuit signal from A6-21 which occurs at the end of each character. The Q and $\overline{Q}$ outputs enable the up-count then down-count gates, A81C8N1 and N2, alternately with each character. In this way the bias distortion of the output alternates between mark and space bias with each successive character.

(6) End Distortion. End distortion affects the trailing edge of the mark character bits. It is "mark end" if the trailing edge occurs after it should, "space end" if the trailing edge occurs before it should.

(7) With the DISTORTION SELECT switch set to SPACE END, a down-count distortion trigger is passed to flip-flop A8IC5 in the same manner as for mark bias distortion. NAND A8IC3N1 is enabled by V_{cc} through resistor A8R1, so the dot-ANDed message and start bit signal is inverted by A8IC3N6, and is passed and inverted by A8IC3N1 (figure 4-10M). This signal is applied to flip-flop A8IC4F2 at the J input and its complement is applied to the K input. Pulses from monostable A8IC6 clock the flip-flop, producing the message at A8IC5 input terminals 4 and 10.

(8) The character reset signal from A4-22, unlike the situation with bias distortion, is passed by NAND A81C9N3 to the S_D input of flip-flop A81C5. Thus, when the logic 0 transition of the A81C4F2 $\overline{Q}$ output output NANDs with the logic 0 transition of the M signal, A81C5. Then the Q of A81C4F2 goes to logic 0 and NANDs with the A81C8N1 distortion trigger to set A81C5.

(9) NAND A81C9N1 is enabled through resistor A8R1, it receives the Q output of A81C5 and inverts it. This is fed to the output circuit on A16 as the composite message signal.

(10) When the DISTORTION SELECT switch is in MARK END, the up-count distortion triggers at A81C8N2 are selected. These,

instead of the down-count triggers, set flip-flop A81C5, resulting in the mark trailing edges ending at a point coincident with the up-count trigger, which occurs at a later time than with no mark end distortion.

(11) Signal Pattern switch allows selecting a steady space or a steady mark output signal in addition to the message or other outputs. When the Signal Pattern switch is in STDY SPACE, the output line to the output drivers on A16 is grounded for any positive signals present so that there is a constant low provided. When the Signal Pattern switch is in STDY MARK, both NANDs A81C9N1 and N4 are constantly disabled so that they supply a constant high signal to the output circuit on A16.

n. SYNCHRONOUS MODE OF TRANSMISSION. In the synchronous mode of transmission, there is no stop mark or start space in the signal generator output signal so that one character code directly follows another. This mode of transmission requires disabling the stop mark circuit so that the bit counter is restarted after the last bit of each character.

(1) Refer to card A6 circuits. With the SYNC-START/STOP switch in SYNC position NAND A61C7N2 is enabled. The start of the sixth bit pulse, which initiates stop mark generation in the start/stop mode, is passed by A61C7N2. With NAND A61C7N3 inhibited by logic 0 through resistor A6R2, its output is a logic 1, permitting NAND A61C6N3 to pass the leading edge of the sixth bit pulse. The other input to A61C6N3 is a logic 1 from disabled single-shot A41C5. NAND A101C3N3 inverts the leading edge to a negative going transition which is applied to the bit counter flip-flops as an S_D input, starting the counter in a new cycle.

(2) Since the character counter is clocked by every cycle of the bit counter, it is clocked after each character code with no interruption of the start space and stop mark. The message generating circuits, which use the bit counter and character counter outputs, thus produce the selected message without interruption.

o. OUTPUT CIRCUIT. The output circuit of the signal generator, on card A16, contains a low level driver and a relay driver. The low level driver and a relay driver. The low level driver provides polar output at the LOW LEVEL jacks. The relay driver operates an electronic relay which controls a neutral or polar output at the HIGH LEVEL OUTPUT jacks.

(1) Low level preamplifier A16Q2-Q1 receives the message output of the signal processing circuit on A8. The preamplifier provides a signal that controls the conduction of transistors Q9-Q10, which in turn control transistor Q8, and Q11, respectively. When the message input at A16-17 is a mark (positive) bit, A16Q10 conducts, forcing A16Q11 into conduction. This action places a nominal 6.8 volt positive voltage at the LOW LEVEL OUTPUT terminals. A space (negative) bit causes A16Q9 and A16Q8 to conduct, thereby applying a nominal 6.8 volt negative voltage at the LOW LEVEL OUTPUT terminals.

(2) The relay driver is similar to the preamplifier circuits for the low level driver. The output of the relay driver controls an electronic relay which closes the loop connected to the HIGH OUTPUT jack when a mark occurs in the message input signal. Loop can be supplied either by an external source or by an internal supply, as selected by front panel HIGH LEVEL OUTPUT MODE switch S5.

(3) The output switch S5 controls the type of output supplied at the HIGH LEVEL OUTPUT jack. In the Ext POLAR position S5 allows the high level preamplifier to control electronic relay K1, which provides polar signals at the HIGH LEVEL OUTPUT jack utilizing an external polar battery voltage applied to the unit through connector J5. When S5 is in EXT NEUT, the output signal is derived from one half of the electronic relay. This action permits current to flow for a mark condition and inhibits current flow for a space. The source of power is external for this switch position and is applied through front and rear panel HIGH LEVEL OUTPUT jacks. In the INT

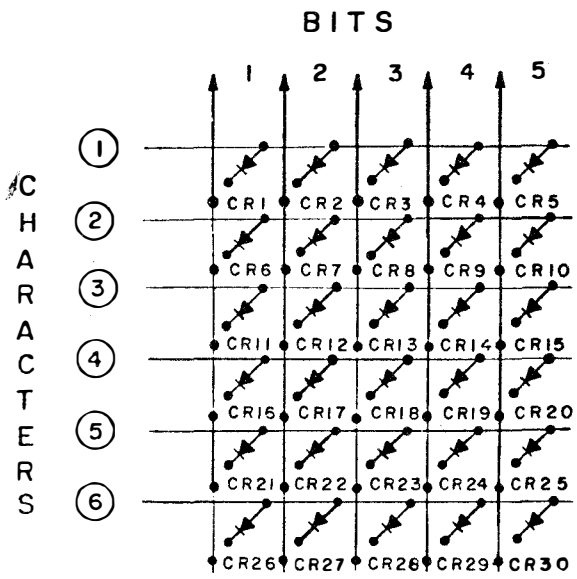
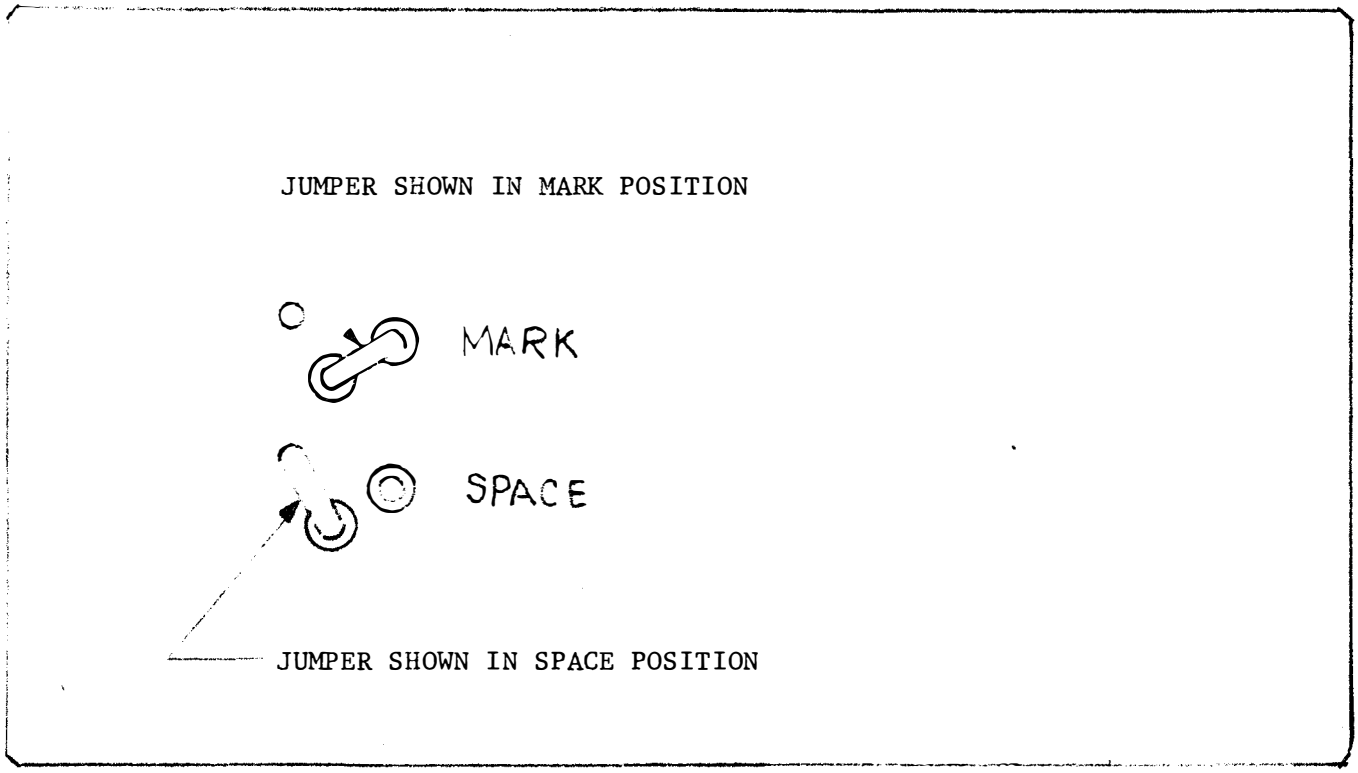


Figure 4-7. Programming Word Matrix 1A2

NEUT position, switch S5 connects an internal 130-volt supply to provide the internal loop current, while the electronic relay controls the current in accordance with the message signals.

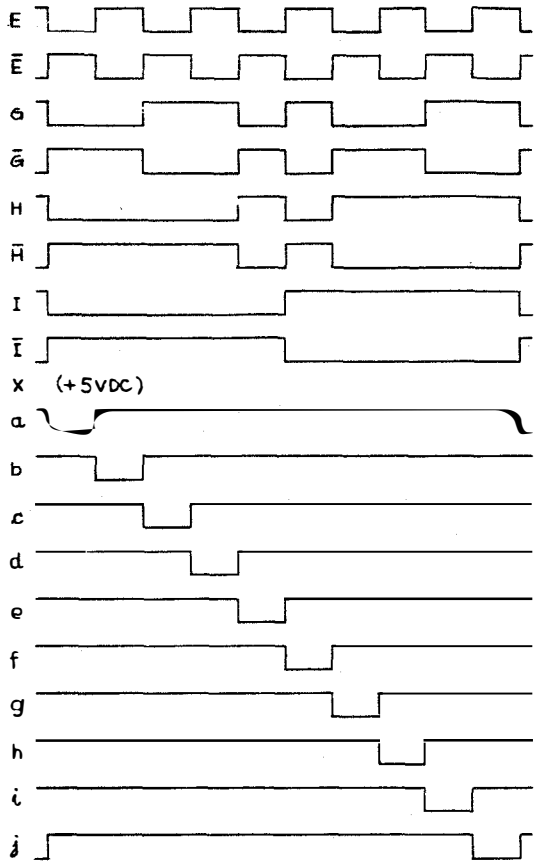
(4) A front panel LOOP POLARITY switch permits the polarity of the high level output signals to be reversed when operated to the + position. In addition, the loop current can be monitored by a LOOP CURRENT meter and adjusted using a front panel LOOP ADJ control.

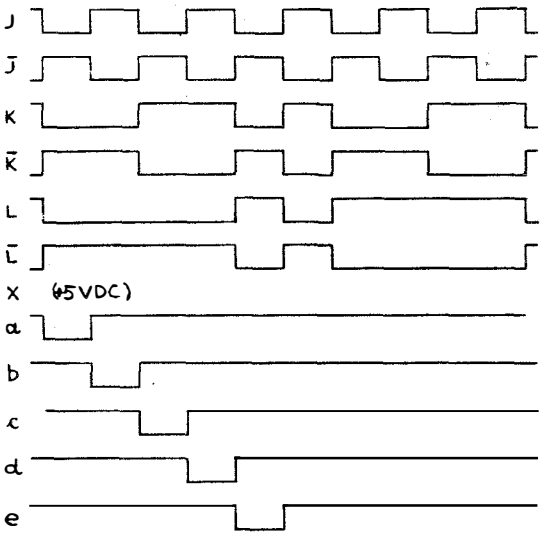
(5) A signal lamp on the front panel is also controlled by the output circuit. A mark in the message signal causes transistor A16Q3 to conduct allowing current to pass through the SIGNAL lamp causing it to light.



This illustration shows the position of the strapping plugs for obtaining either marks or spaces.

Figure 4-8. Strapping for Word Matrix





PERCENT SETTING	A5 IC7 N2 (6)	A5 IC7 N1 (3)	A5 IC8 N1 (3)	A5 IC7 N3 (8)	A5 IC9 N4 (11)	A5 IC8 N2 (6)	A5 IC9 N1 (3)	A5 IC9 N2 (6)	A5 IC7 N4 (11)	A5 IC8 N4 (11)	A5 IC8 N3 (8)	A5 IC9 N3 (8)	A5 IC5 N6 (12)	A5 IC5 N4 (8)	A5 IC5 N5 (6)	A5 IC5 N2 (4)	A5 IC4 N1 (6)	A5 IC4 N2 (8)
0	X	Ē	X	Ḡ	X	H̄	X	Ī	E	G	H	I	Ē	Ḡ	H̄	Ī	a	j
1	E	X	X	Ḡ	X	H̄	X	Ī	Ē	G	H	I	E	Ḡ	H̄	Ī	b	i
2	X	Ē	G	X	X	H̄	X	Ī	E	Ḡ	H	I	Ē	G	H̄	Ī	c	h
3	E	X	G	X	X	H̄	X	Ī	Ē	Ḡ	H	I	E	G	H̄	Ī	d	g
4	X	Ē	X	Ḡ	H	X	X	Ī	E	G	H̄	I	Ē	Ḡ	H	Ī	e	f
5	E	X	G	X	X	H̄	I	X	Ē	Ḡ	H	Ī	E	G	H̄	I	f	e
6	X	Ē	X	Ḡ	H	X	I	X	E	G	H̄	Ī	Ē	Ḡ	H	I	g	d
7	E	X	X	Ḡ	H	X	I	X	Ē	G	H̄	Ī	E	Ḡ	H	I	h	c
8	X	Ē	G	X	H	X	I	X	E	Ḡ	H̄	Ī	Ē	G	H	I	i	b
9	E	X	G	X	H	X	I	X	Ē	Ḡ	H̄	Ī	E	G	H	I	j	a

UNITS DISTORTION TRIGGERS

PERCENT SETTING	A6 IC7 N2 (6)	A6 IC7 N1 (3)	A6 IC8 N1 (3)	A6 IC7 N3 (8)	A6 IC9 N4 (11)	A6 IC8 N2 (6)	A6 IC7 N4 (11)	A6 IC8 N4 (11)	A6 IC8 N3 (8)	A6 IC5 N6 (12)	A6 IC5 N4 (8)	A6 IC5 N3 (6)	A6 IC4 N1 (6)	A6 IC4 N2 (8)
0	X	J̄	X	K̄	X	L̄	J	K	L	J	K	L̄	a	e
10	J	X	X	K̄	X	L̄	J	K	L	J	K	L̄	b	d
20	X	J	K	X	X	L̄	J	K̄	L	J	K	L̄	c	c
30	J	X	K	X	X	L̄	J	K̄	L	J	K	L̄	d	b
40	X	J̄	K	X	X	L̄	J	K̄	L	J	K	L̄	e	a

TENS DISTORTION TRIGGERS

Figure 4-9. Gate Inputs for Distortion Triggers

4-3. SIGNAL GENERATOR POWER DISTRIBUTION. As shown in figure 4-12, power supply A1A3 provides six regulated dc voltages to circuit boards A1 through A7 as well as A1A2 the word matric board and to various front panel switches.

(1) Standard 115vac 60Hz power is applied to input transformer T1,which steps the voltage to various levels. The voltages are rectified, filtered, and regulated. Transistor series regulators or zener diodes perform the voltage regulation. Where series regulators are used, the operating point is adjustable by a variable resistor which controls the output voltage of a dc amplifier. Test points are provided for monitoring each output voltage.

4-4. TROUBLESHOOTING. Troubleshooting the signal generator consists of a performing the procedures given in table 4-8, which refers to particular cards that may be defective. Isolating a trouble on a card is performed using the servicing block diagrams, figure 4-11 and the timing diagrams accompanying the text. When there is a malfunction, the procedures of table 4-8 should be followed completely unless a particular card(s) is suspect. After isolating to particular cards, it may be necessary to refer to the text describing the circuitry involved in the malfunction; this may help eliminate a few components on the suspected cards.

a. In isolating components on a card, use the dual trace oscilloscope to check for the presence and interrelation of signals on the card and signals from other cards. The timing diagrams show the interrelationships of the signals within the signal generator. However, pulse widths and intervals between signals are not specified since these quantities depend on the particular buad rate used. The timing can be calculated by figuring the bit width for the various baud rates and relating the other signals to this quantity. In some cases, a signal is merely a spike or a fixed single-spot pulse, not changing as the baud rates are changed. The text describing the servicing block diagrams and the timing diagrams points out the signals which are constant duration triggers.

b. The equipment listed in table 1-3 is required to troubleshoot the signal generator; refer to table 4-8 for troubleshooting procedures.

TABLE 4-8. TROUBLESHOOTING PROCEDURE FOR SIGNAL GENERATOR

STEP	PROCEDURE	NORMAL INDICATION	IF PRESENT	IF NOT PRESENT
1	Set POWER switch to ON.	POWER lamp lights.	Go to step 2.	Check power input.
2	Check dc voltages at power supply 1A3 test points.	TP1 +6.8 TP2 +5.0 TP3 to TP4 +130 TP5 -6.8_1 TP6 -6.8_2 TP7 +12 TP8 -18	Go to step 3.	Refer to figure 4-12 and check circuit associated with missing or incorrect voltage.

TABLE 4-8. TROUBLESHOOTING PROCEDURE FOR SIGNAL GENERATOR (cont)

STEP	PROCEDURE	NORMAL INDICATION	IF PRESENT	IF NOT PRESENT
3	a. Connect oscilloscope to LOW LEVEL OUTPUT jack. b. Set OUTPUT switch to REVERSAL. c. Set CHARACTER RELEASE switch to FREE RUN. d. Set RATE switch to each rate.	Oscilloscope displays 6 v p-p squarewave of following periods: 37.5 -53.4 msec 45.5 - 44 msec 56.8 - 35.2 msec 61.1 - 32.8 msec 74.2 - 27 msec 75 - 26.6 msec	Go to step 4.	a. If frequencies are off or missing, check cards A2 through A5, A7, and A10IC1P1. b. If no output is present, check A13IC2N1 and low level driver on A16.
4	a. Connect squarewave generator to EXT TIMING binding posts (front or rear) b. Set squarewave frequency to 7500 Hz, ±6V (12V p-p) c. Set CHARACTER RELEASE switch to FREE RUN. d. Set TIME BASE switch to EXT.	Oscilloscope displays 6 v p-p squarewave with period of 26.6 msec.	Go to step 6.	Check A15IC1 and A4IC6N3.
5	a. Connect test setup shown in figure 4-13 and connect oscilloscope to output. b. Set HIGH LEVEL OUTPUT switch to NEUT.	Oscilloscope displays squarewave going from 0.0 to 6.0 vdc.	Go to step 7.	Check relay driver on card A16 and electronic relay on chassis.

TABLE 4-8. TROUBLESHOOTING PROCEDURE FOR SIGNAL GENERATOR (cont)

STEP	PROCEDURE	NORMAL INDICATION	IF PRESENT	IF NOT PRESENT
6	a. Connect test set-up shown in figure 4-14. b. Set HIGH LEVEL OUTPUT switch to POLAR.	Oscilloscope displays 2.0 v p-p squarewave.	Go to step 8.	Check high level driver on A16 card.
7	a. Set OUTPUT switch to CHARACTER. b. Set MARK-SPACE switches to SPACE. c. Set RATE switch to 50. d. Set HIGH LEVEL OUTPUT switch to POLAR. e. Set STOP LENGTH switch to each of the four stop lengths.	Oscilloscope shows positive pulses of the following widths: 1.0 - 20 msec 1.42 - 28.4 msec 2.0 - 40 msec	Go to step 8.	Check cards A10, A6, and A4.
8	Set each of the first five MARK-SPACE switches to MARK leaving the others on SPACE.	Oscilloscope displays positive pulse corresponding to bit switch at MARK.	Go to step 9.	Check A10, A11, and MARK-SPACE switches.
9	a. Set CODE LEVEL switch to 5. b. Set MARK-SPACE switches 1 and 4 to MARK with the others on SPACE. c. Set DISTORTION SELECT switch to MARK BIAS. d. Set units PERCENT DISTORTION to each position.	Oscilloscope shows leading edge of bits 1 and 4 leading the zero distortion point to give bit widths of: 0 - 20 msec 1 - 20.2 msec 2 - 20.4 msec 3 - 20.6 msec 4 - 20.8 msec 5 - 21.0 msec 6 - 21.2 msec 7 - 21.4 msec 8 - 21.6 msec 9 - 21.8 msec	Go to step 10.	Check distortion trigger gates on A5 and A8.

TABLE 4-8. TROUBLESHOOTING PROCEDURE FOR SIGNAL GENERATOR (cont)

STEP	PROCEDURE	NORMAL INDICATION	IF PRESENT	IF NOT PRESENT
10	a. Set units PERCENT DISTORTION switch to 0. b. Set tens PERCENT DISTORTION switch to each position.	Oscilloscope shows leading edge of bits 1 and 4 leading the zero distortion point to give the following bit widths: 0 - 20 msec 10 - 22 msec 20 - 24 msec 30 - 26 msec 40 - 28 msec	Go to step 11.	Check distortion trigger gates on card A16.
11	a. Set PERCENT DISTORTION switches for 34 percent.	Oscilloscope shows leading edge of bits 1 and 4 lagging the zero distortion point to give a bit width of 13.2 msec.	Go to step 12.	Check card A8 and distortion trigger gates on A5 and A7.
12	Set DISTORTION SELECT switch to SWITCH BIAS.	Oscilloscope shows leading edge of bit 1 leading the zero distortion point to give a bit width of 16.8 msec; leading edge of bit 4 lags zero distortion point to give bit width of 13.2 msec.	Go to step 13.	Check A8IC4F1.
13	Set DISTORTION SELECT switch to MARK END.	Oscilloscope shows trailing edge of bits 1 and 4 lagging the zero distortion point to give a pulse width of 26.8 msec.	Go to step 14.	Check card A8.
14	Set DISTORTION SELECT switch to SPACE END.	Oscilloscope shows trailing edge of bits 1 and 4 leading the zero distortion point to give a bit width of 13.2 msec.	Go to step 15.	Check card A8.

TABLE 4-8. TROUBLESHOOTING PROCEDURE FOR SIGNAL GENERATOR (cont)

STEP	PROCEDURE	NORMAL INDICATION	IF PRESENT	IF NOT PRESENT
15	a. Set SYNC-START/STOP switch to SYNC. b. Set MARK-SPACE switch 3 to MARK with the others on SPACE.	Oscilloscope shows positive pulse 20 msec wide occurring every 100 msec.	Go to step 16.	Check card A8 and SYNC-START/STOP switch.
16	Set OUTPUT switch to STDY SPACE.	Oscilloscope shows constant -6 vdc level.	Go to step 17.	Check diode 1A1CR1 and OUTPUT switch.
17	Set OUTPUT switch to STDY MARK.	a. Oscilloscope shows constant +6 vdc level. b. Check that SIGNAL lamp is constantly on.	a. Check for b. b. Go to step 19.	a. Check A8IC9N1 and N4. b. Check bulb of SIGNAL lamp and check A16Q3.
18	a. Disconnect oscilloscope from OUTPUT jack. b. Set OUTPUT switch to MESSAGE. c. Set DISTORTION SELECT switch to ZERO. d. Connect a teletype printer to signal generator. Set RATE and STOP LENGTH switches as required.	Printer types out Fox message including five call letters.	Go to step 19.	a. If whole printout is incorrect, check character counter on A14 and A9, then check A12 and A13. b. If only Fox message is incorrect, check A12. c. If only call letters are incorrect, check character pulse gates on A9, then check A13.
19	Set CHARACTER RELEASE switch to SINGLE CHARACTER and press SINGLE CHARACTER switch several times.	Printer types one letter of Fox message and stops each time SINGLE CHARACTER switch is pressed.	Troubleshooting is complete.	Check card A4.

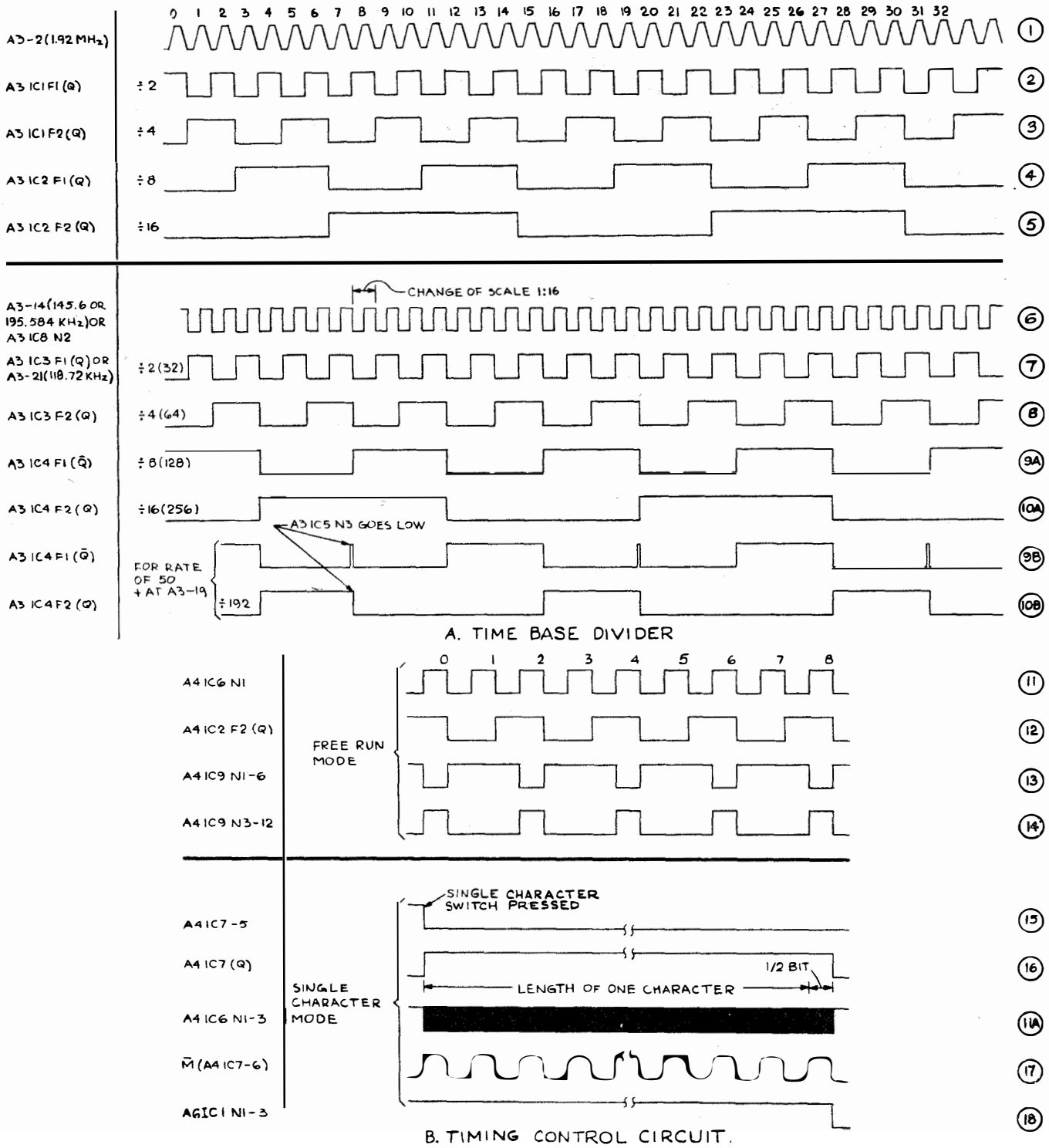


Figure 4-10. Signal Generator Timing Diagrams (Sheet 1 of 9)

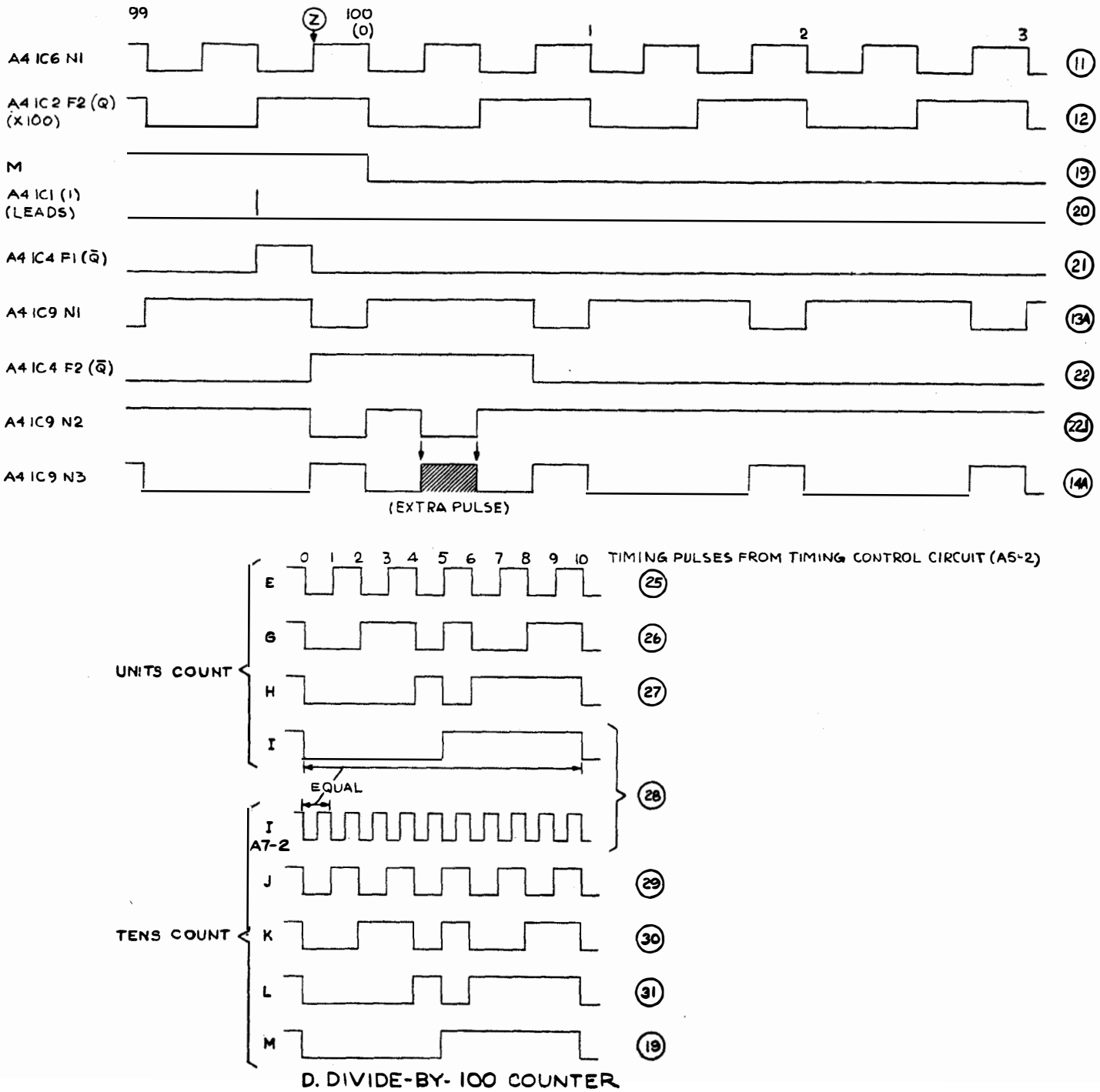
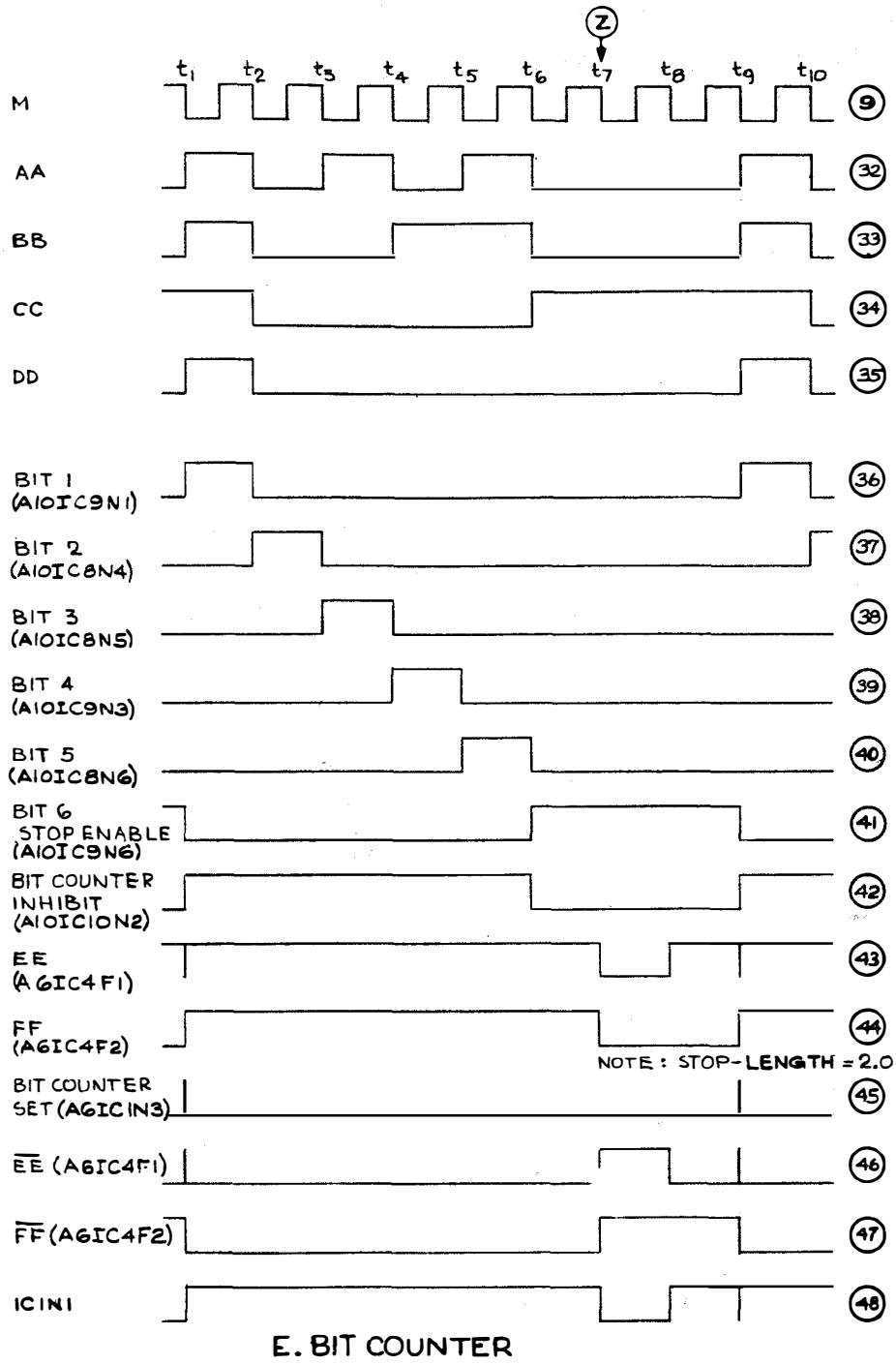
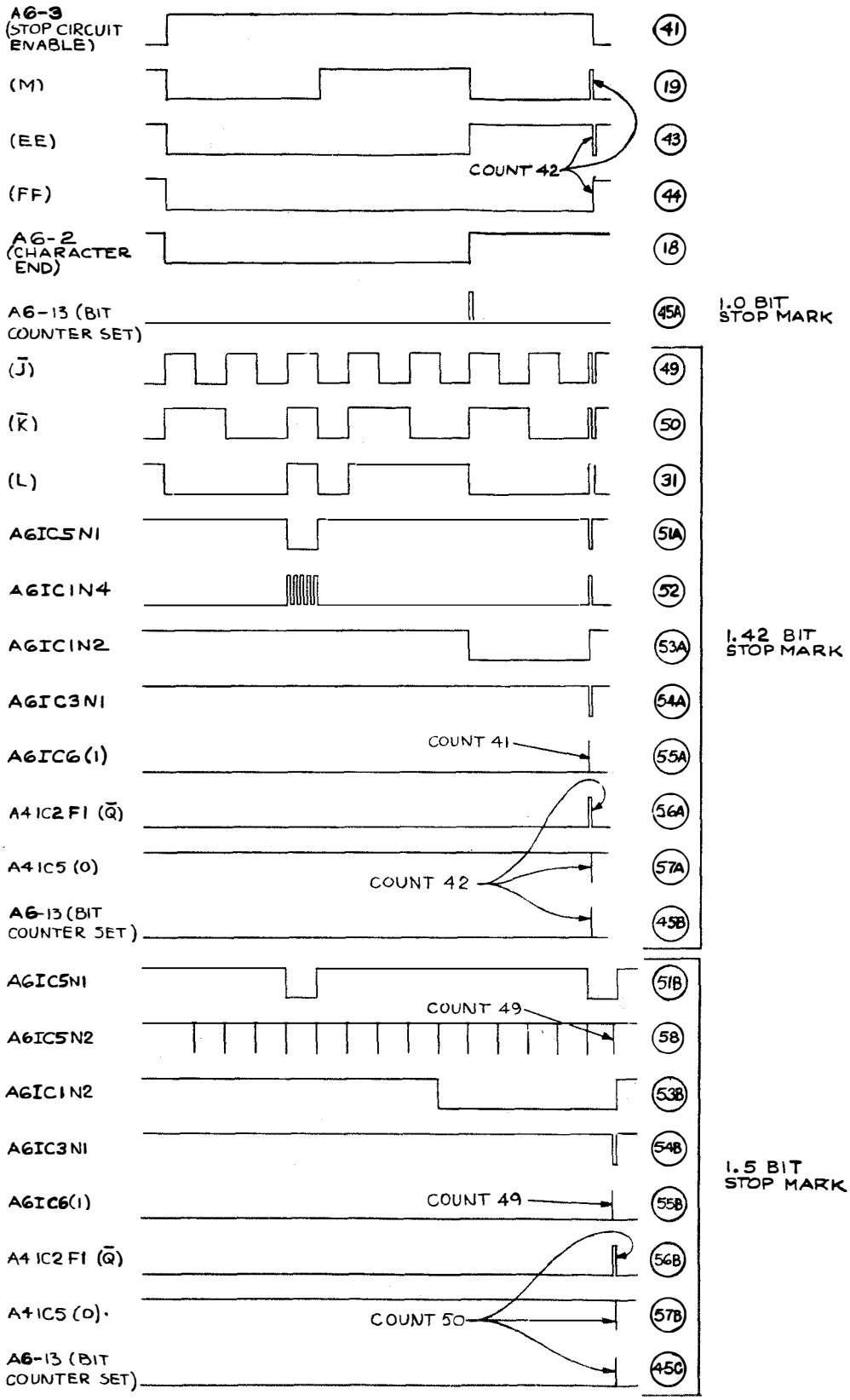


Figure 4-10. Signal Generator Timing Diagrams (Sheet 2 of 9)



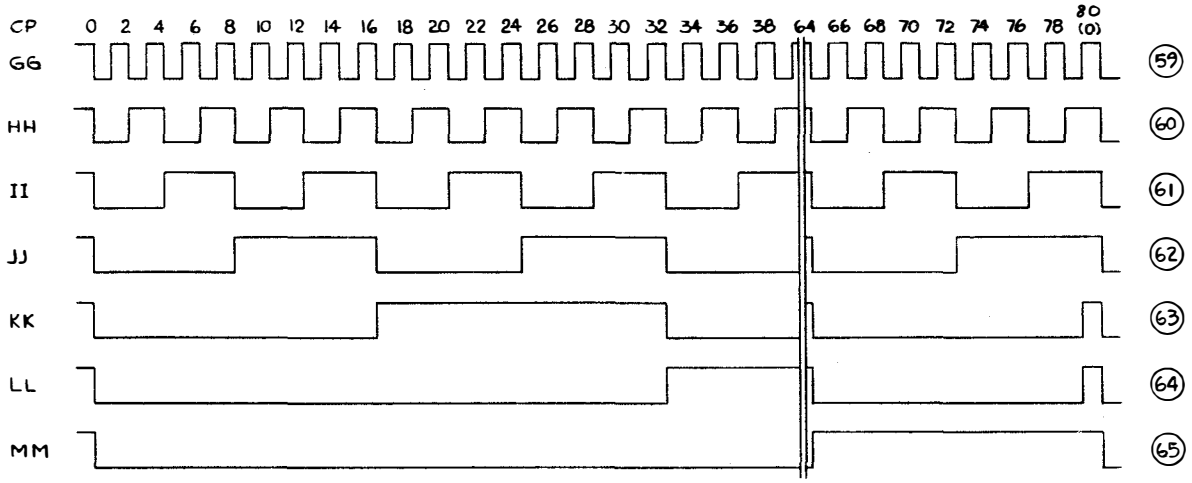
E. BIT COUNTER

Figure 4-10. Signal Generator Timing Diagrams (Sheet 3 of 9)

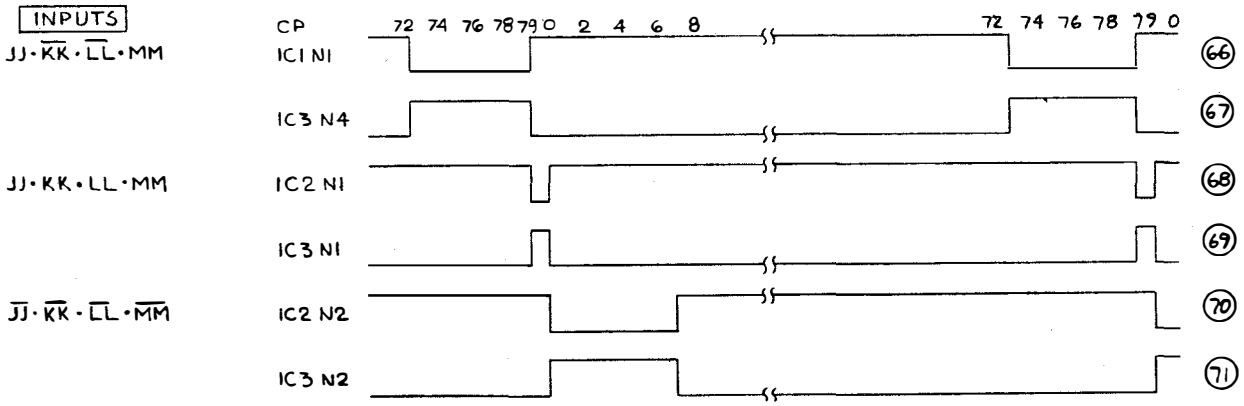


F. STOP CIRCUIT

Figure 4-10. Signal Generator Timing Diagrams (Sheet 4 of 9)



G. CHARACTER COUNTER



H. A9 GATE OUTPUTS FOR MESSAGE MODE

Figure 4-10. Signal Generator Timing Diagrams (Sheet 5 of 9)

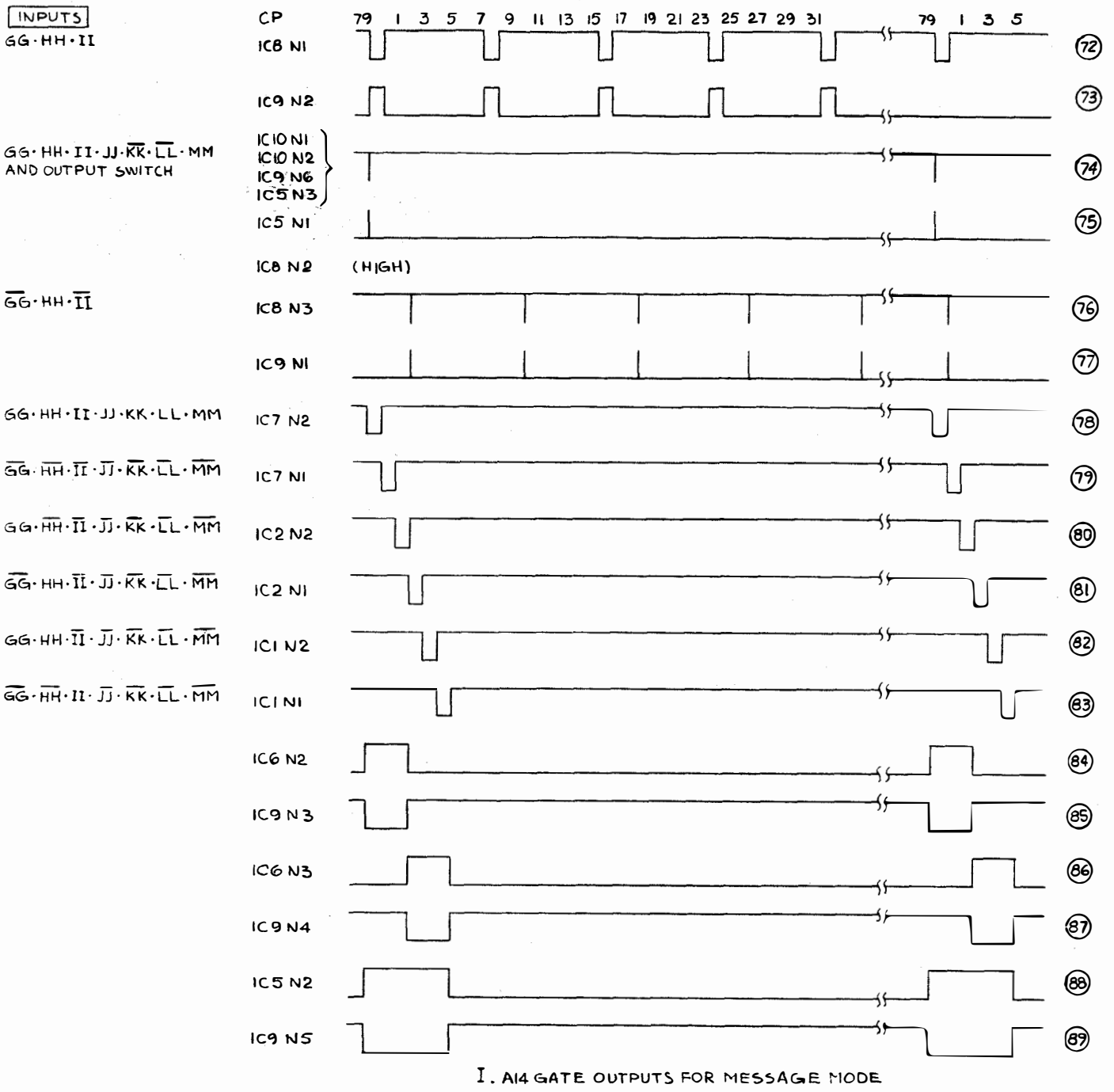


Figure 4-10. Signal Generator Timing Diagrams (Sheet 6 of 9)

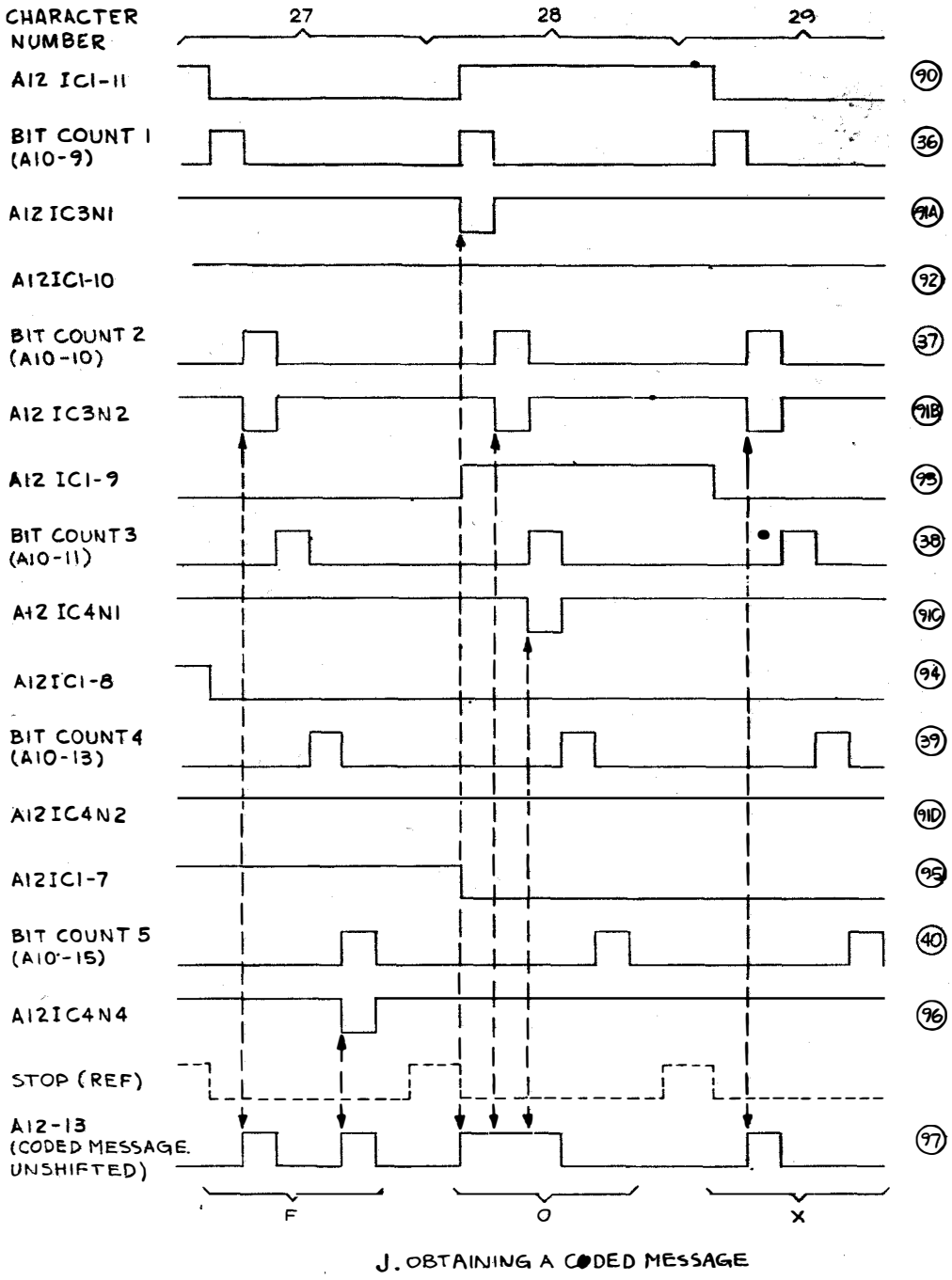


Figure 4-10. Signal Generator Timing Diagrams (Sheet 7 of 9)

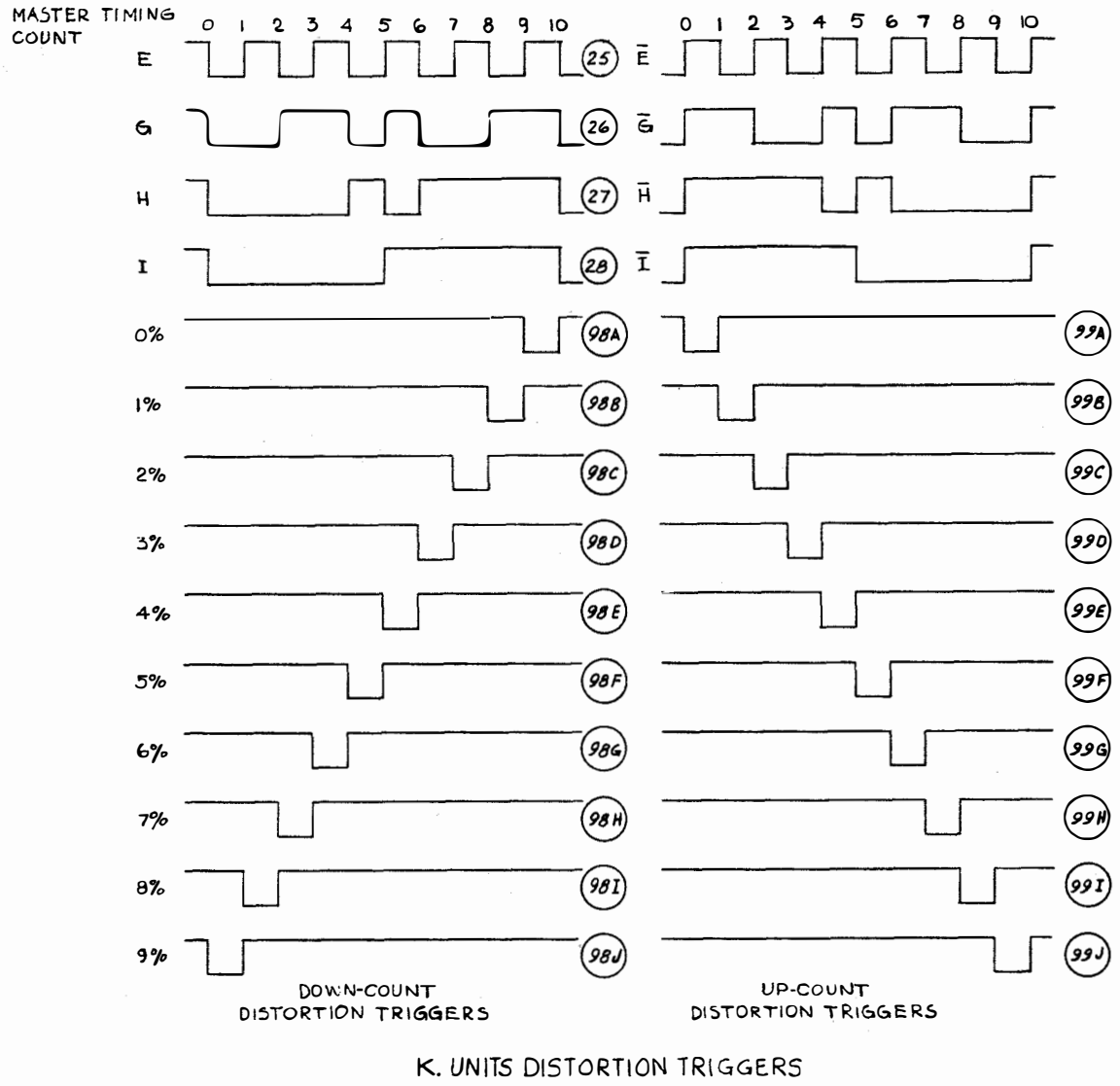


Figure 4-10. Signal Generator Timing Diagrams (Sheet 8 of 9)

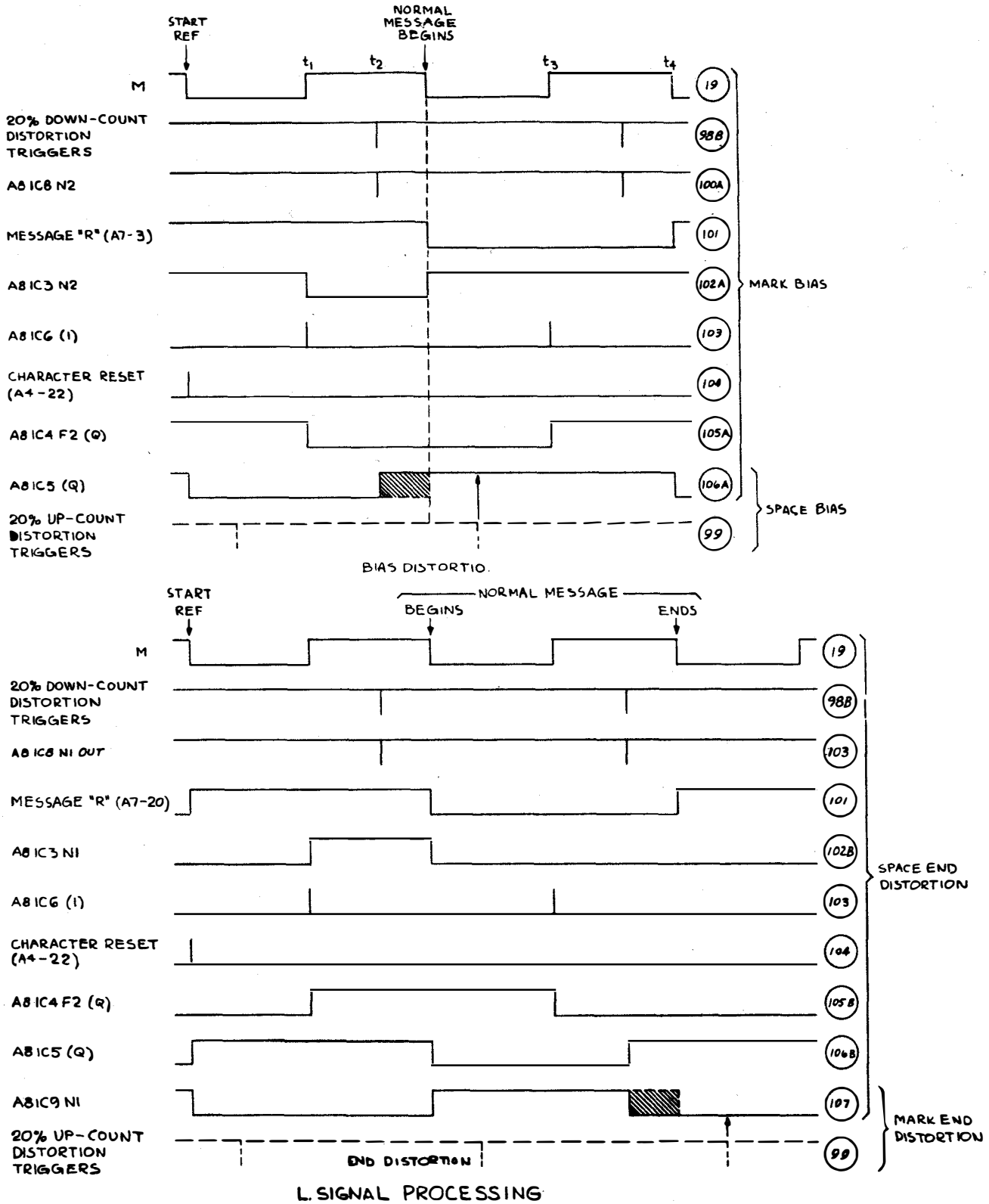


Figure 4-10. Signal Generator Timing Diagrams (Sheet 9 of 9)

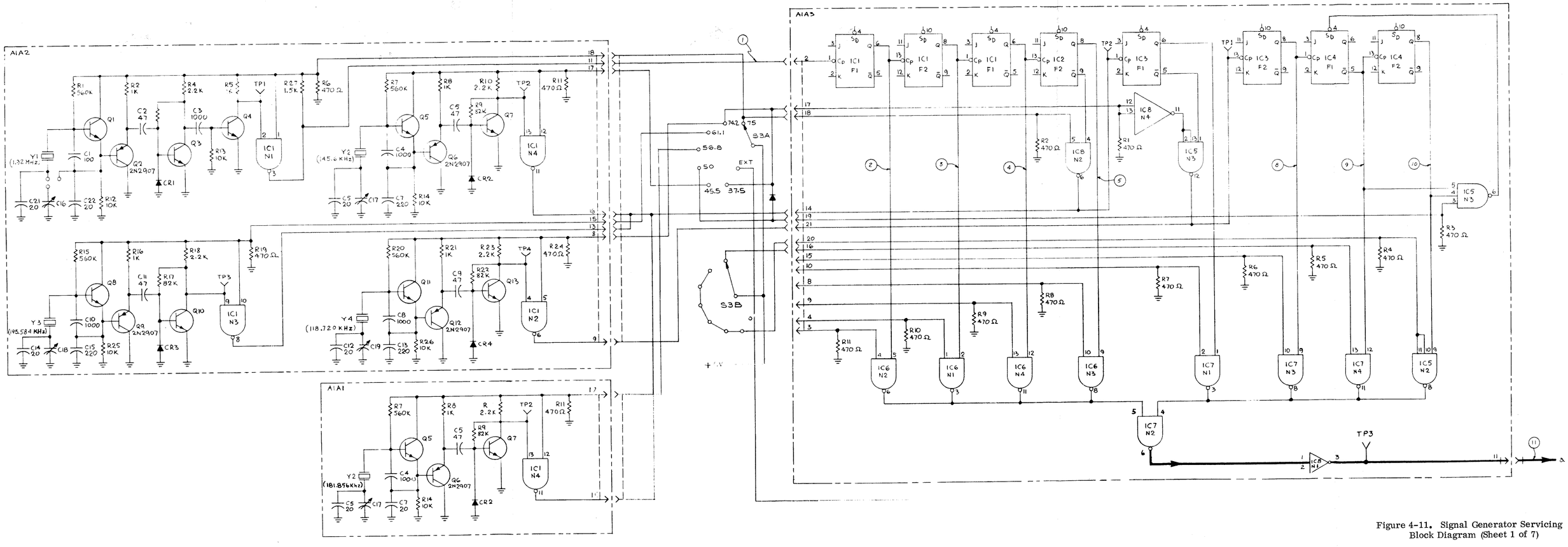


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 1 of 7)

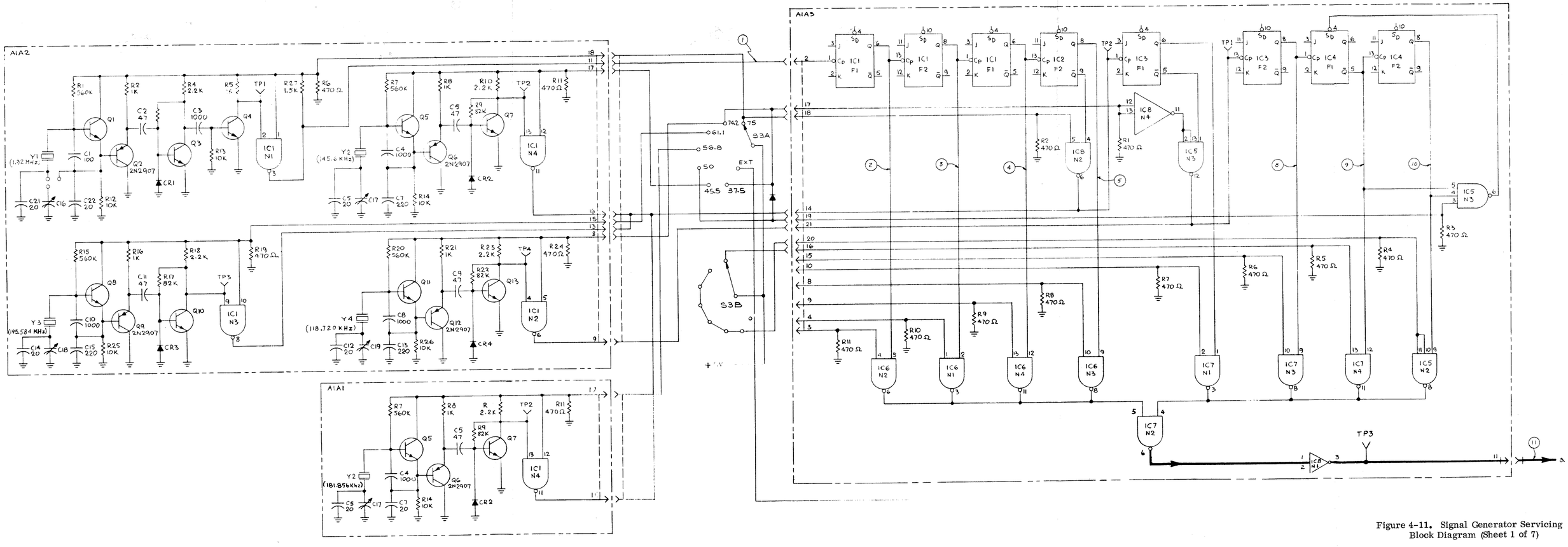


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 1 of 7)

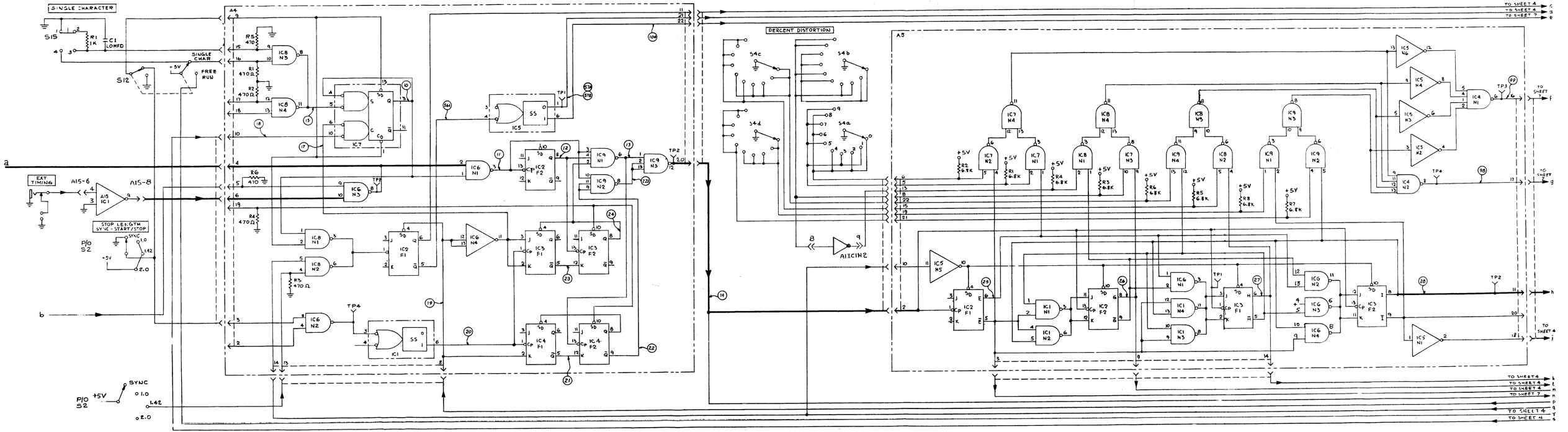


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 2 of 7)

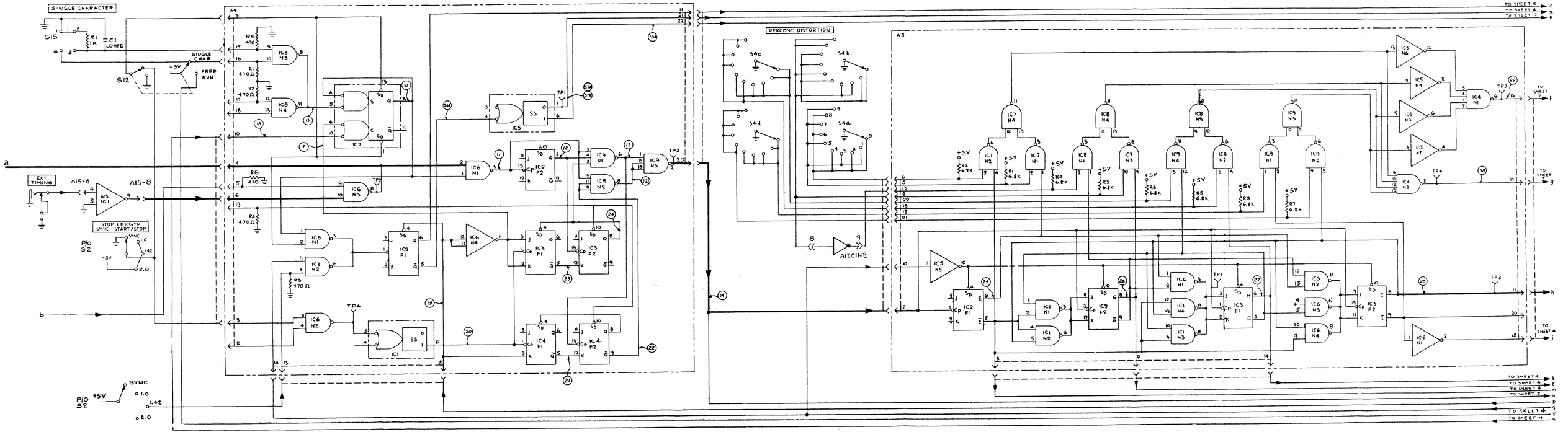


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 2 of 7)

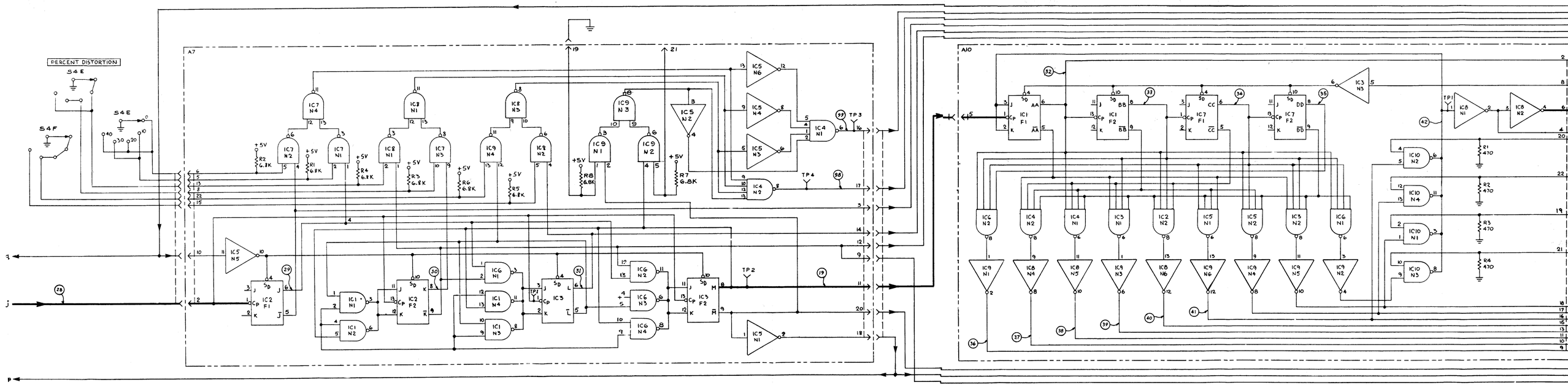


Figure 4-11. Signa
(Block Diagr

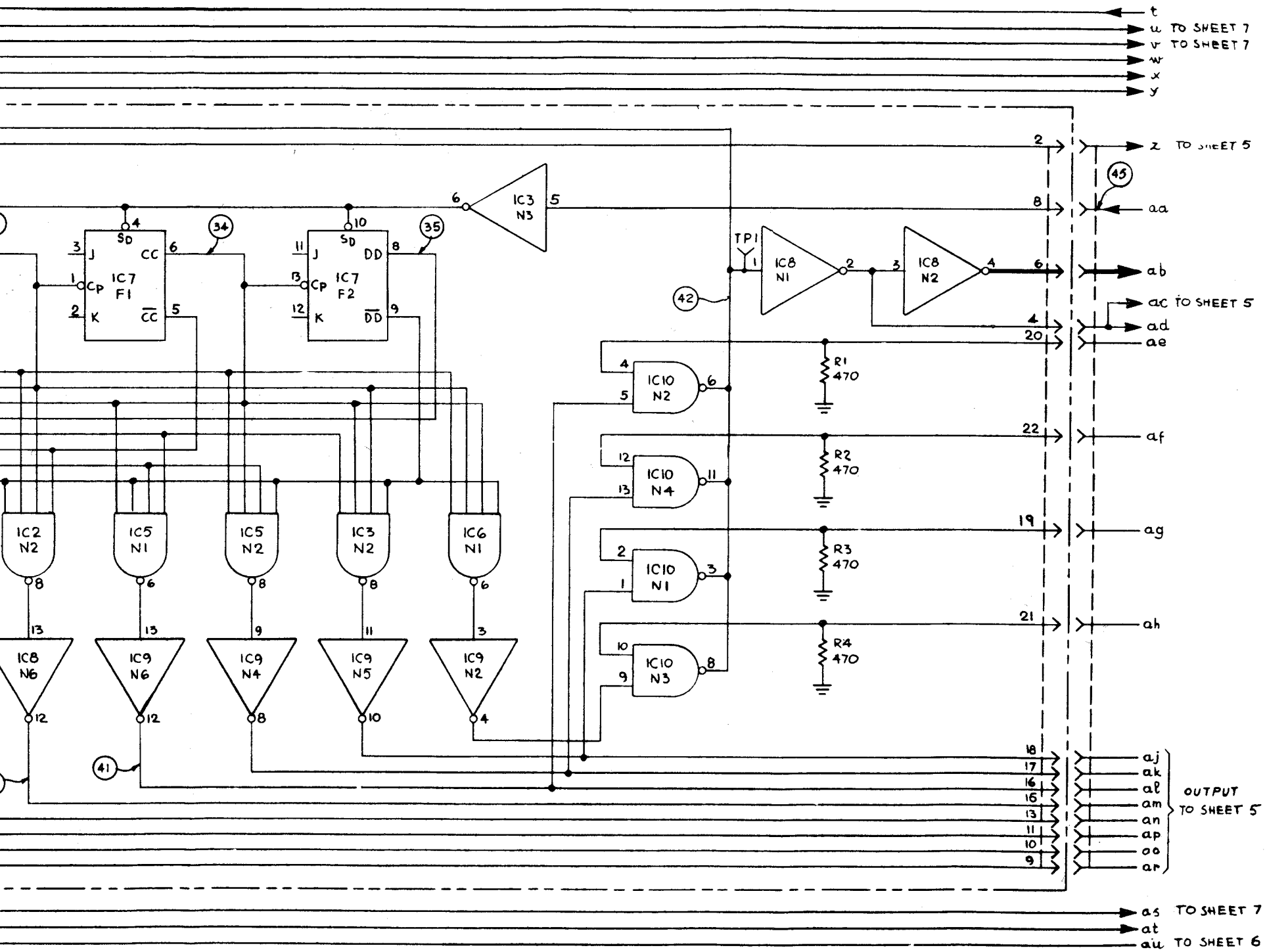


Figure 4-11. Signal Generator Servicing (Block Diagram (Sheet 3 of 7)

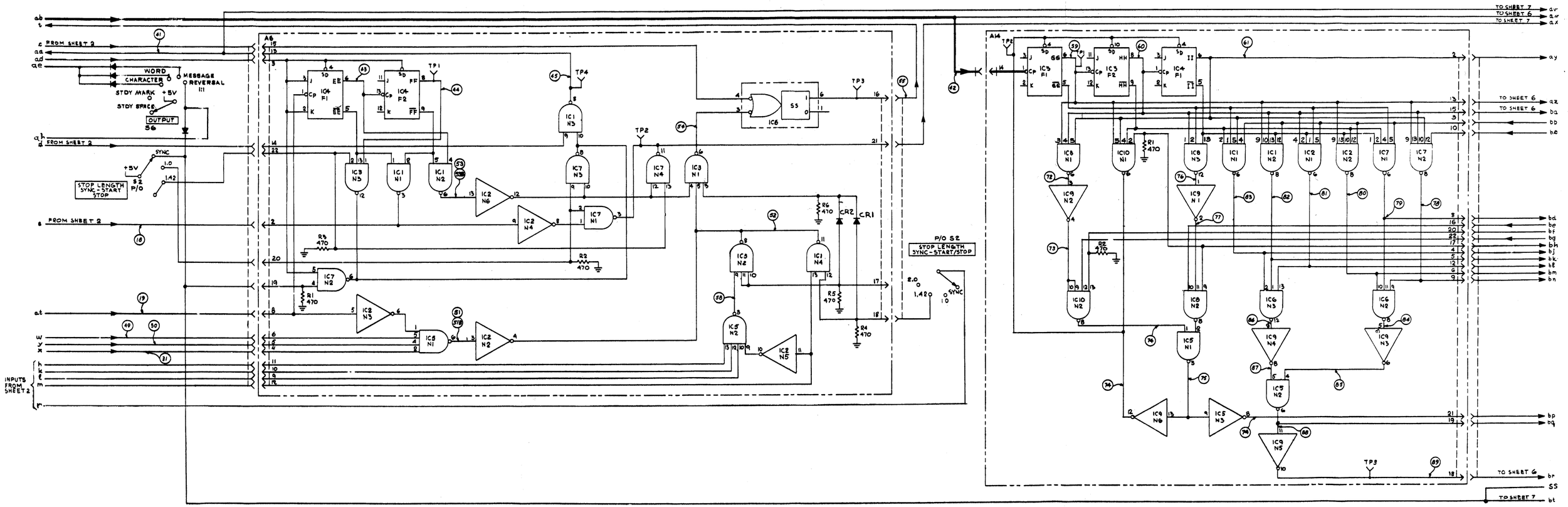


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 4 of 7)

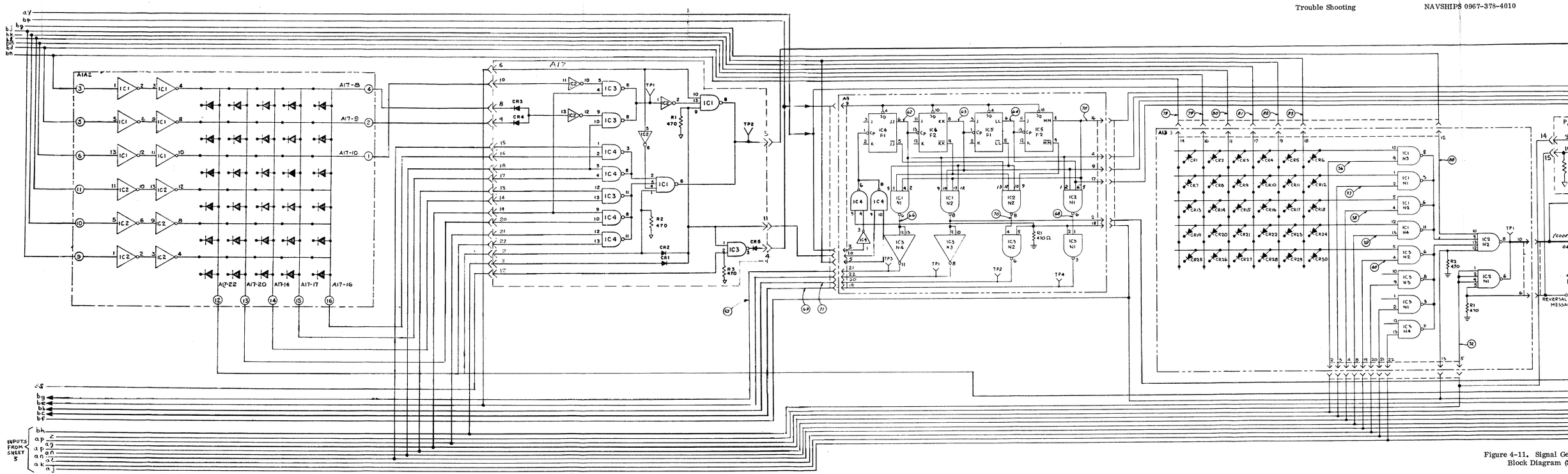


Figure 4-11. Signal Ge
Block Diagram (

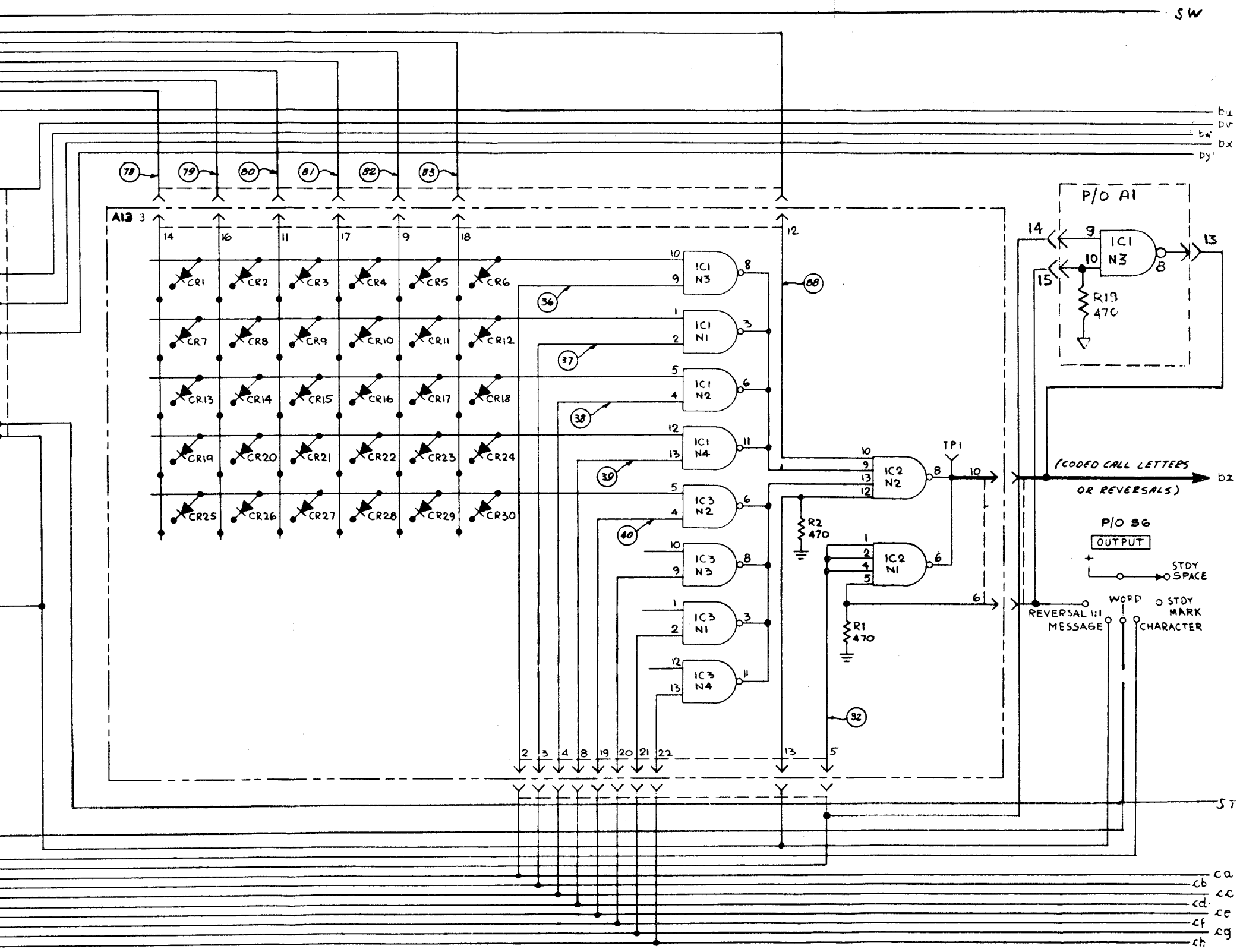


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 5 of 7)

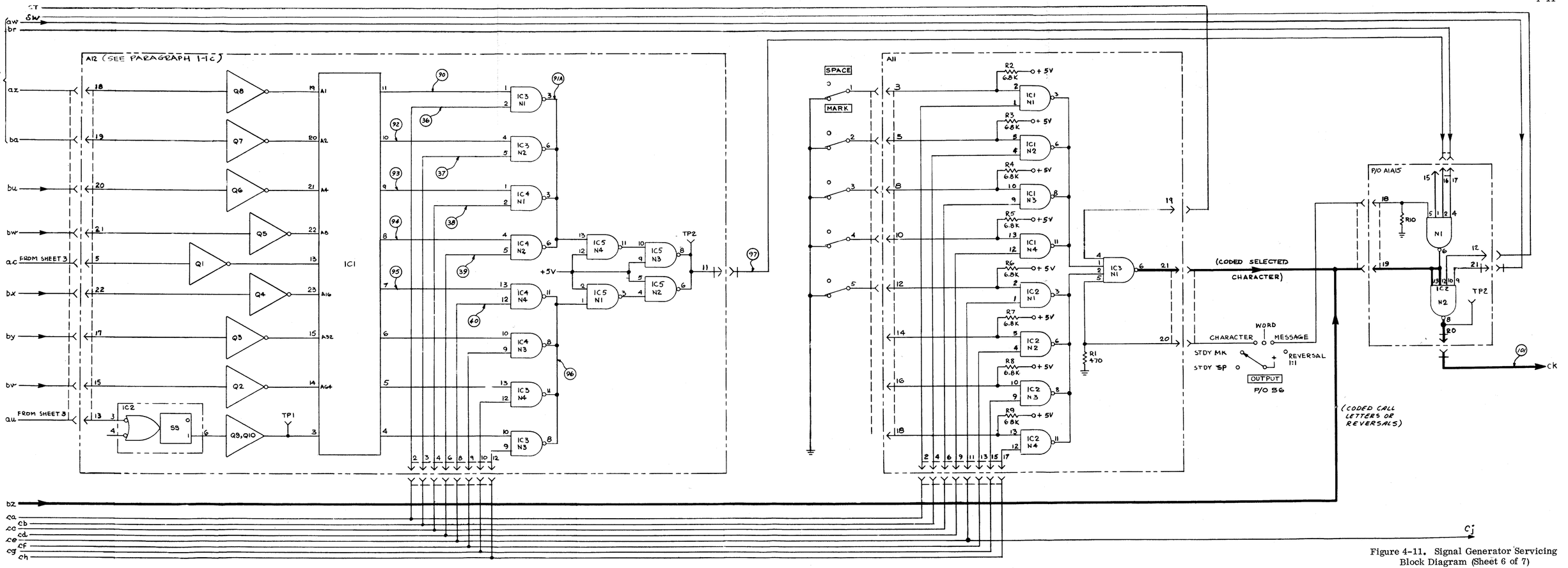


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 6 of 7)

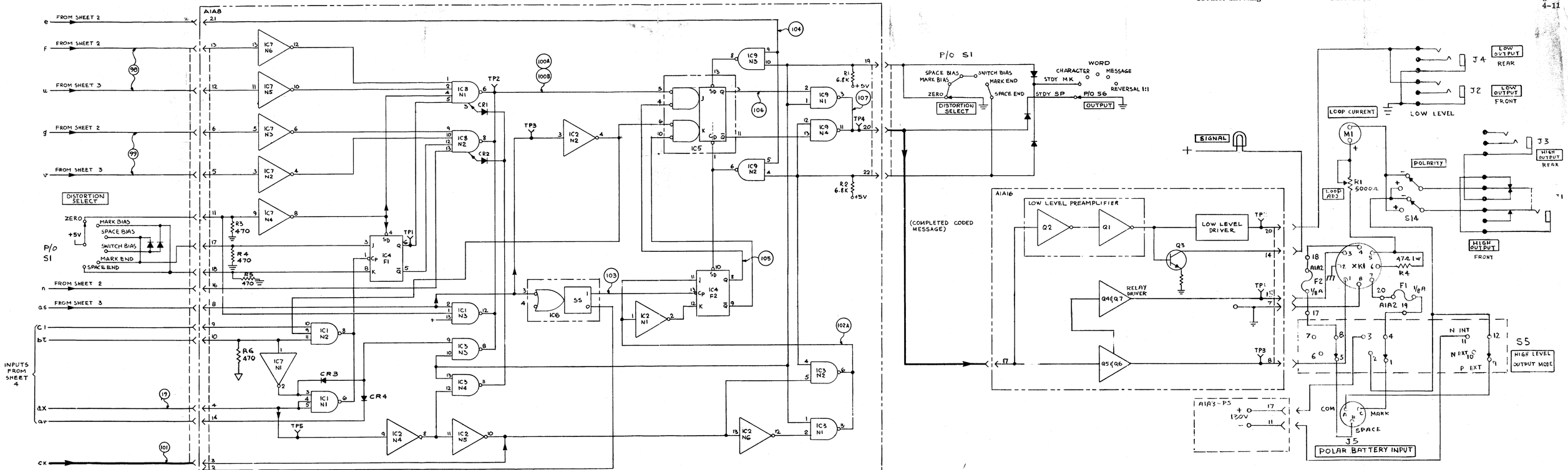


Figure 4-11. Signal Generator Servicing Block Diagram (Sheet 7 of 7)

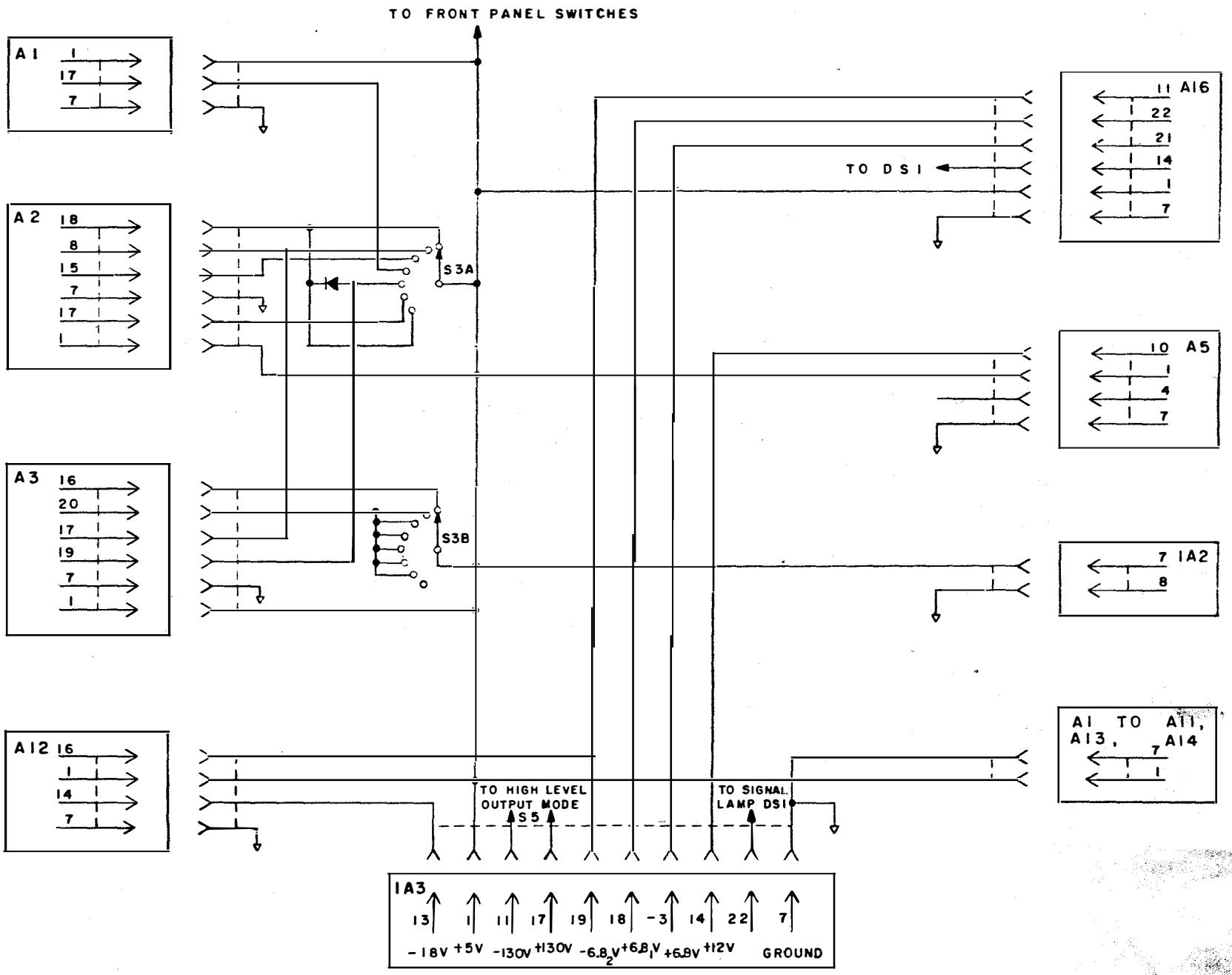


Figure 4-12. Signal Generator Power Distribution Diagram

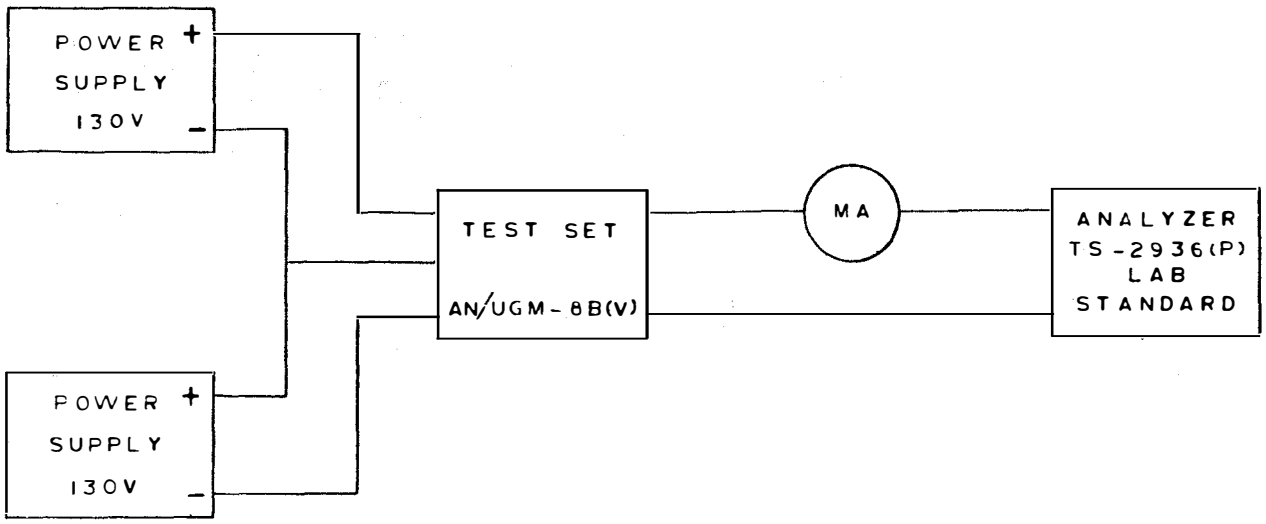


Figure 4-13. Test Setup, High Level Polar

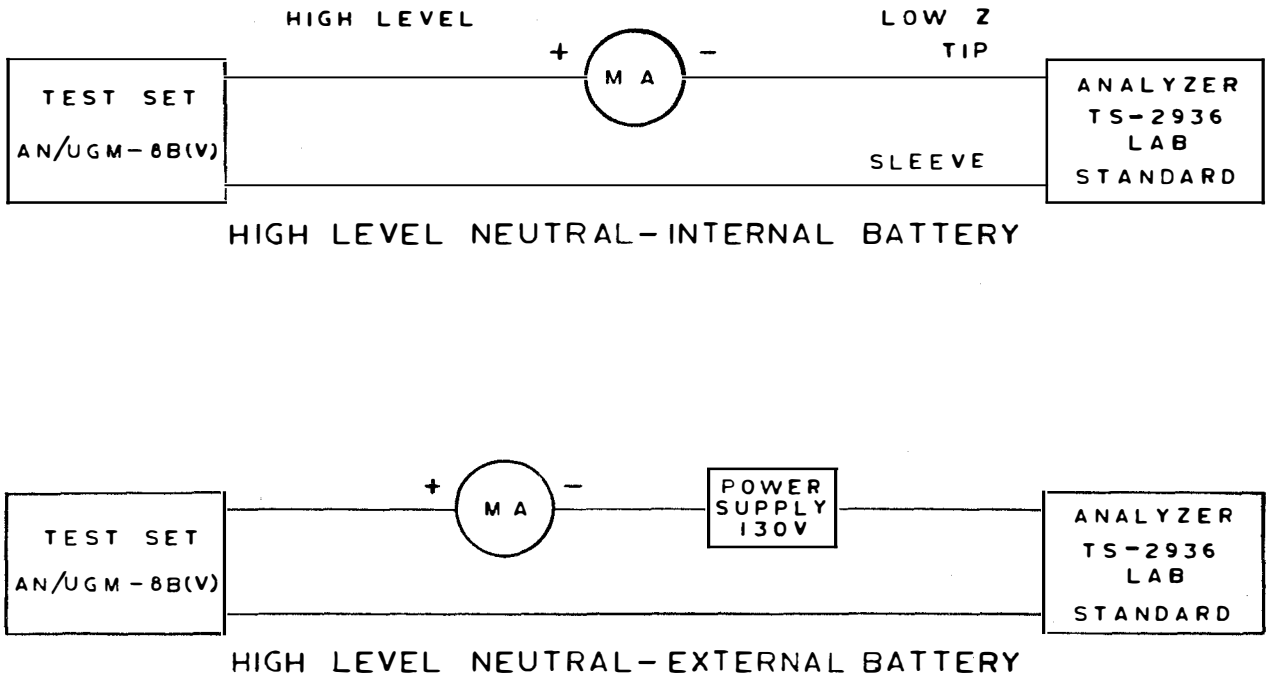


Figure 4-14. Test Setup, Neutral

SECTION 5

MAINTENANCE

5-1. GENERAL.

This section contains the maintenance procedures for the signal generator and includes all preventive maintenance procedures, and diagrams.

5-2. PREVENTIVE MAINTENANCE.

a. OPERATOR'S PROCEDURE. The operator of the signal generator should perform the procedure in 5-7 below at daily intervals, or, if the unit is used intermittently, prior to each use. Materials required are given below.

(1) MATERIALS REQUIRED. - The only materials required for operator maintenance are lint-free cloths (DDD-C-441A, FSN 7920-514-2420) and isopropyl alcohol (MIL-I-10428A, FSN 6810-223-2726).

(2) PROCEDURE. - Proceed as described below, using Table 5-1 as a guide.

(a) Use clean cloth to remove dust, dirt, moisture, or grease from the front panel and controls. If necesssary, dampen cloth with alcohol, then wipe over cleaned area with a clean dry cloth. Also clean case when used with case.

(b) Check that all controls operate smoothly with no binding in any position. Check for proper indexing of rotary selector switches. Check that all knobs are tight on their shafts.

(c) Inspect line cord and plug for evidence of wear, cuts, kinks, or poor electrical connection.

(d) Inspect binding posts for security and inspect work matrix board for loose plugs. Also check rear connectors.

b. TECHNICIAN's PROCEDURE. The procedure given should be performed by a maintenance technician at monthly intervals if the signal generator is used intermittently or at weekly intervals if the signal generator is repeatedly on a daily basis. Table 5-2 contains a list of required test equipment.

NOTE

During the following procedure, it the required results are not obtained, the unit under test must be referred to maintenance for troubleshooting.

(1) FREQUENCY CHECK.

(a) Use extender card A18 to provide access to test points on oscillator cards A1 and A2.

(b) Set up signal generator to provide reversals at baud rate indicated in Table 5-3 for each frequency.

(c) Connect counter to test point indicated in Table 5-3 that corresponds to baud rate.

(d) Check that pulse width measured is within range indicated in Table 5-3.

(2) DISTORTION LEVEL CHECK.

(a) Connect counter to signal generator low level output jack.

(b) Provide reversals at rate indicated in Table 5-4 and check that pulse width is within range specified for that baud rate.

(3) MESSAGE, WORD, AND CHARACTER GENERATION CHECK.

(a) Connect teleprinter to appropriate output jack.

TABLE 5-1. SIGNAL GENERATOR INSPECTION PROCEDURE

ITEM	INSPECT FOR
Case and Panel	Dirt or corrosion; dents, cracks, scratches or other physical damage; loose or missing hardware.
Switches	Loose or missing knobs; defective switch action; bent, broken, or loose terminals.
Meters	Broken facing; loose or missing hardware.
Connectors	Bent, broken, or corroded pins; cracked shell; loose or missing hardware.
Lamps	Cracked or broken lens; missing or defective lamp; loose or missing hardware; bent, broken or corroded terminals.
Wiring	Frayed, broken, or abraded insulation; loose connections; dirty wiring.
Component Boards	Cracked or broken boards; bent, broken, or corroded terminals; loose or missing hardware, damaged components.
Test Cable	Frayed, broken, kinked, or abraded insulation; loose or missing clamps; damaged connectors.
Fuse and Holder	Specified rating, security, corrosion, and evidence of overheating.
Component Parts	Loose connections and obvious damage.

TABLE 5-2. TEST EQUIPMENT REQUIRED FOR PREVENTIVE MAINTENANCE

QTY. PER EQUIP.	NOMENCLATURE	
	NAME	DESIGNATION
1	Frequency Counter	AN/USM-245 or equivalent
1	Teleprinter	AN/UGC-48

TABLE 5-3. INTERNAL OPERATING SPEEDS

RATE (Baud)	LIMITS (msec)
37.5	26.640 - 26.693
45.5	21.948 - 21.992
56.8	17.583 - 17.617
61.12	16.345 - 16.377
74.2	13.457 - 13.483

(b) Set up signal generator to provide fox message with no distortion and check that fox message is printed without error.

(c) Set up signal generator to provide programmed work and check that work printed is work that is programmed.

(d) Set up signal generator to provide single character.

(e) Program character using front panel switches.

(f) Press CHARACTER RELEASE switch and check that character printed is character programmed.

TABLE 5-4A. PULSE WIDTH LIMITS FOR BIAS DISTORTION

RATE	DISTORTION	MARK BIAS	SPACE BIAS
37.5	0	26.13 - 27.20	26.13 - 27.20
	5	24.80 - 25.87	27.47 - 28.53
	10	23.47 - 24.53	28.80 - 29.87
	20	20.80 - 21.87	31.47 - 32.53
	30	18.13 - 19.20	34.13 - 35.20
	49	13.07 - 14.13	39.20 - 40.27

TABLE 5-4B. PULSE WIDTH LIMITS FOR END DISTORTION

RATE	DISTORTION	MARK BIAS	SPACE BIAS
37.5	0	26.13 - 27.20	26.13 - 27.20
	5	27.47 - 28.53	24.80 - 25.87
	10	28.80 - 29,87	23.47 - 24.53
	20	31.47 - 32.53	20.80 - 21.87
	30	34.13 - 35.20	18.13 - 19.20
	49	39.20 - 40.27	13.07 - 14.13

5-3. REPAIR AND REPLACEMENT PROCEDURES.

Figures 5-1 through 5-41 show the location and schematic representation of components in the signal generator. When the location is not known, consult the parts list to determine the illustration on which the component appears.

a. TRANSISTOR AND IC REPLACEMENT TECHNIQUES. Transistors and IC's are extremely sensitive to heat and may be destroyed if subject to excessive temperatures for even short periods of time. For this reason the soldering and desoldering technique used is extremely important.

b. SPECIAL EQUIPMENT REQUIRED.

Pencil-type soldering iron, 25 watts maximum

IC desoldering tip

Twist drill and assorted bits, numbers 30 to 60

Diagonal cutting pliers

Long nose pliers

One-half inch brush

Rosin-alcohol solder flux

Alcohol

Humiseal

Knife, metal pick, or equivalent

(1) Whenever possible provide a heat sink of some sort between the soldering iron and the semiconductor leads. This is easily done by grasping the lead being soldered (using long nose pliers) just above point of soldering iron contact. The pliers will absorb excess heat before it is conducted to the transistor. Apply the soldering iron to the transistor lead only long enough to melt the solder. Never bring the soldering iron into contact with the body of the semiconductor, or metal that is in contact with the body of the semiconductor.

(2) Since transistor and IC connection points are not keyed on the printed circuit card, mark the card with orientation data to prevent improper installation of replacement component. Some soldering irons, when plugged into ac line, have a voltage existing between the metal body of the iron and earth ground. This voltage may cause leakage currents that can destroy a transistor or an IC when the iron is brought into contact with a lead if the printed-circuit card or the signal generator case is connected to ground. Such effects can be nullified by connecting a jumper lead from the metal body of the iron, to the ground point of the printed-circuit card to the chassis or GRD terminal of the signal generator.

b. PRINTED-CIRCUIT REPAIR TECHNIQUES. Printed circuit repair is more difficult and requires more skill than conventional-equipment repair. The following discussion describes acceptable procedures for replacing components and servicing printed-circuit cards. Read these instructions carefully before attempting any printed-circuit repair; follow them scrupulously while performing any repair.

(1) GENERAL - Since the cost of a printed-circuit card is high, particularly when compared with that of any individual component, never try to save the component at the expense of a printed-circuit card. Most components may be clipped from the card, thereby protecting the card's printed-circuit conductor (i.e., the copper foil beneath the visible solder coating) and preventing any undue component damage. In using the soldering iron to remove the leads of a clipped-off component, to connect a new component, or to repair the printed-circuit card itself, take care when applying the iron to the printed circuit card. These cards are easily damaged by heat; prolonged application of heat destroys the adhesiveness of the bonding agent that holds the printed circuit conductor to the card.

(2) REMOVING A DEFECTIVE COMPONENT

(a) REMOVING PROTECTIVE COATING. - Using the metal pick, knife, or equivalent, chip the card's protective

coating (epoxy) from the component leads and from the area surrounding its juncture to the card. If necessary, first soften the coating by applying the tip of a hot pencil-type soldering iron, taking care to keep the iron away from printed-circuit conductor (foil); then scrape the softened coating away. Do not use solvent to remove the coating.

(b) CLIPING OUT THE COMPONENT. Using the wire clipper, cut (close to the lead hole, but allowing some of the lead to the extend through the hole) both leads of the component, and remove the component. Carefully straighten the lead end that extends through each hole, so that it may be easily withdrawn as described in (c) below.

(c) UNSOLDERING LEAD ENDS. Exerting minimum pressure, apply the tip of a hot pencil-type soldering iron to the tip of the lead end. (Keep the iron away from the printed-circuit foil.) As the lead end absorbs the heat, the solder will melt and the lead will break away from its juncture to the printed-circuit foil. Remove the soldering iron immediately, and, using the pliers, quickly pull the lead free; brush away excess solder. Do not force or twist the lead to remove it from the card.

(d) CLEANING LEAD HOLE. As the lead end is removed, solder may flow into the open hole and cause shorts on the printed-circuit foil. To remove the solder, tap the card gently while the solder is soft. Should this fail to clean out the hole, carefully drill (using a drill bit of appropriate size) out the solder. Apply the drill to the printed-circuit side of the card; drilling from the other side may ruin the card by loosening the foil as the drill passes through it.

(e) INSTALLING NEW COMPONENT.

1. Using a knife, scrape leads of component to be installed.

2. Bend the leads so that they fit snugly into the holes where the component is to be installed. Mount the component on the card, gently pushing the leads through the holes. Bend each end of the lead close to the foil.

3. Apply flux to the joint. Touch the lead with the tip of the hot soldering iron and apply a small amount of fluxless 60/40 solder to the junction.

4. Remove the soldering iron as soon as solder flows into the joint. Hold the component firmly until the solder sets.

5. Using a small amount of alcohol, remove excess flux.

6. Once the solder cools, check that the joint is secure and clean. Remove any solder that may have flowed onto the foil, thereby eliminating the possibility of a short circuit.

7. Replace conformal coating by brushing or spraying over the repair area and overlapping the adjacent surfaces. Check that no portion is left uncovered.

(f) REPAIRING PRINTED-CIRCUIT CONDUCTOR. The printed-circuit conductor is, essentially, the thin copper foil which effects required connections to the circuit components; it is bonded to the card proper and is covered by a solder coating. Although the printed-circuit conductor can withstand proper handling and will operate with no trouble under normal rated service conditions, it is liable to damage. Should any part of the conductor be damaged (i.e., split or raised from the card proper), perform required repairs as follows:

1. When part of the conductor has raised from the card, remove it by snipping both its end close to the card; a split in the conductor does not require cutting.

2. Bend a piece of tinned 20- or 22-gauge copper wire into the shape of a staple. The staple should be long enough to span defective portion of

the conductor and to allow clinching at approximately one-fourth of an inch from either end, once placed into position on the printed-circuit card.

3. From the printed-circuit side of the card, drill two small holes (of proper size) to receive the staple ends. Unless the printed-circuit conductor is approximately one-fourth of an inch wide, do not drill these holes directly into the foil, but drill them near enough so that the staple is parallel to the foil. Should the foil be one-fourth of an inch side, drill the two holes directly into the printed-circuit foil. If the repair is not in a congested printed-circuit area, proceed to Step 4 below. Otherwise, insert the staple from the component side of the card, and, on the other side, clinch each end diagonally across the printed-circuit conductor. Then proceed to Step 5, below.

4. If room permits, drill two extra holes in the printed-circuit card, each one adjacent to the one of the previously drilled holes. From the printed-circuit side of the card, insert the staple ends into the holes furthest from the area under repair. Holding the staple flush against the card, bend each end back through to the adjacent hole closest to it. Pulling it taut, clinch each lead end across the printed-circuit conductor.

5. Solder the two joints.

5-4. COMPONENT LOCATION

Component location diagrams are included to aid in trouble-shooting and repair of the signal generator. The component location diagrams are included on the left hand page while the accompanying schematic diagram is included on the right hand page. Interconnections between boards and chassis mounted components are provided in Figures 5-40 and 5-41 at the end of the section.

5-5. POWER SUPPLY ADJUSTMENT.

TABLE 5-5. POWER SUPPLY ADJUSTMENT DATA

POWER SUPPLY	TEST POINTS		ADJUSTMENTS	VOLTAGE
	FROM	TO		
130 vdc	TP-4 (+)	TP-3 (-)	R17	130 ±6 vdc
+5 vdc	TP-2 (+)	GRD	R9	5 ± 0.25 vdc

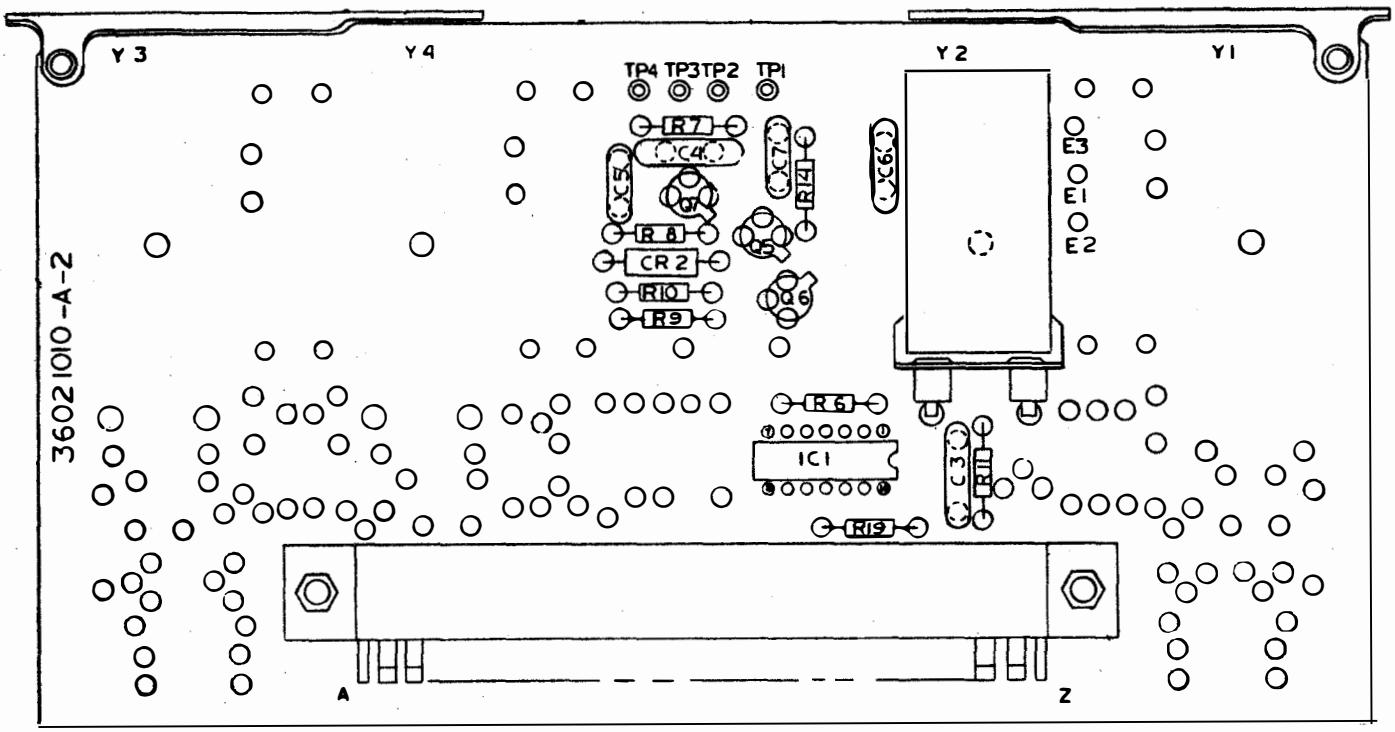


Figure 5-1. Oscillator Board 1A1A1 Component Location

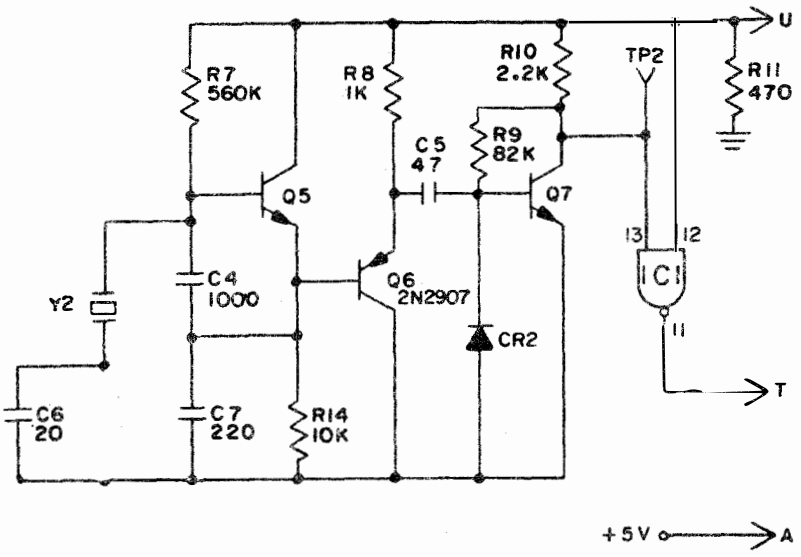


Figure 5-2. Oscillator Board 1A1A1, Schematic

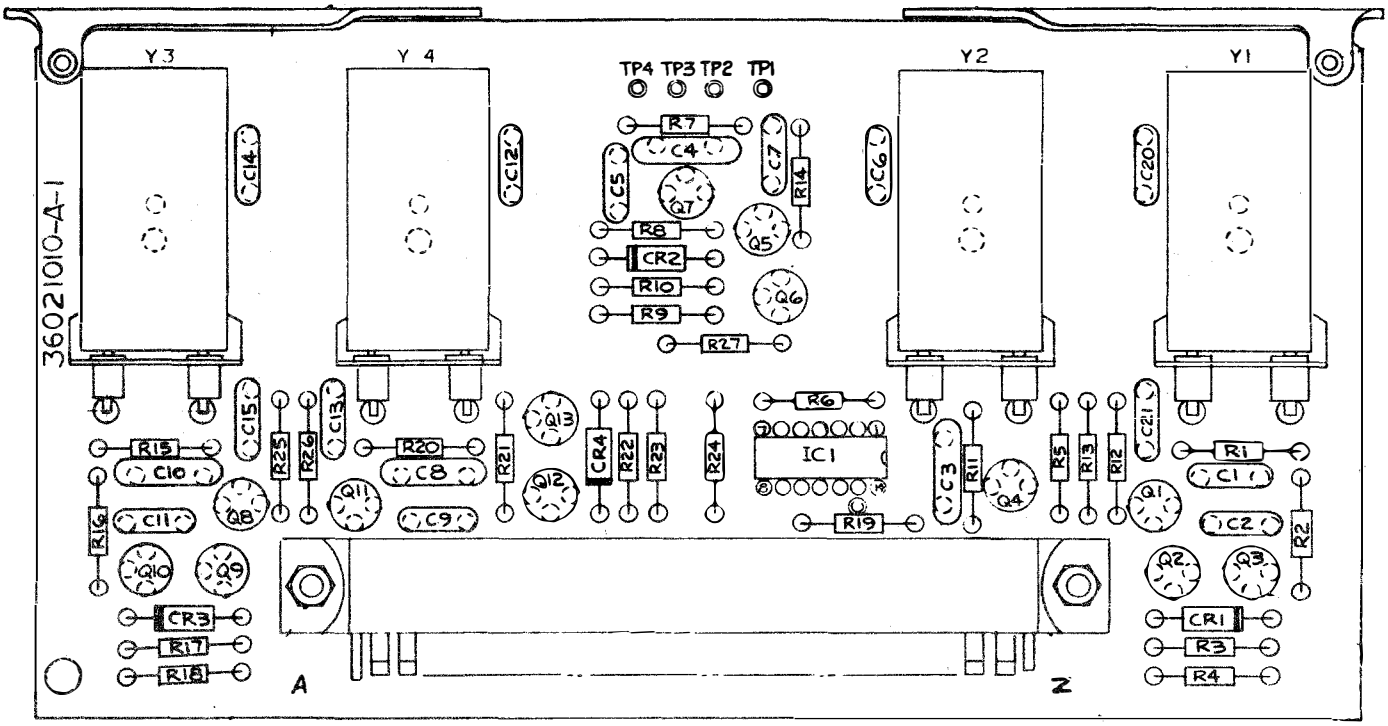
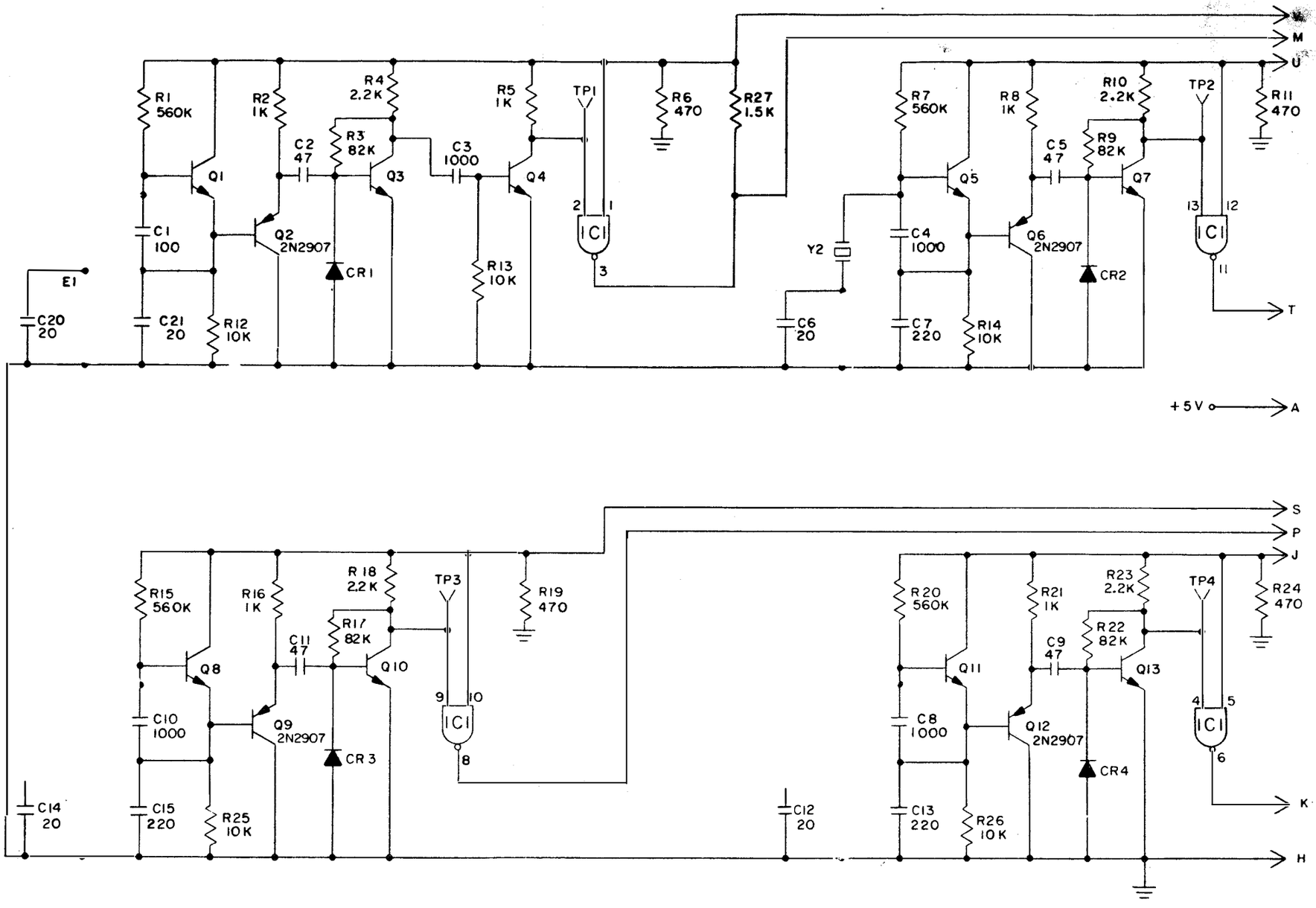


Figure 5-3. Oscillator Board 1A1A2, Component Location



NOTES:

1 - UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS, 1/4W, ±5% TOL. CAPACITANCES ARE IN UUF.
2 - o— DENOTES COMMON TIE POINT OR VOLTAGE BUS.
3 - ←— DENOTES CONNECTOR POINTS.
4 - UNLESS OTHERWISE SPECIFIED ALL TRANSISTORS ARE TYPE 2N760A.
5 - UNLESS OTHERWISE SPECIFIED ALL DIODES ARE TYPE IN3064

Figure 5-4. Oscillator Board 1A1A2 Schematic

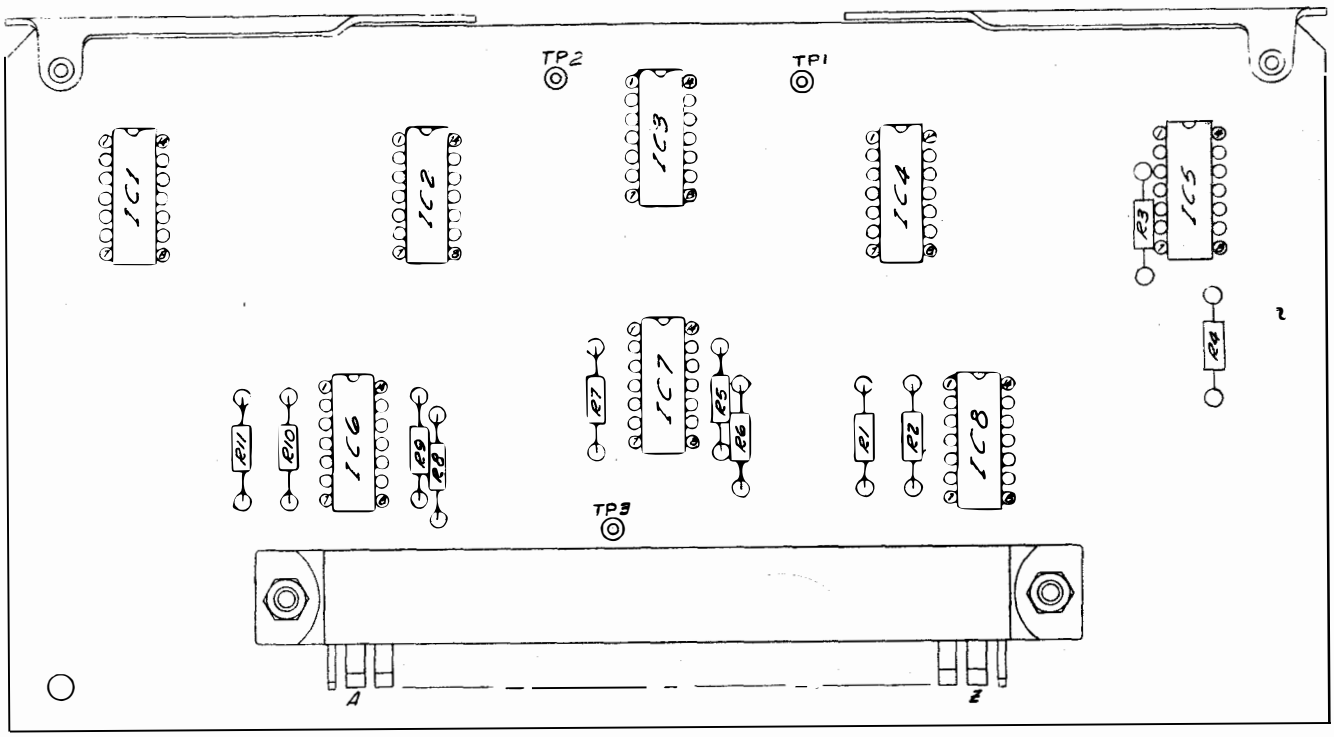


Figure 5-5. Time Base Divider Board 1A1A3 Component Location

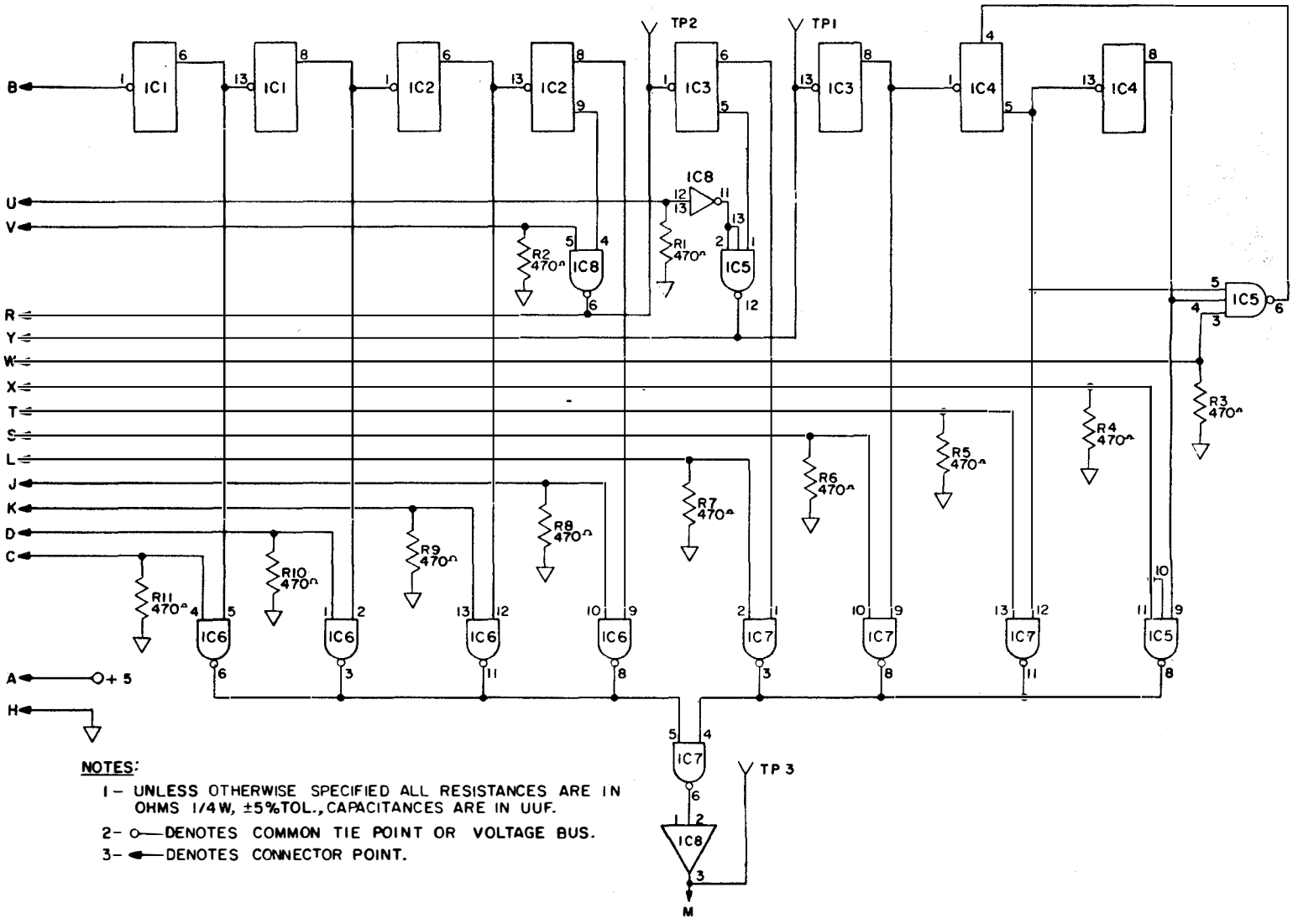


Figure 5-6. Time Base Divider Board 1A1A3 Schematic

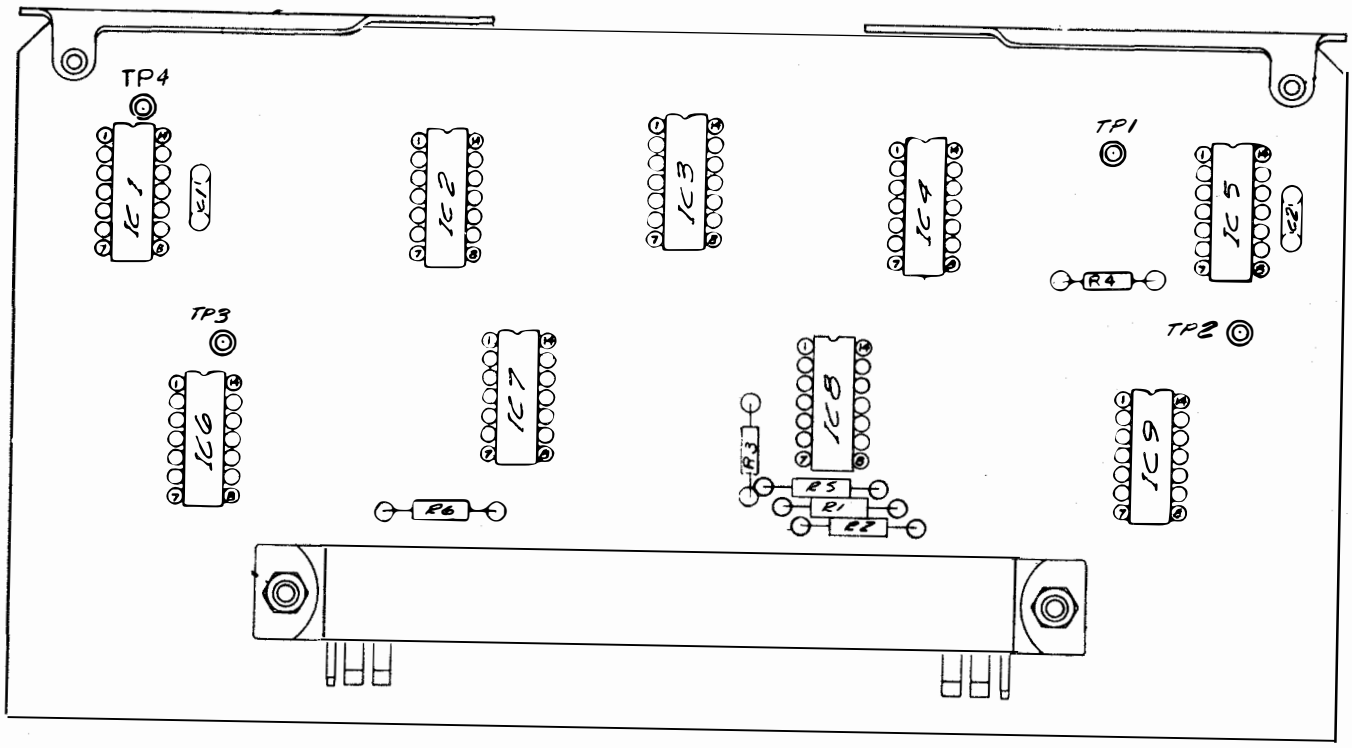
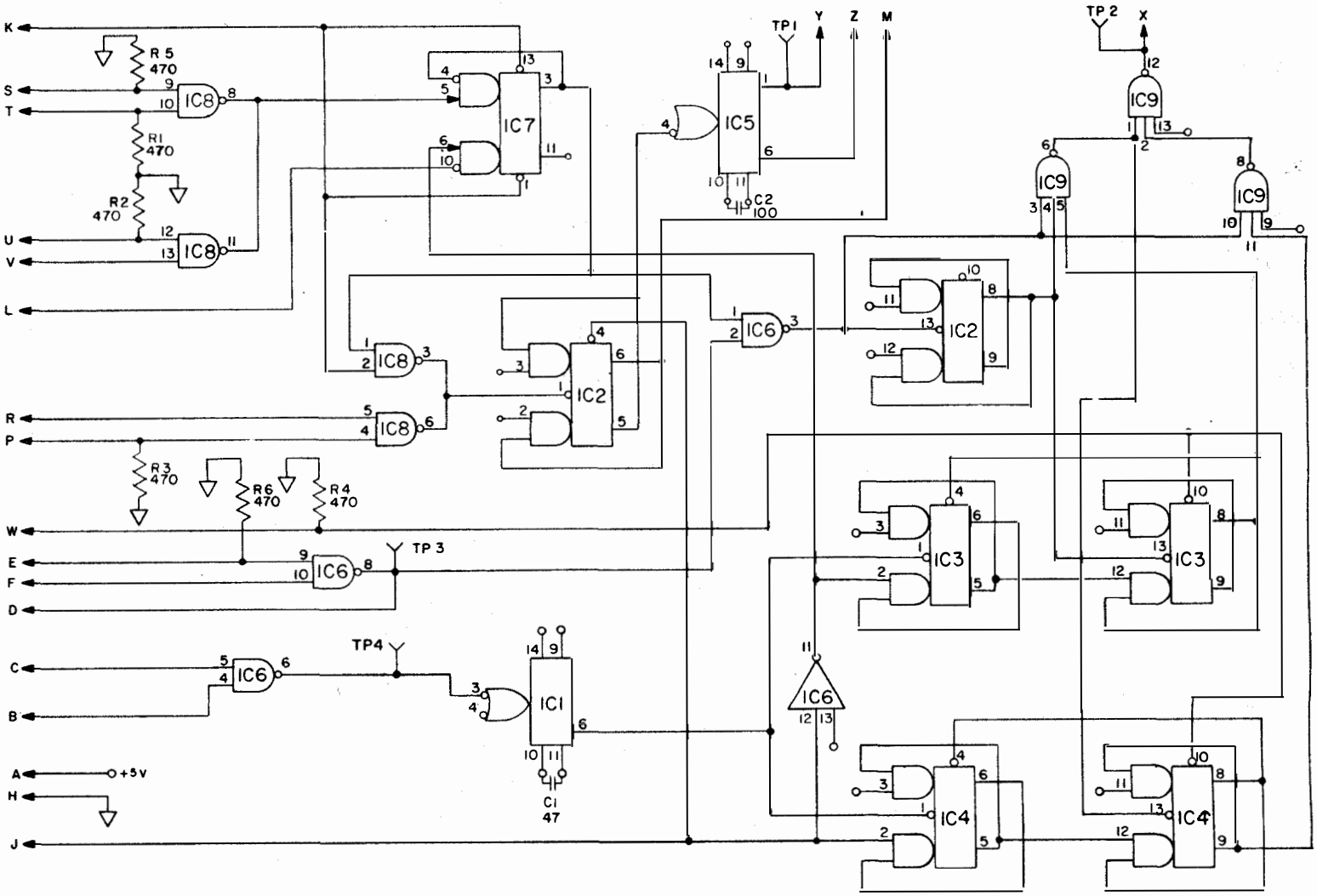


Figure 5-7. Timing Control Board 1A1A4 Component Location



NOTES:

1 - UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, ±5% TOL., CAPACITANCES ARE IN UUF.

2 - DENOTES COMMON TIE OR VOLTAGE BUS.

3 - DENOTES CONNECTOR POINTS.

Figure 5-8. Timing Control Board 1A1A4 Schematic

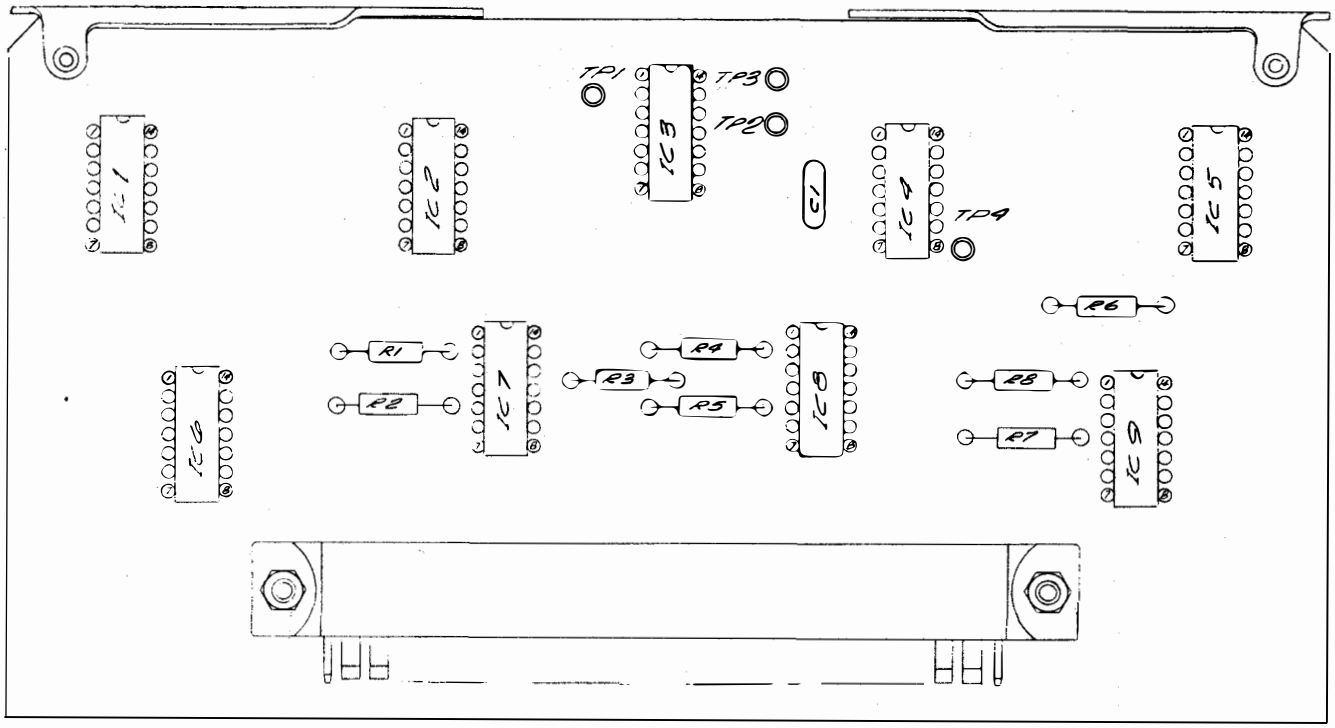
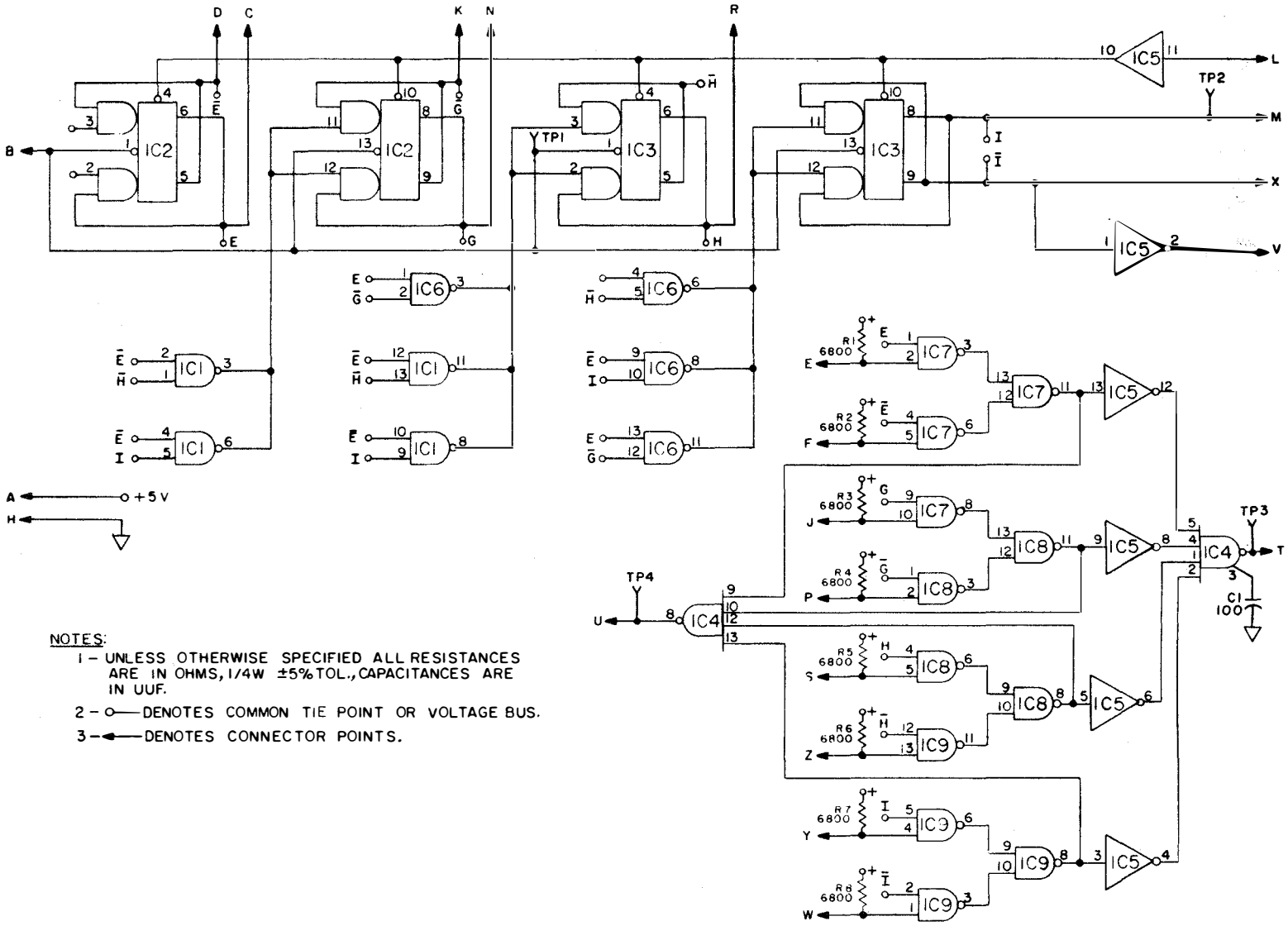


Figure 5-9. BCD Counter and Trigger I Board 1A1A5 Component Location



NOTES:

1 – UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS, 1/4W ±5% TOL., CAPACITANCES ARE IN UUF.

2 – DENOTES COMMON TIE POINT OR VOLTAGE BUS.

3 – DENOTES CONNECTOR POINTS.

Figure 5-10. BCD Counter and Trigger I Board 1A1A5 Schematic

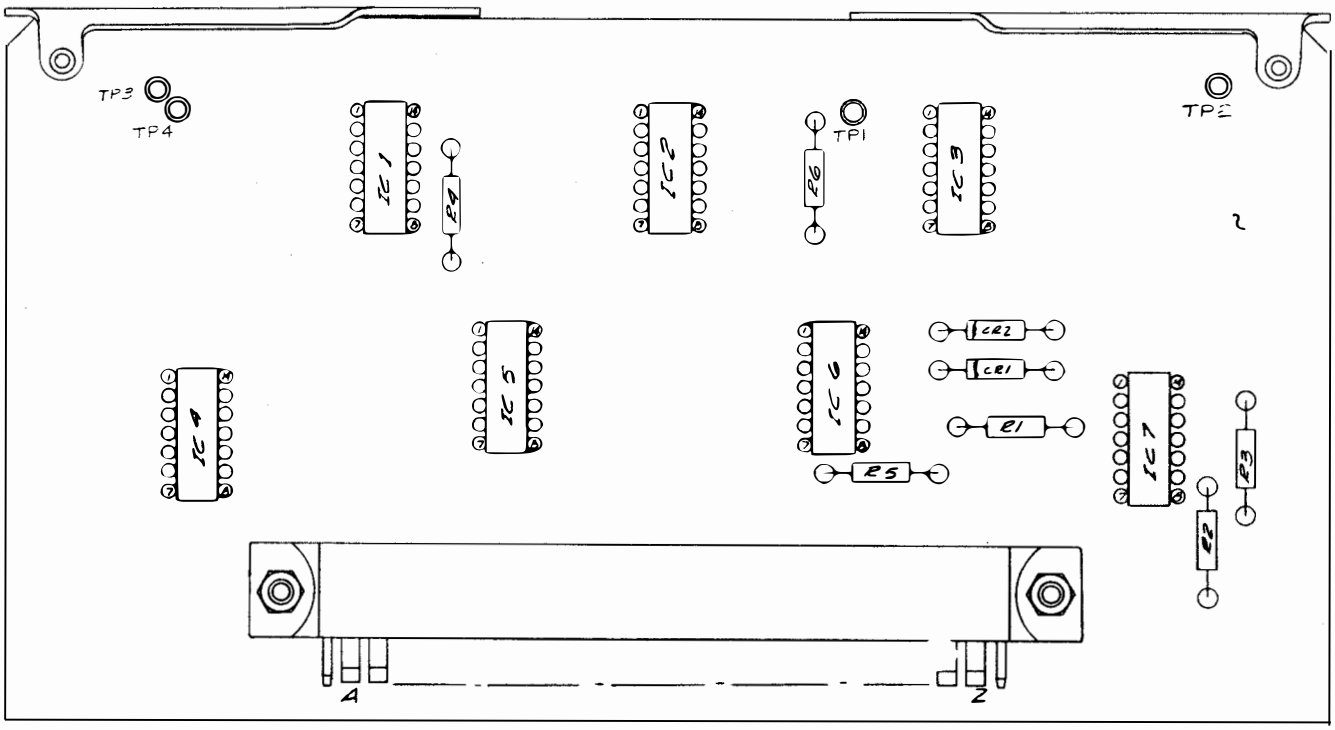


Figure 5-11. Stop Mark Trigger Board 1A1A6 Component Location

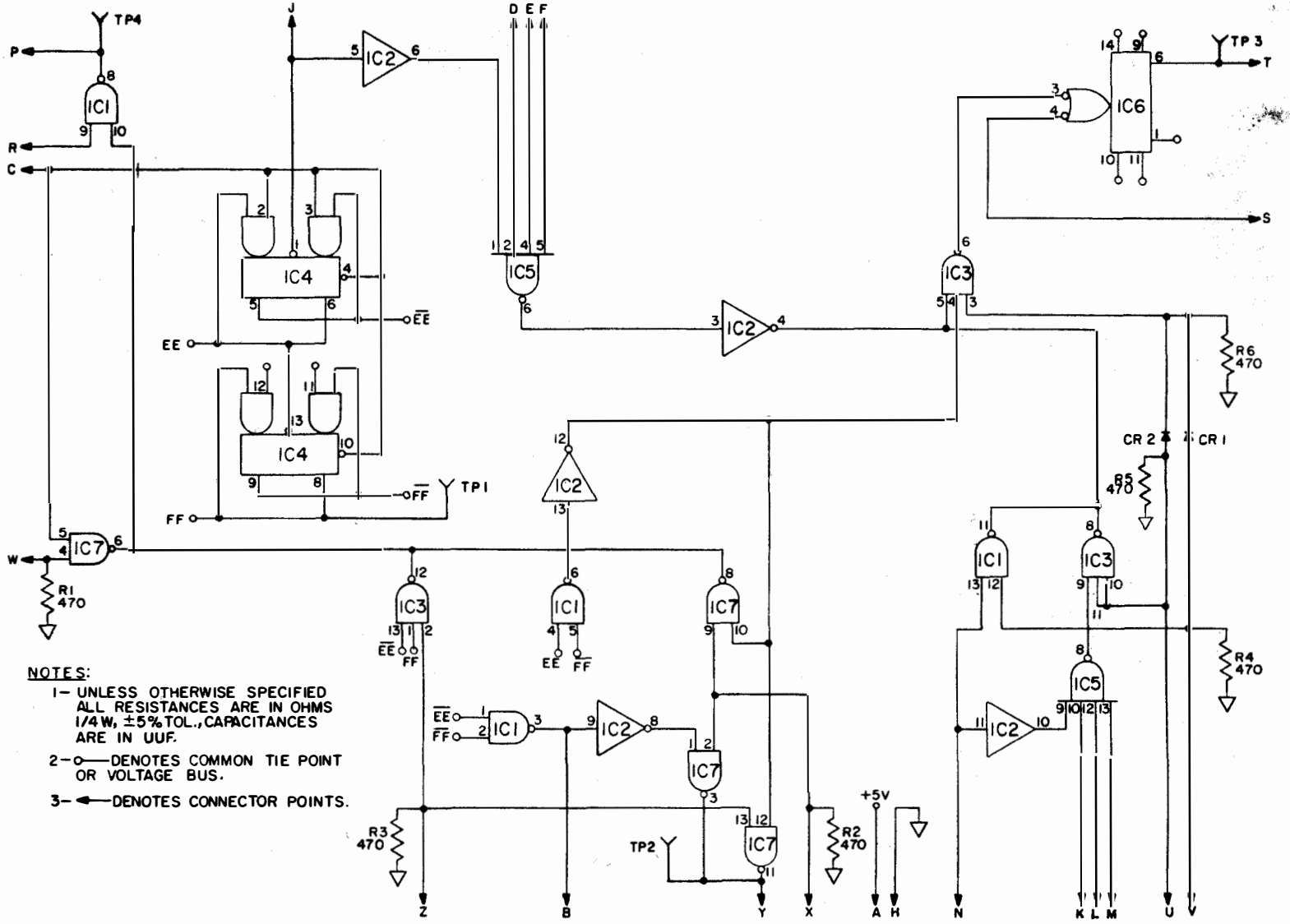


Figure 5-12. Stop Mark Trigger Board 1A1A6 Schematic

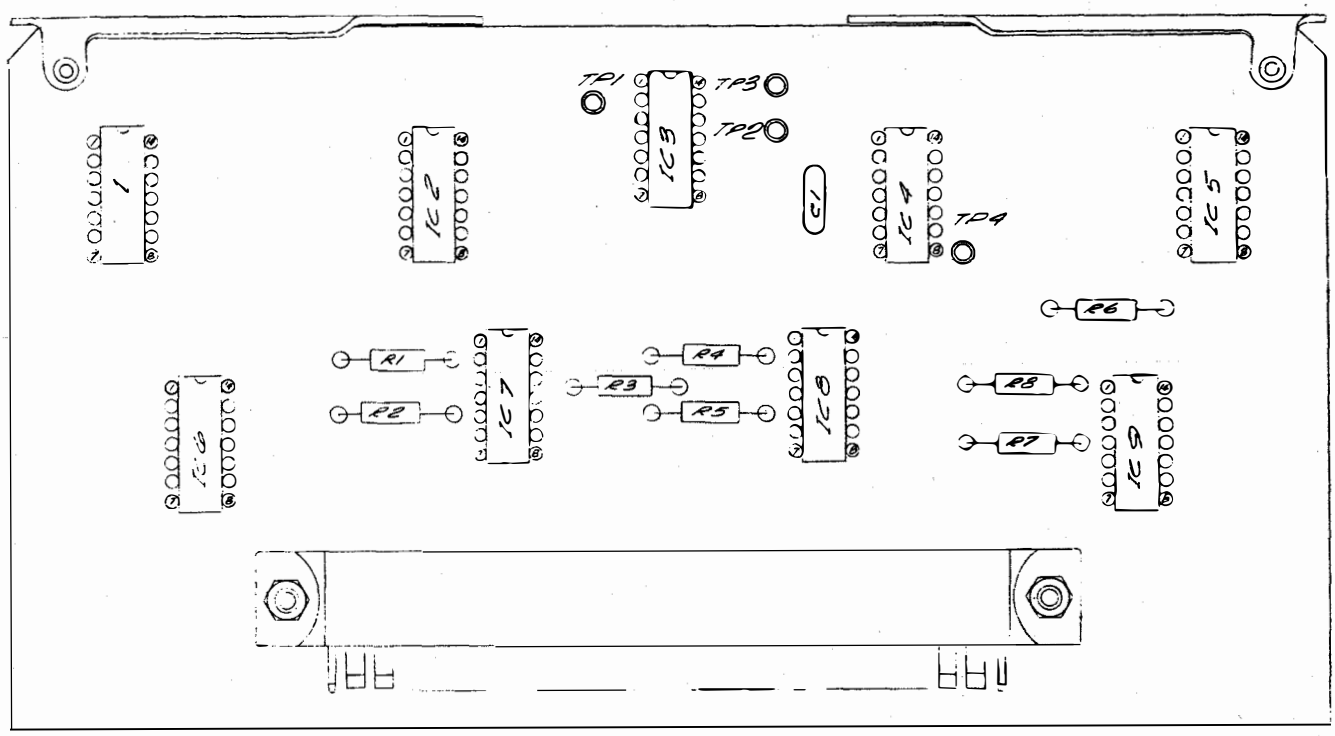


Figure 5-13. BCD Counter and Trigger II Board 1A1A7 Component Location

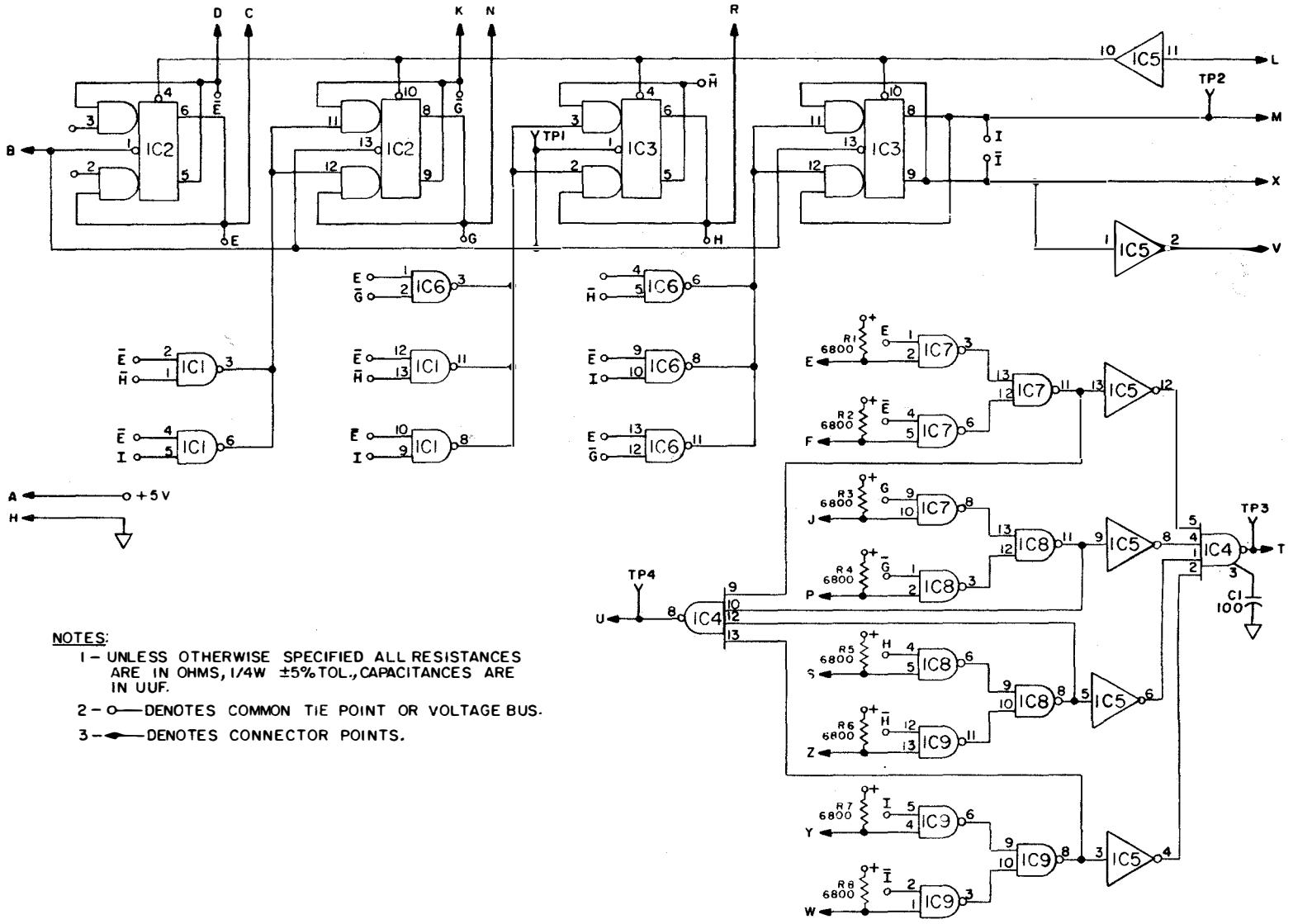


Figure 5-14. BCD Counter and Trigger II Board 1A1A7 Schematic

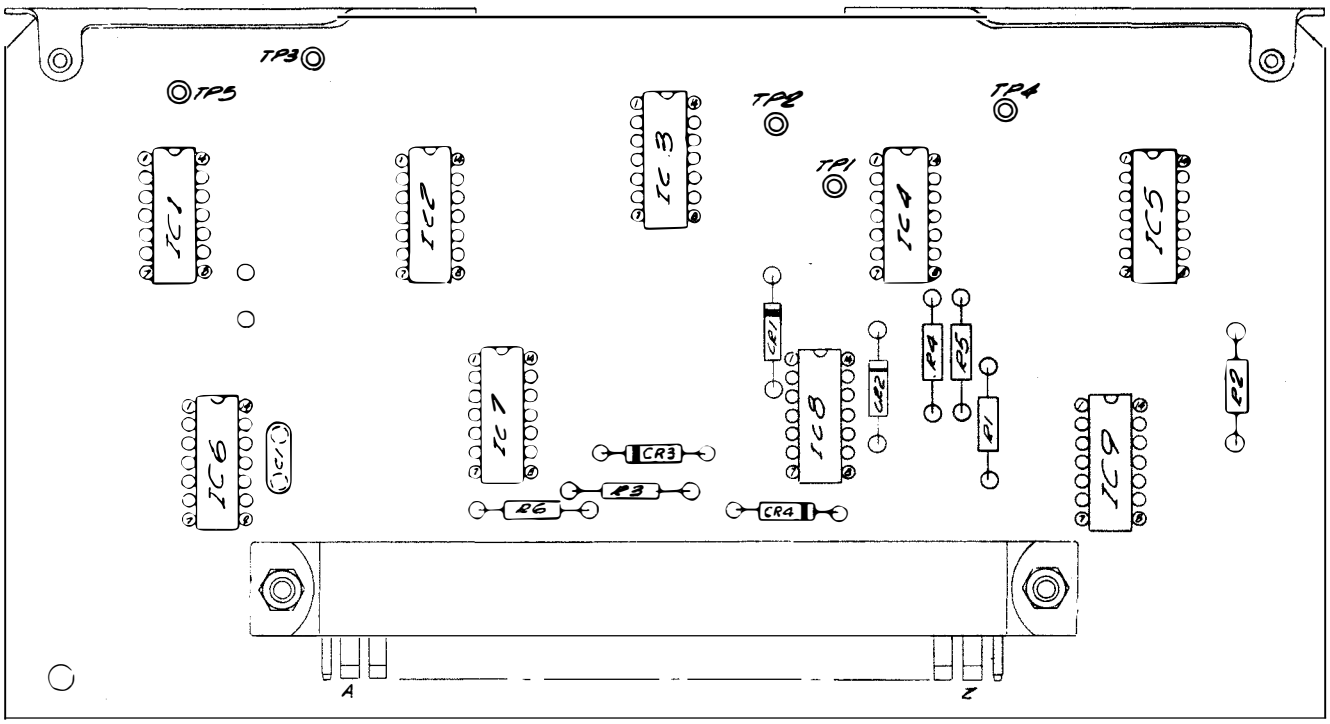
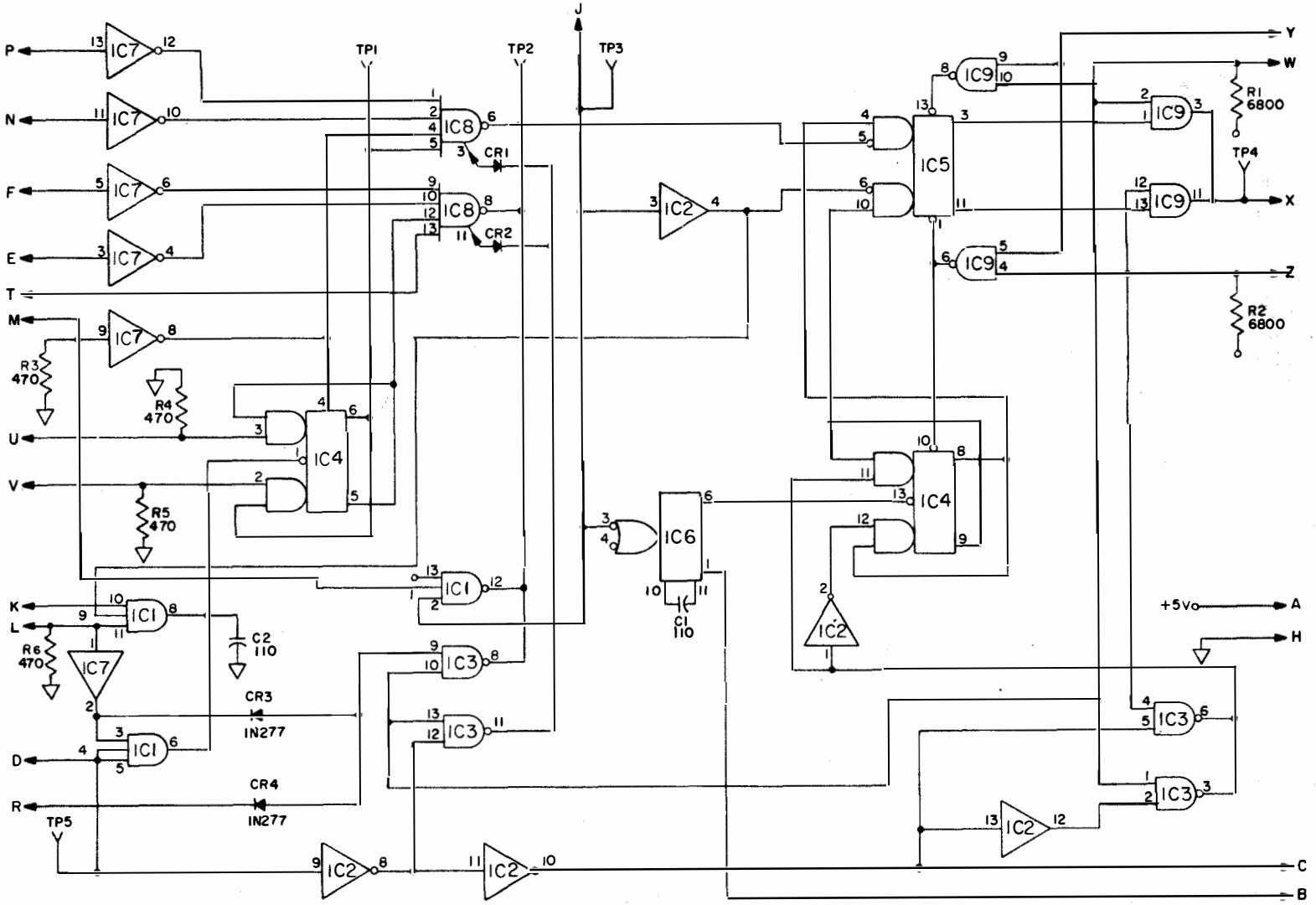


Figure 5-15. Signal Processor Board 1A1A8 Component Location



NOTES:

1— UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, ±5%TOL., CAPACITANCES ARE IN UUF.

2—o—DENOTES COMMON TIE POINT OR VOLTAGE BUS.

3—◄—DENOTES CONNECTOR POINTS.

4— UNLESS OTHERWISE SPECIFIED ALL DIODES ARE TYPE IN3064.

Figure 5-16. Signal Processor Board 1A1A8 Schematic

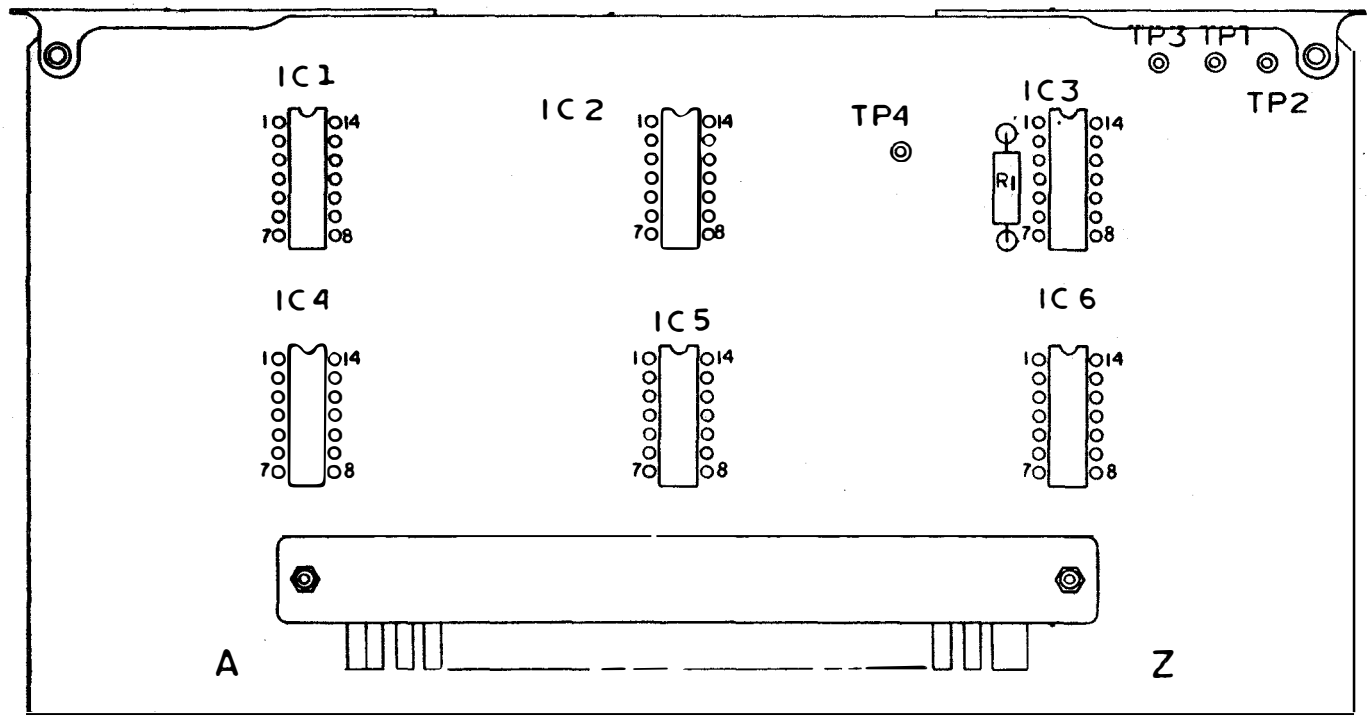
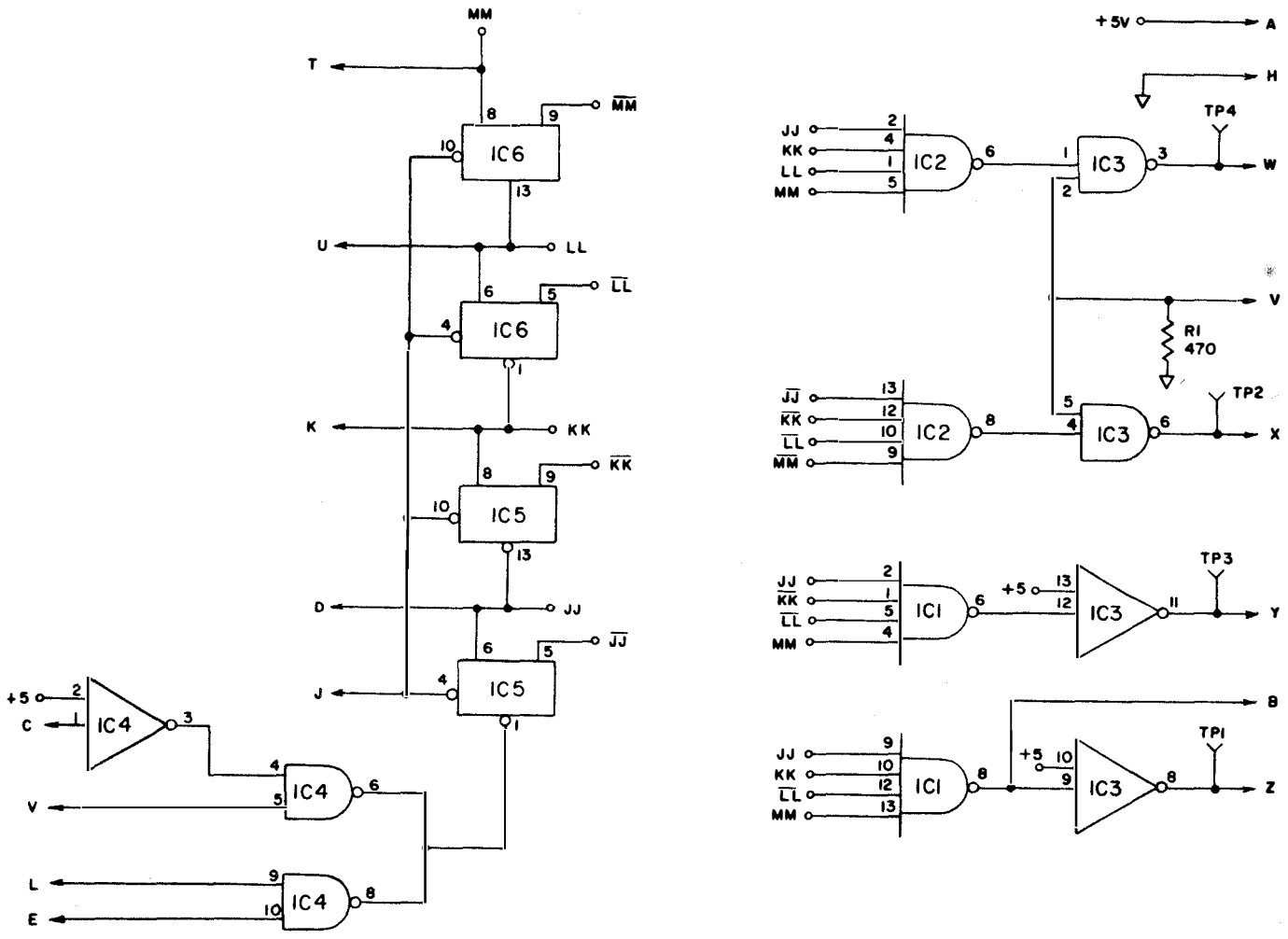


Figure 5-17. Character Counter II Board 1A1A9 Component Location



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, ±5% TOL
2. o— DENOTES COMMON TIE POINT OR VOLTAGE BUS
3. ◄— DENOTES CONNECTOR POINTS

Figure 5-18. Character Counter II Board 1A1A9 Schematic

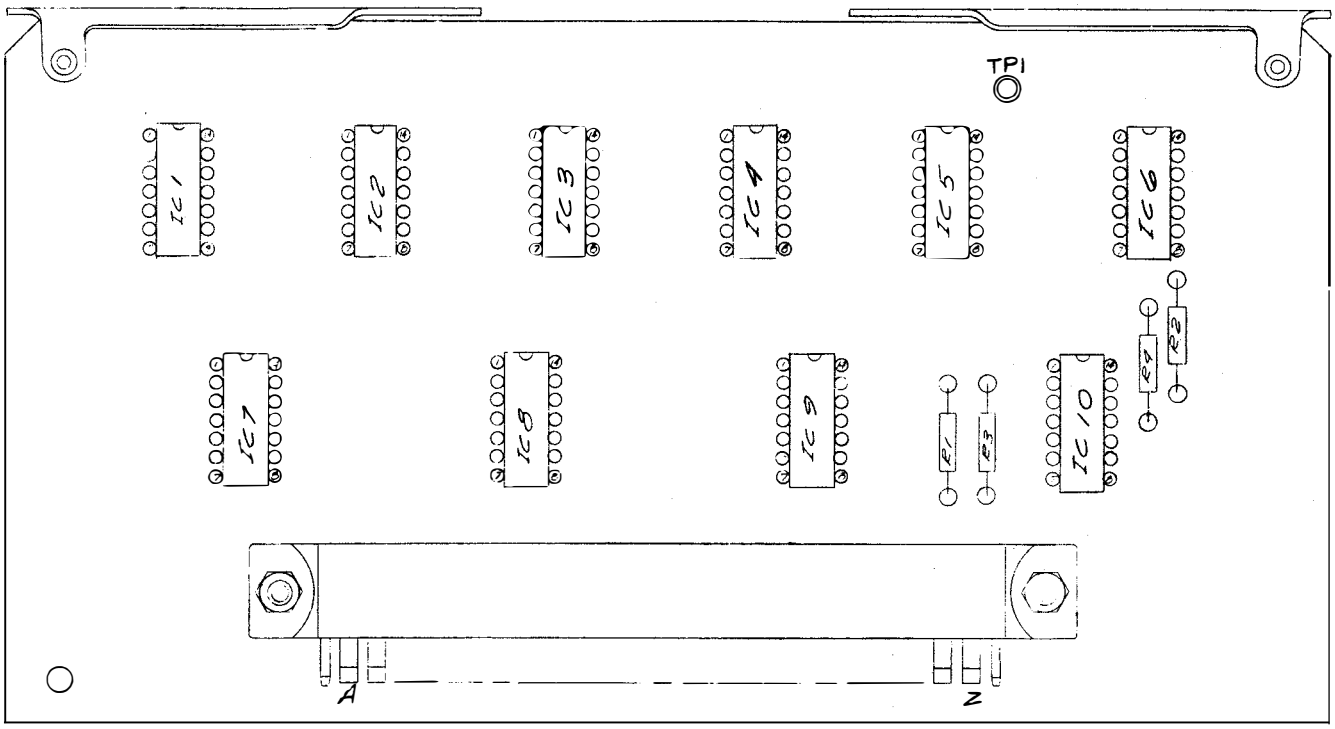
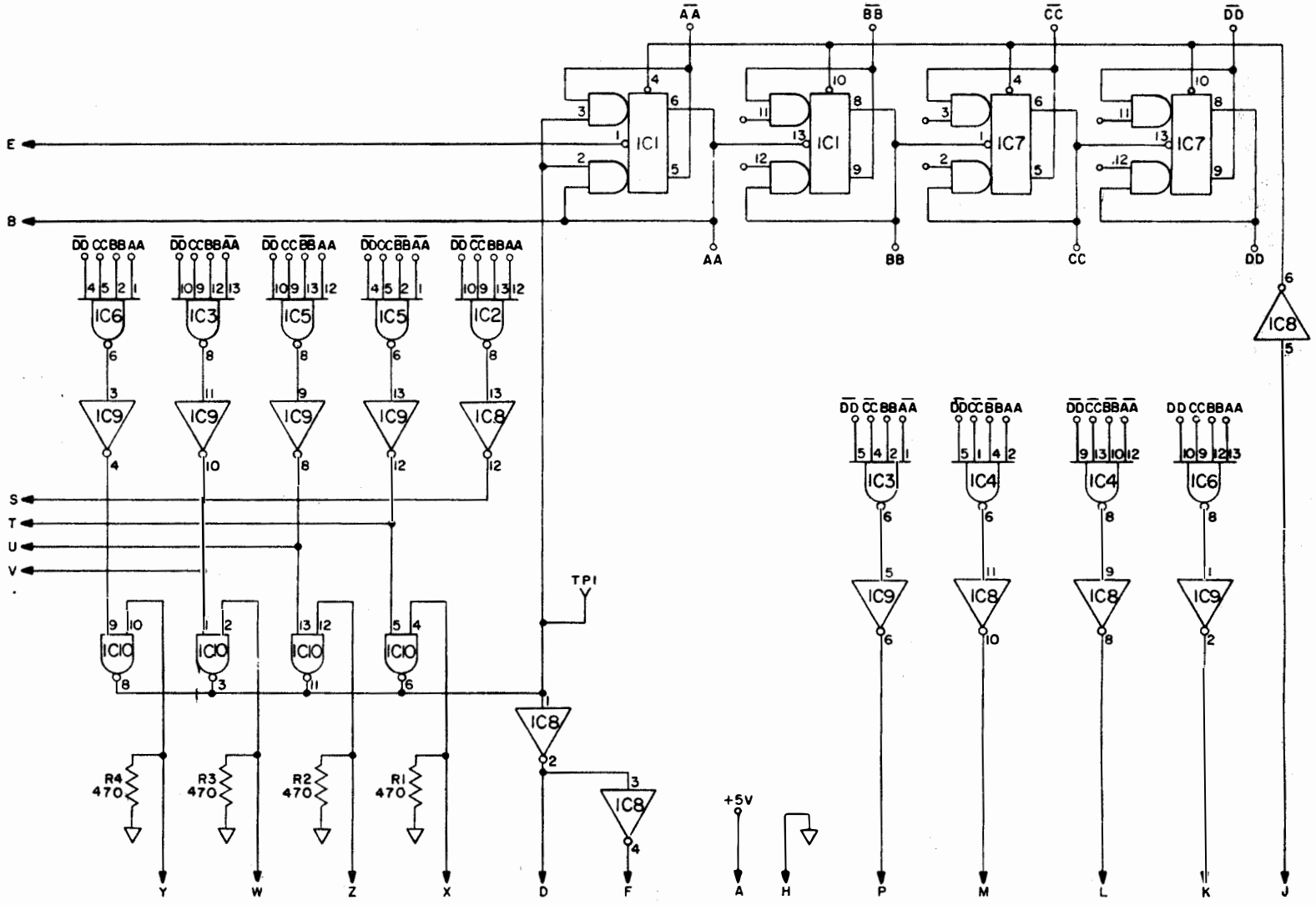


Figure 5-19. Bit Counter and Gates Board 1A1A10 Component Location



NOTES:

1- UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, ±5%TOL., CAPACITANCES ARE IN UUF.

2- o— DENOTES COMMON TIE POINT OR VOLTAGE BUS.

3- ◄— DENOTES CONNECTOR POINTS.

Figure 5-20. Bit Counter and Gates Board 1A1A10 Schematic

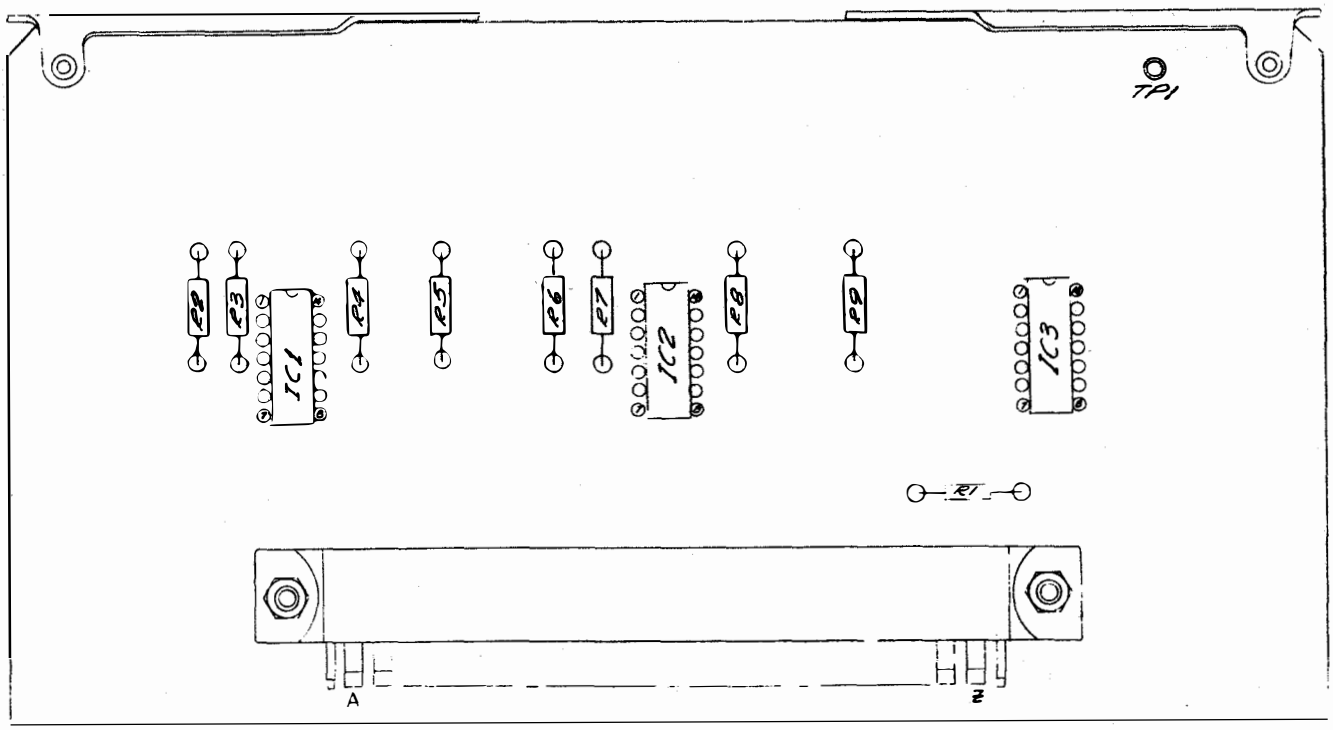


Figure 5-21. Selected Character Board 1A1A11 Component Location

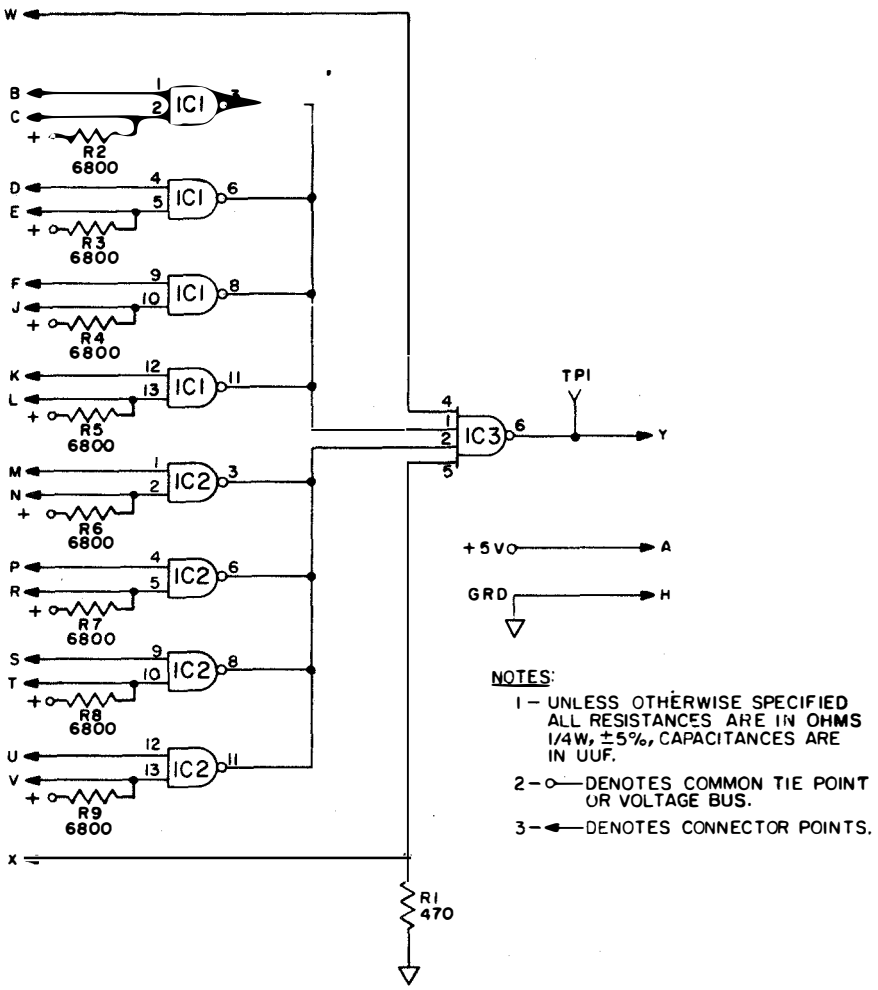


Figure 5-22. Selected Character Board 1A1A11 Schematic

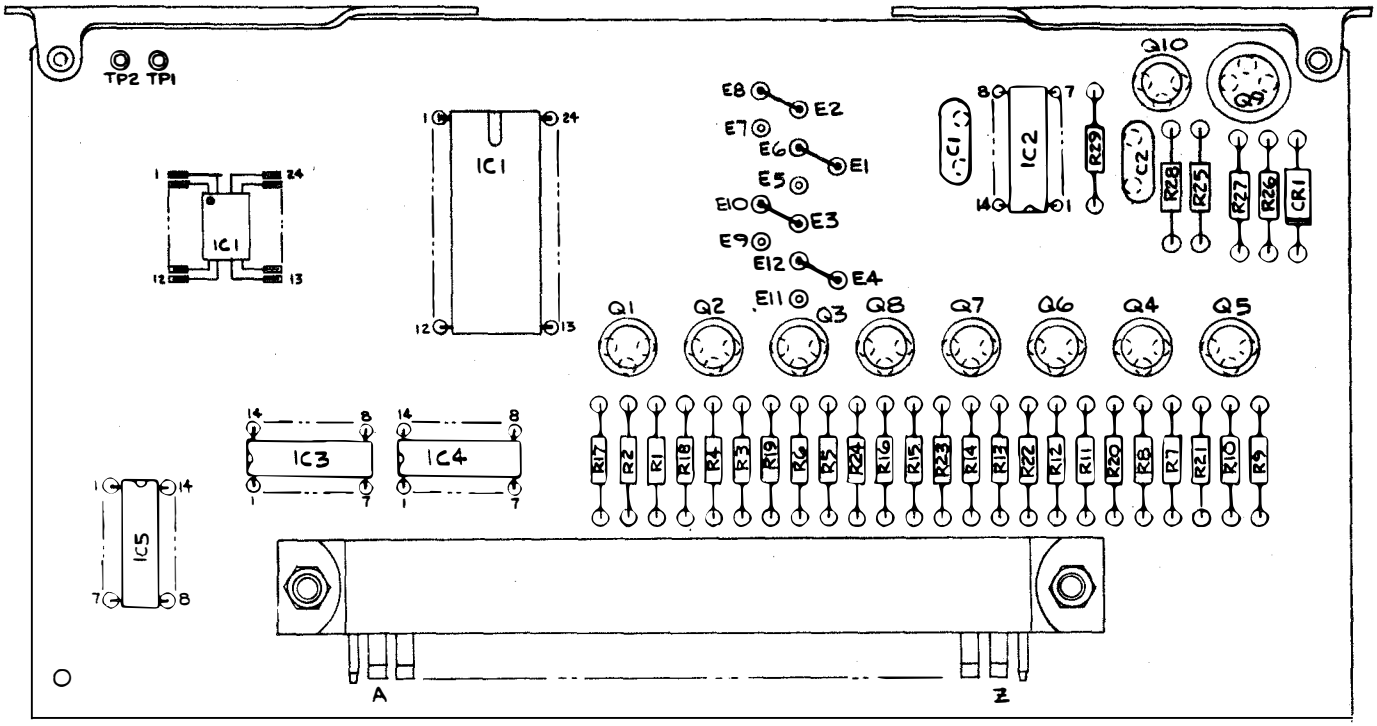
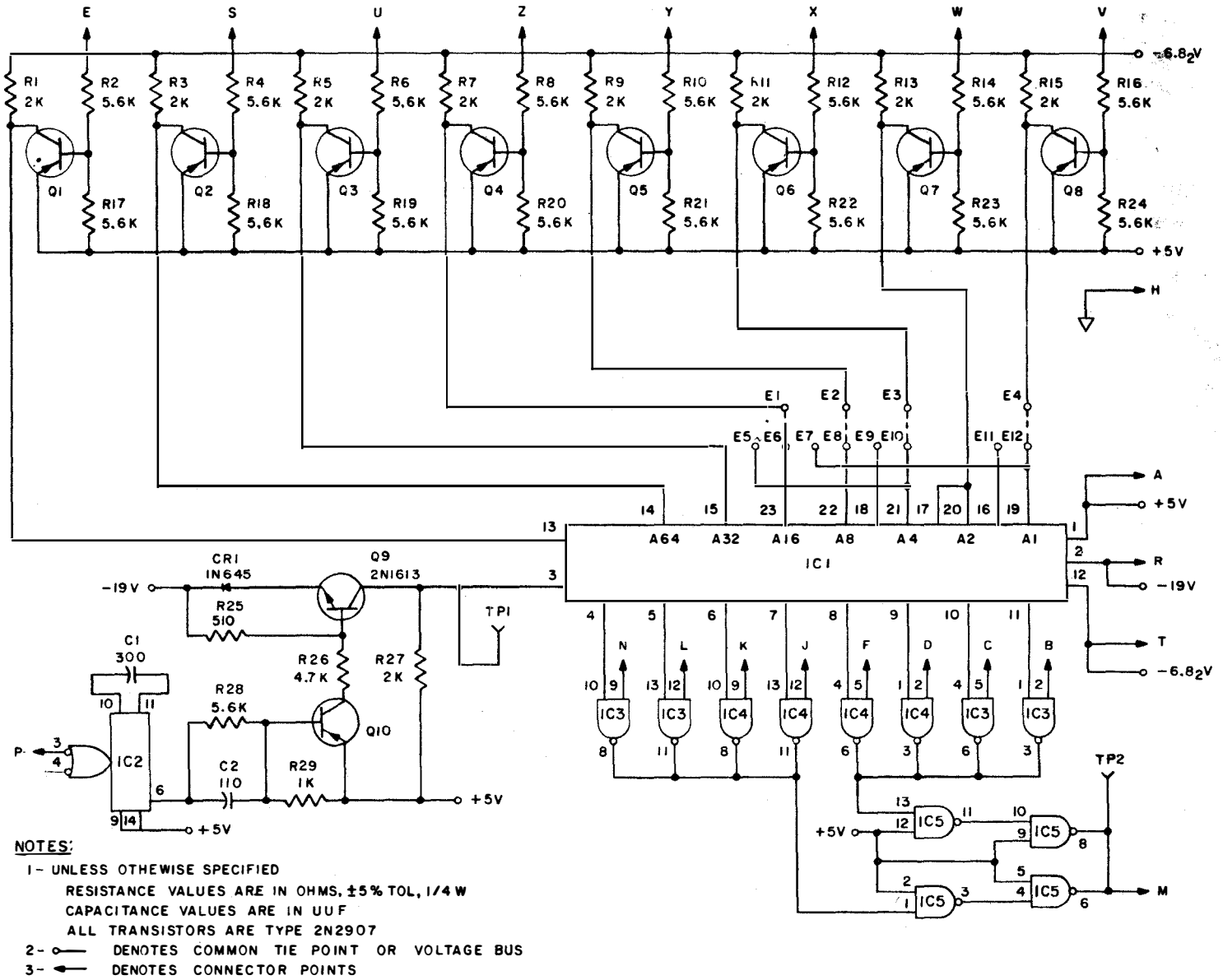


Figure 5-23. Fox Message Board 1A1A12 Component Location (36021120)



NOTES:

1- UNLESS OTHEWISE SPECIFIED
RESISTANCE VALUES ARE IN OHMS, ±5% TOL, 1/4 W
CAPACITANCE VALUES ARE IN UUF
ALL TRANSISTORS ARE TYPE 2N2907

2- —o— DENOTES COMMON TIE POINT OR VOLTAGE BUS

3- ←— DENOTES CONNECTOR POINTS

Figure 5-24. Fox Message Board 1A1A12 Schematic (36021120)

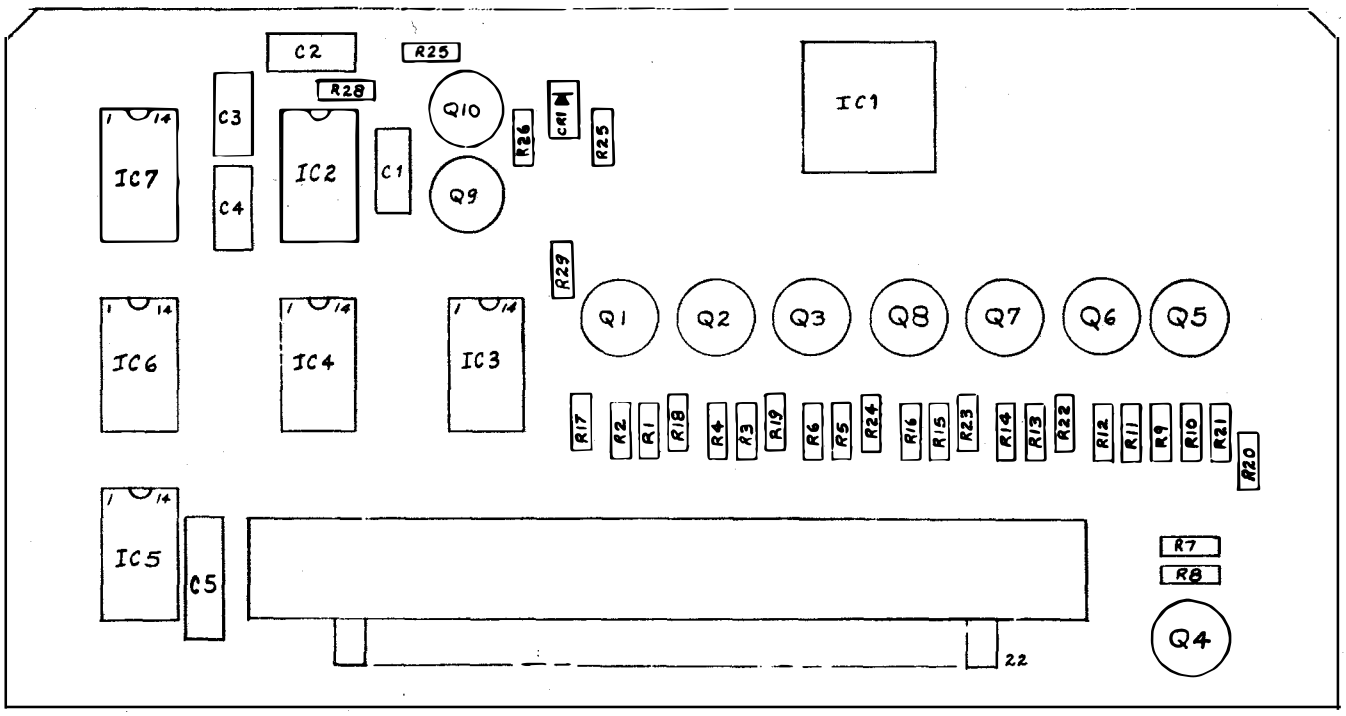


Figure 5-25. Fox Message Board 1A1A12 Component Location (36021220)

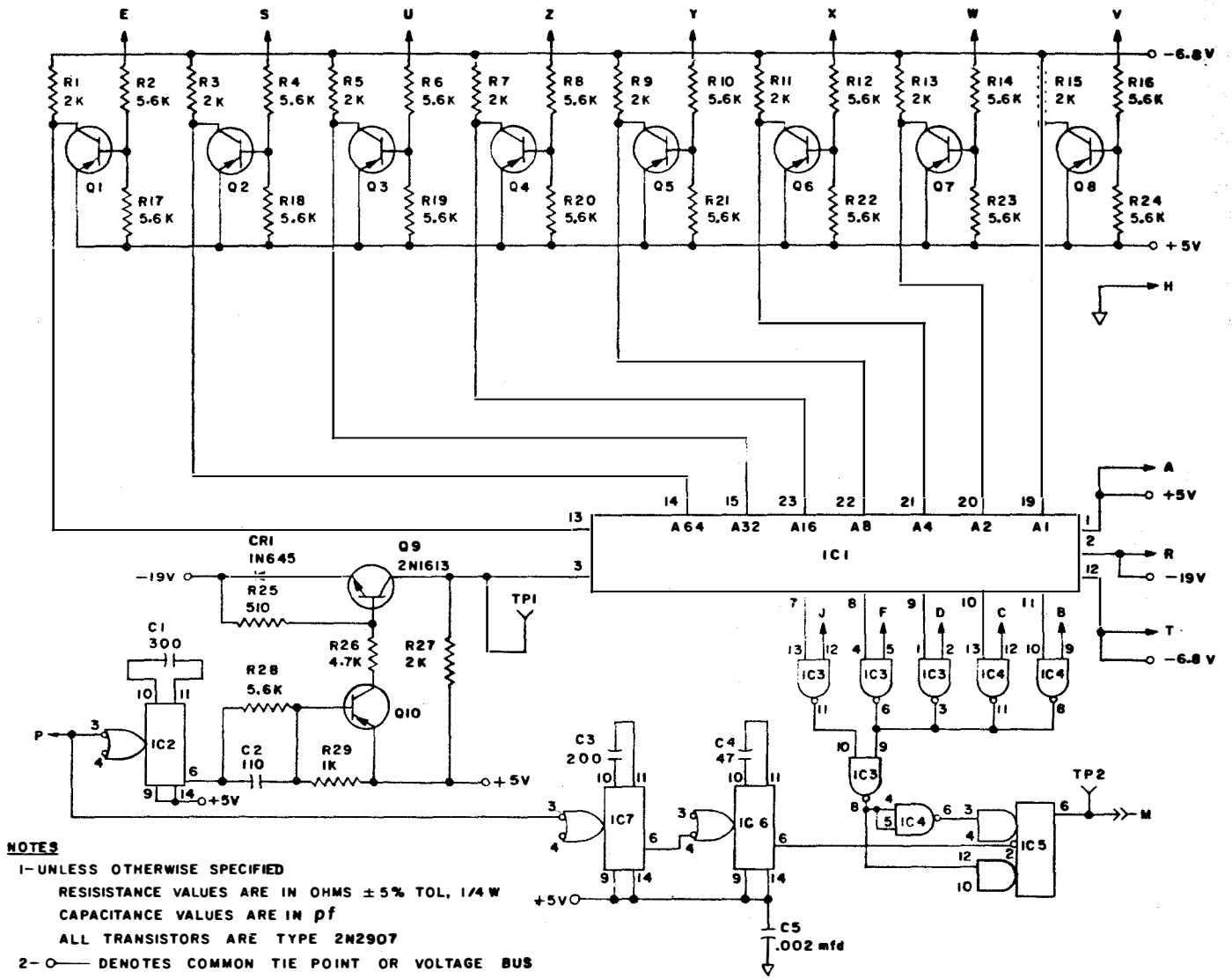
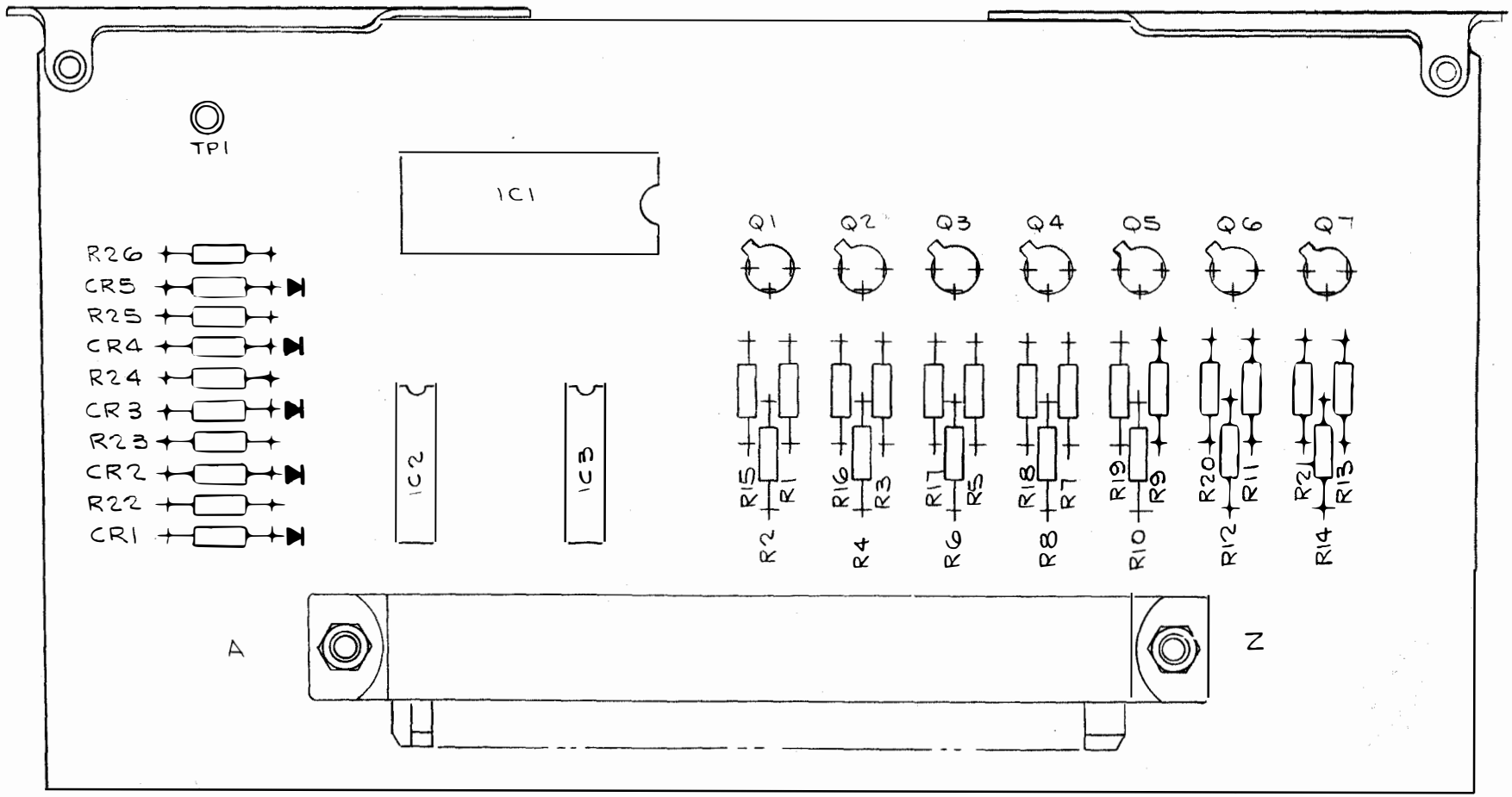
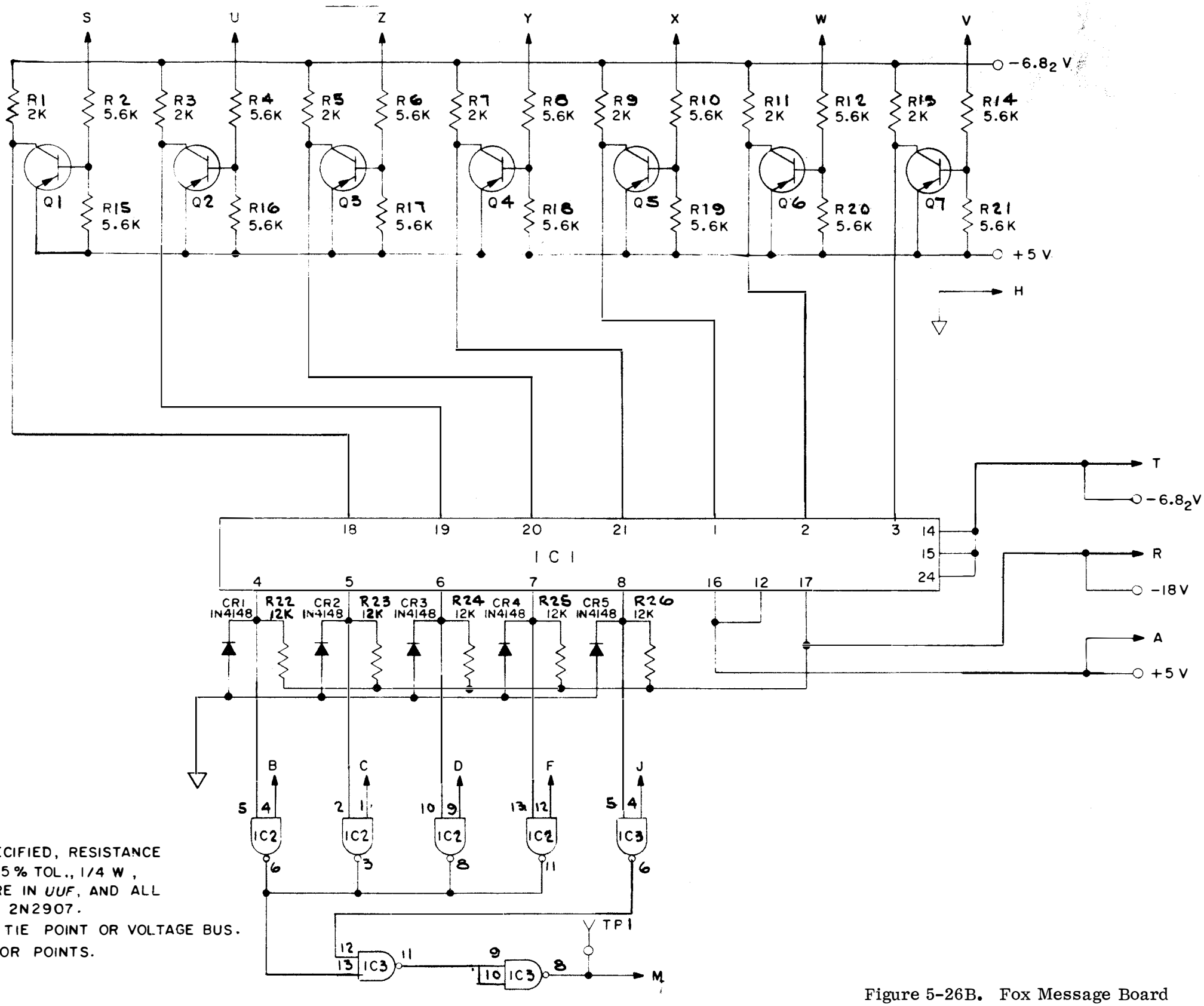


Figure 5-26. Fox Message Board 1A1A12 Schematic (36021220)



NOTES:
1. SOLDER SHALL BE COMPOSITION SN60 WARP 2 PER QQ-S-571.
2. FOR SCHEMATIC SEE DWG. 36022122.

Figure 5-26A. Fox Message Board 1A1A12-2 Component Location (36021120-2)



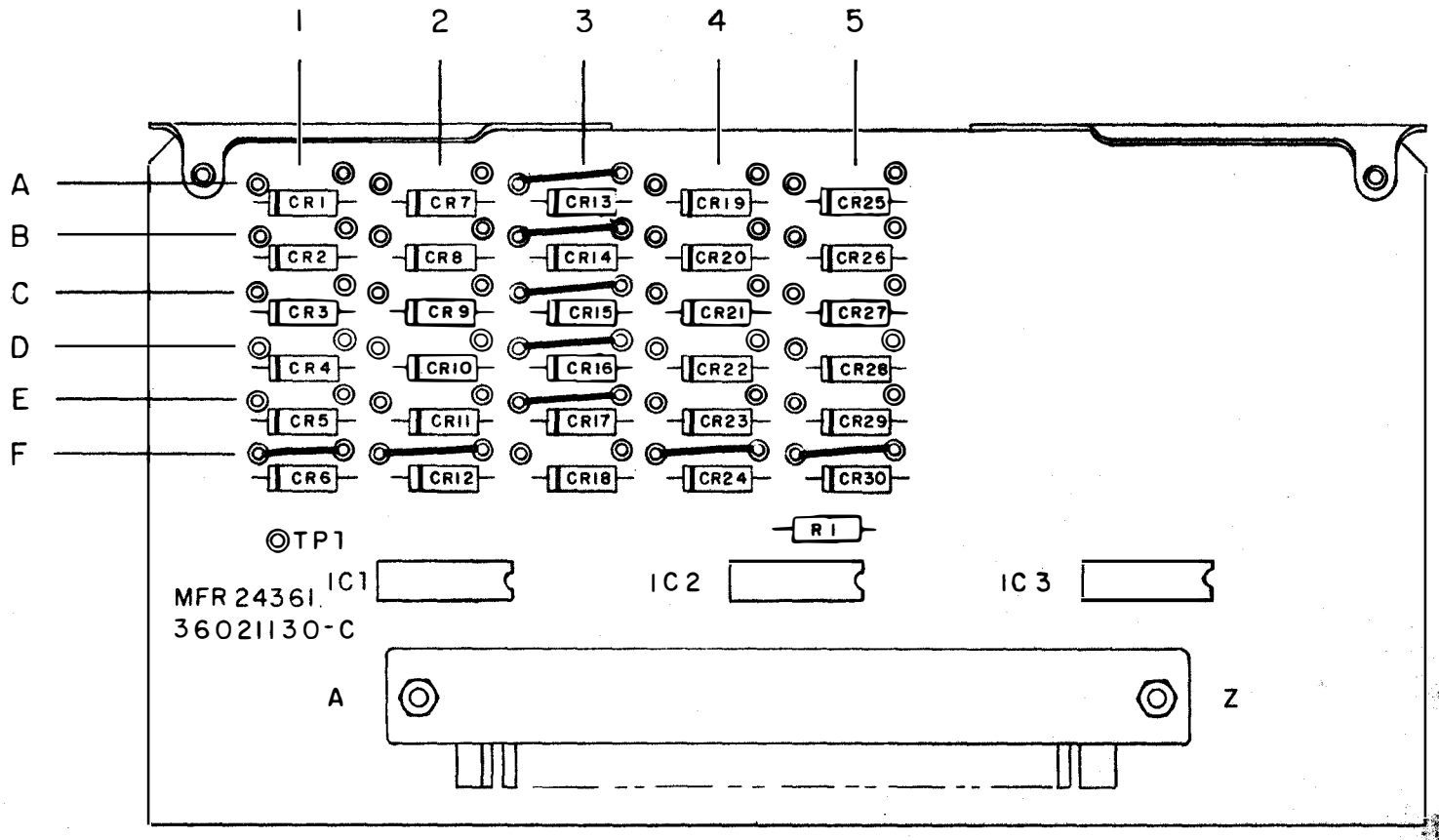
NOTES:

1- UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOL., 1/4 W, CAPACITANCE VALUES ARE IN *UUF*, AND ALL TRANSISTORS ARE TYPE 2N2907.

2- ○— DENOTES COMMON TIE POINT OR VOLTAGE BUS.

3- ◄— DENOTES CONNECTOR POINTS.

Figure 5-26B. Fox Message Board 1A1A12-2 Schematic (36021120-2)



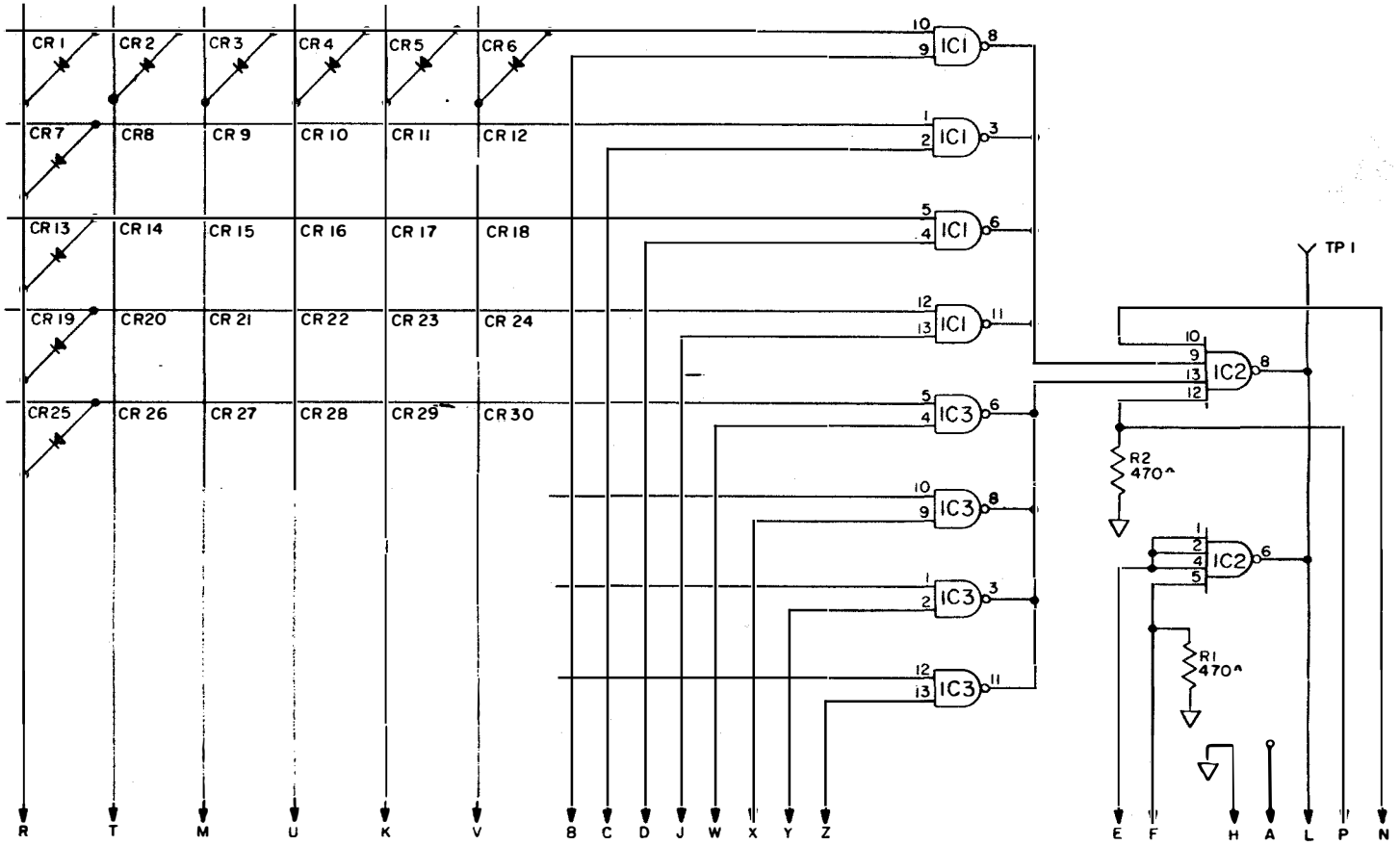
NOTES:

1- FOR STRAGGING, USE APPROXIMATELY 3/4" OF AWG 22 OR 24 SOLID TINNED BUS WIRE.

2- USE STANDARD PRINTED CIRCUIT BOARD SOLDERING TECHNIQUES.

3- THIS BOARD IS NORMALLY SUPPLIED WITH ALL SPACES (NO JUMPERS).

Figure 5-27. Call Letter Matrix Board 1A1A13 Component Location



NOTES:

1 – UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, ±5% TOL., CAPACITANCES ARE IN UUF.
2 – o— DENOTES COMMON TIE POINT OR VOLTAGE BUS.
3 – ◄— DENOTES CONNECTOR POINTS
4 – UNLESS OTHERWISE SPECIFIED ALL DIODES ARE TYPE IN3064.

Figure 5-28. Call Letter Matrix Board 1A1A13 Schematic

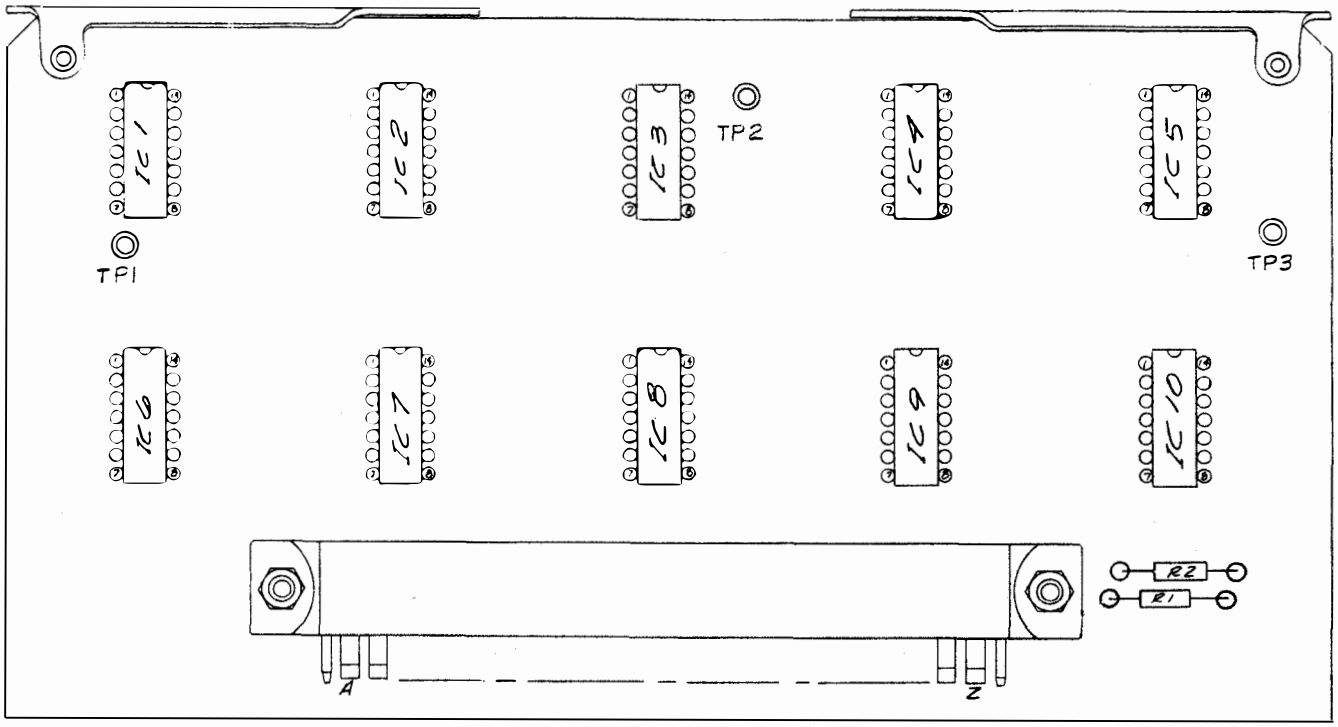
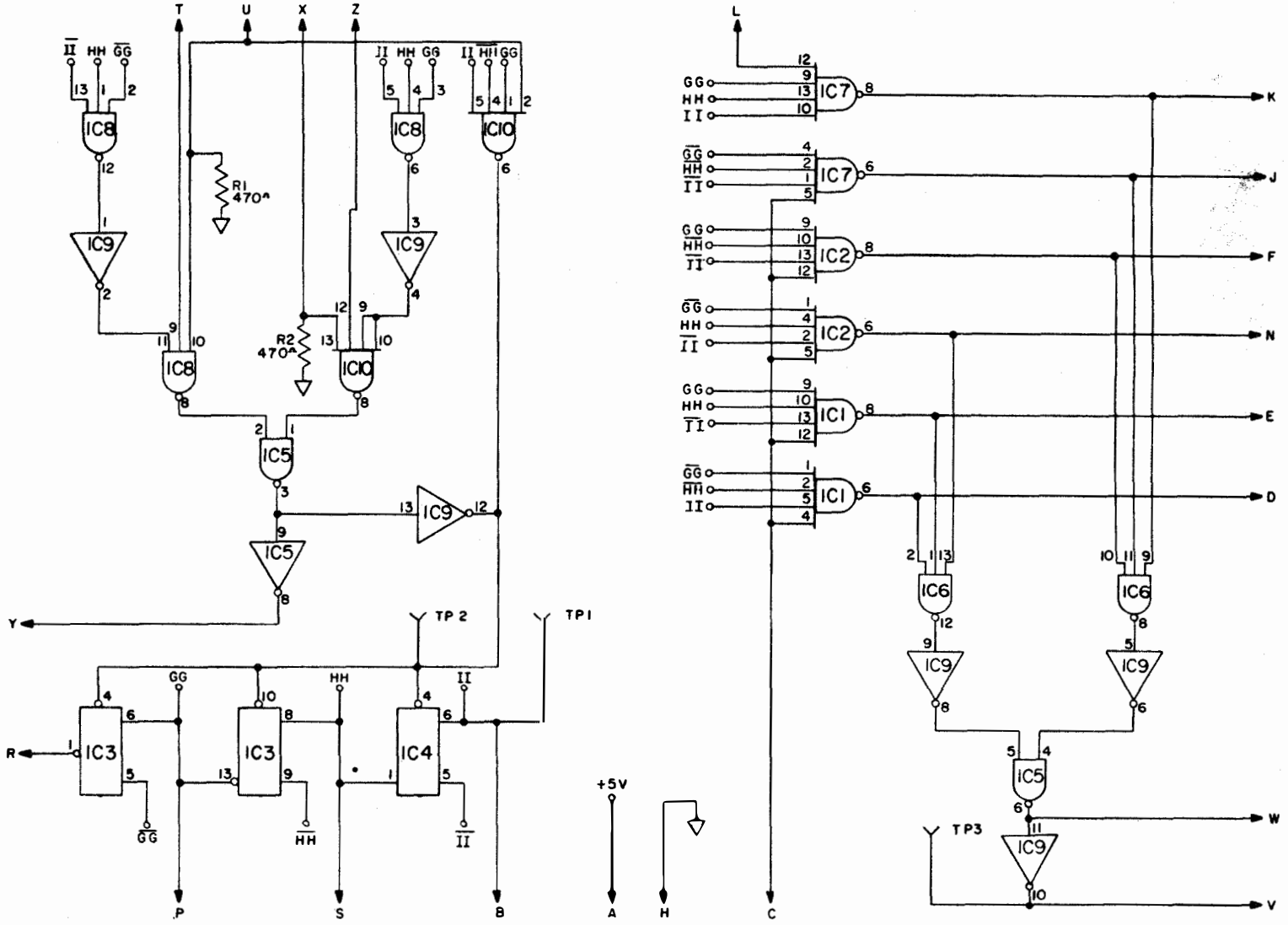


Figure 5-29. Character Counter I Board 1A1A14 Component Location



NOTES:
1- UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W., ±5% TOL., CAPACITANCES ARE IN UUF.
2- o—DENOTES COMMON TIE POINTS OR VOLTAGE BUS.
3- ←—DENOTES CONNECTOR POINTS.

Figure 5-30. Character Counter I Board 1A1A14 Schematic

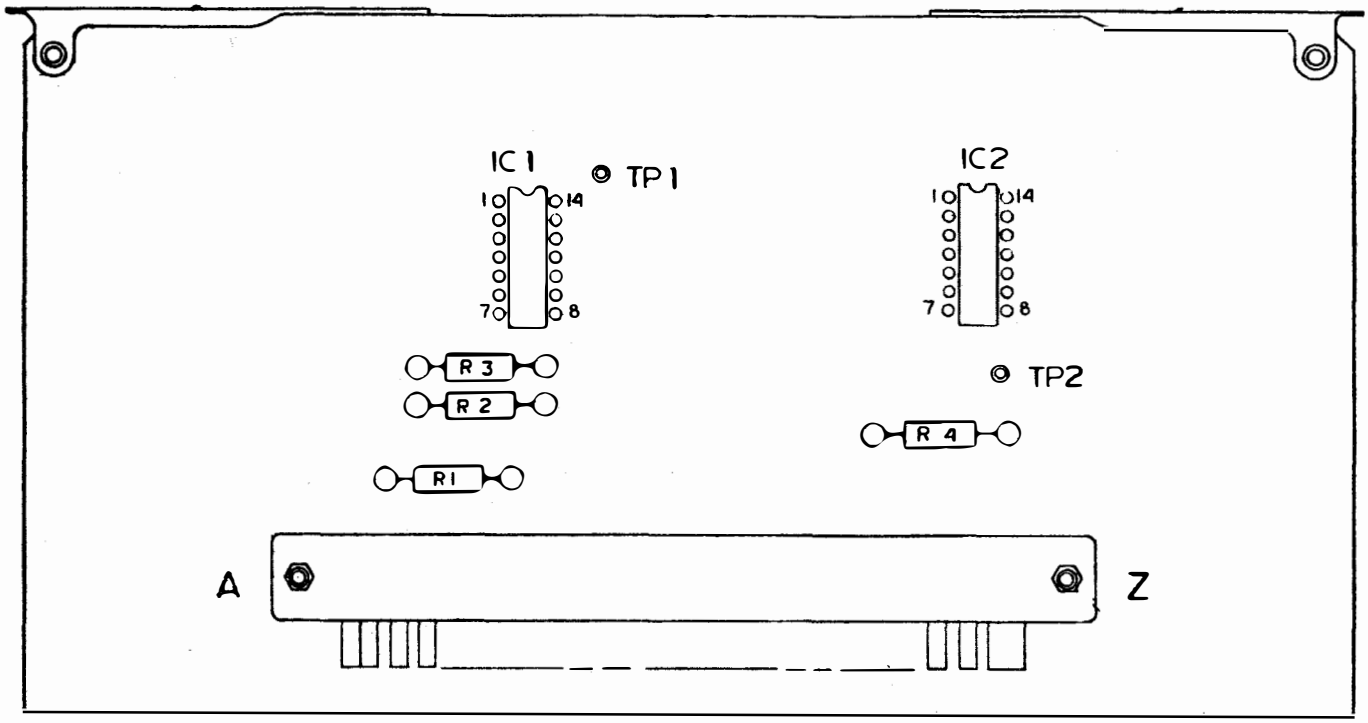
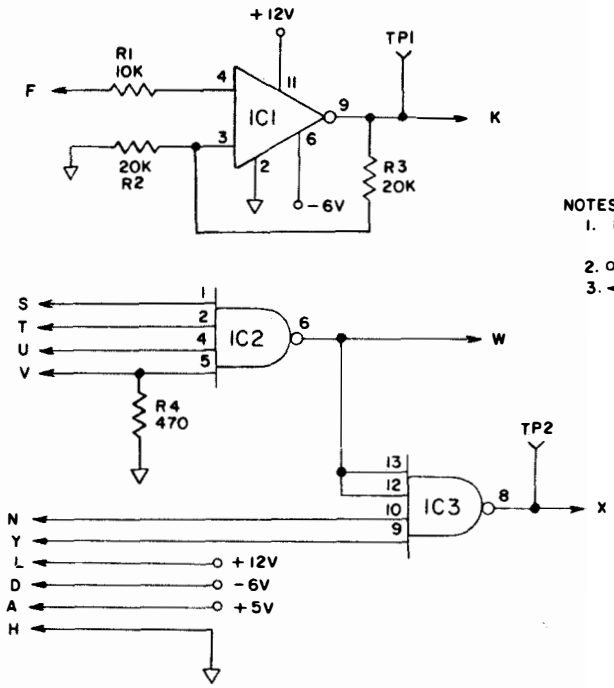


Figure 5-31. Message Select Gates 1A1A15 Components Location



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4W, 5% TOL.
2. o— DENOTES COMMON TIE POINT OR VOLTAGE BUS
3. ◄— DENOTES CONNECTOR POINTS

Figure 5-32. Message Select Gates 1A1A15 Schematic

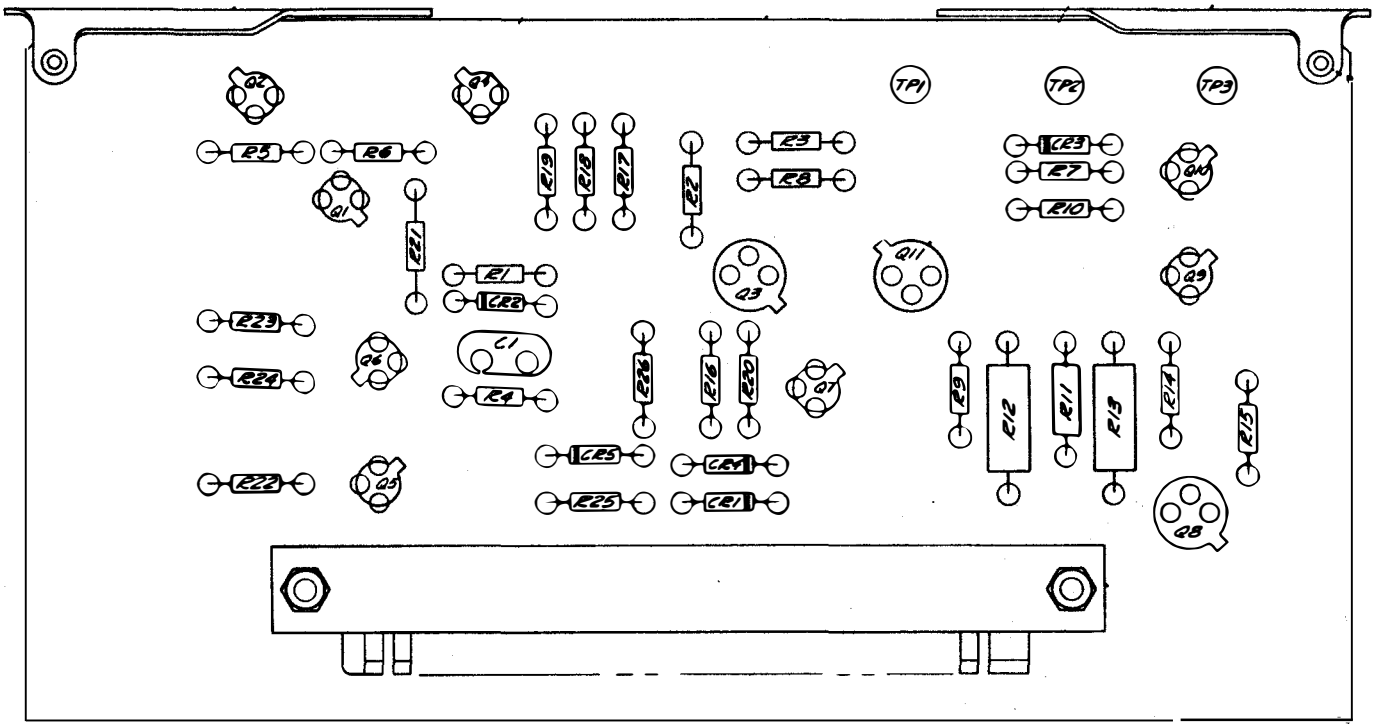
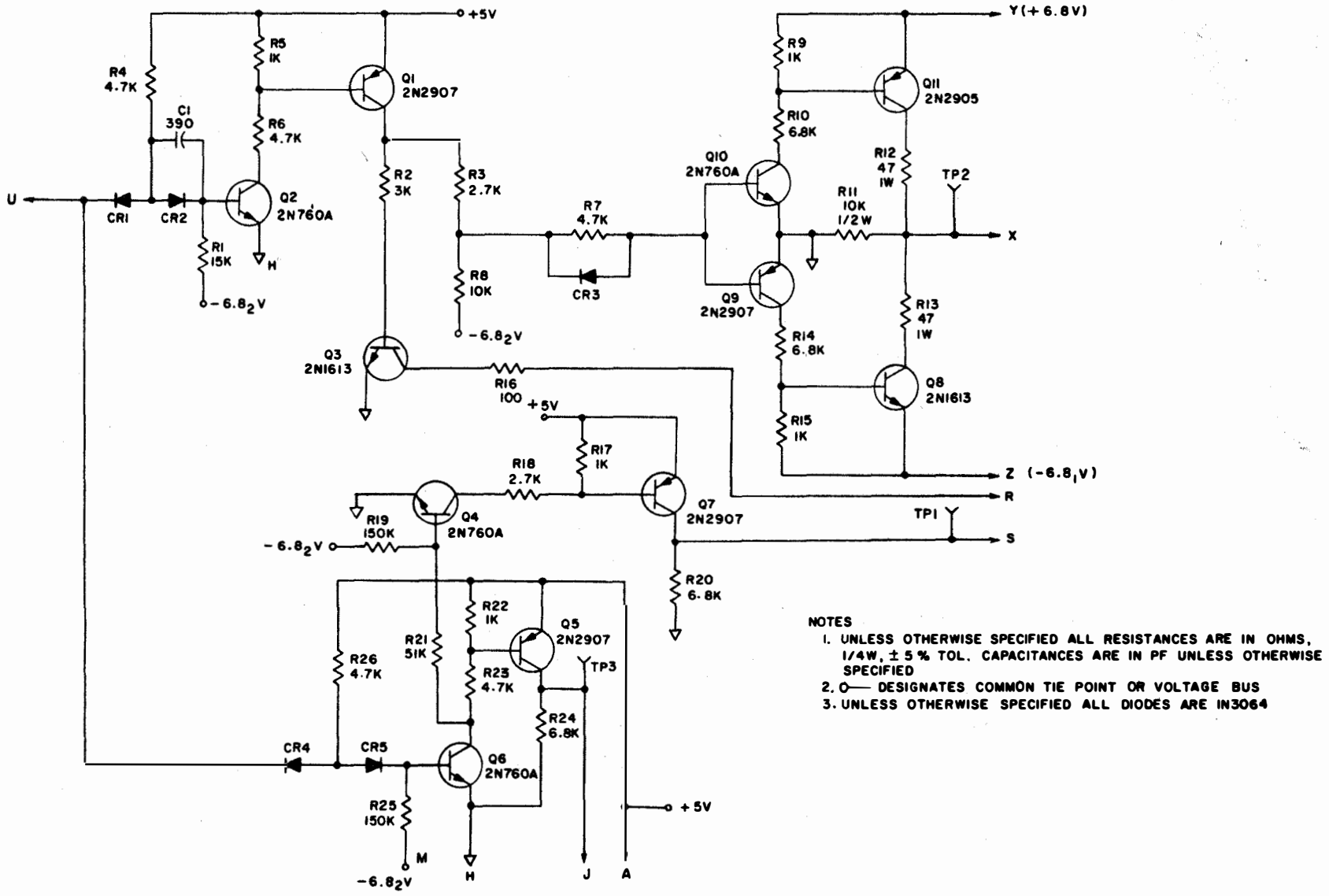


Figure 5-33. Output Driver 1A1A16 Component Location



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS, 1/4W, ± 5 % TOL. CAPACITANCES ARE IN PF UNLESS OTHERWISE SPECIFIED
2. O— DESIGNATES COMMON TIE POINT OR VOLTAGE BUS
3. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE IN3064

Figure 5-34. Output Driver 1A1A16 Schematic

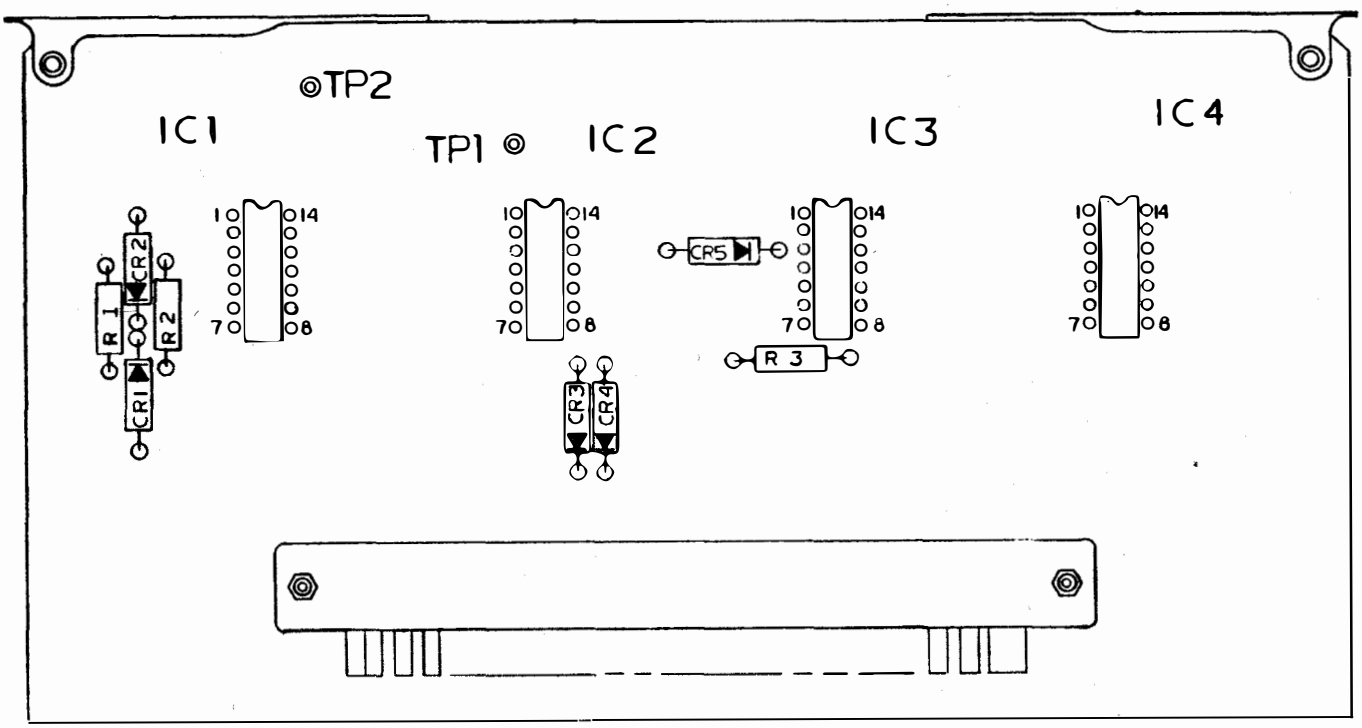
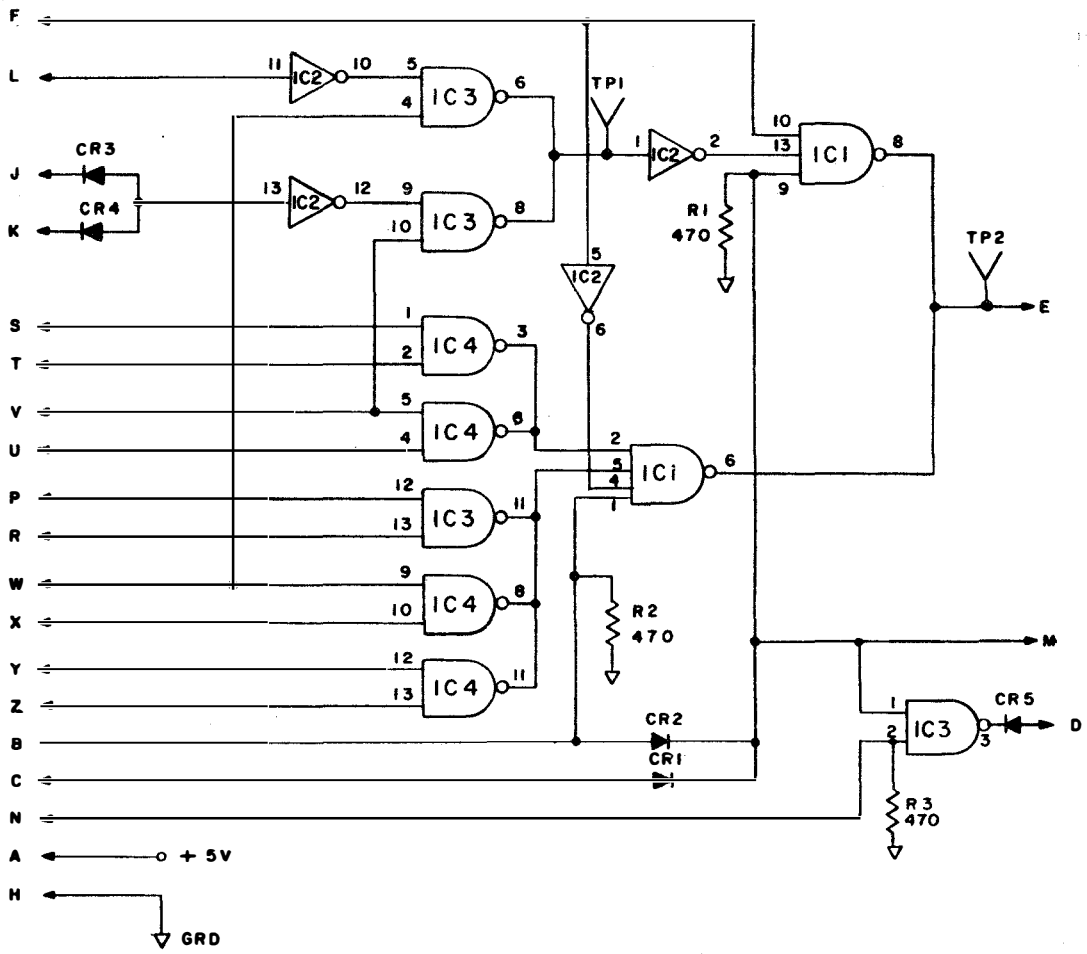


Figure 5-35. Word Matrix Control and Carriage Return 1A1A17 Component Location



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/4 W, 5% TOL.
2. o— DENOTES COMMON TIE POINT OR VOLTAGE BUS.
3. ←— DENOTES CONNECTOR POINTS.

Figure 5-36. Word Matrix Control and Carriage Return 1A1A17 Schematic

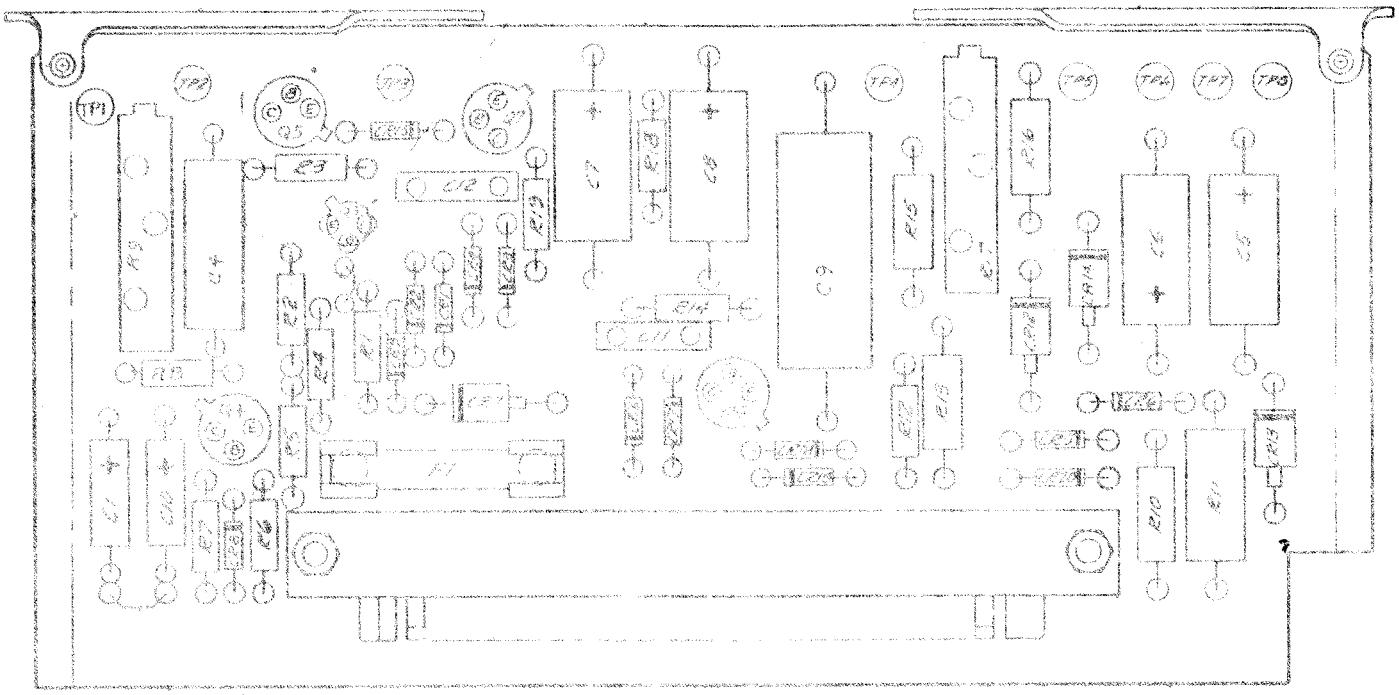
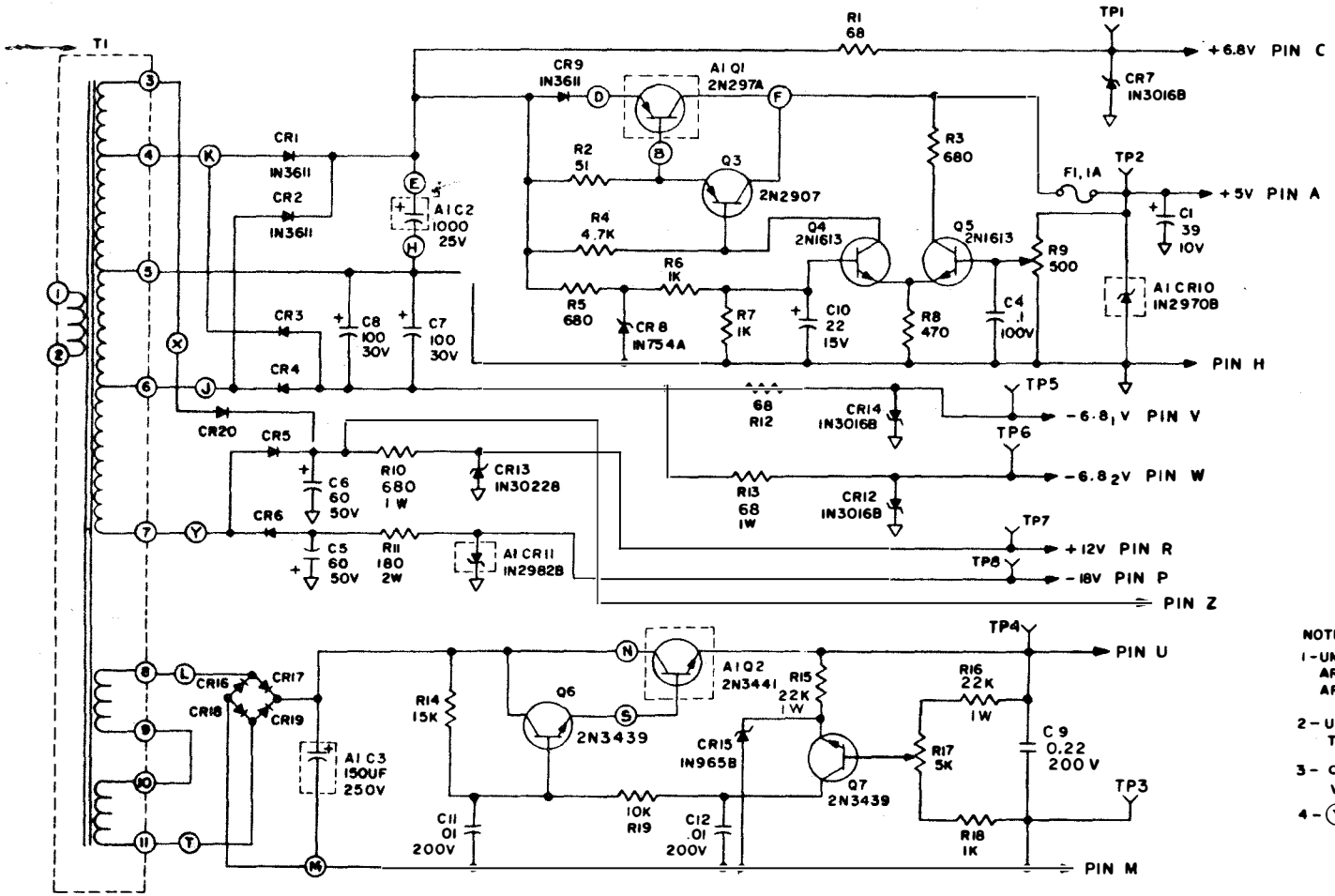


Figure 5-37. Power Supply Board 1A3 Component Location



NOTES:

1 - UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS 1/2W, 5 % TOL., CAPACITANCES ARE IN UF.

2 - UNLESS OTHERWISE SPECIFIED ALL DIODES ARE TYPE IN645.

3 - o—— DENOTES COMMON TIE POINT OR VOLTAGE BUS.

4 - (Y) DENOTES CONNECTOR PIN.

Figure 5-38. Power Supply Board 1A3 Schematic

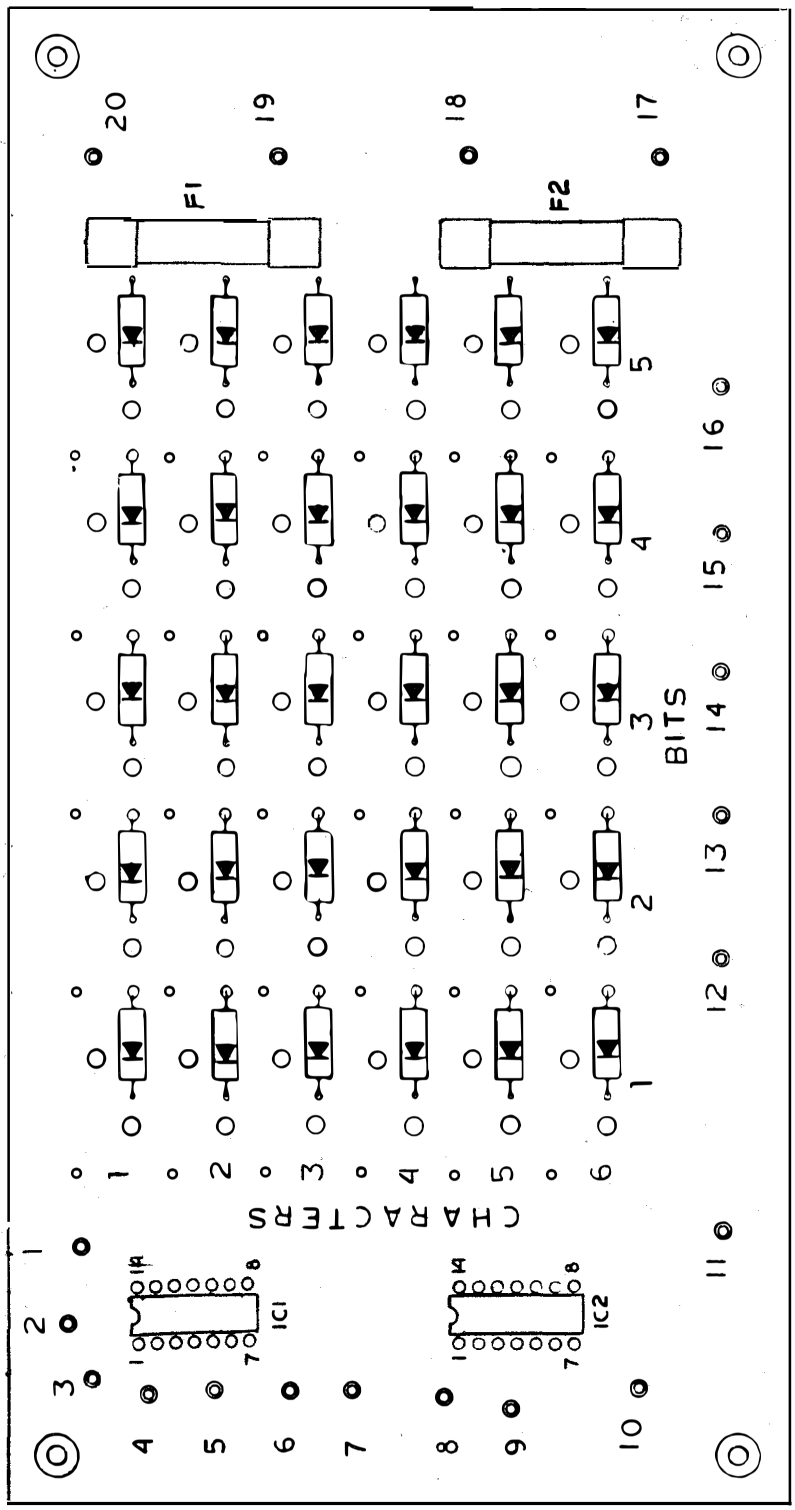


Figure 5-39. Word Matrix Board 1A2 Component Location

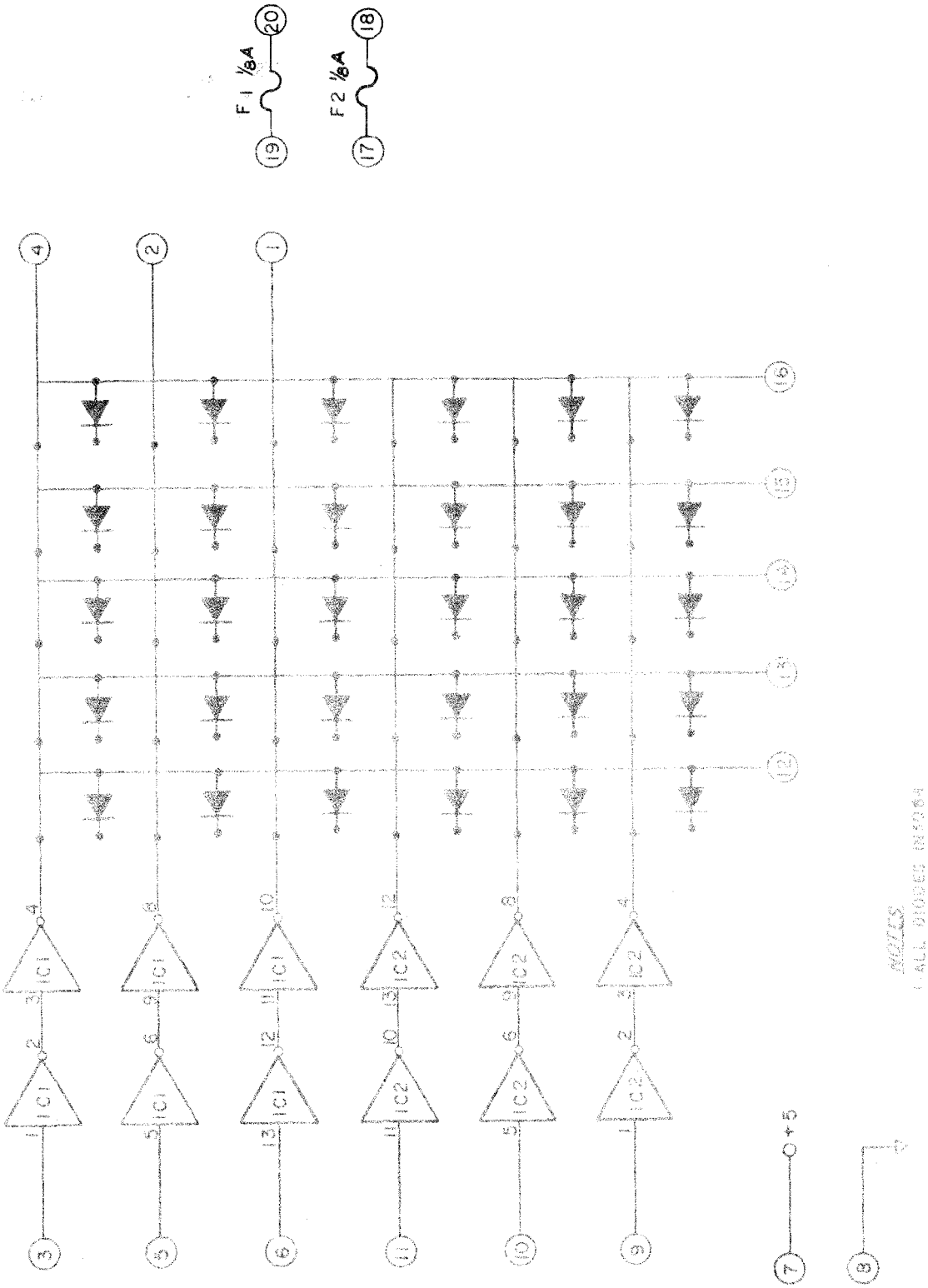


Figure 6-43. Word Matrix Board 1A2 Schematic

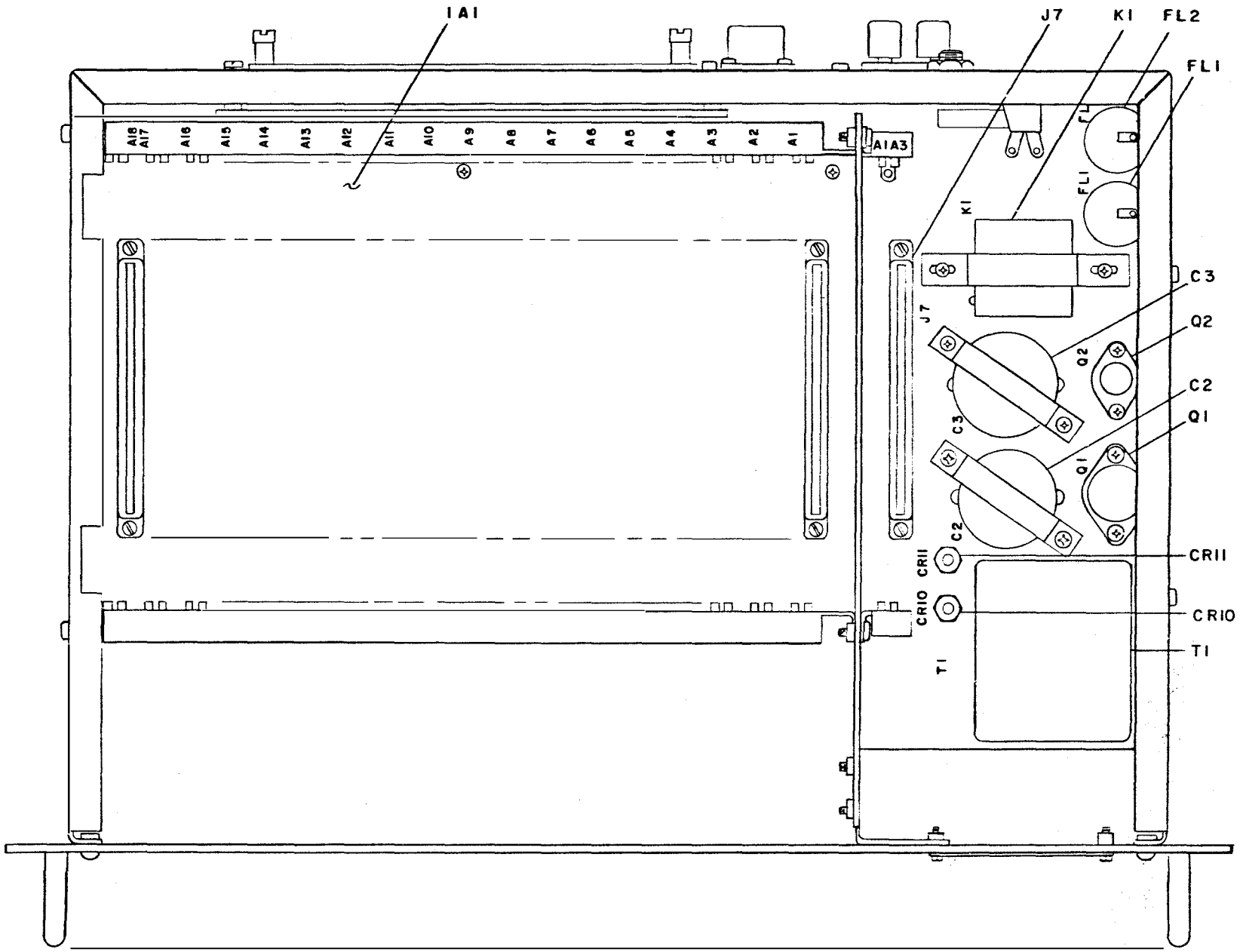


Figure 5-41. Chassis Mounted Components Location (Sheet 1 of 2)

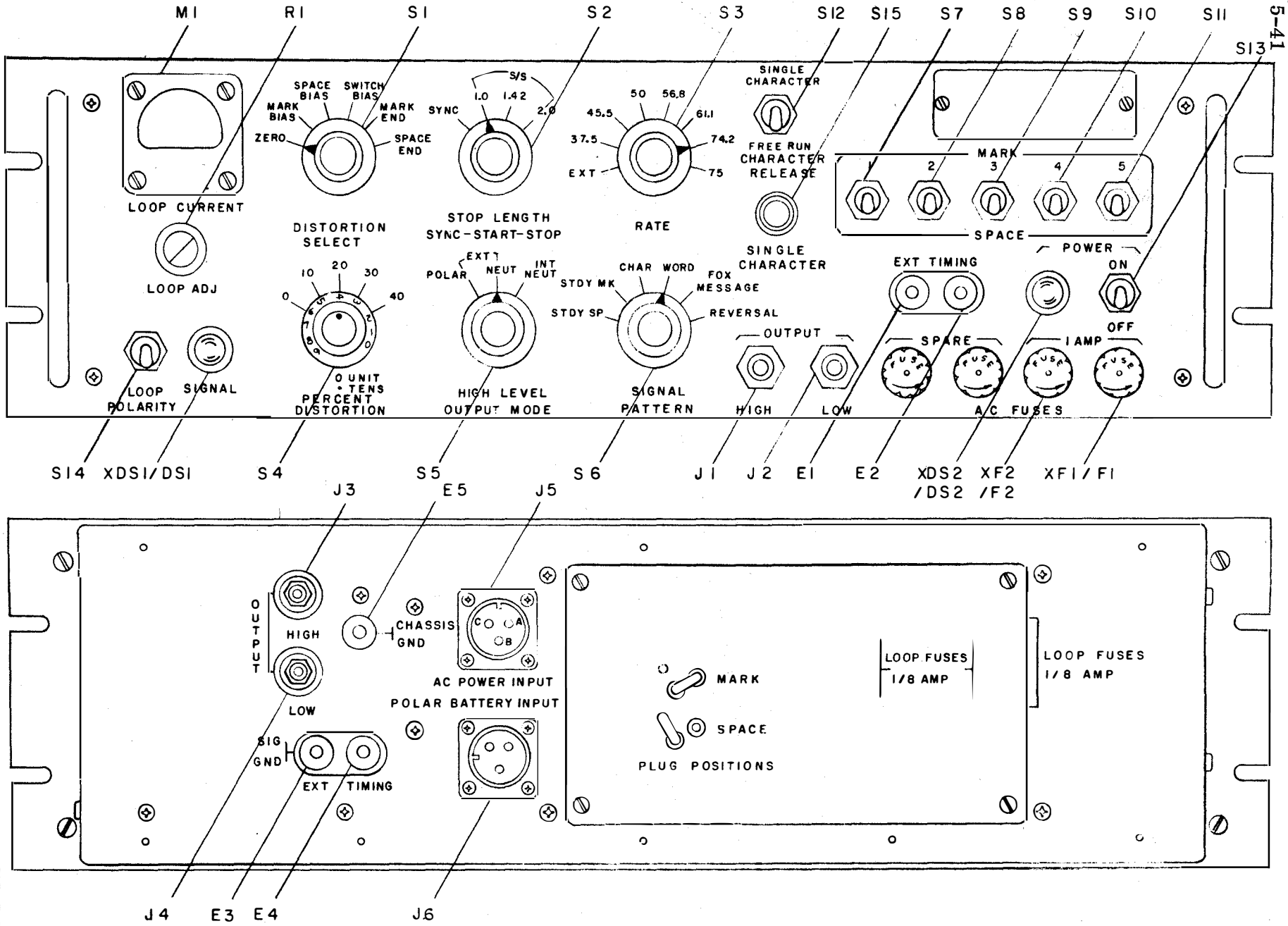


Figure 5-41. Chassis Mounted Components Location (Sheet 2 of 2)

TERM \ BOARD	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
2			A2-11 A3-12	A15-8	A4-12	A4-10	A5-18			A13-5	A10-9 A12-2 A13-2 A17-2	A10-9 A11-2 A13-2 A17-2	A10-9 A11-2 A12-2 A17-21	A12-20 A9-12 A9-3	E2 E4	K1-3	S6-4
3				S12-4 S2A-12		A10-4 A12-5		A15-20	A9-12 A12-20 A14-2	A10-6 A14-14 A15-21	S7	A10-10 A11-4 A13-3 A17-19	A10-10 A11-4 A17-19 A12-3	A10-12 A9-13 A4-20			S6-3 A11-20
4				A3-11	A6-12	A7-4	A6-4	A6-21	A12-21	A12-6 A6-3	A10-10 A12-3 A13-3 A17-19	A10-11 A11-6 A12-4 A17-13	A13-18 A9-5 A1A2	A12-16 A16-11 A19-21			
5				S3A-1	S4A-2	A7-9 A12-13	S4E-2	A7-17	A13-18 A14-4 A1A2-6	A7-11	S8	A10-4 A6-3	A10-2	A13-9 A1A2-7			A14-16 A9-22
6				A15-9	S4A-1	A7-14	S4E-1	A5-17		A10-3 A14-14 A15-21	A10-11 A12-4 A13-4 A17-13	A10-13 A11-9 A13-8 A17-18	S6-6 A10-21	A13-11 A1A2-3			
7	GND●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
8		S3A-7 A3-17		A6-8 A7-18	S4B-3	A4-8 A7-18	S4E-9	A7-20	A14-21	A6-13 A8-14	S9	A8-9 A9-14 A10-15 A11-11 A13-19 A17-15	A10-13 A11-9 A12-6 A17-18	A13-16 A14-11 A1A2-2	A4-2	K1-1	A1A2-14
9		A3-21		S12-5		A5-11	A6-5 A12-13	A17-15 A9-14 A10-15 A11-11 A12-8 A13-19	A12-22	A11-2 A12-2 A13-2 A17-21	A10-13 A12-6 A13-8 A17-18	A10-16 A11-13 A13-20	A14-5 A1A2-7	A13-14 A1A2-1	A4-6		A1A2-15
10				A6-2	A4-14 A6-16 A7-10	A5-12	A4-14 A5-10 A6-16	S2B-7	A17-11 A14-17	A11-4 A12-3 A13-3 A17-19	S-10	A11-17 A17-15 A13-21	A15-19 A11-21	A9-19	A1A3-2		A1A2-16

Figure 5-42. Interconnection Diagram (Sheet 1 of 3)

BOARD / TERM	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
11		A3-12 A3-2	A4-4	A6-15	A6-9	A5-14	A10-5	S1-1		A11-6 A12-4 A13-4 A17-13	A17-15 A8-9 A9-14 A10-15 A12-8 A13-19	A15-16	A14-6 A1A2-3	A13-16 A14-8 A1A2-2		A1A3-2 A15-4 A12-16	A9-10 A14-17
12			A2-11 A3-2	A5-2	A6-10	A5-4		A7-16	A9-23 A12-20 A14-2	A14-3 A9-13 A9-20	S11	A10-18 A11-17 A13-22	A14-19	A13-17 A1A2-8	A17-12		A15-12
13		A3-14 A2-16 A1-16		S2B-9	S4B-1	A8-14 A10-8	S4E-7	A5-16	A9-20 A10-12 A14-3	A11-9 A12-6 A13-8 A17-18	A10-16 A12-9 A13-20	A7-9 A6-5	S6-5 A9-18 A10-20 A14-20 A15-18	A12-18			A10-11 A11-6 A12-4 A13-4
14			A2-13 A2-16 A1-16	A5-10 A6-16 A7-10	A6-11	A4-21	A6-6	A6-13 A10-8	A17-15 A8-9 A10-15 A11-11 A12-8 A13-9			A19-10	A14-9 A1A2-1	A10-3 A10-6 A15-21			A1A2-11
15		S3A-6		S15-6	S4C-5	A4-11	S4F-5			A17-15 A12-8 A13-19 A8-9 A9-14 A11-11	A10-17 A12-10 A13-21	A9-16		A12-19	A4-18		A13-19 A8-9 A9-14 A10-15 A11-11 A12-8
16	A2-16 A2-13 A3-14	A2-13 A3-14 A1-16	S3B-8	S15-4 S12-1	A8-13	A7-10 A4-14 A6-16	A8-12	A4-20	A12-15	A11-13 A12-9 A13-20		A19-21 A15-4 A16-11	A14-8 A14-11 A1A2-8	A9-22 A17-5	A12-11		A1A2-13
17	S3A-5	S3A-3	A2-8 S3A-7		A8-6		A8-5	S1-5	A12-17	A11-15 A12-10 A13-21	A10-18 A12-12 A13-22	A9-17	A14-12 A1A2-8	A17-11 A9-10	A14-18	A8-20	A1A2-12
18		A3-18 S3A-2 S3A-8 CR-	A2-18 S3A-2 S3A-8 CR-	A15-13	A7-2	S2A-3	A4-8 A6-8	S1-6 S1-2	S6-5 A13-13 A10-20 A15-18 A14-20	A11-17 A12-12 A13-22		A14-13	A14-4 A9-5 A1A2-6	A15-17	S6-5 A14-20 A9-18 A13-13 A10-20	XDS1	A10-13 A11-9 A12-6 A13-8

Figure 5-42. Interconnection Diagram (Sheet 2 of 3)

BOARD / TERM	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
19			S3A-4 CR-		S4D-1	S2B-1	A5-7 (GND)	S1-7	A14-10		A17-4 A9-2	A14-15	A17-15 A8-9 A9-14 A10-15 A11-11 A12-8	A13-12	A13-10 A11-21		A10-10 A11-4 A12-3
20			S3B-2 To S3B-7	A8-16		S2B-2	A8-8	A16-17	A9-13 A10-12 A14-3	A14-20 A15-18 A9-18 A13-13 S6-5	S6-3 A17-3	A9-23 A9-12 A14-2	A10-16 A11-13 A12-9	S6-5 A15-18 A9-18 A13-13 A10-20	A8-3	A1A3-5	A1A2-10
21			A2-9	A6-14	S4D-6	A8-4		A4-22	A14-22	S6-6 A13-6	A13-10 A15-19	A9-4	A10-17 A11-15 A12-10	A9-8	A10-3 A10-6 A14-14	A1A3-20	A13-2 A10-9 A11-2 A12-2
22				A8-21	S4C-1	S2B-3 S2B-4	S4F-1	S1-11	A17-5 A14-16			A9-9	A12-12 A10-18 A17-17	A9-21	J2-3 J4-3		A1A2-9

Figure 5-42. Interconnection Diagram (Sheet 3 of 3)

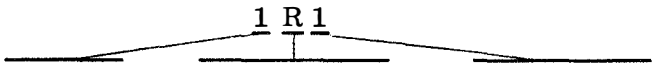
SECTION 6

PARTS LIST

6-1. INTRODUCTION

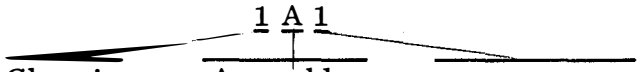
a. REFERENCE DESIGNATIONS. - A uniform identification method has been used to identify the chassis unit, assemblies and maintenance parts of the test set. This method adequately covers the equipment components. An example of this method is illustrated by the following:

Example 1:



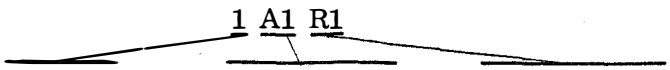
Read as: First (1) resistor (R) of chassis unit (1).

Example 2:



Read as: First (1) assembly (A) of chassis unit (1)

Example 3:



Read as: First (1) resistor (R) of first (1) assembly (A) of chassis unit (1)

6-2. LIST OF ASSEMBLIES

Tables 6-1 and 6-2 identify the assemblies contained in the signal generator.

6-3. MAINTENANCE PARTS

Table 6-2 lists the maintenance parts alphanumerically and contains the complete reference designation, reference to explanatory notes as required, name and description of the maintenance part together with a listing of the illustration which pictorally locates the part.

TABLE 6-1. LIST OF ASSEMBLIES

REF. DESIG.	TITLE	PART NUMBER	FIG. NO.	
			COMP LOC.	SCHEM
1	TEST SET	46016201	1-1	
1A1	CHASSIS	46016202	5-41	
1A1A1	HARNESS BOARD	36011030		
1A1A1A1	OSCILLATOR #1	36021010GR2	5-1	5-2
1A1A1A2	OSCILLATOR #2	36021010GR1	5-3	5-4
1A1A1A3	TIME BASE DIVIDER	36021020	5-5	5-6
1A1A1A4	TIMING CONTROL	36021030	5-7	5-8
1A1A1A5	BCD COUNTER AND TRIGGER I	36021040GP1	5-9	5-10
1A1A1A6	STOP MARK TRIGGER	36021060	5-11	5-12
1A1A1A7	BCD COUNTER AND TRIGGER II	36021040GP2	5-13	5-14
1A1A1A8	SIGNAL PROCESSOR	36021050	5-15	5-16
1A1A1A9	CHARACTER COUNTER II	36011070	5-17	5-18
1A1A1A10	BIT COUNTER AND GATES	36021070	5-19	5-20
1A1A1A11	SELECTED CHARACTER	36021110	5-21	5-22
1A1A1A12*	FOX MESSAGE	36021120	5-23	5-24
1A1A1A12-1*	FOX MESSAGE	36021220	5-25	5-26
1A1A1A12-2*	FOX MESSAGE	36021120-2	5-26A	5-26B
1A1A1A13	CALL LETTER MATRIX	36021130-1	5-27	5-28
1A1A1A14	CHARACTER COUNTER I	36021090	5-29	5-30
1A1A1A15	MESSAGE SELECT GATES	36011060	5-31	5-32
1A1A1A16	OUTPUT DRIVER	36011040	5-33	5-34
1A1A1A17	WORD MATRIX CONTROL AND CARRIAGE RETURN	36011020	5-35	5-36

*SEE PARAGRAPH 1-1c.

TABLE 6-1. LIST OF ASSEMBLIES (cont)

REF. DESIG.	TITLE	PART NUMBER	FIG. NO.	
			COMP LOC.	SCHEM
1A1A1A18	EXTENDER	36021160GR2		
1A1A2	WORD MATRIX	36011010	5-39	5-40
1A1A3	POWER SUPPLY	36011050	5-37	5-38

TABLE 6-2. MAINTENANCE PARTS LIST

FRONT PANEL AND CHASSIS ASSEMBLY, 1A1

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1	46016202	FRONT PANEL AND CHASSIS ASSEMBLY	24361	5-41
1A1A1	36011030	HARNESS BOARD	24361	
1A1A2	36011010	MATRIX BOARD	24361	
1A1A3	36011050	POWER SUPPLY	24361	
C1	CS13BF105K	CAPACITOR: 1 mfd, 35 vdc	81349	
C2	CE56C102F	CAPACITOR: 0.001 mfd	81349	
C3	CE56C151M	CAPACITOR: 150 mfd	81349	
CR1		NOT USED		
CR2		NOT USED		
CR3		NOT USED		
CR4		NOT USED		
CR5	1N3064	DIODE		
CR6	1N3064	DIODE		
CR7		NOT USED		
CR8		NOT USED		
CR9		NOT USED		
CR10	1N2970B	DIODE: Zener	81349	
CR11	1N2982B	DIODE: Zener	81349	
DS1	MS25237-327	LAMP: Clear No. 327	81349	
DS2	MS25237-327	SAME AS DS1		
E1	16018403	TERMINAL: Binding post, black	24361	
E2	16018412	TERMINAL: Binding post, red	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FRONT PANEL AND CHASSIS ASSEMBLY, 1A1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
E3		SAME AS E1		
E4		SAME AS E2		
E5		SAME AS E1		
FL1	FL24DD1EA3	FILTER: RF1	81349	
FL2		SAME AS FL1		
F1	F02A250V1AS	FUSE: lamp, 250v	81349	
F2		SAME AS F1		
J1	M641/16-1	JACK: Type JJ104	81349	
J2	M641/14-3	JACK: Telephone type JJ103	81349	
J3		SAME AS J2		
J4		SAME AS J2		
J5	MS3102A-14S-7PW	CONNECTOR: Receptacle, 7-pin	81349	
J6	MS3102A-14S-7P	CONNECTOR: Receptacle, 7-pin	81349	
J7	M21097/6-49	CONNECTOR: PC card	81349	
K1	36016204-1	RELAY: Electronic, Model 819A	24361	
M1	MR13W1H1DCMAR (Meter)	Meter: DC	81349	
Q1	2N297A	TRANSISTOR	81349	
Q2	2N3441	TRANSISTOR	81349	
R1	M22/03-002415D	RESISTOR: Variable, 5K	81349	
R2	RCR07G102JP	RESISTOR: Fixed, 1K, ±5%, 1/4 watt	81349	
R3	RCR20G221JP	RESISTOR: Fixed, 220, 1/2 watt	81349	
R4	RC32GF470J	RESISTOR: Fixed, 47, 1 watt	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FRONT PANEL AND CHASSIS ASSEMBLY, 1A1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
S1	16028418	SWITCH: Rotary, 6-position	24361	
S2	16018409	SWITCH: Rotary, 4-position	24361	
S3	16018420	SWITCH: Rotary, 8-position	24361	
S4	16018419	SWITCH: Rotary, 5-position	24361	
S5	16028414	SWITCH: Rotary, 3-position	24361	
S6		SAME AS S1		
S7	MS25098-22	SWITCH: Toggle SPDT	81349	
S8		SAME AS S7		
S9		SAME AS S7		
S10		SAME AS S7		
S11		SAME AS S7		
S12	MS25100-23	SWITCH: Toggle	81349	
S13	MS25100-22	SWITCH: Toggle	81349	
S14		SAME AS S12		
S15	M/8805/3-030	SWITCH: Pushbutton	81349	
T1	16028431	TRANSFORMER: Power	24361	
XC2	TS101P01	SOCKET: Octal (8-pin)	81349	
XC3		SAME AS XC2		
XDS1	LH73/1	SOCKET: Lamp	81349	
XDS2		SAME AS XDS1		
XF1	FHN20G	FUSEHOLDER	81349	
XF2		SAME AS XF1		
XK1		SAME AS XC2		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

HARNESS ASSEMBLY, 1A1A1

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1A1	36011030	CIRCUIT BOARD ASSEMBLY	24361	5-41
C1	CLR65BD470MP3	CAPACITOR: MIL type	81349	
C2		SAME AS C1		
C3	CK63AW103M	CAPACITOR: MIL type	81349	
CR1-4	1N3064	DIODE	81349	
CR7-9		SAME AS CR1		
CR12		SAME AS CR1		
J1	M21097/6-049	CONNECTOR: MIL type	81349	
J2		SAME AS J1		
J3		SAME AS J1		
J4		SAME AS J1		
J5		SAME AS J1		
J6		SAME AS J1		
J7		SAME AS J1		
J8		SAME AS J1		
J9		SAME AS J1		
J10		SAME AS J1		
J11		SAME AS J1		
J12		SAME AS J1		
J13		SAME AS J1		
J14		SAME AS J1		
J15		SAME AS J1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

HARNESS ASSEMBLY, 1A1A1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
J16		SAME AS J1		
J17		SAME AS J1		
J18		SAME AS J1		
L1	MS90537-49	INDUCTOR: MIL type	81349	
OSCILLATOR #1 ASSEMBLY, 1A1A1A1				
1A1A1A1	36021010-2	CIRCUIT BOARD ASSEMBLY	24361	5-1
C1		NOT USED		
C2		NOT USED		
C3		NOT USED		
C4	CM06FD102J03	CAPACITOR: Fxd, mica, 1000 uuf, ±5%, 500 vdc	81349	
C5	CM05ED470J03	CAPACITOR: Fxd, mica, 47 uuf, ±5%, 500 vdc	81349	
C6	CM05ED200J03	CAPACITOR: Fxd, mica, 20 uuf, ±5%, 500 vdc	81349	
C7	CM05FD221J03	CAPACITOR: Fxd, mica, 220 uuf, ±5%, 500 vdc	81349	
CR1		NOT USED		
CR2	1N3064	DIODE	81349	
IC1	16028403	INTEGRATED CIRCUIT	24361	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1		NOT USED		
Q2		NOT USED		
Q3		NOT USED		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OSCILLATOR #1 ASSEMBLY, 1A1A1A1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
Q4		NOT USED		
Q5	2N760A	TRANSISTOR	81349	
Q6	2N2907	TRANSISTOR	81349	
Q7		SAME AS Q5		
R1		NOT USED		
R2		NOT USED		
R3		NOT USED		
R4		NOT USED		
R5		NOT USED		
R6	RC07GF471J	RESISTOR: Fxd, comp, 470K, 1/4w, ±5%	81349	
R7	RC07GF564J	RESISTOR: Fxd, comp, 560K, 1/4w, ±5%	81349	
R8	RC07GF102J	RESISTOR: Fxd, comp, 1K, 1/4w, ±5%	81349	
R9	RC07GF823J	RESISTOR: Fxd, comp, 82K, 1/4w, ±5%	81349	
R10	RC07GF222J	RESISTOR: Fxd, comp, 2.2K, 1/4w, ±5%	81349	
R11		SAME AS R6		
R12		NOT USED		
R13		NOT USED		
R14	RC07GF103J	RESISTOR: Fxd, comp, 10K, 1/4w, ±5%	81349	
R15		NOT USED		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OSCILLATOR #1 ASSEMBLY, 1A1A1A1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R16		NOT USED		
R17		NOT USED		
R18		NOT USED		
R19		SAME AS R6		
Y1		NOT USED		
Y2	16028406-6	CRYSTAL: Quartz (181.856KC)	24361	
OSCILLATOR #2 ASSEMBLY, 1A1A1A2				
1A1A1A2	36021010-1	CIRCUIT BOARD ASSEMBLY	24361	5-3
C1	CM05FD101J03	CAPACITOR: Fxd, mica, 100 uuf, ±5%, 500 vdc	81349	
C2	CM05ED470J03	CAPACITOR: Fxd, mica, 47 uuf, ±5%, 500 vdc	81349	
C3	CM06FD102J03	CAPACITOR: Fxd, mica, 1000 uuf, ±5%, 500 vdc	81349	
C4		SAME AS C3		
C5		SAME AS C2		
C6	CM05ED200J03	CAPACITOR: Fxd, mica, 200 uuf, ±5%, 500 vdc	81349	
C7	CM05FD221J03	CAPACITOR: Fxd, mica, 220 uuf, ±5%, 500 vdc	81349	
C8		SAME AS C3		
C9		SAME AS C2		
C10		SAME AS C3		
C11		SAME AS C2		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OSCILLATOR #2 ASSEMBLY, 1A1A1A2 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
C12		SAME AS C6		
C13		SAME AS C7		
C14		SAME AS C6		
C15		SAME AS C7		
C16		NOT USED		
C17		NOT USED		
C18		NOT USED		
C19		NOT USED		
C20		SAME AS C6		
C21		SAME AS C6		
CR1	1N3064	DIODE	81349	
CR2		SAME AS CR1		
CR3		SAME AS CR1		
CR4		SAME AS CR1		
IC1	16028403	INTEGRATED CIRCUIT	24361	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1	2N760A	TRANSISTOR NpN	81349	
Q2	2N2907	TRANSISTOR PNP	81349	
Q3		SAME AS Q1		
Q4		SAME AS Q1		
Q5		SAME AS Q1		
Q6		SAME AS Q2		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OSCILLATOR #2 ASSEMBLY, 1A1A1A2 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
Q7		SAME AS Q1		
Q8		SAME AS Q1		
Q9		SAME AS Q2		
Q10		SAME AS Q1		
Q11		SAME AS Q1		
Q12		SAME AS Q2		
Q13		SAME AS Q1		
R1	RC07GF564J	RESISTOR: Fxd, comp, 560K, 1/4w, ±5%	81349	
R2	RC07GF102J	RESISTOR: Fxd, comp, 1K, 1/4w, ±5%	81349	
R3	RC07GF823J	RESISTOR: Fxd, comp, 82K, 1/4w, ±5%	81349	
R4	RC07GF222J	RESISTOR: Fxd, comp, 2.2K, 1/4w, ±5%	81349	
R5	RC07GF472J	RESISTOR: Fxd, comp, 4.7K, 1/4w, ±5%	81349	
R6	RC07GF471J	RESISTOR: Fxd, comp, 470, 1/4w, ±5%	81349	
R7		SAME AS R1		
R8		SAME AS R2		
R9		SAME AS R3		
R10		SAME AS R4		
R11		SAME AS R6		
R12	RC07GF103J	RESISTOR: Fxd, comp, 10K, 1/4w, ±5%	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OSCILLATOR #2 ASSEMBLY, 1A1A1A2 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R13		SAME AS R12		
R14		SAME AS R12		
R15		SAME AS R1		
R16		SAME AS R2		
R17		SAME AS R3		
R18		SAME AS R4		
R19		SAME AS R6		
R20		SAME AS R1		
R21		SAME AS R2		
R22		SAME AS R3		
R23		SAME AS R4		
R24		SAME AS R6		
R25		SAME AS R12		
R26		SAME AS R12		
R27	RC07GF152J	RESISTOR: Fxd, comp, 1.5K, 1/4w, ±5%	81349	
Y1	16028405-1	CRYSTAL: Quartz	24361	
Y2	16028406-3	CRYSTAL: Quartz	24361	
Y3	16028406-8	CRYSTAL: Quartz	24361	
Y4	16028406-1	CRYSTAL: Quartz	24361	
TIME BASE DIVIDER ASSEMBLY, 1A1A1A3				
1A1A1A3	36021020	CIRCUIT BOARD ASSEMBLY	24361	5-5
IC1	16028423	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

TIME BASE DIVIDER ASSEMBLY, 1A1A1A3 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC2		SAME AS IC1		
IC3		SAME AS IC1		
IC4		SAME AS IC1		
IC5	16028402	INTEGRATED CIRCUIT	24361	
IC6	16028403	INTEGRATED CIRCUIT	24361	
IC7		SAME AS IC6		
IC8		SAME AS IC6		
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
R5		SAME AS R1		
R6		SAME AS R1		
R7		SAME AS R1		
R8		SAME AS R1		
R9		SAME AS R1		
R10		SAME AS R1		
R11		SAME AS R1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
TIMING CONTROL ASSEMBLY, 1A1A1A4				
1A1A1A4	36021030	CIRCUIT BOARD ASSEMBLY	24361	5-7
C1	CM05ED470J03	CAPACITOR: MIL type	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

TIMING CONTROL ASSEMBLY, 1A1A1A4 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
C2	CM05ED101J03	CAPACITOR: MIL type	81349	
IC1	16028410	INTEGRATED CIRCUIT	24361	
IC2	16028423	INTEGRATED CIRCUIT	24361	
IC3		SAME AS IC2		
IC4		SAME AS IC2		
IC5		SAME AS IC1		
IC6	16028403	INTEGRATED CIRCUIT	24361	
IC7	16028409	INTEGRATED CIRCUIT	24361	
IC8		SAME AS IC6		
IC9	16028402	INTEGRATED CIRCUIT	24361	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
R5		SAME AS R1		
R6		SAME AS R1		
BCD COUNTER AND TRIGGER I ASSEMBLY, 1A1A1A5				
1A1A1A5	36021040GP1	CIRCUIT BOARD ASSEMBLY	24361	5-9
C1	CM05FD101J03	CAPACITOR: MIL type	81349	
IC1	16028403	INTEGRATED CIRCUIT	24361	
IC2	16028423	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

BCD COUNTER AND TRIGGER I ASSEMBLY, 1A1A1A5 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC3		SAME AS IC2		
IC4	16028401	INTEGRATED CIRCUIT	24361	
IC5	16028404	INTEGRATED CIRCUIT	24361	
IC6		SAME AS IC1		
IC7		SAME AS IC1		
IC8		SAME AS IC1		
IC9		SAME AS IC1		
R1	RC07GF682J	RESISTOR: 6.8K	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
R5		SAME AS R1		
R6		SAME AS R1		
R7		SAME AS R1		
R8		SAME AS R1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
STOP MARK TRIGGER ASSEMBLY, 1A1A1A6				
1A1A1A6	36021060	CIRCUIT BOARD ASSEMBLY	24361	5-11
CR1	1N3064	DIODE	81349	
CR2		SAME AS CR1		
IC1	16028403	INTEGRATED CIRCUIT	24361	
IC2	16028404	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

STOP MARK TRIGGER ASSEMBLY, 1A1A1A6 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC3	16028402	INTEGRATED CIRCUIT	24361	
IC4	16028423	INTEGRATED CIRCUIT	24361	
IC5	16028401	INTEGRATED CIRCUIT	24361	
IC6	16028410	INTEGRATED CIRCUIT	24361	
IC7		SAME AS IC1		
R1	RC07GF471F	RESISTOR: 470 ohms	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
R5		SAME AS R1		
R6		SAME AS R1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
BCD COUNTER AND TRIGGER II, 1A1A1A7				
1A1A1A7	36021040GP2	CIRCUIT BOARD ASSEMBLY	24361	5-13
C1	CM05FD101J03	CAPACITOR, Fxd, mica, 100 pf, ±5%, 500 v	81349	
IC1	16028403	INTEGRATED CIRCUIT	24361	
IC2	16028423	INTEGRATED CIRCUIT	24361	
IC3		SAME AS IC2		
IC4	16028401	INTEGRATED CIRCUIT	24361	
IC5	16028404	INTEGRATED CIRCUIT	24361	
IC6		SAME AS IC1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

BCD COUNTER AND TRIGGER II, 1A1A1A7 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC7		SAME AS IC1		
IC8		SAME AS IC1		
IC9		SAME AS IC1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
R1	RC07GF682J	RESISTOR: Fxd, comp, 6800 1/4w, ±5%	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
R5		SAME AS R1		
R6		SAME AS R1		
R7		SAME AS R1		
R8		SAME AS R1		
SIGNAL PROCESSOR ASSEMBLY, 1A1A1A8				
1A1A1A8	36021050	CIRCUIT BOARD ASSEMBLY	24361	5-15
C1	CM05FD111J03	CAPACITOR: MIL type	81349	
C2		SAME AS C1		
CR1	1N3064	SEMICONDUCTOR DEVICE: MIL type	81349	
CR2		SAME AS CR1		
CR3	1N277	DIODE	81349	
CR4		SAME AS CR3		
IC1	16028402	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

SIGNAL PROCESSOR ASSEMBLY, 1A1A1A8 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC2	16028404	INTEGRATED CIRCUIT	24361	
IC3	16028403	INTEGRATED CIRCUIT	24361	
IC4	16028423	INTEGRATED CIRCUIT	24361	
IC5	16028409	INTEGRATED CIRCUIT	24361	
IC6	16028410	INTEGRATED CIRCUIT	24361	
IC7		SAME AS IC2		
IC8	16028401	INTEGRATED CIRCUIT	24361	
IC9		SAME AS IC3		
R1	RC07GF682J	RESISTOR: 6.8K	81349	
R2		SAME AS R1		
R3	RC07GF471J	RESISTOR: 470 ohms	81349	
R4		SAME AS R3		
R5		SAME AS R3		
R6		SAME AS R3		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
	COUNTER II ASSEMBLY, 1A1A1A9			
1A1A1A9	36011070	CIRCUIT BOARD ASSEMBLY	24361	5-17
IC1	16028401	INTEGRATED CIRCUIT	24361	
IC2		SAME AS IC1		
IC3	16028403	INTEGRATED CIRCUIT	24361	
IC4		SAME AS IC3		
IC5	16028423	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

COUNTER II ASSEMBLY, 1A1A1A9 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC6		SAME AS IC5		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
R1	RC07GF471J	RESISTOR: Fxd, comp, 470 ohms	81349	
BIT COUNTER AND GATES ASSEMBLY, 1A1A1A10				
1A1A1A10	36021070	CIRCUIT BOARD ASSEMBLY	24361	5-19
IC1	16028423	INTEGRATED CIRCUIT	24361	
IC2	16028401	INTEGRATED CIRCUIT	24361	
IC3		SAME AS IC2		
IC4		SAME AS IC2		
IC5		SAME AS IC2		
IC6		SAME AS IC2		
IC7		SAME AS IC1		
IC8	16028404	INTEGRATED CIRCUIT	24361	
IC9		SAME AS IC8		
IC10	16028403	INTEGRATED CIRCUIT	24361	
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
R2		SAME AS R1		
R3		SAME AS R1		
R4		SAME AS R1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

SELECTED CHARACTER ASSEMBLY, 1A1A1A11

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1A1A11	36021110	CIRCUIT BOARD ASSEMBLY	24361	5-21
IC1	16028403	INTEGRATED CIRCUIT	24361	
IC2		SAME AS IC1		
IC3	16028401	INTEGRATED CIRCUIT	24361	
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
R2	RC07GF682J	RESISTOR: 6.8K ohms	81349	
R3		SAME AS R2		
R4		SAME AS R2		
R5		SAME AS R2		
R6		SAME AS R2		
R7		SAME AS R2		
R8		SAME AS R2		
R9		SAME AS R2		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
FOX MESSAGE ASSEMBLY, 1A1A1A12				
1A1A1A12	36021120	CIRCUIT BOARD ASSEMBLY	24361	5-23
C1	CM05FD301J03	CAPACITOR: MIL type	81349	
C2	CM05FD111J03	CAPACITOR: MIL type	81349	
CR1	1N645	DIODE	81349	
IC1	16028430	INTEGRATED CIRCUIT	24361	
IC2	16028410	INTEGRATED CIRCUIT	24361	
IC3	16028403	INTEGRATED CIRCUIT	24361	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
IC4		SAME AS IC3		
IC5		SAME AS IC3		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1	2N2907	TRANSISTOR: MIL type	81349	
Q2		SAME AS Q1		
Q3		SAME AS Q1		
Q4		SAME AS Q1		
Q5		SAME AS Q1		
Q6		SAME AS Q1		
Q7		SAME AS Q1		
Q8		SAME AS Q1		
Q9	2N1613	TRANSISTOR: MIL type	81349	
Q10		SAME AS Q1		
R1	RC07GF202J	RESISTOR: 2K	81349	
R2	RC07GF562J	RESISTOR: 5.6K	81349	
R3		SAME AS R1		
R4		SAME AS R2		
R5		SAME AS R1		
R6		SAME AS R2		
R7		SAME AS R1		
R8		SAME AS R2		
R9		SAME AS R1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R10		SAME AS R2		
R11		SAME AS R1		
R12		SAME AS R2		
R13		SAME AS R1		
R14		SAME AS R2		
R15		SAME AS R1		
R16		SAME AS R2		
R17		SAME AS R2		
R18		SAME AS R2		
R19		SAME AS R2		
R20		SAME AS R2		
R21		SAME AS R2		
R22		SAME AS R2		
R23		SAME AS R2		
R24		SAME AS R2		
R25	RC07GF511J	RESISTOR: 510 ohms	81349	
R26	RC07GF472J	RESISTOR: 4700 ohms	81349	
R27		SAME AS R1		
R28		SAME AS R2		
R29	RC07GF102J	RESISTOR: 1000 ohms	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12-1

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1A1A12-1	36021220	CIRCUIT BOARD ASSEMBLY	24361	5-25
C1	CM05FD301J03	CAPACITOR: MIL type	81349	
C2	CM05FD111J03	CAPACITOR: MIL type	81349	
C3	CM05FD201J03	CAPACITOR: MIL type	81349	
C4	CM05ED470J03	CAPACITOR: MIL type	81349	
C5	CM06FD202J03	CAPACITOR: MIL type	81349	
CR1	1N645	DIODE	81349	
IC1	16028430	INTEGRATED CIRCUIT	24361	
IC2	16028410	INTEGRATED CIRCUIT	24361	
IC3	16028403	INTEGRATED CIRCUIT	24361	
IC4		SAME AS IC3		
IC5	16028425	INTEGRATED CIRCUIT	24361	
IC6		SAME AS IC2		
IC7		SAME AS IC2		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1	2N2907	TRANSISTOR: MIL type	81349	
Q2-Q8		SAME AS Q1		
Q9		SAME AS Q1		
R1	RC07GF202J	RESISTOR: 2K		
R2	RC07GF562J	RESISTOR: 5.6K		
R3		SAME AS R1		
R4		SAME AS R2		
R5		SAME AS R1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12-1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R6		SAME AS R2		
R7		SAME AS R1		
R8		SAME AS R2		
R9		SAME AS R1		
R10		SAME AS R2		
R11		SAME AS R1		
R12		SAME AS R2		
R13		SAME AS R1		
R14		SAME AS R2		
R15		SAME AS R1		
R16		SAME AS R2		
R17		SAME AS R2		
R18		SAME AS R2		
R19		SAME AS R2		
R20		SAME AS R2		
R21		SAME AS R2		
R22		SAME AS R2		
R23		SAME AS R2		
R24		SAME AS R2		
R25	RC07GF511J	RESISTOR: 510 ohms	81349	
R26	RC07GF472J	RESISTOR: 4.7K	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12-1 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R27		SAME AS R1		
R28		SAME AS R2		
R29	RC07GF102J	RESISTOR: 1K	81349	
FOX MESSAGE ASSEMBLY, 1A1A1A12-2				
1A1A1A12-2	36021120-2	CIRCUIT BOARD ASSEMBLY	24361	5-26A
CR1-CR5	1N4148	DIODE: MIL type	81349	
IC1	16028438	INTEGRATED CIRCUIT	24361	
IC2	16028403	INTEGRATED CIRCUIT	24361	
IC3		SAME AS IC2		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1-Q7	2N2907	TRANSISTOR: MIL type	81349	
R1	RC07GF202J	RESISTOR: 2000 ohms	81349	
R2	RC07GF562J	RESISTOR: 5.6K ohms	81349	
R3		SAME AS R1		
R4		SAME AS R2		
R5		SAME AS R1		
R6		SAME AS R2		
R7		SAME AS R1		
R8		SAME AS R2		
R9		SAME AS R1		
R10		SAME AS R2		
R11		SAME AS R1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

FOX MESSAGE ASSEMBLY, 1A1A1A12-2 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R12		SAME AS R2		
R13		SAME AS R1		
R14		SAME AS R2		
R15		SAME AS R2		
R16		SAME AS R2		
R17		SAME AS R2		
R18		SAME AS R2		
R19		SAME AS R2		
R20		SAME AS R2		
R21		SAME AS R2		
R22	RC07GF123J	RESISTOR: 12K ohms	81349	
R23		SAME AS R22		
R24		SAME AS R22		
R25		SAME AS R22		
R26		SAME AS R22		
CALL LETTER MATRIX ASSEMBLY, 1A1A1A13				
1A1A1A13	36021130-1	CIRCUIT BOARD ASSEMBLY	24361	5-27
CR1	1N3064	DIODE: MIL type	81349	
CR2		SAME AS CR1		
CR3		SAME AS CR1		
CR4		SAME AS CR1		
CR5		SAME AS CR1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

CALL LETTER MATRIX ASSEMBLY, 1A1A1A13 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
CR6		SAME AS CR1		
CR7		SAME AS CR1		
CR8		SAME AS CR1		
CR9		SAME AS CR1		
CR10		SAME AS CR1		
CR11		SAME AS CR1		
CR12		SAME AS CR1		
CR13		SAME AS CR1		
CR14		SAME AS CR1		
CR15		SAME AS CR1		
CR16		SAME AS CR1		
CR17		SAME AS CR1		
CR18		SAME AS CR1		
CR19		SAME AS CR1		
CR20		SAME AS CR1		
CR21		SAME AS CR1		
CR22		SAME AS CR1		
CR23		SAME AS CR1		
CR24		SAME AS CR1		
CR25		SAME AS CR1		
CR26		SAME AS CR1		
CR27		SAME AS CR1		
CR28		SAME AS CR1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

CALL LETTER MATRIX ASSEMBLY, 1A1A1A13 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
CR29		SAME AS CR1		
CR30		SAME AS CR1		
IC1	16028403	INTEGRATED CIRCUIT	24361	
IC2	16028401	INTEGRATED CIRCUIT	24361	
IC3		SAME AS IC1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
CHARACTER COUNTER-I ASSEMBLY, 1A1A1A14				
1A1A1A14	36021090	CIRCUIT BOARD ASSEMBLY	24361	5-29
IC1	16028401	INTEGRATED CIRCUIT	24361	
IC2		SAME AS IC1		
IC3	16028423	INTEGRATED CIRCUIT	24361	
IC4		SAME AS IC3		
IC5	16028403	INTEGRATED CIRCUIT	24361	
IC6	16028402	INTEGRATED CIRCUIT	24361	
IC7		SAME AS IC1		
IC8		SAME AS IC6		
IC9	16028404	INTEGRATED CIRCUIT	24361	
IC10		SAME AS IC1		
R1	RC07GF471J	RESISTOR: 470 ohms	81349	
R2		SAME AS R1		
P1	M21097/7-038	CONNECTOR: MIL type	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

MESSAGE SELECT GAGES ASSEMBLY, 1A1A1A15

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1A1A15	36011060	CIRCUIT BOARD ASSEMBLY	24361	5-31
IC1	16028413	INTEGRATED CIRCUIT	24361	
IC2	16028401	INTEGRATED CIRCUIT	24361	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
R1	RC07GF103J	RESISTOR: Fxd, comp; 10K	81349	
R2	RC07GF203J	RESISTOR: Fxd, comp, 20K	81349	
R3		SAME AS R2		
R4	RC07GF471J	RESISTOR: Fxd, comp, 470 ohms	81349	
OUTPUT DRIVER ASSEMBLY, 1A1A1A16				
1A1A1A16	36011040	CIRCUIT BOARD ASSEMBLY	24361	5-33
CR1	1N3064	DIODE	81349	
CR2		SAME AS CR1		
CR3		SAME AS CR1		
CR4		SAME AS CR1		
CR5		SAME AS CR1		
C1	CM05FD391J03	CAPACITOR: MIL type	81349	
Q1	2N2907	TRANSISTOR	81349	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q2	2N760A	TRANSISTOR	81349	
Q3	2N1613	TRANSISTOR	81349	
Q4		SAME AS Q2		
Q5		SAME AS Q1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OUTPUT DRIVER ASSEMBLY, 1A1A1A16 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION.	MFR CODE	FIG. NO.
Q6		SAME AS Q2		
Q7		SAME AS Q1		
Q8		SAME AS Q3		
Q9		SAME AS Q1		
Q10		SAME AS Q2		
Q11	2N2905	TRANSISTOR	81349	
R1	RC07GF153J	RESISTOR: Fxd, 15K, 1/4w, ±5%	81349	
R2	RC07GF302J	RESISTOR: Fxd, 3K, 1/4w, ±5%	81349	
R3	RC07GF272J	RESISTOR: Fxd, 2.7K, 1/4w, ±5%	81349	
R4	RC07GF472J	RESISTOR: Fxd, 4.7K, 1/4w, ±5%	81349	
R5	RC07GF102J	RESISTOR: Fxd, 1K, 1/4w, ±5%	81349	
R6		SAME AS R4		
R7		SAME AS R4		
R8	RC07GF103J	RESISTOR: Fxd, 10K, 1/4w, ±5%	81349	
R9		SAME AS R5		
R10	RC07GF682J	RESISTOR: Fxd, 6.8K, 1/4w, ±5%	81349	
R11	RC20GF103J	RESISTOR: Fxd, 10K, 1/2w, ±5%	81349	
R12	RC32GF470J	RESISTOR: Fxd, 47, 1w, ±5%	81349	
R13		SAME AS R12		
R14		SAME AS R10		
R15		SAME AS R5		
R16	RC07GF101J	RESISTOR: Fxd, 100 ohms, 1/4w, ±5%	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

OUTPUT DRIVER ASSEMBLY, 1A1A1A16 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R17		SAME AS R5		
R18		SAME AS R3		
R19	RC07GF154J	RESISTOR: Fxd, 150K, 1/4w, ±5%	81349	
R20		SAME AS R10		
R21	RC07GF513J	RESISTOR: Fxd, 51K, 1/4w, ±5%	81349	
R22		SAME AS R5		
R23		SAME AS R4		
R24		SAME AS R10		
R25		SAME AS R19		
R26		SAME AS R4		
WORD MATRIX CONTROL AND CARRIAGE RETURN ASSEMBLY, 1A1A1A17				
1A1A1A17	36011020	CIRCUIT BOARD ASSEMBLY	24361	5-35
CR1	1N3064	DIODE	81349	
CR2		SAME AS CR1		
CR3		SAME AS CR1		
CR4		SAME AS CR1		
CR5		SAME AS CR1		
IC1	16028401	INTEGRATED CIRCUIT	24361	
IC2	16028404	INTEGRATED CIRCUIT	24361	
IC3	16028403	INTEGRATED CIRCUIT	24361	
IC4		SAME AS IC3		
P1	M21097/7-038	CONNECTOR: MIL type	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

WORD MATRIX CONTROL AND CARRIAGE RETURN ASSEMBLY, 1A1A1A17 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R1	RC07GF471J	RESISTOR: Fxd, 470, 1/4w, ±5%	81349	
R2		SAME AS R1		
R3		SAME AS R1		
EXTENDER BOARD ASSEMBLY, 1A1A1A18				
1A1A1A18	36021160-2	CIRCUIT BOARD ASSEMBLY	24361	
J1	M21097/6-049	CONNECTOR: MIL type	81349	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
WORD MATRIX ASSEMBLY, 1A1A2				
1A1A2	36011010	CIRCUIT BOARD ASSEMBLY	24361	5-39
CR1	1N3064	DIODE	81349	
CR2		SAME AS CR1		
CR3		SAME AS CR1		
CR4		SAME AS CR1		
CR5		SAME AS CR1		
CR6		SAME AS CR1		
CR7		SAME AS CR1		
CR8		SAME AS CR1		
CR9		SAME AS CR1		
CR10		SAME AS CR1		
CR11		SAME AS CR1		
CR12		SAME AS CR1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

WORD MATRIX ASSEMBLY, 1A1A2 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
CR13		SAME AS CR1		
CR14		SAME AS CR1		
CR15		SAME AS CR1		
CR16		SAME AS CR1		
CR17		SAME AS CR1		
CR18		SAME AS CR1		
CR19		SAME AS CR1		
CR20		SAME AS CR1		
CR21		SAME AS CR1		
CR22		SAME AS CR1		
CR23		SAME AS CR1		
CR24		SAME AS CR1		
CR25		SAME AS CR1		
CR26		SAME AS CR1		
CR27		SAME AS CR1		
CR28		SAME AS CR1		
CR29		SAME AS CR1		
CR30		SAME AS CR1		
F1	F02A250V1/8AS	FUSES: 1/8 A 250 v	81349	
F2		SAME AS F1		
IC1	16028404	INTEGRATED CIRCUIT	24361	
IC2		SAME AS IC1		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

POWER SUPPLY ASSEMBLY, 1A1A3

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
1A1A3	36011050	CIRCUIT BOARD ASSEMBLY	24361	5-37
C1	CS13BC396K	CAPACITOR: Tantalum, 39MFD, 10v	81349	
C2		NOT USED		
C3		NOT USED		
C4	CP05A1KB104K3	CAPACITOR: Fxd, Paper 0.1 MFD, 100v	81349	
C5	CLR65BJ600MP3	CAPACITOR: Fxd, electrolitic, 60 MFD 50v	81349	
C6		SAME AS C5		
C7	CLR65BH101MP3	CAPACITOR: Fxd, electrolitic, 100 MFD, 30v	81349	
C8		SAME AS C7		
C9	CP09A1KC224K3	CAPACITOR: Fxd, paper, .22 MFD, 200v		
C10	CS13BD226K	CAPACITOR: Fxd, tantalum, 22 MFD, 15v	81349	
C11	CK63AW103MP3	CAPACITOR: Fxd, ceramic, .01 MFD 200v	81349	
C12		SAME AS C11		
CR1	1N3611	DIODE	81349	
CR2		SAME AS CR1		
CR3	1N645	DIODE	81349	
CR4		SAME AS CR3		
CR5		SAME AS CR3		
CR6		SAME AS CR3		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

POWER SUPPLY ASSEMBLY, 1A1A3 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
CR7	1N3016B	DIODE	81349	
CR8	1N754A	DIODE	81349	
CR9		SAME AS CR1		
CR10		NOT USED		
CR11		NOT USED		
CR12		SAME AS CR7		
CR13	1N3022B	DIODE	81349	
CR14		SAME AS CR7		
CR15	1N965B	DIODE	81349	
CR16		SAME AS CR3		
CR17		SAME AS CR3		
CR18		SAME AS CR3		
CR19		SAME AS CR3		
CR20		SAME AS CR3		
F1	F02A250V1AS	FUSE: Lamp, 250v	81349	
P1	M21097/7-038	CONNECTOR: MIL type	81349	
Q1		NOT USED		
Q2		NOT USED		
Q3	2N2907	TRANSISTOR	81349	
Q4	2N1613	TRANSISTOR	81349	
Q5		SAME AS Q4		
Q6	2N3439	TRANSISTOR	81349	
Q7		SAME AS Q6		

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

POWER SUPPLY ASSEMBLY, 1A1A3 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R1	RC20GF680J	RESISTOR: Fxd, comp, 68 ohms, 1/2w, ±5%	81349	
R2	RC20GF510J	RESISTOR: Fxd, comp, 51 ohms, 1/2w, ±5%	81349	
R3	RC20GF681J	RESISTOR: Fxd, comp, 680 ohms, 1/2w, ±5%	81349	
R4	RC20GF472J	RESISTOR: Fxd, comp, 4.7K, 1/2w, ±5%	81349	
R5		SAME AS R3		
R6	RC20GF102J	RESISTOR: Fxd, comp, 1K, 1/2w, ±5%	81349	
R7		SAME AS R6		
R8	RC20GF471J	RESISTOR: Fxd, comp, 470 ohms, 1/2w, ±5%	81349	
R9	RJ11CP501	RESISTOR: Var., 500 ohms	81349	
R10	RC32GF681J	RESISTOR: Fxd, comp, 680 ohms, 1w, ±5%	81349	
R11	RC42GF181J	RESISTOR: Fxd, comp, 180 ohms, 2w, ±5%	81349	
R12		SAME AS R1		
R13	RC32GF680J	RESISTOR: Fxd, comp, 68 ohms 1w, ±5%	81349	
R14	RC20GF153J	RESISTOR: Fxd, comp, 15K, 1/2 w, ±5%	81349	
R15	RC32GF223J	RESISTOR: Fxd, comp, 22K, 1w, ±5%	81349	
R16		SAME AS R15		
R17	RJ11CP502	RESISTOR: Var, 5K	81349	

TABLE 6-2. MAINTENANCE PARTS LIST (cont)

POWER SUPPLY ASSEMBLY, 1A1A3 (cont)

REF DESIG	PART NUMBER	NAME AND DESCRIPTION	MFR CODE	FIG. NO.
R18		SAME AS R6		
R19	RC20GF103J	RESISTOR: Fxd, comp, 10K, 1/2 w, ±5%	81349	

TABLE 6-3. LIST OF MANUFACTURERS

MFR CODE	NAME	ADDRESS
24361	T M Systems, Inc.	25 Allen Street Bridgeport, Conn. 06604
81349	Military Specification	

USER ACTIVITY TECHNICAL MANUAL COMMENT SHEET
NAVSHIPS 5600/2(REV.9/67)
(Formerly NAVSHIPS 4914)

NAVSHIPS _____
VOLUME NO. _____

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