DATASPEED TAPE TO TAPE SYSTEM

TYPE 1 AND TYPE 2 TAPE SENDERS AND RECEIVERS

ELECTRONIC CIRCUITRY

GENERAL DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS PAGE

1. INTRODUCTION

1.01 This section presents both a general and detailed description of the electronic circuitry (with the exception of the power supply modules) used in the DATASPEED 1A and 2A Tape Senders and 1B and 2B Tape Receivers. Refer to related sections for information regarding the power supply module, and the electromechanical units, (ie, tape reader and tape punch) used in the Tape Sender and Tape Receivers.

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1.02 The circuit description within this section, assumes that the Tape Sender and/or Tape Receiver are operated with a Bell System type 202A data set. Provisions have been made for mounting these data sets directly within the Tape Sender or Tape Receiver cabinet.

1.03 The information appearing in this section was formerly included in circuit descriptions CD3831WD, CD3833WD, CD4439WD, and CD4441WD as part of the Bell System Practice entitled "DATASPEED Tape-to-Tape System, Electronic Circuitry, Schematic Wiring Diagrams and Circuit Board Drawings." The wiring diagrams (WD) and etched card (EC) drawings referenced in this section can be found in the appropriate Bell System Practice in the 592 Division of the Plant Series.

2. GENERAL DESCRIPTION

TAPE SENDER

2.01 The Tape Sender converts the parallel output signals generated by the tape reader into a serial, start-stop signal for driving the modulator contained in the data set. A block diagram of a complete Tape Sender terminal is shown in the top half of Figure 1. The electronic components required to convert the parallel output signals from the reader into serial, start-stop form are a sending signal converter and a sending distributor. The signal converter and the sending distributor are each housed in separate electronic modular assemblies.

TAPE RECEIVER

2.02 The Tape Receiver converts the start-stop serial code from the data set to a parallel signal which will operate the tape reperforator. A block diagram of a complete Tape Receiver terminal is shown in the bottom half of Figure 1. The electronic components required to convert the start-stop serial code into parallel form are a receiving signal converter and a receiving distributor. The receiving distributor and the signal converter are each separately housed in electronic modular assemblies.

ELECTRONIC MODULES

2.03 The modules which house the electronics associated with the Tape Senders and Receivers are designed to provide easy access to the circuitry. They are of steel frame construction, and are 5-1/2 inches by 7 inches by 15 inches in dimension.

2.04 The electronic circuitry is contained on plug-in etched circuit cards. Each circuit card is equipped with accessible test points for voltmeter and oscilloscope checking. The modules are equipped with 15-pin connectors to accept each circuit card. Each connector is interconnected by surface wiring. All circuit components are contained on the pluggable circuit cards. All signal connectors and power supply connections are made through a connector mounted on the rear of each module.

TABLE 1 - MAXIMUM DC CURRENT DRAIN

Nominal Voltage	Sending Distributor (TTD)	Sending Signal Converter (TTSC)	Tape Sender Total Drain	Receiving Distributor (TRD)	Receiving Signal Converter (TRSC)	Tape Receiver Total Drain
+6	-	37MA	37MA	-	75MA	75MA
+1.5	131MA	4MA	135MA	130MA	135MA	265MA
-6	-	-	-	-	200MA	200MA
-6R	-21MA	-6MA	27MA	-25MA	-30MA	55MA
-12	170MA	51MA	221MA	230MA	240MA	470MA
-28	-	1900MA	1900MA	-	2200MA	2200MA

TABLE 2 - SIGNAL CHARACTERISTICS

Unit	Type	Code Levels	Baud	WPM
Sending Distributor	1 2	5 5 to 8	1050 1050	1050 1050
Sending Signal Converter	1 2	5 5 to 8	1050 1050	1050 1050
Tape Reader	1 2	5 5 to 8	1050 1050	1050 1050
Receiving Distributor	1 2	5 5 to 8	1050 1050	1050 1050
Receiving Signal Converter	1 2	5 5 to 8	1050 1050	1050 1050
Tape Reperforator	1 2	5 5 to 8	1050 1050	1050 1050

POWER AND SIGNAL REQUIREMENTS

A. Power Requirements

2.05 Power required for the above units is obtained from the power supply mounted in the lower enclosure of each terminal (multi-voltage rectifier (TP-177149). Voltage and current requirements are listed in Table 1.

(a) AC power - 115 V AC ±10 V AC 60 cycles.
250 watts (nominal max) Sender
300 watts (nominal max) Receiver

(b) DC power - see Table 1.

B. Output Signal Requirements - Tape Sender

2.06 The Tape Sender terminal output signal has the following characteristics:

(1) Start-stop type polar signal.

(2) Nominal output signal voltage across a load of 1,000 ohms.

(a) Space: +6 volts

(b) Mark: -6 volts

(3) Unit codes, code levels, baud (bits-per-second), and wpm (words-per-minute) are listed in Table 2.

C. Input Signal Requirements - Tape Receiver

2.07 The Tape Receiver terminal is designed to operate from an input signal with the following characteristics:

(1) Start-stop polar signal.

(2) Nominal input signal voltage from a 1,000-ohm source:

(a) Space: +3V or more positive (+25V maximum).

(b) Mark: -3V or more negative (-25V maximum).

(3) Unit codes, code levels, baud (bits per second), and wpm (words per minute) are listed in Table 2 above.

3. TAPE SENDER - PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape sender terminal block diagram, Figure 2.

General

3.01 Electronic circuitry of Tape Sender terminal is physically and functionally divided into two parts: a sending signal converter and a sending distributor. The signal converter is represented by schematic diagram 3831WD and the sending distributor by 4439WD. All circuits are shown in symbolic logic. Each circuit is indicated by an EC number, an etched circuit board number, and a Z number which represents an element number. A detailed description of each circuit board can be obtained by referring to the respective part drawing. For information concerning power supply used with the above equipment, refer to appropriate 592 Division section.

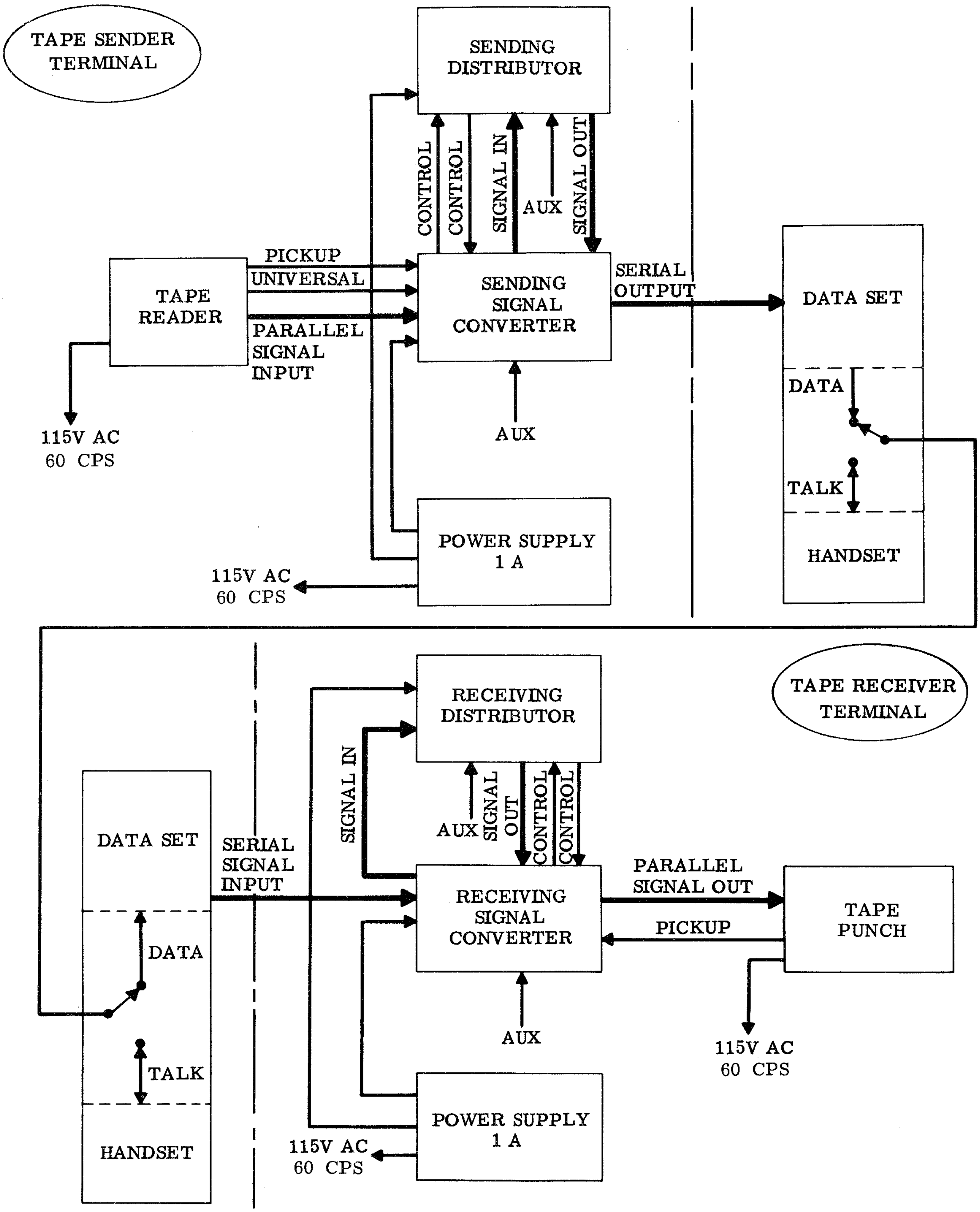


Figure 1-System Block Diagram

3.02 The function of the signal converter is to receive N-level parallel signals from the high speed tape reader, and convert the input to N standard output pulses (N refers to the number of code levels used. Type 1 units utilize 5 level code, while Type 2 (universal) units may utilize 5 to 8 level code, depending upon selective conditions). The signal converter also converts the standard output of a sending distributor to signals suitable for driving the modulator of a data set.

3.03 The function of the sending distributor is to convert N parallel input pulses to an N-level binary start-stop code. The Type 3 distributor contains 6 register elements and generates a 10-bit (1050 baud) code. The zero (0) level bit (which is the first bit after the start bit signal) is always transmitted as a mark. Bit levels 1 through 5 are used to transmit the serial information. After level 5 has been transmitted, a 3 bit stop pulse will follow where normally levels 6 and 7 along with the unity stop pulse bit are transmitted. The Type 2 distributor contains 8 register elements, and will accept up to 8 information pulses. If level zero (0) is not used, it will be transmitted as a space pulse. If levels 6 and 7 are not used, each will be transmitted as a mark pulse along with the unity stop pulse.

Operation

3.04 The heart of the circuit operation is the signal register in the sending distributor. This group of circuit elements, commonly known as a shift register, is arranged so that each element of the register accepts one code information bit at the same time the respective level in the tape is sensed by the tape reader. This information is accepted in parallel form. Since only one bit can be transmitted at a time, the information is then shifted out of the register, each bit in succession, until all the bits have been transmitted. This occurs during the time the tape is being advanced to the next character. Before the next character is read, the register is reset to accept the new information.

3.05 The basic block diagram, Figure 2, is arranged to illustrate the functions of the various sections of the tape sender terminal. Note that there are two sources of timing in this unit. One timing signal is developed in a magnetic pickup on the tape reader, and is used to initiate the stop pulse for each character. This pulse, then, occurs at the character rate. The other timing signal operates at the bit rate and is used to advance the code in the shift register. This timing signal is generated by the start-stop oscillator (see Figure 2). During the stop interval, the start-stop oscillator is stopped, and is then restarted at the beginning of the next start pulse. This assures that the deviation in the bit rate will not be cumulative and that the first code bit will always occur at the proper instant with regard to the machine character rate.

B. Signal Converter (Sending)

3.06 The signal converter contains the signal inhibit gate, pickup pulse amplifier, and output signal amplifier.

3.07 The pickup pulse amplifier shapes and amplifies the magnetic pickup output, and sends it to the signal delay in the sending distributor.

3.08 The inhibit gates transmit the signal from the reader contacts to the signal register in the sending distributor.

3.09 The output amplifier converts the signal from the sending distributor to a signal having the characteristics necessary to drive the data set.

C. Sending Distributor

3.10 When the unit is initially turned on, a reset pulse is automatically generated to reset the output element of the signal register. The start-stop oscillator (advance pulse generator) is controlled by a bi-stable circuit called the oscillator control. The stop condition is initiated by the timing signal from the magnetic pickup. The timing signal is applied to the stop timer, a mono-stable device which develops a signal approximately equal in duration to the desired stop pulse. This signal is then applied to the start pulse gate through the start amplifier. If the gate is open, it will pass the trailing edge of the stop pulse (beginning of start) to the oscillator start lead of the oscillator control to provide the start condition. The start pulse gate is under the control of the universal contact in the tape reader. This contact closes for every character position on the tape as it is being pulled through the reader. Thus, if tape is being read, the oscillator will start; but if tape is not being read, the gate will remain closed, the oscillator will not start, and the unit will generate a continuous stop signal.

3.11 The sample delay circuit, which is also triggered at the end of the stop pulse, develops a pulse to control the inhibit gates in the signal converter, and to control the pulse control gate. This control pulse is delayed approximately one-half a bit, since the signal register must have time to generate a start signal before the new character code is set into it. When this set "1" pulse is applied to the inhibit gates, the information from the reader contacts is supplied through the gates to set the elements of the signal register to record the code. When the contact is closed, it represents a MARK condition (a hole in the tape) and the corresponding shift register element is set to the "1" condition. If it is SPACE (no hole in tape) the register element remains in the "0" condition. When the sample delay is applied to the pulse control gate, it enables the set "0" side, providing a set "0" pulse for the signal registers, and inhibits the "advance pulses" side to prevent a false signal from being sent on the line. Upon relaxing, the set "0" is inhibited and the "advance pulse" side is enabled so information can be shifted through the register.

3.12 The last element of the signal register (labeled R on the block diagram, Figure 2) does not receive a code pulse. At the end of the previous character, this element was left in the "1" condition as will be shown below. When the set "0" pulse arrives, the R element will be shifted to the "0" condition, causing a space to be generated representing the start pulse. Immediately following this, the information is set into the register. The next advance pulse shifts this entire code one element to the right, bringing the first bit of the code from element 1 to element R. This produces an output signal corresponding to the first bit. With the next advance pulse, the code is advanced another position to the right so that now the second bit is in element R, producing an output signal which represents that bit. This action continues until all bits have been advanced out of the register, each bit producing its output signal in turn.

3.13 Element R is continuously primed in such a way that it will be shifted to the "1" state by the first advance pulse following reset, and will remain that way until the next set "0" pulse. This condition is transferred down the shift register, causing each element to go to the "1" state as the last code bit is shifted out of it. Thus, the stop pulse is generated in element R when the last bit is shifted out of it, since it will be set to the "1" state. It will remain in this state until the next set "0" pulse causes it to shift to SPACE to create the start pulse of the next character. If no code is to be transmitted, due to no tape in the reader or the reader having been stopped, advance pulses would not be generated since no start pulse would be received by the oscillator control (universal contact open). Thus, element R would remain in the "1" state generating a continuous mark or stop signal until the code transmission is resumed.

DETAILED CIRCUIT DESCRIPTION

A. Signal Converter (Sending)

Note: Refer to schematic wiring diagram 3831WD.

Initial Conditions

3.14 The first action which takes place in the signal converter is automatic reset. This occurs when the power switch is turned on. At this time -6 volts is applied to terminal H of the integrator pulse shaper, Z210. This circuit, after a delay of about 300 milliseconds, provides a negative-going pulse on terminal K. The pulse is applied to the input terminal D, of the pulse amplifier circuit, Z211B. The pulse amplifier produces a positive-going -6 volts to 0 volt pulse and sends it to terminal C6 of connector J201. From terminal C6, the signal is sent to the reset of the output element of the signal register.

3.15 The timing signal from the magnetic pickup of the reader is applied to terminal C1 of connector J201 and from there to terminal A of Z209A. The lead on terminal B1 of J201 applies a -6 volt bias to the pickup coil and the pickup amplifier. The timing signal leaves terminal L of the pickup amplifier, and is inverted by Z209B. The output of Z209B is sent to the sending distributor through terminal C2 of connector J201.

Reader Input

3.16 The tape reader-mark contacts are connected to integrators Z201A-E through Z202A-D. The integrators are used to clean up any noise which may be caused by the mechanical switching of the tape reader contacts. The outputs of the integrators are applied to the prime input of inhibit gates Z203 through Z206, and a sample pulse is sent from the sending distributor via connector J101, terminal F2, to the drive side of the inhibit gates. At this time, all inhibit gates which are primed by the integrators pass a positive-going -6 volts to 0 volt pulse to OR gates Z207A-D through Z208A-D, and from them via J201 to the sending distributor. The function of the OR gate is described in Paragraph 3.35.

Universal Input

3.17 The universal signal from the reader is applied to terminal E of the integrator, Z202D, through connector J201, terminal H9. The output, terminal P of Z202D, appears on terminal C4 of J201. Subsequently, this signal is applied to the sending distributor.

Polar Signal Output

3.18 The parallel input signal is transferred from the signal converter to the sending distributor, and the serial output signal from the distributor is applied to the data set 202A. It is necessary, therefore, to convert the dc neutral signal from the sending distributor to a polar signal capable of driving the data set. This signal conversion is accomplished by an amplifier, Z212A. The signal from the sending distributor is applied to terminal C10, connector J201; from there it goes to terminal B of Z211A, an inverter. The signal output of the inverter is applied to terminal F of output amplifier Z212A, which converts the signal to a +6 volts and -6 volts polar signal. The output of the amplifier terminal P, is sent to the data set through terminal D10, connector J201.

Request-to Send

3.19 The data set requires a signal to inform it that the sending distributor is ready to send. This signal is called the Request-to-Send. The signal is provided by applying some bias through element Z212B to an external switch (i.e., reader motor switch). When the switch is open, -12 volts is applied to the data set via terminals E1 and D1 of J201. The Request-to-Send is off in the above condition. When the external switch is closed, +6 volts appears on the Request-to-Send lead; this is the on condition. On High Speed Tape-to-Tape System units, the data set Request-to-Send lead is permanently biased on with +17.5 volts.

Power Requirements

3.20 Power is applied through connector J201 to the module from the dc power supply. Minus 6 volts is found on terminal A4, +1.5 volts on terminal B8, -12 volts on terminal B7, and +6 volts on terminal B3. From these points the voltages are passed through filter elements Z213A-B through Z214A-B, which filter out extraneous noise. Terminal B4 has -28 volts; terminal B6 is circuit ground and terminal B5 is frame ground.

B. Sending Distributor

Note: Refer to schematic wiring diagram 4439WD, and timing diagram, Figure 3.

Initial Conditions

3.21 The first action to occur in the sending distributor is automatic reset. When the power switch is put in the ON position, a -6 volt to 0 volt pulse is generated in the signal converter (see Paragraph 3.14) and applied to terminal C6, connector J101. This pulse is presented to the set "1A" input of the output element, Z110, terminal C, in the signal register switching the normal output, terminal L, to 0 volt. This places a stop signal on the line, keeping it closed.

Clock Pulse

3.22 While the reader motor is running, a clock pulse, shaped in the signal converter, is applied through terminal C2, connector J101, to the signal delay input. The signal delay output, which is identical to its input only delayed about 50 microseconds, is applied to the stop timer's set "1" input and the oscillator control's set "0A" input. The clock pulse applied to terminal D of Z104, the oscillator control, switches the normal output, terminal L, to -6 volts to turn off the start-stop oscillator, Z108. The clock pulse is also applied to the set "1" input of the stop timer, Z101, terminal C, causing the output, terminal L, to go from -6 volts to 0 volts and remain at that potential for a period of time a little less than a bit in length.

Stop Timer

3.23 When the Z101 one-shot times out, its normal output will relax and produce a negative transition from 0 to -6 volts. This negative transition is applied to terminal B of start amplifier Z102A, a pulse amplifier, which generates a positive-going -6 volt to 0 volt pulse on its output, terminal K.

Oscillator Control

3.24 The positive pulse from Z102A is applied to the inhibit gate, Z103B, terminal N. If there is no tape in the reader, the universal contact will be open and zero volt appears on terminal D of inhibit gate Z103B. If a tape is in the sensing head and the reader is operating, the universal contact is closed and a -6 volt or greater signal is sent from the signal converter to connector J101, terminal C4, and from there to terminal D of the inhibit gate. The presence of this signal on terminal D permits the positive signal applied on terminal N to pass through the inhibit gate and on to the oscillator control flip-flop.

3.25 The oscillator control flip-flop, Z104, receives the positive-going pulse on terminal C. The pulse causes the circuit to switch and the normal output, terminal L, goes to 0 volts. This signal is now applied to the sample delay circuit, Z105, and the start-stop oscillator, Z108.

Sample Delay

3.26 The positive-going signal from the oscillator control, Z104, is received on the set "1" input, terminal C, of the sample delay, Z105. This one-shot serves two functions: (1) it provides the initial signal for the sample lead, and (2) it provides one pulse for the signal register reset. The sample delay one-shot goes negative on its inverted output, terminal K, and positive on its normal output, terminal L. The negative transition primes the set "0" side of the pulse control gate, Z106A, terminal B and permits the first pulse from the squaring amplifier to pass through this gate to set "0" all the signal registers (Z110 through Z115, Z116, Z117, or Z118 depending on number of levels). When the sample delay one-shot, Z105, relaxes, its inverted output goes to 0 volts and removes the prime from the set "0" side of the pulse control gate, Z106A. Simultaneously, the normal output of Z105 goes to -6 volts and primes the advance pulse side of the pulse control gate, Z106B, terminal D, allowing pulses from the squaring amplifier to pass through. The negative transition from the normal output is also sent to the input of the set "1" amplifier, Z102B, terminal D.

Start-Stop Oscillator

3.27 The start-stop oscillator, Z108, receives a -6 volts to 0 volt signal from the oscillator control flip-flop as described in Paragraph 3.25. The oscillator begins to oscillate as soon as the 0 volt signal is applied to its input terminal. The output appears as sinusoidal oscillations on terminal A, and is sent to the input of the squaring amplifier, Z109, terminal H. The squaring amplifier shapes the sine-wave in such a way as to produce a positive going -6 volts to 0 volt transition every cycle. Thus, one pulse is produced in every period of the sine-wave cycle. The time interval between the clock pulses and the frequency of the start-stop oscillator will permit only N+2 pulses on terminal A of Z109.

Squaring Amplifier

3.28 The pulses from the squaring amplifier are applied to the pulse control gate, Z106A and Z106B, on terminal A and terminal N, respectively. The sample delay one-shot primes terminal B of the pulse control gate long enough to permit the first pulse from the squaring amplifier to pass through to terminal K. This positive-going pulse is applied to the set "0A" input, terminal D, of the signal register, and resets all the registers to the set "0" condition prior to their receiving information from the signal converter.

Pulse Control Gate

3.29 The positive signal from the sample delay closes the advance pulses side of the pulse control gate, terminal D, Z106B, long enough to prevent the first pulse from the squaring amplifier from passing through the gate. The N+1 remaining pulses are passed through the gate's output, terminal L, and on to the set "1B" and set "0B" inputs on all the signal registers and the output element (terminals E and F, Z110 to Z118).

3.30 The negative-going signal which occurs when the sample delay one-shot, Z105, relaxes appears on terminal L. This signal is applied to terminal D of pulse amplifier Z102B, which generates a positive-going pulse, -6 volts to 0 volt, on its output at terminal L. The pulse is sent to terminal B of emitter follower Z103A. The output of Z103A is wired to connector J101, terminal C3, and is designated as the sample lead. The positive-going pulse on the sample lead is sent to the signal converter to trigger the inhibit gates passing the reader information into the signal register elements (refer to Paragraph 3.16).

Sample Pulse

3.31 When the sample pulse is sent from the set "1" amplifier (Z102B and Z103A) in the sending distributor to the inhibit gates in the signal converter, any inhibit gate which has a MARK condition on its input (-6 volts on terminal B or D) will pass a positive-going pulse to the sending distributor via connector J101, terminals D2 through D9, and from there to the storage registers set "1A" input, terminal C or Z111 through Z115, Z116, Z117, or Z118 (depending on number of code levels). Thus, if a

MARK condition appears in the reader, the corresponding signal register flip-flop switches to a set "1" condition (terminal L of flip-flops at 0 volts).

Signal Register

3.32 For purposes of description, assume that a MARK input is appearing only in the 4th level. Thus, only the flip-flop, Z114, will go into the set "1" condition; in this condition, its normal output, terminal L, will be at 0 volt and its inverted output, terminal K, will be at -6 volts. The normal output is wired to the prime "1B" input of the 3rd level flip-flop, Z113, terminal J, and the inverted output is wired to the prime "0B" input of Z113, terminal H. In this particular example, the 3rd level flip-flop will have its prime "1B" input primed, and when the 1st advance pulse arrives at the set "1B" input, terminal E, this flip-flop switches from the set "0" state to the set "1" state.

3.33 When the MARK pulse is passed from the 4th level to the 3rd level (that is, from Z114 to Z113), the 2nd level prime "1B" terminal is primed and the prime "0B" terminal remains at -6 volts. Thus, when the second advance pulse arrives at terminals E and F of Z112, and as each advance pulse comes in, this MARK signal is passed from the 3rd element to the 2nd element and so on until the N+1 advance pulse arrives. At this time the MARK signal is transferred into the output element of the register and then to the data set. Emitter follower Z107, passes the output signal from element Z110 to terminal C10 of connector J101.

C. Auxiliary Connections

3.34 All auxiliary connections, needed to operate in conjunction with supplementary equipment, are available at connector J202 of the singal converter.

3.35 Additional levels 0 through 7 are available, (terminals F3, F4, F5, F6, F7, F8, F9, and G2) to permit insertion of additional characters in the signal registers through OR gates Z207A to D through Z208A to D.

3.36 The sample lead is connected to terminal F2 of connector J201, and is used to let the auxiliary equipment know that the information has been passed into the signal registers.

3.37 Terminals G3, G4, and G5 on J201 in the signal converter are used to provide -28 volts, signal ground, and frame ground connections.

3.38 A start lead is connected to terminal C5, J101 in the sending distributor. This lead is wired to the output of the start amplifier, Z102A, terminal K, and will permit the auxiliary equipment to use the clock pulse as described in Paragraph 3.15.

3.39 The oscillator control is connected to terminal C1 of connector J101 in the sending distributor. This lead is wired to the set "1B" input of the oscillator control flip-flop, terminal E, Z104. It provides a means for equipment to turn on the oscillator.

4. TAPE RECEIVER - PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape receiver terminal block diagram, Figure 4.

General

4.01 The electronic circuitry of the Tape Receiver terminal is physically and functionally divided into two parts: a receiving signal converter and a receiving distributor. The signal converter is represented by schematic 3833WD, and the receiving distributor by 4441WD. All circuits are shown in symbolic logic. Each circuit is indicated by an EC number, an etched circuit board number, and a Z number which represents an element number. A detailed description of each circuit can be obtained by referring to the respective drawing. For information concerning the power supply used with the above equipment refer to the appropriate 592 Division section.

4.02 The function of the receiving distributor is to separate the N-bit serial input telegraph code into an N-level parallel binary output signal (N refers to the number of code levels used). The function of the receiving signal converter is to provide buffer storage and change the N-level parallel electrical pulses into an N-level driving signal for the tape reperforator. Type 1 units utilize 5-level code, while Type 2 (universal) units may utilize 5 to 8 level code depending upon selective conditions.

Operation

4.03 Like the Tape Sender terminal (Paragraph 3.04), the operation of the Receiving terminal centers around the signal register. In the receiving terminal, however, the code is advanced into the register as it arrives, and then is shifted out of each element simultaneously to a storage register as shown in the block diagram, Figure 4. The code remains in the storage register until the punch is ready to operate, and is then transferred into magnet pulsers which cause the proper punch position to be energized.

4.04 Since the operation of this system depends upon synchronizing mechanical motion of the punch at the Receiving terminal with the motion of the tape reader at the Tape Sender terminal, the control functions at the receiver are considerably more complex than at the transmitter. So that there will always be a new character position available on the tape, the tape punch is made to run slightly faster than the tape reader. In this way, a character will never be lost for want of a place in which to punch it.

4.05 The major control function in the receiving distributor is accomplished by the control register. In Figure 4, the output lead of the control register has been labeled control bus to show its importance in the operation of this equipment. The control register is responsible for the following:

(a) Starting and stopping the sensing operation of the signal register.

(b) Shifting the code from the signal register to storage in the signal converter.

(c) Priming the storage register to allow transfer of the code to the magnet pulsers.

4.06 The basic operation of the receiving distributor and the receiving signal converter can be best understood by following the sequence of events which occurs as a code group for a character arrives. The following conditions exist prior to receiving the character.

(a) Signal register: Set "1"

(b) Advance pulse generator: Off

(c) Control register: Set "0"

(d) Signal gate: Open

(e) Transfer prime: Set "1"

(f) Storage register: Storing last character

(g) Input gate: Open

(h) Start OR gate: Closed

(i) Start AND gate: Open

4.07 Two distinct timing operations occur in the Receiver terminal. These are related to the basic operating actions (ie, code punching and code registering), and occur throughout the same interval.

B. Signal Converter (Receiving)

4.08 The first operation to be considered is the punching process. The above list of conditions (Paragraph 4.06) following the reception of the last complete character, shows that the character is stored in the storage register. A timing pulse generated in the magnetic pickup on the punch is converted to a pulse by the pickup pulse amplifier and presented to the variable delay circuit. The variable delay acts like a one-shot whose delay time changes as a function of the transfer prime's condition. Since the transfer one-shot is primed by the transfer prime, the trigger pulse will be passed through the transfer pulse generator to operate the magnet pulsers. The magnet pulsers are so arranged that the feed magnet is energized together with the code magnets that are primed from the code in the storage register. Thus, holes are punched in the tape representing the code stored in the storage register.

4.09 The punching operation must take place within the character interval following the shifting of code into the storage register. Thus, the punch period must be less than this time (about 95 to 98 per cent of the character interval).

C. Receiving Distributor

4.10 During the waiting period for the punching to take place, a new code group may be forming in the signal register. This action, that is code registering, will be considered next. An input signal applied to the signal gate, finding the gate open, passes through this gate and actuates the register drive circuit. The register drive circuit reshapes the input signal so that the transitions between bits displays the rapid rise time desired, and corrects for some of the deterioration of the signal that may have occured along the line. The output of the register drive is applied to the signal register, where it is advanced into the register one bit at a time under the control of the advance pulses.

4.11 The start-stop oscillator is turned off between code groups and must, therefore, be turned on again before the signal can be registered. The start-stop oscillator determines the bit rate. Since this is one of the circuits controlled by the control register, the control register must be in the "1" state in order to get the start-stop oscillator started. The incoming code group, after being shaped in the register drive, is applied to one of the inputs on the now open input gate. The first element (bit) of this code group is the start pulse, which triggers the start delay circuit after it passed through the input gate. The signal developed is equal to approximately one-half of a bit in length, and is used to delay the sampling of each bit until about its midpoint. This position was selected as being the most reliable under poor transmission conditions.

4.12 The output of the start delay is applied to the start OR gate which was opened when the start pulse passed through the signal delay circuit. This delay is provided to aid in the prevention of false starts. Since the action here is more of the integrator type action, only pulses of long duration will pass through it. Thus, short noise pulses ("hits") on the line will not be applied to the start gate, and this gate will not open to a false start. When a true start pulse is applied through the delay to the start gate, the gate will open and the pulse from the start delay circuit will pass through the start gate. The trailing edge of this pulse is formed into a trigger pulse in the start pulse amplifier, and applied to the control register.

4.13 Upon receipt of the trigger pulse, the control register shifts to its "1" state and causes the following action to take place:

(a) Start-stop oscillator starts.

(b) Start AND gate closes.

(c) Prime is removed from start delay.

The first advance pulse is generated about 50 microseconds after the start-stop oscillator is turned on, and causes the start pulse to register in the Nth element of the signal register. Since this is a space, it causes this element to return to the "0" state. (All signal register elements were set in the "1" state before the code arrived.)

4.14 The closing of the start AND gate, and removal of the prime from the start delay prevents any further transitions in the code input from feeding through to the control register and causing it to operate too soon.

4.15 All the register elements will receive a shift pulse, but no shift takes place since all but the first (Nth) element in the signal register are in the "1" state and the prime is in the "1" state.

4.16 About the middle of the first code bit, the second advance pulse occurs causing the "0" condition of the Nth element to advance to element N-1, and the code bit to be registered in the Nth element. With the arrival of the next advance pulse, the "0" condition in element N-1 moves to element N-2; the state of element N moves to element N-1, and the new code bit is registered in the Nth element. This continues as each advance pulse arrives until, with the N-1 code bit, the start pulse, registered as state "0", will have advanced to element 1, and the N registered bits will be recorded in elements 2 through N. The next advance pulse moves all code bits and the start pulse one position to the right, advancing the start pulse into the control register and registering the last code bit in element N. The control register, upon receipt of the start pulse, shifts from the "1" state to the "0" state, causing the following action to take place:

(a) Start-stop oscillator stops.

(b) Stop inserter develops signal, priming synchronizer flip-flop.

(c) Synchronizer flip-flop triggers, closing signal gate.

(d) Start delay is primed.

(e) Start AND gate opens.

(f) The 100-microsecond shift delay circuit is triggered.

(g) The 200-microsecond set "1" delay circuit is triggered.

4.17 With the signal gate closed, no further transitions on the line will affect the operation of the receiver until the stop inserter acts to open the signal gate. After an elapse of 100 microseconds, the signal applied to the shift delay circuit emerges and causes each element of the storage register to shift to the same state as its corresponding element in the signal register. Thus, the information is cleared from the signal register and stored in the storage register. There, 200 microseconds after the last advance pulse, the set "1" pulse emerges from the set "1" delay circuit. This pulse is used to reset the signal register to its "1" condition, and the transfer prime to its "1" condition. The signal register is now prepared to accept a new code.

4.18 The transfer prime circuit, together with the variable delay, determines the amount of time the transfer pulse is delayed from the pickup pulse. This delay is necessary to prevent loss of a character due to the jitter of the incoming signal.

4.19 The synchronizer flip-flop, which is triggered by the stop inserter, keeps the signal gate closed during the stop time. The gate then opens, and is ready to accept a start signal at any time after this. With the next start pulse, the cycle will begin over again, and the same sequence of operation will be repeated to register and punch the next code character.

DETAILED CIRCUIT DESCRIPTION

A. Signal Converter (Receiving)

Note: Refer to schematic wiring diagram 3833WD.

Initial Conditions

4.20 Initially, when the power switch is turned ON, -6 volts is applied to terminal H of the integrator pulse shaper Z405. After a delay of about 100 to 300 milliseconds, Z405 provides a negative going transition on its output, terminal K. This signal is applied to the input of pulse amplifier Z408B, terminal D, which produces a positive-going pulse, -6 volts to 0 volt, on its output, terminal L. This positive pulse is sent to terminal E4 of connector J401, and from there to the receiving distributor to reset the control register (see Paragraph 4.37).

Storage Register

4.21 The normal and inverted sides of the signal register in the receiving distributor are applied through connector J401 to the prime "1B" and prime "0B" inputs of the signal converter storage register elements, terminals E and F of Z411 through Z418. Thus, if a particular bit is a MARK in a signal register element, that element will be in the set "1" condition and its normal output will prime the "1B" input of the corresponding flip-flop in the storage register. When the shift pulse from the receiving distributor, which comes in on terminal C1 of connector J401, is applied to the set "1B" input of this storage register element, it switches to the set "1" condition. If a SPACE condition exists in a signal register element, the corresponding storage register element will shift to the set "0" condition when the shift pulse comes in on its set "0B" lead, terminal F of Z411, Z412, or Z413 through Z418, depending on the number of code levels used.

4.22 If any of the elements in the storage register are in the set "1" condition, this provides a prime for their respective magnet pulsers on terminal E. A transfer pulse on the input of the magnet pulser, terminal B, will cause the primed magnet pulsers to fire and remain on for a period of approximately 4.5 milliseconds. The output of this card, terminal A, Z419 through Z427, is applied to the punch magnets. When triggered, the output of the magnet pulser, terminal A, switches from -28 volts to ground.

Transfer Circuitry

4.23 One hundred (100) microseconds after the information is passed from the signal register into the storage register, a transfer prime pulse from the set "1" delay appears at terminal B1 of connector J401. This pulse is sent to the set "1A" input of the transfer prime flip-flop, terminal C of Z403, causing this flip-flop to switch to the set "1" condition. The normal output, terminal L, goes to 0 volt and is sent to the prime "1" input of the transfer one-shot, Z407. The inverted side of the transfer flip-flop, terminal K, goes to -6 volts and is applied to the bias input of the variable pulse delay circuit, terminal A of Z406. The pickup pulse is received from the punch on terminal D1 of connector J402 and is sent to the pickup amplifier, terminal A, Z404A. The output of the pickup amplifier, terminal L, is applied to the input of the pickup inverter circuit, terminal F, Z404B. The output of Z404B produces a positive-going pulse (-6 volts to 0 volt) which is applied to the set "1" input of the variable pulse delay, terminal C.

4.24 The variable pulse delay circuit now acts like a one-shot triggered by the output of the pickup inverter; however, the time duration of the variable pulse delay circuit depends on the amount of time the bias signal exists on terminal A of Z406, and the pickup pulse is applied to the set "1" input, terminal C. Thus, after a period of time, the variable pulse delay relaxes and produces a positive going pulse on its inverted output, terminal K. This output is applied to terminal C of Z407, the transfer one-shot, causing it to fire. The time-out of the pulse delay varies between 0.4 to 1.2 milliseconds.

4.25 A positive transition occurs initially on the normal output of Z407, terminal L, and is applied to the set "0A" input of the transfer prime flip-flop, terminal D of Z403, switching it to the set "0" condition. A negative transition occurs on the normal output of the transfer one-shot 100 microseconds after the receipt of a pulse from the variable pulse delay, and is applied to the input of pulse amplifier Z408A, terminal B. See Paragraphs 4.28 through 4.34 for a detailed description of the variable pulse delay circuit, and Paragraphs 4.35 through 4.36 for a detailed description of the transfer circuitry timing.

Magnet Pulsers

4.26 The pulse amplifier produces a positive-going pulse, -6 volts to 0 volt, and applies it to the input of inhibit gate Z402B, terminal N. The pulse is passed through the gate and is applied to the input of emitter follower Z409, terminal B. The output of Z409 is applied to terminal B of all the magnet pulsers, Z419 through Z427, causing all the magnet pulsers primed by the set "1" condition of the storage registers to fire. Since the feed magnet pulser, Z419, is continuously primed (ground on terminal E), it always fires upon the receipt of a transfer pulse. The firing of the magnet pulsers provides a ground path for the corresponding magnets in the punch. This causes those magnets to energize, punching the stored information into the tape.

Incoming Signal

4.27 The incoming signal from the data set is received on terminal D10 of connector J401 in polar form. This input is converted to a -6 volts to 0 volt signal by passing it through the receiver input amplifier, Z401. The output of Z401 appears at terminal C10 of connector J401. From here, the signal is applied to the signal input of the receiving distributor.

B. Variable Pulse Delay Circuit

General

4.28 The variable delay is used in the Tape Receiver terminal for two reasons. First, to develop a proper time relationship between the pickup and the transfer prime, and second, to generate a transfer pulse for the magnet pulsers. The reader, at the Tape Sender terminal, has inherent mechanical jitter which appears on the signal, causing the start pulse to occur at slightly different times each cycle. At a critical time in the punching operation, this jitter could possibly cause the loss of a whole character. The variable delay circuit prevents this from occuring.

4.29 The variable delay circuit is a stable-state device which may be switched to a semi-stable condition. It will remain in its semi-stable state for a length of time determined by a bias prime which acts to effect the time-out of the circuit. Figure 5(A) is a schematic representation of this circuit. Its element number is Z406 (EC351), and it is used in the receiving signal converter (3833WD).

Operation - Fixed Bias Prime

4.30 Stable state: In the normal stable-state condition of the circuit, Q2 is forward biased and Q1 is reverse biased. Q2 is forward biased by virtue of the -6 volt potential on its base through R10 and R2. Its collector potential, about 0.85 volt, holds Q1 in the OFF condition. The 0.85 volt potential at the collector of Q2 is derived from the emitter side of R9 and, therefore, also appears at the emitter of Q1.

4.31 Triggering:

Note: During the following discussion, reference is made to Figure 5(B). This figure portrays the wave forms which appear at the various points mentioned below, and which are circled on Figure 5(A).

A positive going square wave applied at the input, C, of the differentiator network produces a positive pulse at point A. This pulse reverse biases Q2, turning it OFF. The collector of Q2 drops to -6 volts (point B), clamped at that potential by CR3. The negative transition is coupled to the base of Q1 (point C) forward biasing that transistor. When Q2 conducts, its collector voltage rises to 0.85 volt (point D) from its -6 volt clamp level. The base of Q2 now swings positive at point E, due to the previously changed condition of C3 (plus to minus as indicated on Figure 5(A)). Capacitor C3 immediately begins to discharge toward the voltage level V1 or V2, depending on the prime voltage level at the bias input A. Levels V1 and V2 are established by the voltage divider action of R11 and R3. The rate of discharge of C3 is determined by R11, R3, and R2.

4.32 Time-out: Assuming a -6 volt bias input, C3 begins to discharge toward that level. The time the circuit remains in this semi-stable state is determined by the time required for C3 to discharge to a level which allows Q2 to turn ON. The discharge of C3 follows the expotential decoy shown for point E until a level more negative than about 1 volt is reached at t1. When this point is reached, Q2 turns ON and Q1 turns OFF. Capacitor C3 recharges to its 6 volt potential during the stable state condition. Diode CR2 is reverse biased while C3 charges, preventing any distortion of the Q1 collector wave form. If the bias input voltage level had been 0 volt instead of -6 volts, it would have taken C3 a longer time (t2) to discharge to the level where Q2 turned ON, resulting in a longer time-out for the circuit.

Operation - Variable Bias Prime

4.33 General: The above paragraphs consider the cases when the bias is fixed at either -6 volts (V1) or 0 volt (V2) throughout a complete operating cycle. This, however, is not the normal operating condition of the circuit. Normally, the bias input will switch from 0 volt to -6 volts somewhere between times t1 and t2. This will cause the circuit to operate in its semi-stable state for a period of time (t3) occurring between t1 and t2.

4.34 Operation: The wave forms in Figure 5(C) are those associated with the points mentioned below, and which are circled on Figure 5(A). Note that wave forms A, B, and E, Figure 5(C), represent the same points as A, B, and E, Figure 6. During normal operation, the bias prime switches from 0 volt to -6 volts somewhere between t1 and t2. When the trigger pulse at point A switches Q2 OFF, C3 discharges toward the 0 volt bias prime level, V2. At some time, t, the bias prime level switches to -6 volts, V1, causing C3 to change its discharge rate. The voltage at the base of Q2 now reaches the forward bias level (about 1 volt) at time t3 - before t2, but after t1. Transistor Q2, therefore switches ON at this time. Times t1 and t2, Figure 5(C), indicate the time durations for C3 to discharge to about 1 volt if the bias had been fixed at either -6 volts or 0 volt.

C. Transfer Circuitry Timing

4.35 Figure 6 is a timing diagram of the transfer circuitry during the critical time after a character has been inhibited and remains in storage until the next cycle. Referring to the timing diagram, a shift pulse, (A), transfers the information from the signal register to the storage register. 100 microseconds after the shift occurs, the set "1" delay pulse, (C), sets the transfer prime flip-flop, Z403, to the set "1" condition (normal output, (D), goes positive). The clock pulse, (K), which triggers the variable pulse delay circuit Z406, (F), has come in and the variable pulse delay begins its time out. The inverted output, (E), of the transfer prime flip-flop provides bias for the variable pulse delay circuit. Since the transfer prime is in the set "0" condition, the variable pulse delay circuit times out to its longest pulse width. The normal output of the transfer prime flip-flop primes transfer one-shot Z407, (G), and the positive transition of the variable pulse delay triggers the one-shot. In Figure 6, the first character, A, has been shifted, the variable pulse delay has timed out, and the transfer prime flip-flop is still in the set "0" condition (normal output at -6 volts). Thus, the transfer prime one-shot will not be triggered, a transfer pulse, (H), will not be generated, and character A will not be punched. The character will remain in storage until the next punch cycle. The set "1" delay pulse comes in and the transfer prime flip-flop goes to the set "1" condition.

4.36 When the next clock pulse comes in, the variable pulse delay circuit, Z406, times out to its shortest pulse width and triggers the transfer one-shot, Z407. The positive transition of the transfer one-shot is used to reset the transfer prime flip-flop to the set "0" condition. The negative transition, which occurs 100 microseconds later, generates a transfer pulse which triggers the magnet pulser (J). Character A is punched. The dotted signals in the timing diagram indicate the worst possible condition if the start pulse of the next character, B, appeared earlier in the cycle and the motor speed reduced causing jitter in the clock pulse. As indicated, character A will be punched and character B will remain in storage until the next punch cycle. Figure 7 is a similar timing diagram of the transfer circuitry, but illustrates several cycles of operation.

D. Receiving Distributor

Note: Refer to schematic wiring diagram of receiving distributor 4441WD and receiving terminal timing diagram Figure 8.

Initial Conditions

4.37 Approximately 150 to 300 microseconds after the power switch is operated to the ON position, the -6 volts to 0 volt reset pulse generated in the receiving converter appears at terminal E4 of connector J301, the set "1B" terminal of control register Z310, and the set "0A" terminal of element Z320. The reset pulse places element Z320 in the set "0" condition, and the control register flip-flop in the set "1" condition. The events are as follows:

(a) The start-stop oscillator turns on for one cycle, generating one advance pulse.

(b) The control register is triggered after completion of one cycle of oscillation, and the oscillator is turned off.

(c) The stop inserter one-shot is turned on and starts its time out.

(d) At the completion of the stop inserter time out, the synchronizer flip-flop is triggered to the set "1" condition.

(e) The start OR gate, Z301A, is opened to accept a start pulse.

(f) The start AND gate, Z301, is opened.

(g) The input gate on the start delay is primed.

Signal Input

4.38 The receiving distributor receives a +1 volt to -6 volts start signal from the receiving signal converter on terminal C10 of connector J301. This start signal is applied through the operate switch to terminal C of the signal gate, Z301A. The start signal is also applied to the set "1B" and prime "1A" input of the synchronizer flip-flop. The signal will pass through the gate, Z301A, on terminal A provided the synchronizer flip-flop, Z324 (output on terminal K) is in the set "1" condition.

Register Drive

4.39 From the output of the signal gate, the signal is sent to the input of emitter follower Z302A, terminal D, and from terminal N of Z302A, to the first inverter of the register drive, Z303A, terminal B. The output of Z303A, terminal K, applies the inverted signal to:

(a) The prime "0B" side of the last element in the signal register, terminal H (element Z313, Z314, or Z315, depending on number of code levels).

(b) The input of the next inverter, Z303B, terminal D.

(c) The input of the start delay, Z305, terminal C.

4.40 The second inverter, Z303B, inverts the signal so that it is back to normal. From the output of Z303B, terminal L, the signal is applied to:

(a) The prime "1B" side of the last flip-flop of the signal register (element Z313, Z314, or Z315, depending on number of code levels).

(b) To the input terminal of the signal delay, Z304.

4.41 A start transition consists of a +1 to -6 volt transition lasting for a period of one bit. When this transition passes through the first inverter it becomes a -6 to 0 volt pulse. This pulse is sent to the set "1" input of the start delay one-shot, terminal C, Z305, causing it to begin a time-out for approximately a half a bit. The normal output of this one-shot, terminal L, goes from -6 to 0 volts and is applied to terminal N of Z301B, the start OR gate.

4.42 The second inverter, Z303B, brings the -6 to 0 volt transition from the output of the first inverter, Z303A, terminal K, back to the original 0 to -6 volt transition, and applies it to the input of the signal delay, terminal C, Z304. The output of the signal delay, terminal L, delays the 0 to -6 volt transition by 40 microseconds, to prevent a false start, and sends this delayed transition to terminal M of Z301B.

Start Circuits

4.43 The output of the start OR gate, Z301B, is 0 volt, if 0 volt appears on any of its inputs, and -6 volts, if -6 volts appears on all of its inputs. This is an important fact to remember while trying to understand how the start OR gate performs its function in the circuit. If a true start signal has been sent, then 40 microseconds after the signal is received, terminal M of Z301B goes to -6 volts for a period of one bit. Terminal N of Z301B goes from -6 volts to 0 volt as soon as the start transition is received, and remains at 0 volt until the start delay timer, Z305, relaxes (about one-half bit time duration). The start delay relaxes before terminal M of the OR gate has a chance to return to 0 volt. This results in a 0 to -6 volt transition on terminal N of the OR gate, which will appear on the output, terminal L. If a false start is received (i.e., a short 0 to -6 volt transition), terminal M of the OR gate will be at 0 volt when the false start arrives on terminal N of the OR gate, preventing the 0 to -6 volt transition from appearing on the output. See timing diagram, Figure 8.

4.44 The negative transition from terminal L of the start OR gate is passed through the start AND gate, terminal F, Z301C, to the input of the start pulse amplifier, Z302B, terminal B. The start pulse amplifier shapes the negative transition on its input into a positive going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to the set "1A" input of the control register, terminal C, Z310, switching it to the set "1" condition.

4.45 When control register Z310 switches to the set "1" condition, the following events take place:

(a) Start-stop oscillator Z311 starts, due to the 0 volt potential appearing on its input, terminal H, from the normal output of the control register.

(b) Start gate Z301C, closes due to the -6 volt potential on its input, terminal E, from the inverted output of the control register.

Start-Stop Oscillator

4.46 The start-stop oscillator, Z311, receives a -6 volt to 0 volt signal from the control register flip-flop as described in Paragraph 4.45. The oscillator begins to oscillate as soon as a 0 volt signal is applied to its input, terminal H, and the output appears as a sinusoidal oscillation on terminal A. This output is sent to the input of the squaring amplifier, Z312, terminal H. The squaring amplifier shapes the sine wave to produce a positive going -6 to 0 volt advance pulse every cycle. One advance pulse is produced for each period of the sine wave output. The advance pulses are applied to both the set "1B" and set "0B" inputs of the signal register flip-flops, terminals E and F of Z313 through Z320, and to the set "0B" input of the control register, terminal F, Z310.

Signal Register

4.47 The signal input is applied to the prime inputs of the Nth register element - Z313, Z314, Z315, or Z316 depending on the level of operation (8, 7, 6, or 5 respectively) being considered. Although 8-level operation is assumed in the following discussion, theory of the other levels is similar, the signal input priming the correct element of the signal register.

4.48 The input signal advances through the signal register bit-by-bit. To analyze operation of the register, consider what happens as a start pulse is shifted through the register.

(a) The start pulse, after passing through Z301A and Z302A, appears at the input of the first of the two register drive inverters, Z303A and Z303B. The first inverter output applies a 0 volt prime signal to the "P0B" input of the Nth element in the signal register (terminal H of Z313 for 8-level operation).

(b) This same 0 volt signal is applied to the input of the second inverter, Z303B. Its output, a -6 volts signal, is applied to the "P1B" input of the Nth element, terminal J.

(c) The Nth element is now primed for set "0." When the first advance pulse arrives at terminal F, the Nth element flip-flop switches. Its inverted output, terminal K, applies a prime to the "P0B" input of the next register element, and its normal output, terminal L, applies a prime to the "P1B" input of the same register element (Z314).

(d) When the second advance pulse appears at the set "0B" input of Z314, this register element switches to the set "0" condition. Simultaneously, the next bit passes through the double inverter, Z303A and Z303B, priming the Nth signal register element as described in Sub-Paragraph (a) above.

(e) Thus, the signal is inserted into the signal register bit-by-bit until the N+1 advance pulse shifts the start pulse into the control register, Z310. The start pulse primes the "P0B" input of Z310, and the advance pulse causes this flip-flop to switch to the "0" state.

4.49 When the control register flip-flop switches to the set "0" condition, seven things happen.

(1) The start-stop oscillator stops and suspends further generation of advance pulses.

(2) The 100-microsecond shift delay one-shot, Z307, begins to time out.

(3) The 200-microsecond set "1" delay one-shot, Z306, begins to time out.

(4) The start AND gate, Z301C, opens.

(5) The start delay one-shot, Z305, is primed.

(6) The start inserter one-shot starts its time out.

(7) The synchronizer flip-flop is triggered.

Shift Delay

4.50 The shift delay one-shot, Z307, becomes active on receiving the -6 to 0 volt transition on its set "1" input, terminal C, from the control register. After a period of 100 microseconds, the circuit relaxes, and sends a negative going pulse from its normal output, terminal L, to the input of pulse amplifier Z308A. Pulse amplifier Z308A provides a positive going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to the input of an emitter follower circuit, terminal B, Z309A, which provides power amplification of the pulse. From the output of the emitter follower, terminal A, the pulse is sent to terminal C1 of connector J301. From there it passes to the signal converter to shift the information in the signal register into the storage register.

Set "1" Delay

4.51 200 microseconds after the positive transition from the control register excites the set "1" delay one-shot, Z306, a negative transition is generated at its normal output, terminal L. This transition is fed to pulse amplifier Z308B, terminal D, and appears as a positive -6 to 0 volt transition on the output, terminal L. The pulse is sent to emitter follower Z309B, terminal D, for power amplification, and from the output of the amplifier, terminal N, to the set "1A" input of all the signal register flip-flops (terminal C of elements Z313 through Z320). The positive transition on the set "1A" input of the flip-flops causes them to reset to the set "1" state, since all the elements are primed with +1.5 volts on terminal M, the "P1A" input.

4.52 Thus, 100 microseconds after the control register goes into the set "0" condition, the shift delay transmits a pulse to the signal converter to shift the information in the signal register into the storage register. And, 200 microseconds after the control register goes into the set "0" condition, the set "1" delay transmits a pulse to reset the signal registers to the set "1" condition. In addition to reset, the set "1" delay performs another function. The output of emitter follower Z309B is also applied to terminal B1 of connector J301. From there the output of Z309B (-6 to 0 volt transition) is sent to the transfer prime, Z403, in the signal converter. This informs the signal converter that the signal is in the storage register and is ready to be punched.

4.53 The -6 to 0 volt transition from the inverted output of the control register is applied to terminal E of the start AND gate, Z301C, keeping the gate open. The purpose of this gate, which closes while the control register is in the set "1" state, is to prevent signals from being applied to the control register while the start-stop oscillator is in operation. The same positive transition, when applied to the prime "1" input of the start delay one-shot, primes the start delay gate so that it can be triggered to generate a start pulse when the start-stop oscillator is not oscillating.

Synchronizing Flip-Flop

4.54 The positive transition from the control register is also applied to the set "1" input of stop inserter Z321, terminal C. This element triggers, producing a -6 to 0 volt transition on its normal output, terminal L. This signal is applied to the set "0A" input of the synchronizer flip-flop, triggering this circuit to the set "0" condition. Refer to Paragraph 5.29 through 5.34 for a detailed description of the resynchronizer circuit.

Test Conditions

4.55 With the test-operate switch in the TEST position, a -12 volt bias is applied to terminal C of input gate Z301A. This simulates an open line condition.

4.56 In the TEST position, the circuit path from the resynchronizer circuit to terminal D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This condition results in local regeneration of blank characters, the stop inserter applying the stop pulse. Local electronic testing can, therefore, be performed. Note that the resynchronizer circuit will not be triggered; it will remain in the set "0" condition.

4.57 A jack, J302, has been provided to facilitate local testing and to permit receiving margins to be taken using a 905A or 905B Data Test Set. The test signal applied shall be -6 volts for SPACE and 0 volt for MARK working into a 1200 ohm load. With a test signal applied, the resynchronizer circuit will be triggered randomly.

E. Auxiliary Connections

4.58 Receiving distributor:

(a) Set "1" delay, terminal E2, connector J101 informs the auxiliary equipment that the character in the signal register has been transferred to the storage register.

(b) Start-stop control lead, terminal E3, connector J301 is used to permit the auxiliary equipment to turn the start-stop oscillator on and off.

4.59 Signal converter:

(a) Signal blind, terminal E9, connector J401, is used to permit the auxiliary equipment to prevent the receiver from receiving the incoming signal.

(b) Clock, terminal F1, connector J401, is used to monitor the shaped magnetic pickup and to provide timing in the auxiliary equipment.

(c) Transfer inhibit, terminal E7, connector J401, is used to inhibit the punch magnets.

(d) Transfer, terminal E6, connector J401, is used to monitor the transfer pulse for use in the auxiliary equipment.

(e) Terminals E2 and E3, connector J401, are used in conjunction with auxiliary equipment for vertical parity checks.

5. OPTIONAL FEATURES

TAPE SENDER

A. Signal Converter (Sending) With Rubout Delete

General

5.01 The signal converter with rubout delete feature is basically identical to the signal converter described in Paragraphs 3.02, 3.06 through 3.09 and 3.14 through 3.20. The important difference between these units is the rubout delete feature - a feature which prevents the transmission of an all MARK signal from the Tape Sender to the Tape Receiver.

5.02 In certain data systems the operator, while preparing a message tape, may insert errors into the tape. To "erase" these mistakes, the errored characters are deleted by punching all levels (rubout) of the entire group of characters involved. The correct message is then repunched into the tape in a new location.

5.03 When the tape is transmitted, the receiving station would normally receive all information sensed by the tape reader at the sending station, including the all MARK or rubout characters. If, however, a sending signal converter with rubout delete is utilized at the sending station, the all MARK (rubout) signals will be suppressed. Consequently, only the valid data information will be reproduced by the Tape Receiver.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 5917WD.

5.04 General: Since the circuit analysis of this signal converter is similar to that already covered elsewhere in this section (see Paragraph 5.01), reference will be made to the applicable paragraphs whenever possible.

5.05 The rubout delete function of this signal converter is controlled by five logic elements: Z215A, Z215B, Z216A, Z216B, and Z217A. These elements function to control operation of the start-stop oscillator in the sending distributor.

5.06 Initial conditions: Refer to Paragraphs 3.14 and 3.15.

5.07 Reader input: Refer to Paragraph 3.16.

5.08 Rubout delete: The universal contact signal from the reader is applied to integrator Z202D via terminal H9 of J201. The output of Z202D, terminal P, is applied to OR gate Z215B, terminal P. This signal is gated with the inverted output of Z215A, and is applied to terminal R of emitter follower Z216B. The output of Z216B is connected to terminal C4 of J201, and is applied to the start inhibit gate in the receiving distributor. When the output from Z216B is 0 volt, the start-stop oscillator in the distributor is prevented from starting (refer to Paragraph 3.24).

(a) SPACE and MARK input: If any one of the levels sensed by the reader is SPACE, the corresponding integrator output is about 0 volt. A MARK signal, on the other hand, produces a -10 volts signal. When the MARK and SPACE signals are gated together in OR gate Z215A, its output, terminal B, will assume the most positive potential (0 volt). This 0 volt signal is amplified through emitter follower Z216A, and applied to pin B of inverter Z217A. The inverter output, terminal K, goes to -6 volts and is gated with the universal input in Z215B, causing the output of Z215B to go to -6 volts. This -6 volts level is amplified by Z216B and applied, via terminal C4 of J201, to the start inhibit gate in the distributor. A -6 volts input to the start inhibit gate allows the start-stop oscillator to start, and the character sensed by the reader to be transmitted to the receiving station.

(b) All MARK input: If all levels are MARK, however, the output of Z215A will go to -6 volts, and the inverter, Z217A, will present a 0 volt signal to OR gate Z215B. The output of Z215B remains at 0 volt even though the universal contact closes. Consequently, the start-stop oscillator in the distributor will be inhibited, and the all MARK character will not be transmitted to the receiving station.

5.09 Polar signal output: Refer to Paragraph 3.18.

5.10 Request-to-send: Refer to Paragraph 3.19.

5.11 Power requirements: Refer to Paragraph 3.20.

B. Line Break and Automatic Answer Modification Kit

General

5.12 The line break and automatic answer feature allows a Tape Sender terminal to automatically transmit its message tape in answer to a call placed by a Tape Receiver terminal. Operation of both terminals is controlled by the operator at the receiver location. This feature is available in kit form (TP-146527) for field or factory installation.

5.13 Proper operation of the line break and automatic feature depends upon use of a data set with the following features:

(a) Unattended answering.

(b) Reverse channel carrier.

Although these data set features are not currently available, the automatic answer feature may be added to an existing tape sender pending their availability.

- Another modification kit - interim unattended answer - is available which allows Tape Senders equipped with the line break and automatic answer feature to make use of that feature until the necessary data set features are available (see Paragraph 5.19).

- The following discussion assumes availability of reverse channel carrier and unattended answering.

Detailed Circuit Description

Note: Refer to schematic wiring diagrams 3843WD, 4772WD and 5941WD.

5.14 Manual operation with line break: The tape sender is prepared to operate in the manual mode when the following conditions exist:

- Tape reader loaded with a message tape; tape-out contact closed.

  Tape reader and tape winder motor switches OFF.

  Data set in TALK condition; telephone receiver on hook.

  Interlock and line break outputs at 0 volt and -8 volts respectively.

  Test-operate switch, S101A and S101B, in OPERATE position.

  Manual-automatic switch in MANUAL position.

  Normally open tape-out contact closed.

  Tape reader run-stop switch in STOP position (open).

(a) A call may be placed by the operator at either the Receiver or Sender location. When verbal agreement is reached to start transmission, the operator at the Sender location starts the tape reader and winder motors by placing their respective switches in the ON position. Next, he depresses the DATA button. The data set goes into the

DATA mode, placing the Sender on the line and switching the voltage level on the interlock output (terminal 6 of J601) from 0 volt to +8 volts. Since the automatic-manual switch is in the MANUAL position (breaking the circuit between relay driver Z601B and the motor start relay), the motor start relay will not energize on this +8 volts input.

(b) When the operator at the Receiver location places his data set in the DATA mode, a line break signal (400 cycles-per-second tone) is transmitted continuously. In the data set at the Sender location, a detector recognizes this signal and causes the line break output to switch from -8 volts to +8 volts. The +8 volts signal is applied through S101A to terminal F of relay driver Z601A. The relay output, terminal J, switches from -28 volts to 0 volt, energizing the line break relay via the tape out contacts. When the line break relay energizes, normally closed contact C4 opens and normally open contact C5 closes.

(c) The Tape Sender operator (after a few seconds wait to allow the tape receiver operator time to place his data set in the DATA mode) operates the run-stop switch on the reader to the RUN position. This completes the energizing circuit to the reader clutch coil; from ground, through the run-stop contacts, through the normally closed B9 contact and the normally open C5 contact, to one side of the clutch magnet. The tape reader starts sensing tape. Note that the tape reader will not start sensing tape unless contact C5 is closed. Contact C5 is controlled via the data set at the Receiver location; if the Tape Receiver is not in DATA mode, or the line is disconnected, contact C5 is opened. If this is the case, and if the run-stop switch is in the RUN position, then the alarm relay will energize actuating the audible and visual alarms to indicate a line break condition. The reader will start, pending receiver action.

(d) When an end of message (EOM) condition occurs (in this case, end of tape), the tape-out contacts open. The line break relay de-energizes, and contacts C4 and C5 return to their normal conditions. Contact C5 opens the energizing path to the reader clutch coil, stopping the reader, and contact C4 completes the energizing path to the alarm relay; from ground, through the run-stop switch, through the normally closed B9, B10 and C4 contacts, then through the alarm relay to -28 volts. Both the audible and visual alarm indicators are energized, and the auxiliary alarm circuit is conditioned to operate.

(e) The alarms are disabled when the operator at the sender location moves the run-stop switch to the STOP position. The reader and winder motors can now be de-energized. If verbal confirmation to disconnect is required, the Sender operator may contact the receiver operator via his telephone hand set after depressing the TALK button. If no verbal confirmation is necessary, the disconnect can be made in the normal manner.

5.15 Operation of line break: If for some reason (trouble at the Tape Receiver location, for example) the Receiver operator wants to stop transmission and contact the Sender operator, all he need do is remove his telephone hand set from hook and depress the TALK button. This interrupts the line break signal tone, causing the line break output from the Sender data set to switch to -8 volts. The output of relay driver Z601A, terminal J, switches to -28 volts, and the line break relay de-energizes operating contacts C4 and C5 as outlined in Paragraph 5.14 (d). The alarms are disabled when the run-stop switch is operated to the STOP position. The Sender operator may talk to the Receiver operator by lifting his telephone hand set off hook and depressing the TALK button. Transmission may be restarted at the discretion of the Sender operator.

5.16 Automatic answer and line break: The Tape Sender is prepared to operate in the automatic mode when the following conditions exist.

- Automatic-manual switch in AUTO position.

  Tape reader and tape winder motors OFF.

  Tape reader loaded with a message tape; tape-out contact closed.

  Data set in AUTO position; telephone receiver on hook.

(a) If the above conditions are met, the automatic answer relay will be energized via the tape out contact and the automatic manual switch. When energized, the automatic answer relay closes normally open contact B11, shorting the remote control common and ready leads to the data set. This primes the Tape Sender data set to automatically answer an incoming call.

(b) A call is originated by the operator at a Tape Receiver location. The Tape Sender data set will answer this call (1200 cycles-per-second tone) and, after several seconds, go into the DATA mode. When it does, its interlock output switches from 0 volt to +8 volts. This +8 volts signal causes the output of relay driver Z601B to switch from -28 volts to 0 volt, energizing the motor start relay via the automatic-manual switch. Normally open contacts K1 and K3 close, energizing the tape reader and winder motors.

(c) Upon hearing the answer tone from the Sender data set, the Receiver operator places his data set in the DATA mode. A line break signal (400 cycles-per-second tone), transmitted from the Receiver terminal data set to the Sender terminal data set, causes the line break output at the sender location to switch from -8 to +8 volts. A +8 volts input to relay driver Z601A switches its output to 0 volt, energizing the line break relay which operates contacts C4 and C5. The energizing path for the reader clutch coil is from ground, through normally open contacts B9 and C5, the reader clutch coil, and the 25 ohm resistor to -28 volts. The Tape Receiver operator can control transmission, therefore, depending upon the operating mode of the Receiver data set.

5.17 End-of-message: When the message tape is exhausted, the tape-out contact opens de-energizing the automatic answer and line break relays. These relays return their associated contacts to their normal conditions, causing disconnect of the automatic answer prime to the Sender data set (contact B11) and stopping the tape reader (contacts B9 and C5). The interlock output at the Sender terminal switches from +8 volts to 0 volts, causing the output of relay driver Z601B to switch from 0 volt to -28 volts. The motor start relay de-energizes, disconnecting the tape reader and winder motors. The Receiver operator can now take action to disconnect his terminal. Future calls placed to the Sender terminal will not activate the Sender terminal. Since the automatic answer relay is de-energized, contact B11 is open and the initial automatic answer conditions are not satisfied (Paragraph 5.16). To complete the automatic answer conditions, a message tape must be loaded into the tape reader.

5.18 Test-operate switch: The test-operate switch must be in the OPERATE position for normal operation in both the manual and automatic modes. When in TEST position, this switch places a +6 volts bias on the Z601A and Z601B relay driver inputs. This simulates the DATA mode of the data set, permitting local testing and trouble shooting.

- When installed in Tape Senders before reverse channel carrier and unattended answering are available - and if the interim unattended answer modification kit (Paragraph 5.19) has not been installed - the test-operate switch must be in the TEST position.

C. Interim Unattended Answer Modification Kit

General

5.19 The interim unattended answer feature, when used in conjunction with the line break and automatic answer kit (Paragraph 5.12), provides facilities for automatically starting an unattended Tape Sender from a remote Receiver location. It is specifically designed to be used with the line break and automatic answer kit until the data set reverse channel carrier and unattended answer features are available (Paragraph 5.13). The interim unattended answer feature is available in kit form (TP-148161) for field or factory installation.

Detailed Circuit Description

Note: Refer to schematic wiring diagrams 3843WD, 4772WD, and 5941WD; the 177543 etched circuit board drawing and Figure 9.

5.20 Unattended automatic answer: The following conditions should exist at the tape sender for unattended automatic answer:

- Power on.

  Operate-test switch in TEST position.

  Tape reader loaded with a message tape.

  Tape reader run-stop switch in RUN position.

  Automatic-manual switch in AUTO position.

  Data set in AUTO mode; telephone receiver on hook.

(a) A call is originated by the operator at the Receiver location in the normal manner. If the above initial conditions are satisfied, the automatic answer relay will be energized: from ground, through the relay, the 250 ohm resistor, the automatic-manual switch, and the tape-out contacts (closed when reader is loaded with tape) to -28 volts. Normally open contacts B8, B9 and B11 will be closed, conditioning the circuit for automatic answer. The Sender terminal data set automatically answers the incoming call (contact B11 closed), transmitting a 1200 cycles-per-second tone. Within 4 seconds after hearing this tone, the Receiver operator must depress the DATA button on his data set, placing the Receiver terminal on line.

(b) The Sender data set, after a period of several seconds, automatically goes into the DATA mode, and its interlock output switches from 0 volt to +8 volts. This +8 volts is applied, through the test-operate switch, to the input, terminal M, of the motor start relay driver (Q4 and Q5). The relay driver turns on, and the motor start relay energizes to activate the tape reader and winder motors.

(c) The output of the relay driver (0 volt) is applied to the emitter of Q1, a unijunction transistor, which is part of a time delay circuit. Between about 4.5 seconds and 8.5 seconds after the trigger from the relay driver is applied (time-out determined by the size of C1 and R1), a positive pulse is coupled from the base of Q1 to the gate of Q2, a silicon controlled rectifier (SCR). The SCR turns on (contact B8 closed), turning on amplifier Q3. The output of Q3, terminal J, switches to 0 volt, energizing the line break relay (C) via the tape-out contact. When the line break relay energizes, normally open contact C5 closes and completes the energizing path for the tape reader clutch coil: from ground, through normally open contacts B9 and C5, the clutch coil, and the 25 ohm resistor to ground. The reader starts to sense tape.

(d) When the tape is exhausted, the tape-out contact opens causing the automatic answer relay (B) and the line break relay (C) to de-energize. Normally open contacts B8, B9, B11 and C5 are returned to their normal state. Contact B8 causes the SCR to turn off, which in turn switches amplifier Q3 off. Contact B11 disconnects the data set, and contacts B9 and C5 operate to disconnect the tape reader clutch circuit. The tape reader stops sensing tape.

(e) When the tape reader stops transmitting, the Receiver operator should disconnect his terminal. The Sender terminal data set will automatically disconnect, and its interlock output will switch from +8 volts to 0 volt. This causes the motor start relay driver to turn off, motor start relay to de-energize and the tape reader and winder motors to turn off. The Sender terminal will not automatically answer any future incoming calls until the tape reader is reloaded with a message tape.

5.21 Manual operation: The Tape Sender may be operated manually in the normal manner (see the appropriate section) by not depressing the data set AUTO button, and leaving the manual-automatic switch in the AUTO position. When the Sender operator depresses the DATA button, the tape reader will start after a 4.5 second to 8.5 second delay.

5.22 The unattended automatic answer feature can be disabled by operating the test-operate switch to the TEST position. This switch by-passes the relay driver and time delay circuitry on the TP-177543 (EC543) circuit board, and operates the line break relay. This switch also provides a means for local testing and trouble shooting of the sender terminal.

5.23 When reverse channel carrier is available, the Sender terminal may be enabled to operate with this data set feature by substituting circuit board TP-177543 (EC543) with circuit board TP-146520 (EC520). Operation will then be as described in Paragraphs 5.12 through 5.18. These paragraphs cover operation of the line break and automatic answer feature.

TAPE RECEIVER

A. Automatic Answer Modification Kit

General

5.24 The automatic answer feature allows a Tape Receiver terminal to automatically answer to a call placed by a Tape Sender terminal. Operation of both terminals is controlled by the operator at the sender location. This feature is available in kit form (TP-146528) for field or factory installation.

Detailed Circuit Description

Note: Refer to schematic wiring diagrams 3845WD and 4773WD.

5.25 Automatic answer, or unattended operation, of the Tape Receiver requires that the following conditions exist at the receiver locations:

- Data set in AUTO condition; telephone receiver on hook.

  Data set properly wired (see the appropriate section).

  Sufficient tape supply.

5.26 A call is originated by the operator at the Sender location in the normal manner. The Receiver data set automatically answers the call, and goes into the DATA mode (terminals 19, 20 and 21 of J501 strapped together). When in DATA mode, the data set transmits a brief 1200 cycles-per-second tone to the Sender terminal data set. Simultaneously, the interlock output switches from 0 volt to +8 volts. This +8 volts level is applied to the input of the motor control relay driver, Z501A, terminal F, causing its output, terminal J, to go to 0 volt. The motor control relay (B) energizes, closing the tape punch and tape winder motor contacts (B3 and B1), turning the punch and winder motors on. The Receiver input amplifier, Z501B, acts to blind the receiver signal amplifier, Z401, in the receiving signal converter (refer to schematic wiring diagram 3833WD, terminal E9 of J401). The output of Z501B is determined by the condition of the carrier on-off signal from the data set. When in the OFF condition (i.e., no transmission in process) -8 volts is applied to the input, terminal N, of Z501B. Its output, about +1.5 volts, holds the output of Z401 (EC355) at a positive potential simulating a MARK (or stop) condition.

5.27 Upon hearing the answer-back tone from the Receiver data set, the Sender operator places his data set in the DATA mode. The Receiver data set carrier detector recognizes the 1200 cycles-per-second tone now being transmitted by the Sender data set, and switches the carrier signal from OFF to ON (+8 volts). This +8 volts input to Z501B causes its output to go to -6 volts, unblinding the Receiver signal amplifier, Z401, in the receiving signal converter. The Receiver terminal is now prepared to accept data.

5.28 At the end-of-message, the Sender operator disconnects his data set by lifting the telephone receiver off hook, depressing the data set TALK button, and replacing the receiver on hook. The Receiver data set disconnects automatically, returning the interlock output to 0 volt -- to turn off the winder and punch motors -- and returning the carrier on-off signal to OFF -- to blind the Receiver signal input. The receiver is now prepared to accept the next incoming call.

B. Resynchronizer Modification Kit

General

5.29 The purpose of the resynchronizer circuit feature is to guarantee resynchronization of a Tape Receiver with the incoming signal, when a synchronization error has occurred due to a noise burst on the line. The circuit will achieve positive resynchronization under all random code structures or transmission conditions.

5.30 This feature is available in kit form (TP-148153) for field or factory installation.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 4441WD.

5.31 Normal operation: Operation, as described below, assumes the following conditions:

- Test-operate switch in OPERATE position.

  Unit receiving traffic.

(a) The stop inserter, Z321, is a one-shot circuit which, when triggered, will turn on and remain on for a preadjusted time interval (for example, the time out for 5-level units is adjusted to 2.9±.1 milliseconds; for universal 5 to 8-level units, however, the stop inserter time out is .95±.1 milliseconds). In the following description, a 5-level unit is considered.

(b) The function of the stop inserter is to locally regenerate a stop pulse, at the end of each received character cycle, to prevent the premature start of the receiving distributor due to line noise. When a pulse is received, the start delay one-shot Z305, is triggered and times out for one-half a bit (475 microseconds at 1050 baud). The output, terminal L, of Z305 triggers OR gate Z301B which, in turn, triggers the Z301C AND gate to produce a 0 volt to -6 volts transition. This negative going pulse triggers the start pulse amplifier, Z302B, generating a -6 to 0 volt pulse. This pulse is applied to the set

"1A" input of the control register flip-flop, Z310, placing it in the set "1" condition. The normal output (L) of Z310 goes to 0 volt turning on the start-stop oscillator which generates advance pulses. The pulse, followed by information bits, is shifted down the signal register until it reaches the last element, Z320. This element (0 level) primes the control register input (P0B) so that the next advance pulse generated by the oscillator will place the control register in the set "0" condition.

(c) The oscillator will turn off and simultaneously, the stop inserter, Z321, will be triggered. The normal output (L) of the stop inserter goes from -6 to 0 volts. This signal is applied to the set "0A" input of the synchronizing flip-flop, Z324.

(d) The inverted output signal (K) of the synchronizing flip-flop goes from -6 to 0 volts. This positive pulse passes through the test-operate switch to terminal D of signal gate Z301A. The output of Z301A goes to 0 volt and remains at this level (or slightly more positive) until the incoming transition of the next character, or until the synchronizing flip-flop goes to the set "1" condition. The latter action takes place when the stop inserter completes its time out and the inverted out (K) switches from -6 volts to 0 volt. This signal, when applied to the set "1A" input of the synchronizing flip-flop, triggers it to set "1" only if the prime 1A input is at 0 volt, or if a MARK signal appears at terminal C10 of J301. The synchronizing flip-flop action follows the stop inserter whenever the received unit is in synchronization with the incoming signal.

5.32 Resynchronization: In the timing diagram (Figure 10), character 1 contains an errored start pulse. The next MARK to SPACE transition occurs on receipt of the third bit. The receiver accepts this SPACE signal (ie, bit 3) as a start pulse, resulting in a "late start" or "out of sync" condition. At the end of the character cycle, the stop inserter begins its time out during the middle of the start pulse of character 2. The resynchronizer flip-flop is also triggered at this time. However, it is not reset when the stop inserter finishes timing out because a SPACE bit (bit 2 of character 2) is present at the signal input. This SPACE signal is applied to inputs M (prime "1A") and E (Set "1B") of the synchronizing flip-flop, while the prime "1B" input (J) is primed by the output (K) of the stop inserter. The overall effect of the above action is to move the next start signal to the right. The fifth bit of character 2 is now recognized as the start signal. In character 3, similar action takes place, and by character 4 the receiver is resynchronized with the incoming signal. During correction (or resynchronization) of the above error condition, two incorrect characters would have been recorded by the unit.

5.33 Automatic reset: If power is interrupted for some reason and restored, the synchronizer flip-flop could possibly be triggered to the set "1" condition. This would place a 0 volt signal on the input gate, preventing passage of a start pulse through the gate. To eliminate this problem, the automatic reset is utilized. When power is turned on, a reset pulse is generated and applied to the set "0A" input of the 0-level flip-flop and also to the set "1B" input of the control register flip-flop. This turns the start-stop oscillator on for one cycle to generate one shift pulse. The control register is triggered to the set "0" condition, and its inverted output (K) goes from -6 volts to 0 volt. This signal is applied to the stop inverter. The normal output (L) of the stop inserter is applied to the set "0A" input of the synchronizer flip-flop, resetting the circuit and preparing the unit to receive data.

5.34 Test conditions: With the test-operate switch in the TEST condition, a -12 volts bias is applied to pin C of OR gate Z301A to simulate an open-line condition. In the TEST position, the circuit path from the synchronizer circuit to the pin D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This allows local regeneration of blank characters (the stop inserter applying the stop pulse), so that local electronic testing can be carried out. Note that the synchronizer circuit will not be triggered; it will remain in the set "0" condition. A jack, J302, has been provided to facilitate local testing and to determine receiving margins. Using a data test set TTSG801 or 800 (905A or 905B) working into a 1200 ohm load, apply a -6 to 0 volt (SPACE to MARK) test signal at this point. With the test signal applied, the synchronizer circuit will be triggered randomly.

C. Transmit-Receive Terminal Modification Kit

General

5.35 The transmit-receive terminal modification kit provides a means of connecting a Tape Sender terminal and a Tape Receiver terminal -- located at the same installation -- to a common model 202A or 202B data set. This feature allows both terminals to be serviced alternately by one data set.

5.36 Switching of the common data set from one terminal to the other terminal is facilitated by a three-position switch mounted on the front of the Tape Sender cabinet. Either terminal may be selected to operate with the data set. It is not possible, however, to operate both terminals at the same time. This feature is available in kit form (TP-146532) for field or factory installation.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 4799WD.

5.37 The selector switch mounted on the front of the Tape Sender cabinet has three positions: TEST, RECEIVE, and SEND. Depending upon which position the switch is in, either the Sender or Receiver terminal is connected to the data set, or the terminals are tied together for test purposes.

(a) In the TEST position, the interlock signal path is completed to both the sender and receiver terminals and the request-to-send path is completed to the data set, turning on the modulator. In this condition, the sender terminal can transmit to the receiver terminal for local test purposes. The remote control common path to the receiver terminal is also open, disabling the automatic answer feature.

(b) In the RECEIVE position, the interlock signal path is completed to the Receiver terminal only, turning on the tape punch and tape winder motors. The request-to-send path to the data set is open, disabling the modulator in the data set. The remote control common path to the receiver is completed, enabling the automatic answer circuit at the receiver terminal.

(c) In the SEND position, the interlock signal path is completed to the Sender terminal only, turning on the tape reader and tape winder motors. The request-to-send path to the data set is completed, enabling the modulator. The remote control common path is completed to the Sender, enabling the line break and automatic answer feature at the Sender terminal.

5.38 For automatic operation, the Tape Sender line break and automatic answer test-operate switch must be in OPERATE position, and the auto-manual switch must be in AUTO position. The data set AUTO and DATA push buttons must be depressed.

5.39 Until the line break feature is incorporated in the 202A and 202B data sets, the tape reader motor and tape winder motor must be manually turned on, and the tape reader manually started. To manually energize these motors, the auto-manual switch must be in the MANUAL position. The respective motor switches may then be operated to their ON position. The tape reader is started by first loading the reader with tape, and then operating the run-stop switch to the RUN position.

5.40 Full duplex operation with the 202B data set is available when the transmit-receive selector switch is in the TEST position.

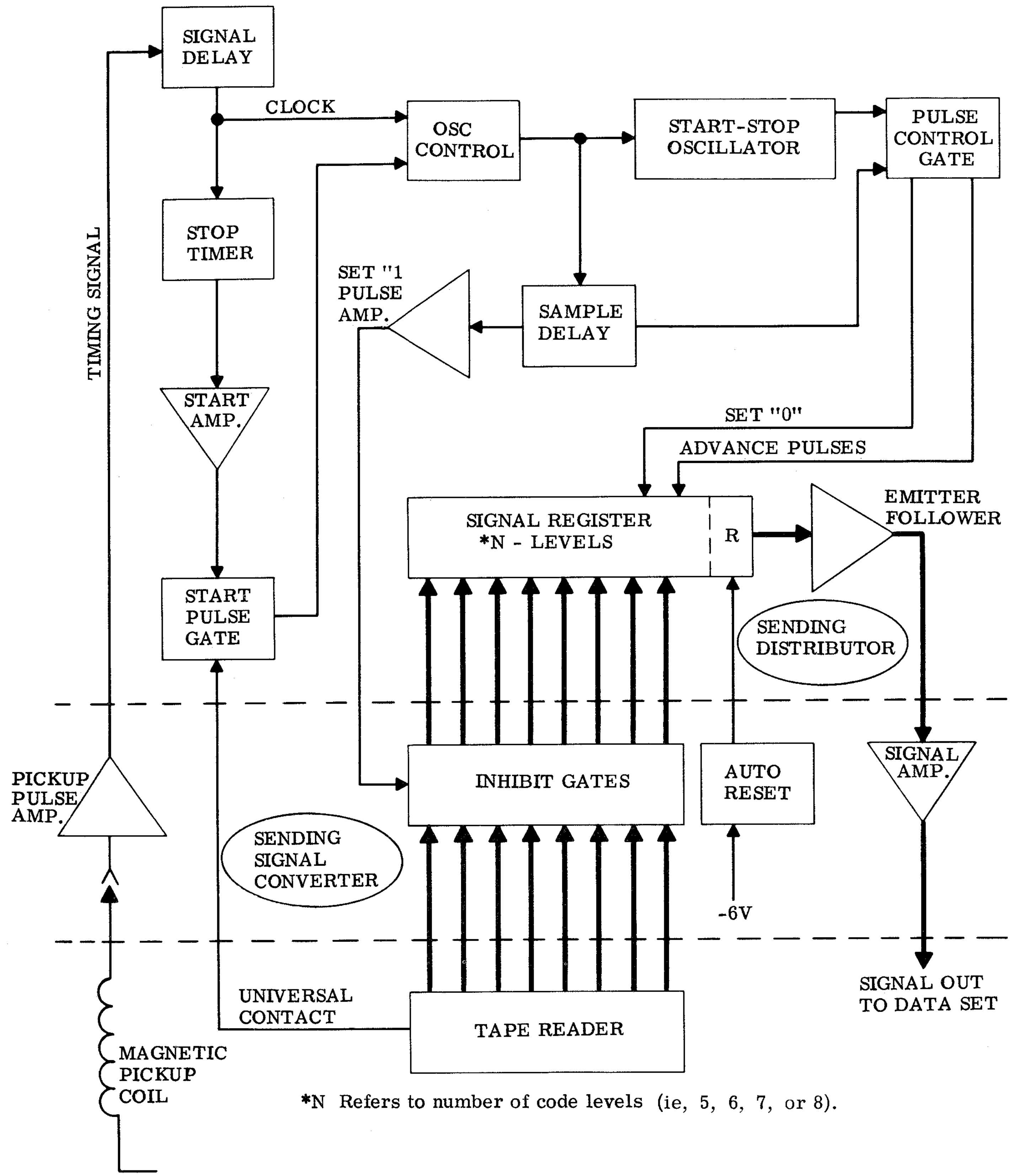


Figure 2 - Tape Sender Block Diagram

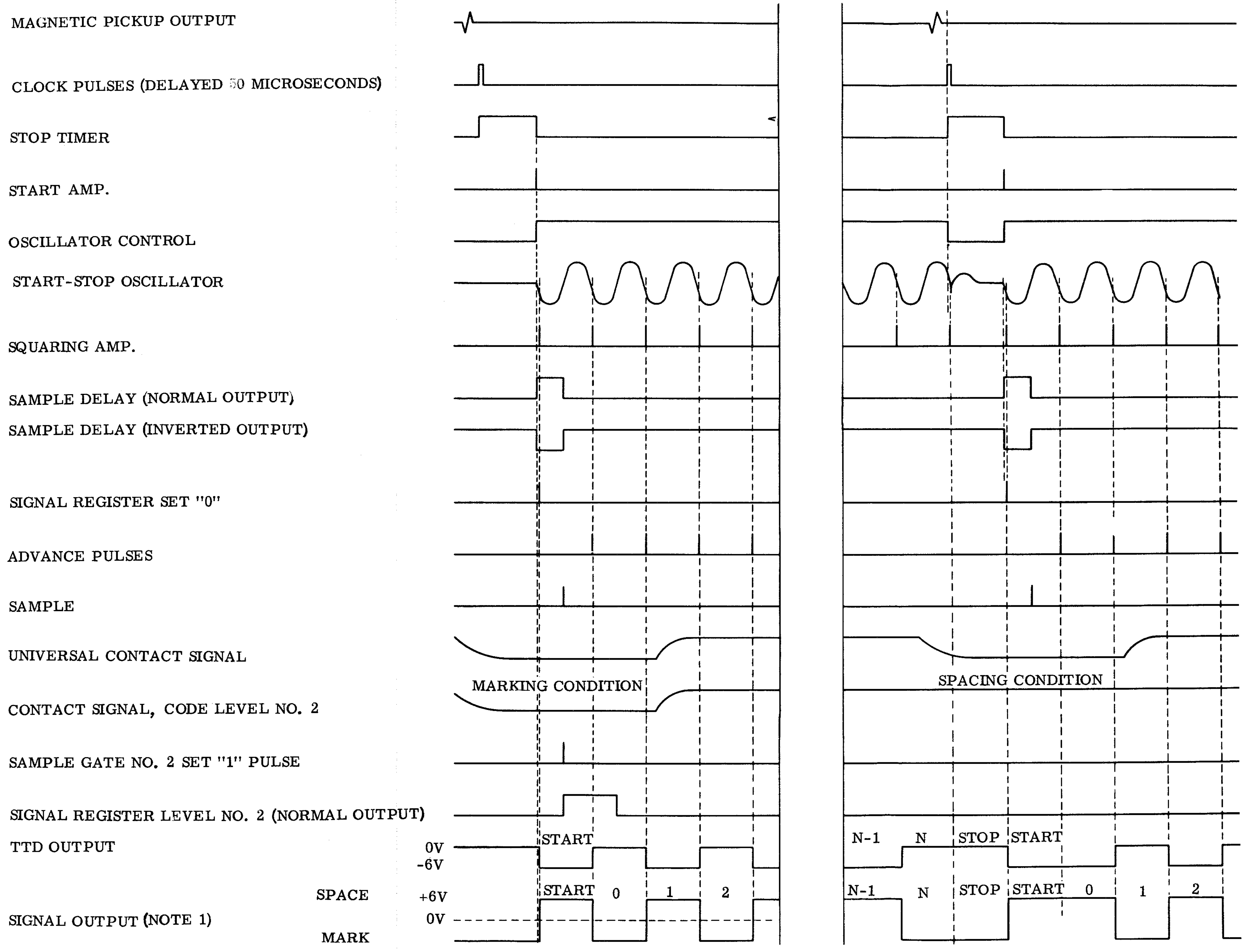
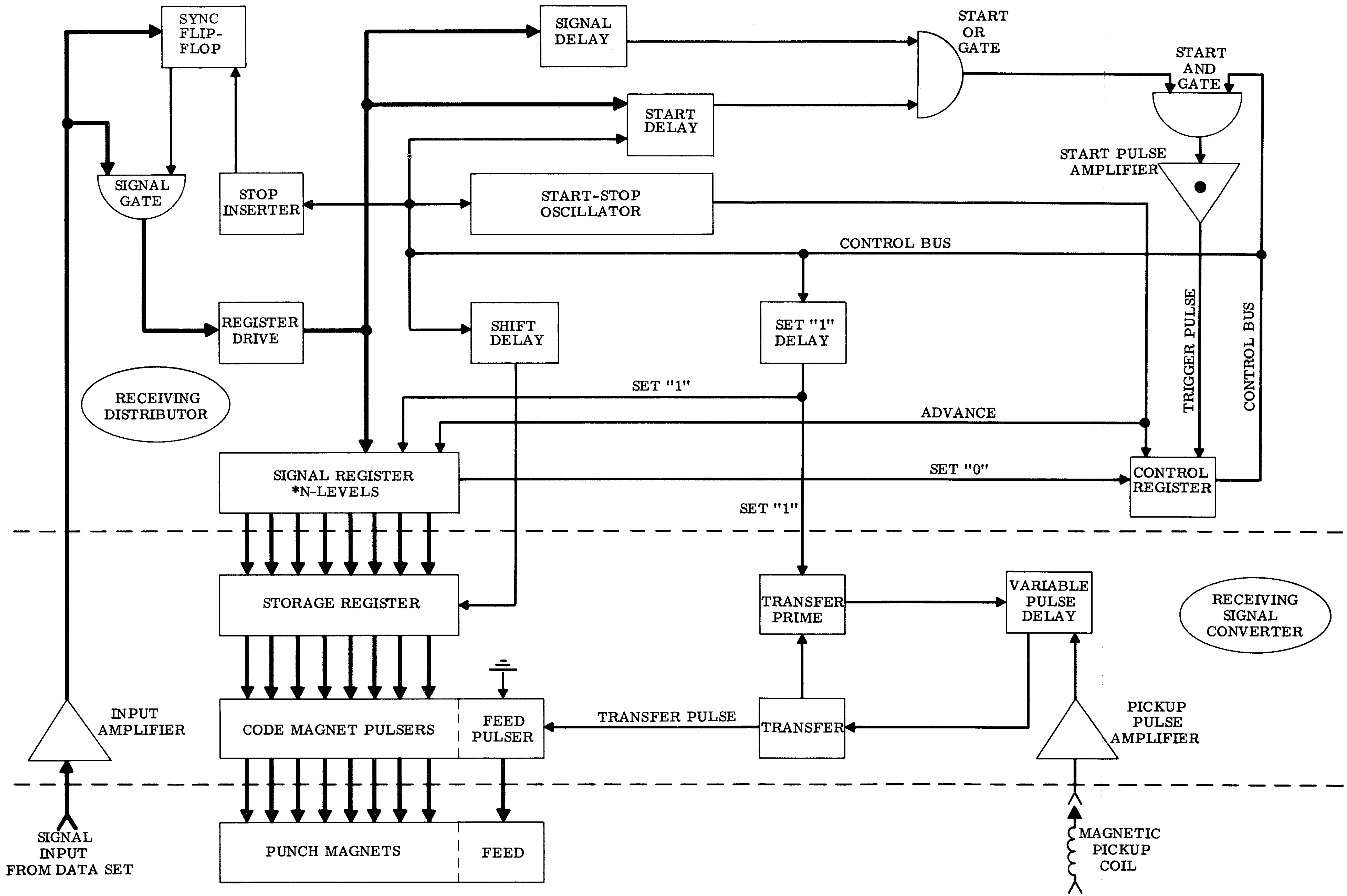


Figure 3 - Tape Sender Timing Diagram

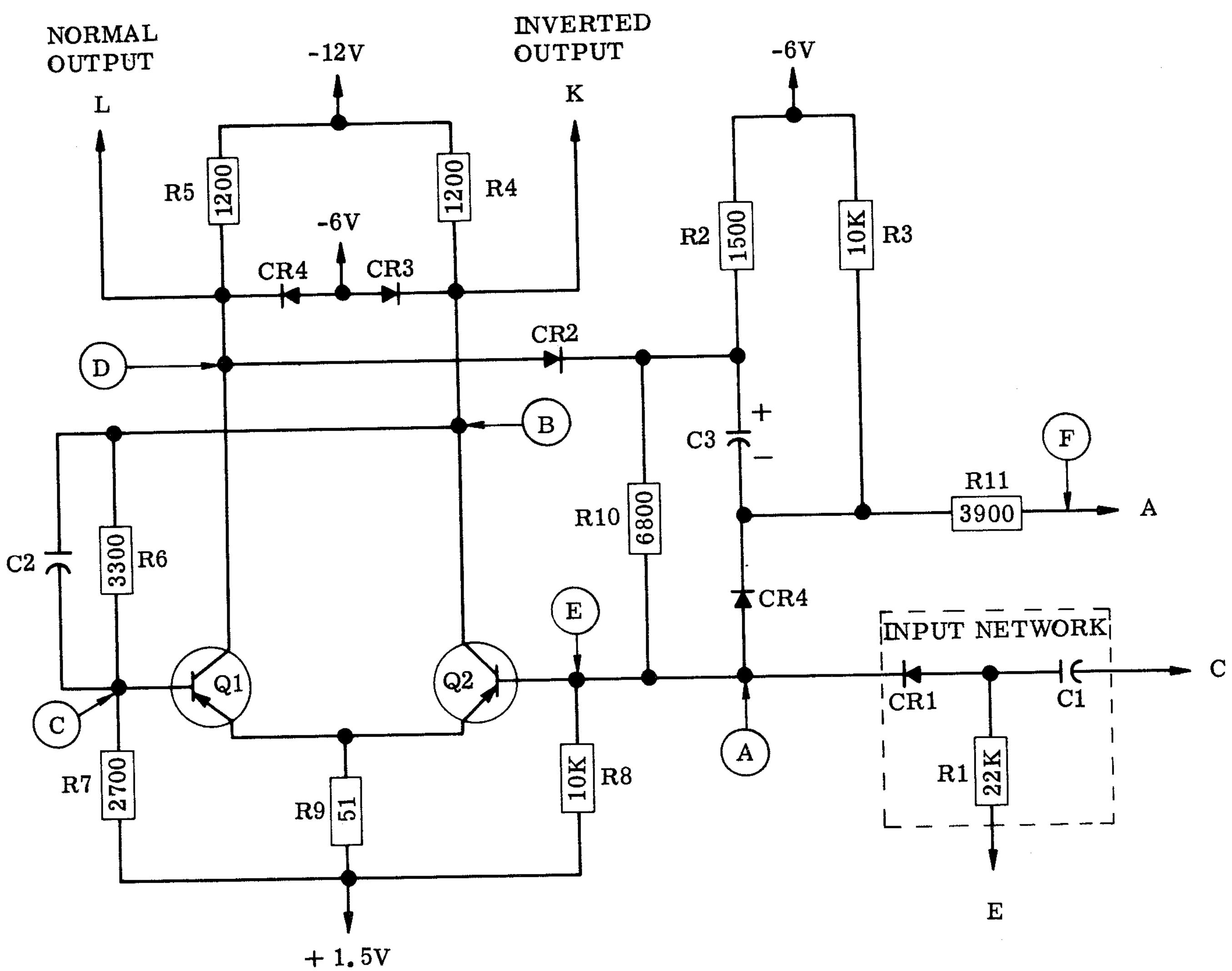
NOTE 1: BIT WIDTH

BAUD	OSCILLATOR FREQUENCY	BIT WIDTH MILLISECONDS
600	600 CPS	1.66
750	750 CPS	1.33
900	900 CPS	1.11
1050	1050 CPS	0.95

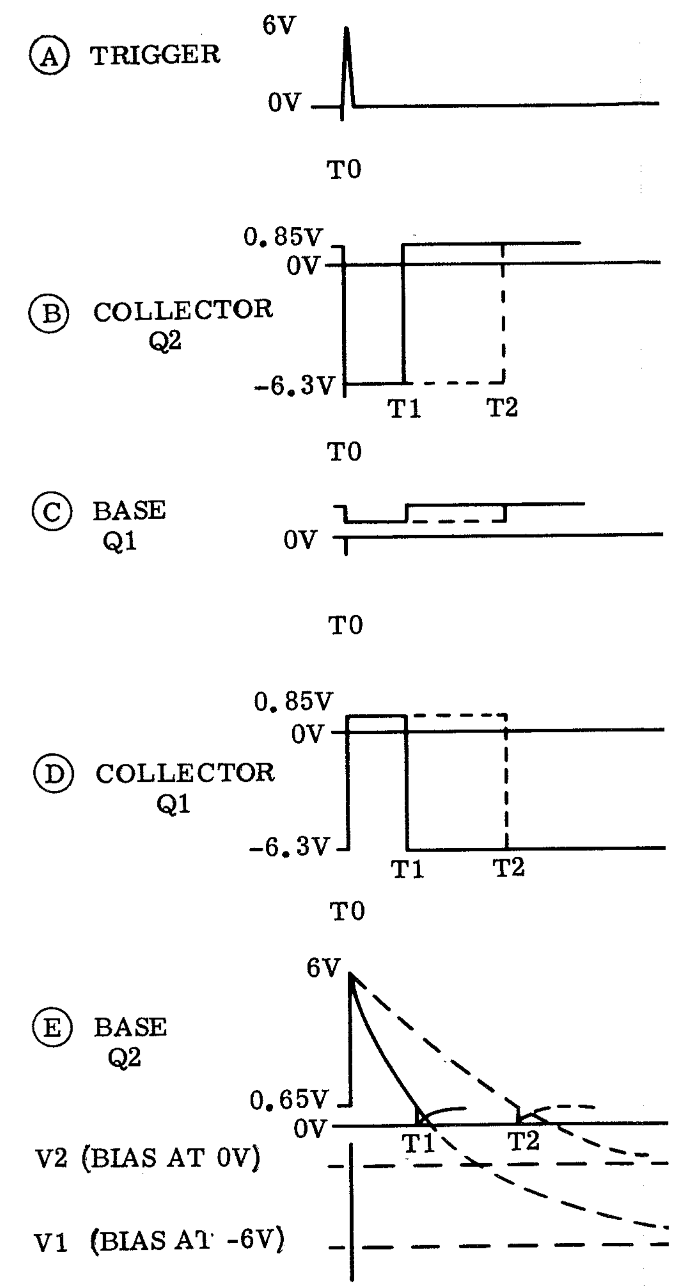


*N REFERS TO NUMBER OF CODE LEVELS (IE, 5, 6, 7 OR 8).

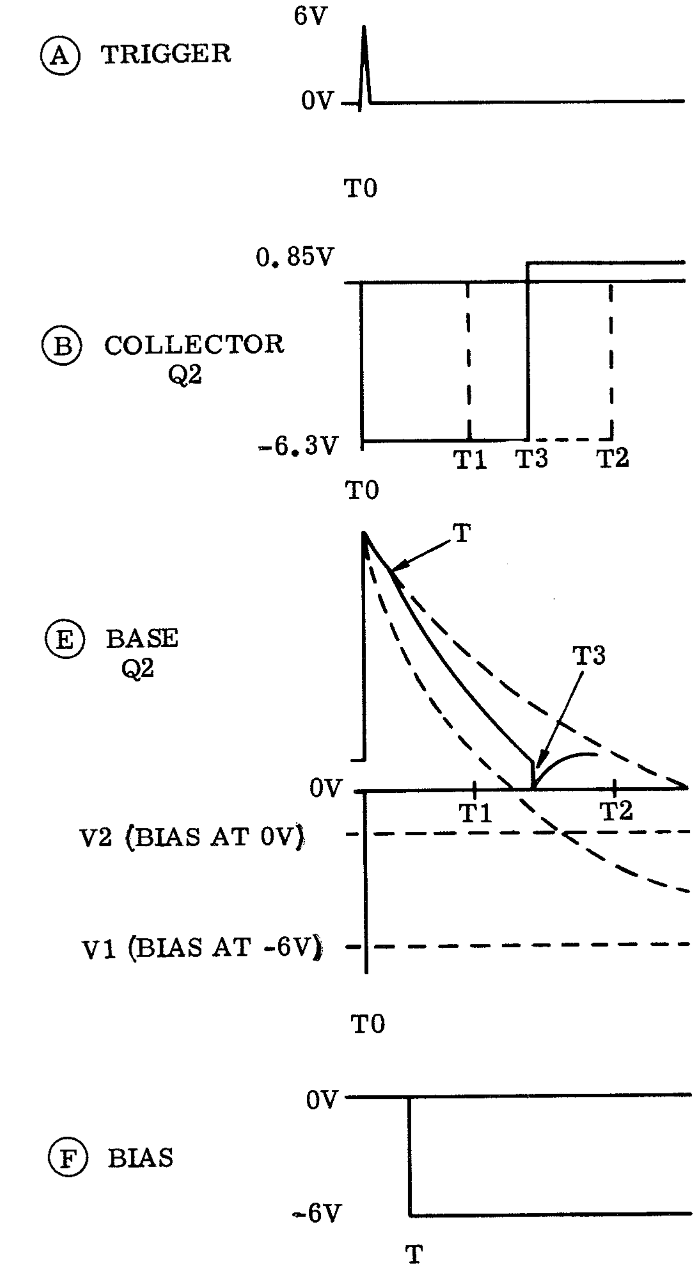
Figure 4 - Tape Receiver Block Diagram



(A) Variable Pulse Delay Circuit



(B) Variable Delay Waveforms, Fixed Bias Condition



(C) Variable Delay Waveforms, Variable Bias Condition

Figure 5 - Variable Pulse Delay

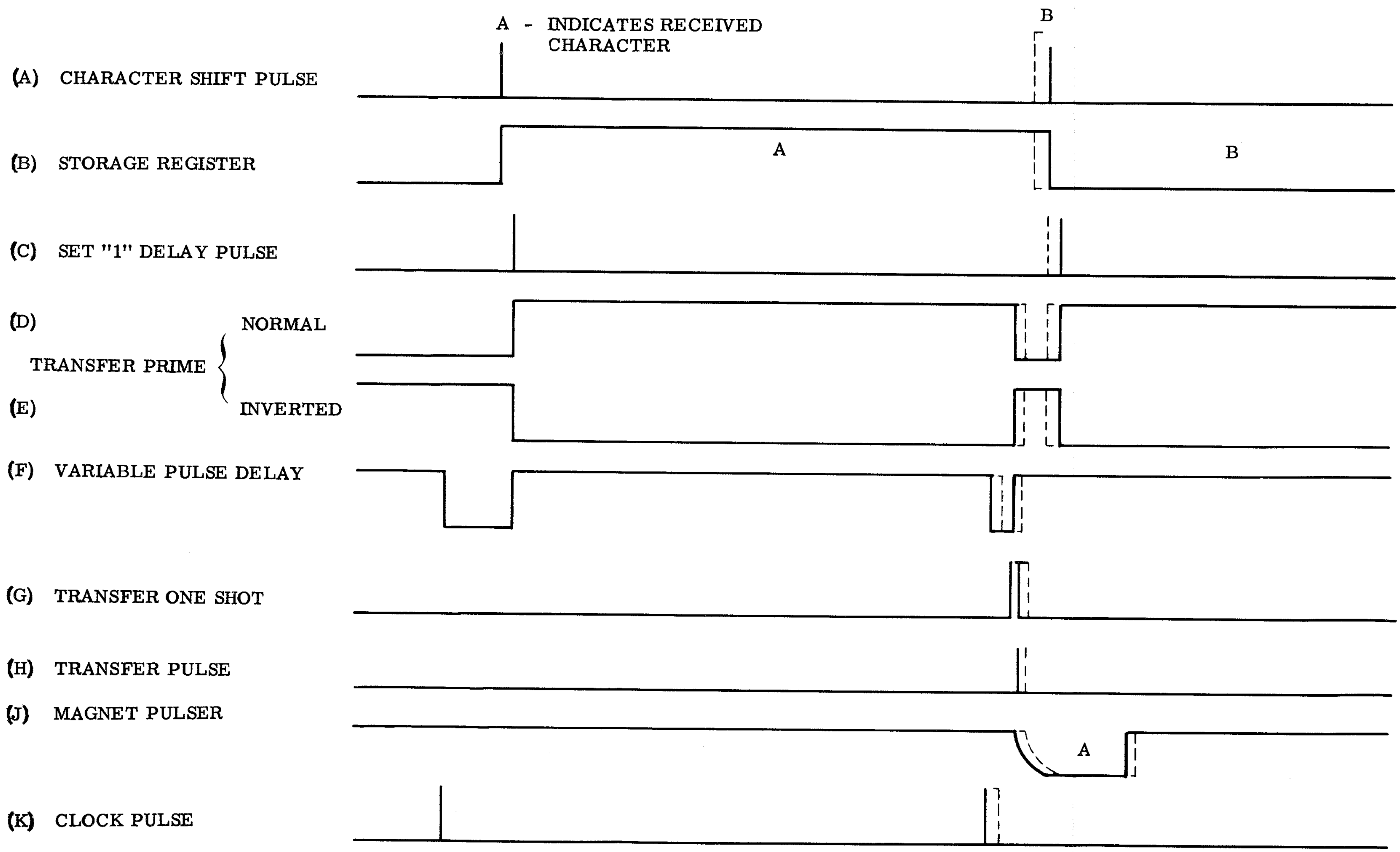


Figure 6 - Transfer Circuitry Timing Diagram, One Cycle of Operation

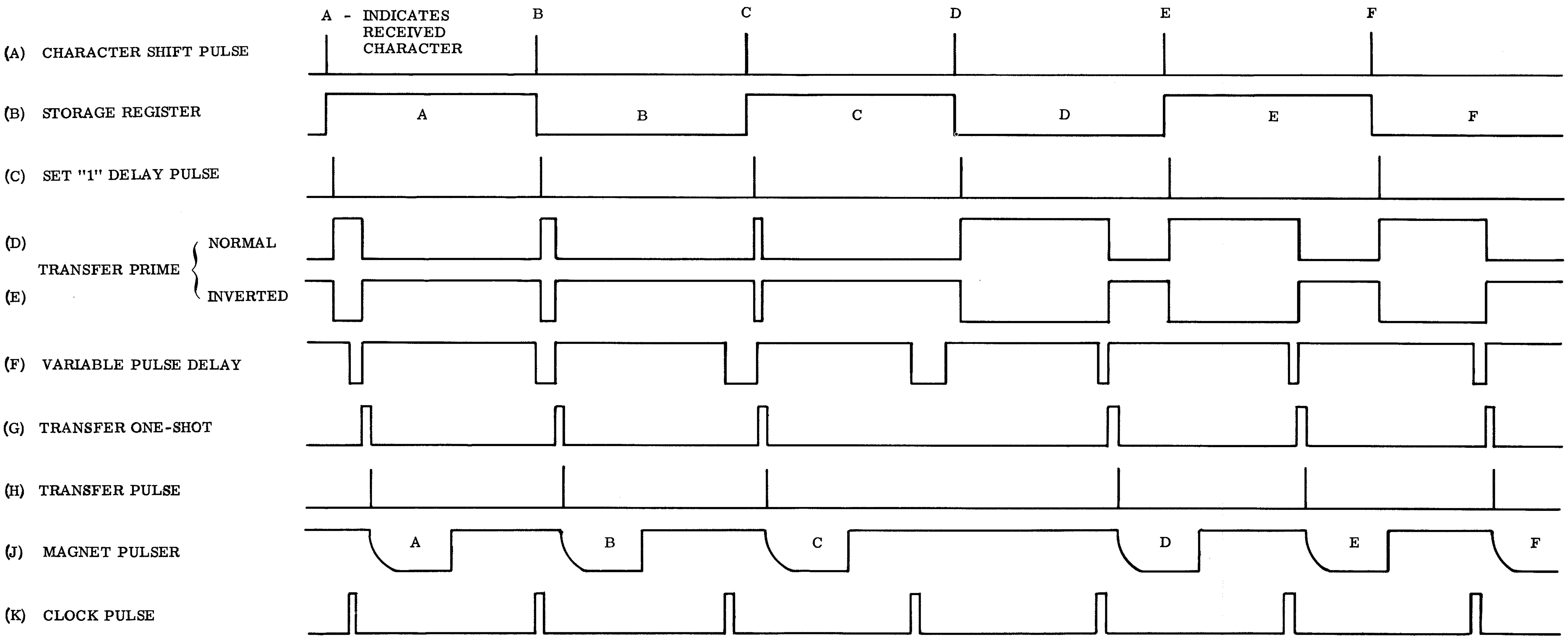


Figure 7 - Transfer Circuitry Timing Diagram, Several Cycles of Operation

NOTE 1: BIT WIDTH

BAUD	OSCILLATOR FREQUENCY	BIT WIDTH MILLISECONDS
600	600 CPS	1.66
750	750 CPS	1.33
900	900 CPS	1.11
1050	1050 CPS	0.95

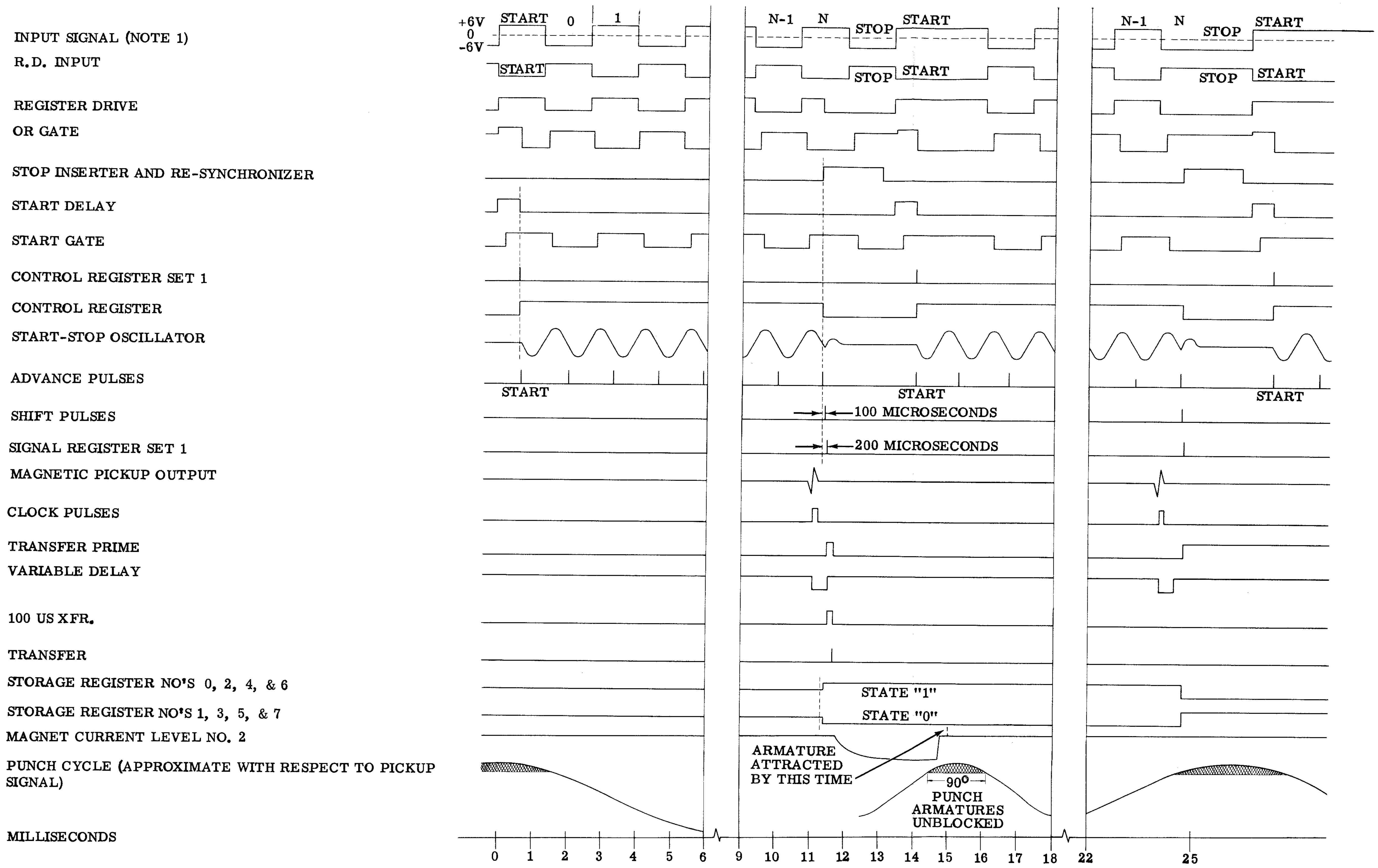


Figure 8 - Tape Receiver Timing Diagram

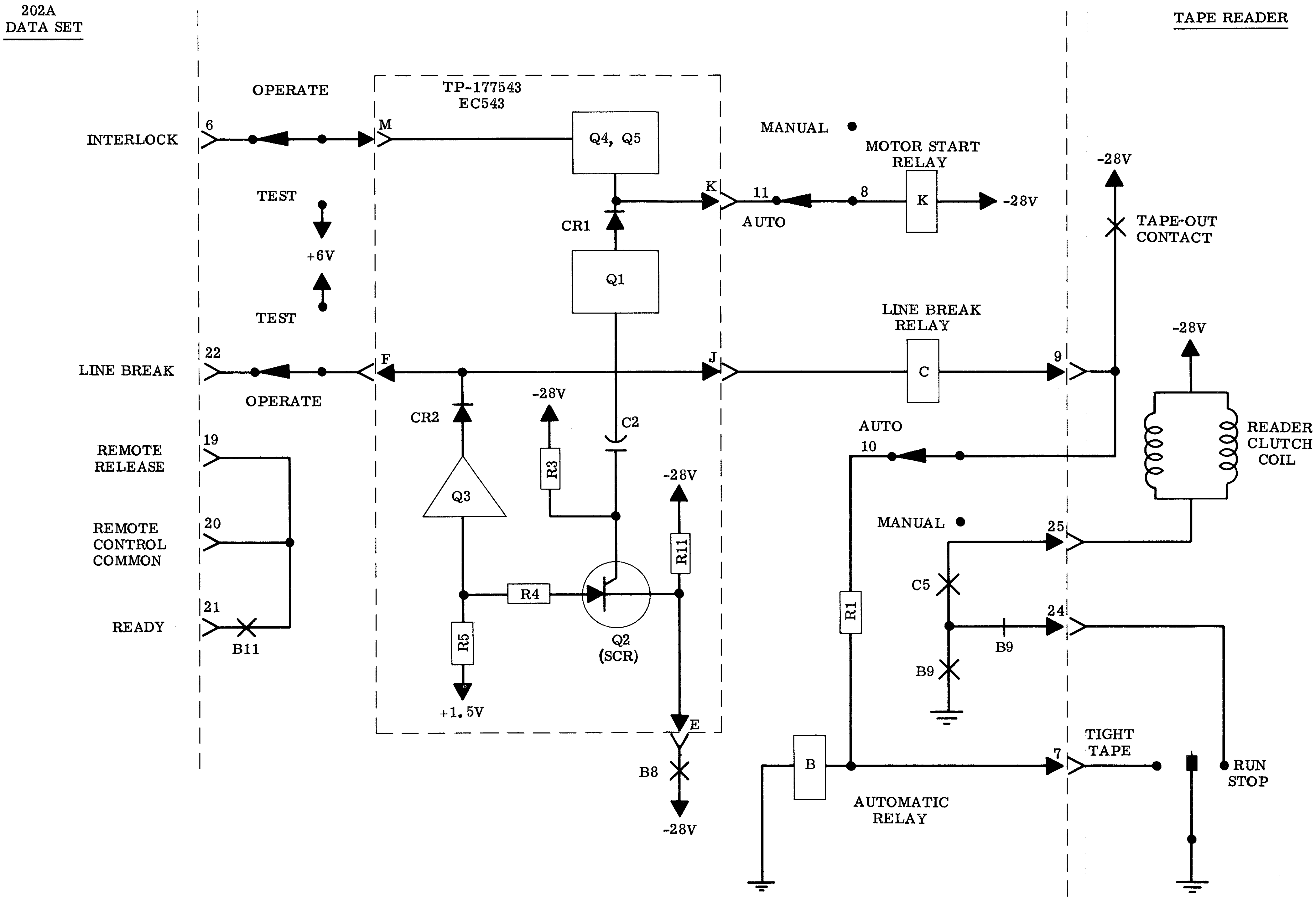


Figure 9 - Interim Unattended Answer Circuit

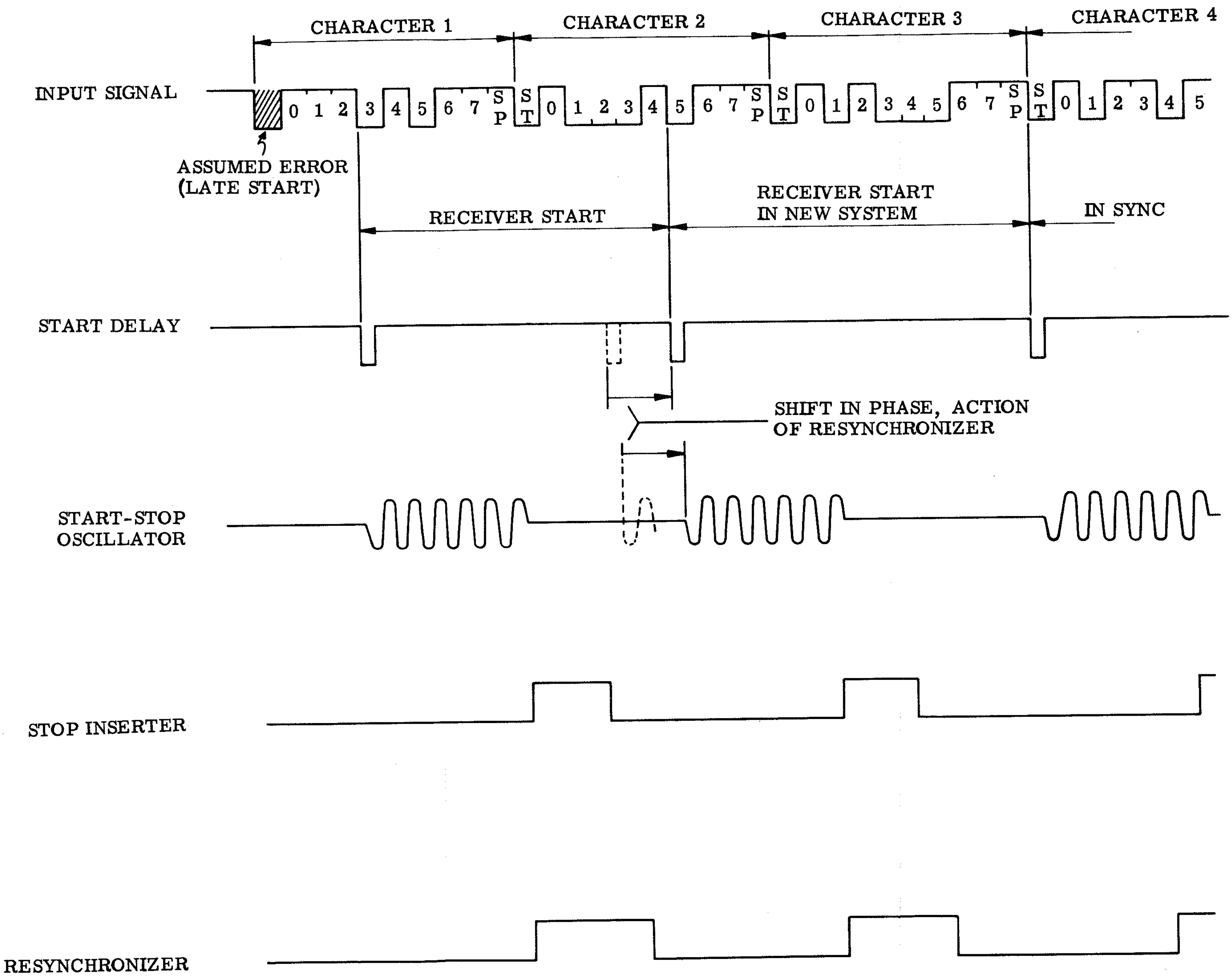


Figure 10 - Resynchronizer Circuit
Timing Diagram