Specification 62979S
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SECTION I

GENERAL TECHNICAL DATA

1. FEATURE DESCRIPTION

The 6542 Communications Controller (Mini) provides a low cost connection to a host computer for up to 8 PCM type terminals using synchronous protocols. A 6542 system includes the base card, zero to two ***expansion*** cards, and zero to one ***option*** card. The expansion and option cards are user installable upgrades. These are described in more detail in section 5. The hardware features of the basic unit and expansion cards are described below. An option card, if used, may provide additional connectivity.

1.1 Terminal Ports

The minimum 6542 configuration provides 4 ports for PCM devices. These ports use TPC connectors, allowing use of either RG62A/U coaxial cabling or IBM twisted pair (types 1, 2 or 3). A maximum cable length of 5000 feet is allowed when coaxial cabling is used. Twisted pair of types 1 or 2 may extend up to 3280 feet, while type 3 may extend up to 1000 feet. The addition of the Coax Expansion Card provides an additional 4 identical ports. A coax multiplexer such as the 6599 may alternately be used to acquire the full 8 ports. Other types of terminals may be supported by adding an option card; the type supported is determined by which type of option card is selected.

1.2 Host Port

A host port using a DB-25 connector is provided to support synchronous traffic. It may function as either an EIA-232 port or a V.35 port. The selection between the two is accomplished using a jumper block on the base card (see section V). The V.35 option requires an adaptor cable to connect to standard V.35 equipment.

1.3 Diagnostic Port

A second DB-25 connector functions as the system diagnostic port. This port is used for system diagnostics and may be used to perform remote station manager functions. It will support baud rates of 1200 and 9600 maintaining class A operation.

1.4 Microfloppy Disk Drives

The 6542 hardware will support either one or two microfloppy disk drives. These drives use 3.5" diskettes with a formatted capacity of 1.44Mbytes each. The drives are used for software downloading and will allow an unattended reboot in the case of a temporary power outage.

1.5 Control Panel

Operator controls are located on a control panel on the front of the unit. This control panel consists of four membrane switches and six LED displays. The switches and their intended functions are described below:

- SELF-TEST: The self-test switch, when depressed, issues a hardware reset to the system. After the reset, the 6542 immediately enters self test, executing a detailed ROM-based test of the system hardware. During the test, the self-test LED flashes indicating that the test is in progress. At the end of the test, this LED will stop flashing, indicating that the test is complete. If the LED is on continuously after the test, then the controller has passed. If the LED is off continuously, then the controller has failed. The function of the self-test switch may be masked by software during disk writes and when the controller is on line. If the controller is on line, a self test may be initiated anyway by pressing the off line switch and the self-test switch simultaneously. If the switch is masked because of a disk write, self-test may not be initiated until the write is complete to prevent disk damage.
- PROGRAM LOAD: The Program Load switch also issues a hardware reset when depressed. After the reset, the 6542 attempts to read the code from the microfloppy. It will continue to attempt to read from either drive until it succesfully loads code or until it is interrupted by a reset. The function of the program load switch may be masked by software during disk writes and when the controller is on line. If the controller is on line, a program load may be initiated anyway by pressing the off line switch and the program load switch simultaneously. If the switch is masked because of a disk write, program load may not be initiated until the write is complete to prevent disk damage.
- ON LINE: The On Line switch issues an interrupt to the microprocessor when pressed. It is intended to be used to indicate to the code that the controller should go "on-line" to the host.
- OFF LINE: The Off Line switch issues an interrupt to the microprocessor when pressed. It is intended to be used to indicate to the code that the could controller should go "off-line" from the host.

The control panel LEDs and their meanings are similarly described below:

- SELF-TEST: The self-test LED is used to report the status of the ROM-based system test. It only has meaning during and immediately after self test. During self test it flashes on and off to indicate that the test is in progress. After self test, it reports the results by staying on continuously for a pass and going out for a fail.
- OFF LINE: The off-line LED is used to indicate whether the controller is on or off line. The LED is on when the controller is off line, and the LED is off when the controller is on line.
- ACTIVE: The active LED is used to indicate that the software is running. It must be written to every half second to remain on. If the software gets hung up, it will not write to this LED and it will go out, indicating that the controller is no longer executing code properly.
- POWER: This LED is on whenever the 6542 has power applied and the power switch is on.
- SEND: This LED is used to indicate activity on the synchronous host port. It is on whenever the controller is sending data out that port.
- RECEIVE: This LED is used to indicate activity on the synchronous host port. It is on whenever the controller is receiving data from that port.

1.6 Power Requirements

The 6542 may be ordered in versions using either U.S. or European voltage ranges.

2. PHYSICAL DESCRIPTION

Figure I-1a shows the 6542 Communications Controller. It is a "table top" unit, designed to fit on the shelf of a 19 inch rack. The outside dimensions are LL" x WW" x HH", with a weight of approximately NN pounds with a full compliment of option cards. The door in the center of the front panel, when closed, covers the microfloppy disk drive and allows the power LED to be seen through the back of the door. The other control panel LEDs and the control panel switches are found on the inside surface of the door. The layout of these is shown in figure I-1b, a view of the inside surface of the door. The power cord and all communications cables plug into the back of the unit, shown in figure I-1c. This figure shows an Asynchronous Port Option Card present in the option card slot. If a different option card is installed, the option card ports may look different.

3. ENVIRONMENTAL DATA

The 6542 Communications Controller requires the following environmental conditions to be maintained:

3.1 Temperature/Humidity

TABLE I-1. Temperature and Humidity Limits

Device	Temperature (Operating)	Temperature (Non-Operating)	Humidity (non-condensing)
Controller	+4c to +38c	-40c to +60c	5 to 95%
Floppy disk media	+4c to +38c	-40c to +60c	20 to 80%

Operation outside the disk media humidity range may result in higher disk read errors.

3.2 Electromagnetic Susceptibility

3.2.1 Fields

The controller will remain operational in the presence of electromagnetic fields with strengths up to 3 volts/meter and frequencies from 10 Khz to 1 Ghz.

3.2.2 Electrostatic Discharge

TABLE I-2. Electro-Static Discharge Effects

Voltage	Effect
4,000V	No observable effect
8,000V	5% soft errors with automatic recovery, no permanent damage
15,000V	25% soft errors, no permanent damage

3.3 Altitude

TABLE I-3. Altitude Limits

Device	Altitude (Operating)	Altitude (Non-operating)
Controller	-1,000 to 14,000 ft	-1,000 to 30,000 ft

4. OPTIONAL COMPONENTS

The following are user installable parts used to upgrade a 6542 system.

4.1 RAM Expansion Card

The 6542 base system contains 1.5Mbytes of dynamic RAM. For configurations which require more RAM, the RAM Expansion Card is used to add an additional 0.5Mbytes of dynamic RAM. This is a user installable option. The configurations requiring additional RAM will be specified by the software groups.

4.2 Coax Expansion Card

The 6542 base system provides 4 TPC coaxial ports. An additional 4 ports may be added by using the Coax Expansion Card. This is a user installable option.

4.3 Asynchronous Port Option Card

Each 6542 system may include up to one option card. If the Asynchronous Port Option Card is used, the 6542 will acquire two EIA-232 ports for asynchronous operation. This is a user installable option.

Figure I-1. The 6542 Communications Controller

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. OVERVIEW

The 6542 Mini Controller contains two devices capable of executing stored programs, thus naturally dividing the logic into two sets of processors and peripherals. These devices are the master processor, an Intel 80C186, and the slave processor, a Coax Micro-Controller.

1.1 80C186 Microprocessor

The main processing and control functions are carried out by the 80C186 acting upon the following peripherals:

1.1.1 EPROM

32K of EPROM is mapped into the top 32K of address space. This may be expanded to 64K if necessary.

1.1.2 Main RAM

The first 512K of address space is mapped to 512K of DRAM, which is the main RAM for the 80C186.

1.1.3 Paged RAM

1Mbyte of paged RAM is included on the basic unit; this may be expanded to 1.5M by adding the RAM Expansion Card. This RAM is accessed through two 128K windows in 80C186 address space. The base of each of these windows may be moved, in 64K steps, through the entire paged RAM region.

1.1.4 Dual Port RAM

8K of SRAM is dual ported to allow access by either the Coax Micro-Controller or the 80C186. This is directly mapped into 80C186 address space.

1.1.5 Control Panel

The control panel consists, electrically, of 4 switches and 6 LEDs. There is a Program Load switch, a Self Test switch, an On-Line switch, and an Off-Line switch. Any switch closure is latched until cleared under program control. The LEDs are labeled Power, Test, Active, Off Line, Send, and Receive.

1.1.6 Microfloppy Disk Drives

Using a Western Digital 37C65B floppy disk controller, either one or two 3.5" microfloppy drives are supported in the high density mode. This yields 1.44Mbytes of data space per disk.

1.1.7 Serial Ports

Two serial communication ports are supported by an 8530 Serial Communications Controller (SCC).

1.1.7.1 EIA/V.35 Port

Port 0 may be optioned as either an EIA-232 port or a V.35 port by setting jumper plugs on the base board. (V.35 operation requires an adapter cable also) It is intended to be used as a synchronous host port.

1.1.7.2 Diagnostic Port

Port 1 is designed to support asynchronous operation at either 1200 or 9600 baud using an EIA-232 interface. It may also be optioned, under program control, to support synchronous operation.

1.2 Coax Micro-Controller (CMC)

The Coax Micro-Controller acts as a slave processor to handle the coax line interface utilizing the following peripheral devices:

1.2.1 Program RAM

8K of SRAM is provided in a 4K x 16 configuration for CMC code. This RAM must be downloaded by the 80C186 before use.

1.2.2 Dual Port RAM

8K of SRAM is dual ported to allow access by either the Coax Micro-Controller or the 80C186.

1.2.3 FIFO Buffer

A 64 x 8 FIFO buffer is provided between the CMC and the 80C186. The CMC may write to the FIFO directly as one of its external registers. Any data in the FIFO generates a hardware interrupt to the 80C186, which may read the FIFO as an I/O port.

1.2.4 Coax Interface Ports

4 coax ports are accessible by the CMC in a time multiplexed fashion in the basic unit (with no option cards).

1.2.5 Coax Expansion Card

If the Coax Expansion Card is present, the CMC may access a total of 8 coax ports, with the additional 4 residing on the option card.

1.3 Option Card Interface

In addition to having two connector interfaces dedicated to the to previously mentioned expansion cards (Coax Expansion Card and RAM Expansion Card), the 6542 Base Card has a general purpose connector interface to support one of the following option cards:

1.3.1 Asynchronous Port Option Card

The Asynchronous Port Option Card provides an additional 8530 SCC and two more EIA-232 ports configured for asynchronous operation only.

1.3.2 CDB Development Option Card

This card is identical to the Asynchronous Port Option Card, but has been optioned as a software debugging aid. This option card is for use by developers only.

2. PROGRAMMING INFORMATION

2.1 80C186 Programming

2.1.1 Memory Map

Table II-1 represents the memory address space of the 80C186. Each region is described in the following paragraphs.

2.1.1.1 EPROM (0xf0000 - 0xfffff)

The upper 64K of address space is reserved for EPROM. If only 32K of EPROM is installed, it will occupy the upper 32K of address space, leaving the lower 32K of EPROM space unused.

2.1.1.2 Dual Ported RAM (0xe0000 - 0xe1000)

The 8K of dual ported RAM may be accessed sequentially by the 80C186 starting from address 0xe0000. It will support byte reads and writes, but no word operations. The address space following this 8K through the start of EPROM is also mapped into this same 8K of memory. Reads or writes to that area will not produce a watchdog timeout, though it is an invalid address range.

2.1.1.3 Main RAM (0x00000 - 0x7ffff)

The first 512K of address space is mapped to 512K of DRAM operating with zero wait states.

2.1.1.4 Paged RAM Windows (0x80000 - 0xbffff)

The first window into the paged RAM, called the low window, extends from address 0x80000 through address 0x9ffff. The high window extends from address 0xa0000 through address 0xbffff. These windows may be placed on 32K boundaries through the entire paged RAM region using the Page Register (see section 2.1.2.2). Both of these windows operate with zero wait states.

2.1.2 I/O Map

The following table shows the I/O space of the 80C186. The used sections are described in the following paragraphs.

TABLE II-1. Memory Map

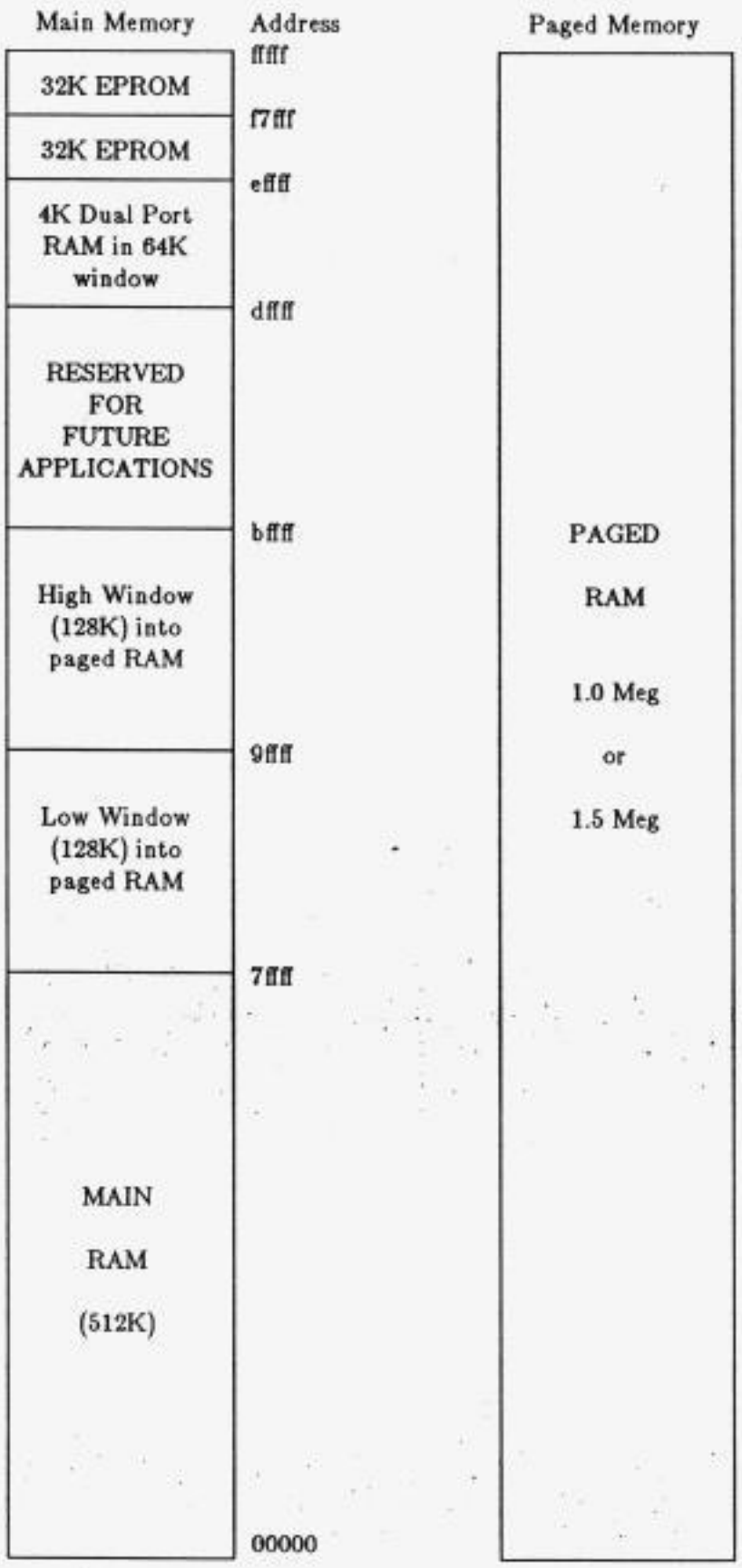

TABLE II-2. I/O Map

Range	Subrange	Address	Name
80C186 Control	Relocation	0xfffe	Relocation
	Power Save	0xfff0	Power Save Control
	Refresh Control Unit	0xffe0	MDRAM (Memory Partition)
		0xffe2	CDRAM (Clock Pre-Scaler)
		0xffe4	EDRAM (Enable RCU)
	DMA Channel 1	0xffda	Control Word
		0xffd8	Transfer Count
		0xffd6	Destination Pointer
		0xffd4	Destination Pointer
		0xffd2	Source Pointer
		0xffd0	Source Pointer
	DMA Channel 0	0xffca	Control Word
		0xffc8	Transfer Count
		0xffc6	Destination Pointer
		0xffc4	Destination Pointer
		0xffc2	Source Pointer
		0xffc0	Source Pointer
	Chip Select Control	0xffa8	MPCS
		0xffa6	MMCS
		0xffa4	PACS
		0xffa2	LMCS
		0xffa0	UMCS
	Timer 2	0xff66	Mode/Control
		0xff62	Max.Count A
		0xff60	Count
	Timer 1	0xff5e	Mode/Control
		0xff5c	Max.Count B
		0xff5a	Max.Count A
		0xff58	Count
	Timer 0	0xff56	Mode/Control
		0xff54	Max.Count B
		0xff52	Max.Count A
		0xff50	Count
	Interrupt Controller	0xff3e	INT3 Control
		0xff3c	INT2 Control
		0xff3a	INT1 Control
		0xff38	INT0 Control
		0xff36	DMA1 Control
		0xff34	DMA0 Control
		0xff32	Timer Control
		0xff30	Interrupt Status
		0xff2e	Interrupt Request
		0xff2c	In-Service
		0xff2a	Priority Mask
		0xff28	Mask
		0xff26	Poll Status
		0xff24	Poll
		0xff22	EOI

Range	Subrange	Address	Name
OPEN	0x2380-0xfeff		
PCS Region	PCS6	0x2300	Card Type
	PCS5(CMC)	0x22c0	FIFO
		0x22b0	Address Bus
		0x2a0	WritePS
		0x2290	Instruction Bus
		0x2289	PSOff
		0x2288	PSOn
		0x2287	ILOn
		0x2286	ILOff
		0x2285	StepOn
		0x2284	StepOff
		0x2283	HaltOff
		0x2282	HaltOn
		0x2281	ResetOff
		0x2280	ResetOn
	PCS4	0x2250	Control/Status
		0x2248	Switches(R)/Active LED(W)
		0x2240	Clear Panel(R)/LEDs(W)
		0x2220	Page
	PCS3		not used
	PCS2(FDC)	0x210e	DMA Data
		0x210a	Control
		0x2106	Operations
		0x2102	Data
		0x2100	Status
	PCS1		option card defined
	PCS0(SCC)	0x2040	EIA Status
		0x2006	Channel A Data
		0x2004	Channel A Command
		0x2002	Channel B Data
		0x2000	Channel B Command
OPEN	0x0100 - 0x1fff		
Intel Reserved	0x00f8 - 0x00ff		
OPEN	0x0000 - 0x00f7		

2.1.2.1 80C186 Internal Integrated Peripheral Control Registers

Requirements for the use of the Peripheral Control Registers in the 80C186 are outlined below.

2.1.2.1.1 Relocation Register

The value in the Relocation Register determines the location of the control block of registers. Upon reset this block is located from 0xff00 to 0xffff in I/O space. All following discussion assumes that this block is not moved. A reset also initializes this register such that the interrupt controller is in master mode, which must not be changed for proper operation of the interrupt controller, and ESC traps are inhibited. If ESC traps are desired, a write of 0xa0ff will enable them. To return to the reset state of the register, write 0x20ff. The address of this register is 0xfffe.

2.1.2.1.2 Chip Select Registers

There are 5 registers that control the operation of the 80C186 memory and peripheral chip selects. Three of these need to be initialized for proper access to memory and peripherals, as outlined below:

TABLE II-3. Chip Select Registers

Address	Register	Value	Conditions
0xffa0	UMCS	0xf83e	for 32K of EPROM
0xffa0	UMCS	0xf03e	for 64K of EPROM
0xffa2	LMCS	--------	unused
0xffa4	PACS	0x0239	
0xffa6	MMCS	--------	unused
0xffa8	MPCS	0x81b8	

UMCS must be initialized before using EPROM addresses below 0xffc00. The others must be initialized before using I/O addresses from 0x2000 through 0x237f.

2.1.2.1.3 RAM Refresh

Three registers must be initialized with the values shown below to start the RAM refresh for the main and paged RAM.

TABLE II-4. Refresh Control Registers

Address	Register	Value	Conditions
0xffe0	MDRAM	0x0000	
0xffe2	CDRAM	0x00bd	
0xffe4	EDRAM	0x8000	to enable refresh
0xffe4	EDRAM	0x0000	to disable refresh

EDRAM should be written last. After a reset, 8 RAM cycles are required before RAM can be trusted. These can be refresh cycles or reads or writes or any combination thereof, but reads and writes will not necessarily yield correct data. The refresh cycles are set to occur every 15.2 microseconds, so a wait of 150 microseconds after enabling the refresh counter will be sufficient to initialize the RAM.

2.1.2.1.4 Timers (Watchdog Timeout)

Two of the three timers on the 80C186 are available for software and firmware general purpose use. Timer 0, however, is used as the watchdog timer. It is reset at the start of every bus cycle, and will time out if another cycle does not begin within approximately 10 microseconds. When it times out, it sends a ready signal to the 80C186, ending the bus cycle. This will prevent the processor from locking up on an invalid memory or I/O access. The watchdog timeout period must be smaller than the RAM refresh period or refresh problems may occur. The watchdog timer may be set up to interrupt the processor on a timeout or not to interrupt, in which case it

must be polled to determine whether it has timed out. Initialization requires the Timer 0 registers to be set as shown:

TABLE II-5. Watchdog Timer Registers

Address	Register	Value	Conditions
0xff50	Count	--------	do not ever write
0xff52	Max.Cnt.A	0x0020	
0xff54	Max.Cnt.B	--------	not used
0xff56	Mode/Cntrl	0xc011	enable with no interrupt
0xff56	Mode/Cntrl	0xe011	enable with interrupt
0xff56	Mode/Cntrl	0x4011	disable

The Max Count A register must be initialized first. After that, the watchdog may be enabled or disabled simply by writing the appropriate value to the Mode/Control register.

2.1.2.1.5 Interrupts

The interrupt controller handles interrupts from several devices as shown below:

TABLE II-6. 80C186 External Interrupts

Channel	Devices Served
Int 0	Base Card SCC + Option Card Zbus interrupts
Int 1	CMC FIFO
Int 2	Acknowledge for Int 0
Int 3	Control Panel, Floppy Controller, and Option Card
NMI	Option Card

These interrupts may be configured as desired providing that Int 0 is always in cascade mode and all interrupts are level triggered.

2.1.2.1.6 DMA Control

The two DMA channels are allocated as follows:

TABLE II-7. 80C186 External Interrupts

Channel	Devices Served
DMA Channel 0	Base Card SCC or Option Card
DMA Channel 1	Floppy Controller or Option Card

The DMA controller may be configured as desired.

2.1.2.1.7 Power Save Control

The power save feature of the 80C186 is not supported by the 6542 hardware. This feature should always be disabled to prevent problems with the dual port RAM control.

2.1.2.2 Page Register (0x2220)

TABLE II-8. Page Register (0x2220)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	H4	H3	H2	H1	H0	X	X	X	L4	L3	L2	L1	L0

Address: 0x2220

H0-H4: (R/W) Page address for high window
L0-L4: (R/W) Page address for low window

The page register contains two 5-bit addresses which determine the portions of paged RAM looked at by the two Paged RAM Windows (see section 2.1.1.4). Each 5-bit address may be set to a value from 0x00 through 0x0f if the RAM Expansion Card is not present, or from 0x00 through 0x17 if the RAM Expansion Card is present. The bottom of the window is mapped into paged RAM at 64K times the value of the page address above the bottom of paged RAM. If the page address is set to the highest allowable value for the amount of memory present, the low half of the window will be mapped to the top of paged RAM while the high half of the window will be mapped to the bottom of paged memory in a wrap-around effect.

2.1.2.3 Control/Status Register (0x2250)

TABLE II-9. Control/Status Register (0x2250)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	DI	OI	PI	FI	RE	CE	LB	MR	DS	RO	RF	RS

Address: 0x2250

RS: (R/W) SCC Reset, Active Low

A zero written to this position presents a hardware reset to all SCCs in the system. A one removes the reset. This bit must remain low for at least 6 clock cycles to ensure a valid reset. After reset is removed, no accesses are allowed for 12 clock cycles. This recovery time must be provided for in software/firmware. This bit is set to zero upon reset.

RF: (R/W) Floppy Disk Controller Reset, Active Low

A zero written to this position presents a hardware reset to the WD37C65 floppy disk controller. A one removes the reset. This bit must remain low for at least 14 microseconds to ensure a valid reset. After reset is removed, no accesses are allowed for 8 microseconds. This recovery time must be provided for in software/firmware. This bit is set to zero upon reset.

RO: (R/W) Option Card Reset, Active Low

A zero written to this position presents a hardware reset to the option card. A one removes the reset. Pulse width and recovery time constraints will depend on which option card is present. See section 7 for details on option cards. This bit is set to zero upon reset.

DS: (R/W) Diagnostic port clock Select

A one in this position allows synchronous operation of the diagnostic port (port B of the base card SCC). A zero in this position presents an 8-MHz clock at pin 28 of the SCC (RTxCB) to provide a clock for asynchronous operation. This bit is set to zero upon reset.

MR: (R/W) Mask Reset, Active High

A one in this position prevents the TEST and PROGRAM LOAD buttons on the control panel from generating a reset when they are pressed alone or with OFF-LINE (they will generate a reset when pressed in conjunction with ON-LINE). This is intended to be used during writes to the microfloppy to prevent disk corruption. This bit is set to zero upon reset.

LB: (W) Reserved

Write only zeros to this location. This has no effect on the loopback flags.

LB: (R) Loopback Flag, Active Low

A zero in this position indicates that the 6542 is in Loopback Test Mode. This bit is reset only when a hardware jumper is placed on the appropriate pack on the base card. It is intended for R&D applications.

CE: (R) Coax Expansion Present, Active Low

A zero in this position indicates that the Coax Expansion Card is present.

RE: (R) RAM Expansion Present, Active Low

A zero in this position indicates that the RAM Expansion Card is present.

FI: (R) Fan Failure Interrupt, Active High

A one in this position indicates that the 6542 is overheating, probably due to a fan failure, and should be turned off. INT3 will be active whenever this bit is set. If this bit is found set, it should be rechecked after XX seconds to verify that it is a true reading. If it is still set, a warning should be issued and the system should shut down within XX minutes.

PI: (R) Control Panel Interrupt, Active Low

A zero in this position indicates that the control panel is requesting an interrupt on INT3 due to a depression of the OFF-LINE or ON-LINE buttons.

OI: (R) Option Card Interrupt, Active Low

A zero in this position indicates that the option card is requesting an interrupt on INT3.

DI: (R) Floppy Disk Controller Interrupt, Active Low

A zero in this position indicates that the floppy disk controller is requesting an interrupt on INT3.

2.1.2.4 Control Panel

Two different I/O addresses are used to access the control panel switches and LEDs. They have different functions for read than for write. Some may be accessed as either 8-bit or 16-bit ports at the programmers discretion. Each port is described below:

2.1.2.4.1 Test and Off-Line LEDs (Write only)

TABLE II-10. Test and Off-Line LEDs (0x2240 write only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	L	T	X	X	X	X	X	X	X	X	X	X

Address: 0x2240 (Write only)

TABLE II-11. Test and Off-Line LEDs (0x2241 write only)

7	6	5	4	3	2	1	0
X	X	X	X	L	T	X	X

Address: 0x2241 (Write only)

T: (W) Test LED, Active High

A one in this position turns the Test LED on; a zero turns the Test LED off.

L: (W) Off-Line LED, Active High

A one in this position turns the Off-Line LED on; a zero turns the Off-Line LED off.

2.1.2.4.2 Control Panel Clear (Read only)

8-bit Address: 0x2241
16-bit Address: 0x2240

A read of one of these addresses clears the control panel latches. These latches are cleared on power up but not on any other reset. If the Program Load or Self-Test latch is being cleared, the following procedure must be followed to prevent a condition where these two switches can not generate a reset. After a read of this address, wait a minimum of 50 microseconds and then read the Control Panel Switches register (see section 2.1.2.4.4). If both the Program Load and Self-Test switch bits are cleared, then the clear was successful. If one of them is set, the procedure must be repeated until they are both cleared 50 microseconds after the Control Panel Clear address has been read.

2.1.2.4.3 Active LED (Write only)

16-bit Address: 0x2248
8-bit Address: 0x2248 or 0x2249

A write to one of these addresses turns the control panel Active LED on for approximately 3/4 second. To insure that the LED stays on continuously, this address must be written at least

once every 500ms.

2.1.2.4.4 Control Panel Switches (Read only)

TABLE II-12. Control Panel Switches (0x2248 read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	T	OL	PL	LN	X	X	X	X	X	X	X	X

Address: 0x2248 (read only)

TABLE II-13. Control Panel Switches (0x2249 read only)

7	6	5	4	3	2	1	0
X	X	X	X	T	OL	PL	LN

Address: 0x2249 (read only)

T: (R) Test Switch, Active High

A one in this position indicates that the Test button on the control panel has been pressed since the control panel latches were last cleared while one of the following is true:

(1) The Off-Line LED is on and the Mask Reset bit in the Control/Status register is reset.

(2) The Mask Reset bit in the Control/Status register is reset and the Off-Line button is simultaneously depressed.

(3) The On-Line button is simultaneously depressed.

The setting of this bit generates a hardware reset to the 6542.

OL: (R) Off-Line Switch, Active High

A one in this position indicates that the Off-Line button has made a transition from unpressed to pressed since the control panel latches were last cleared. While this bit is set it requests an interrupt on INT3 and causes the Control Panel Interrupt bit in the Control/Status register to be active (reset).

PL: (R) Program Load Switch, Active High

A one in this position indicates that the Program-Load button on the control panel has been pressed since the control panel latches were last cleared while one of the following is true:

(1) The Off-Line LED is on and the Mask Reset bit in the Control/Status register is reset.

(2) The Mask Reset bit in the Control/Status register is reset and the Off-Line button

is simultaneously depressed.

(3) The On-Line button is simultaneously depressed.

The setting of this bit generates a hardware reset to the 6542.

LN: (R) On-Line Switch, Active High

A one in this position indicates that the On-Line button has made a transition from unpressed to pressed since the control panel latches were last cleared. While this bit is set it requests an interrupt on INT3 and causes the Control Panel Interrupt bit in the Control/Status register to be active (reset).

2.1.2.5 Floppy Disk Controller

A Western Digital WD37C65/B Floppy Disk Subsystem Controller (FDC) is used to control the 3.5" microfloppy drives used in the 6542. The hardware will support either one or two drives and requires that the 37C65/B is used in "PC AT mode." All features of the 37C65/B in PC AT mode are supported. Though the manual claims that in PC AT mode commands do not require US0 and US1 to be set, it should be noted that if they are left at zero, only one of the four cylinder registers will be used, which will complicate operations involving both drives. Setting US0 and US1 in the commands will circumvent this problem. Because a PLCC package is used, the diskchange function is available. The internal registers of the 37C65/B are mapped into 80C186 I/O space as shown below:

TABLE II-14. Floppy Disk Controller Registers

Address	Register	Conditions
0x2100	Status Register	
0x2102	Data Register	for non-DMA access
0x2106	Operations Register	
0x210a	Control Register	
0x210e	DMA Data Register	for DMA access only

All registers are 8 bits wide. To save hardware, a separate address has been created for the Data register to be used during DMA transfers. This address reaches the same register as the non-DMA address, but must be used during DMA transfers to provide the proper control signals to the 37C65/B. For WD37C65/B register definition and programming information see references in sections 6.4.5 and 6.4.6.

2.1.2.6 Serial Communications Controller

The 6542 uses an 8 MHz Z8530 Serial Communications Controller (SCC) to control its EIA-232 and CCITT V.35 ports. Port A is designated the synchronous host port, also called port 0. Jumper plugs on the board will option this port as either an EIA-232 port or a CCITT V.35 port. The setting of the jumper plugs is not readable. Port B is designated the diagnostic port, also called port 1. This port may be optioned as a synchronous port using the Diagnostic Port Clock Select bit of the Control/Status register. In diagnostic mode, this port will support asynchronous traffic at 1200 or 9600 baud. In synchronous mode, this port is identical to port 0 in EIA-232 mode. Detailed information on the SCC may be obtained from the reference

described in section 6.4.4.

2.1.2.6.1 SCC Interrupts

The SCC uses INT0 of the 80C186 in cascade mode. It has the highest priority of all devices using INT0. The SCC must be programmed to provide the interrupt vector during the interrupt acknowledge cycle.

2.1.2.6.2 SCC Register Addresses

The four 8-bit registers within the SCC are accessed using the following addresses:

TABLE II-15. SCC Registers

Address	Register
0x2000	Channel B Command
0x2002	Channel B Data
0x2004	Channel A Command
0x2006	Channel A Data

2.1.2.6.3 EIA Status Register (0x2041)

TABLE II-16. EIA Status Register (0x2040 read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	S1	D1	S0	D0	X	X	X	X	X	X	X	X

Address: 0x2040 (Read only)

TABLE II-17. EIA Status Register (0x2041 read only)

7	6	5	4	3	2	1	0
X	X	X	X	S1	D1	S0	D0

Address: 0x2041 (Read only)

D0: (R) Port 0 (channel A) DSR
This bit is the inverted state of pin 6 of port 0.

S0: (R) Port 0 (channel A) SPEED
This bit is the inverted state of pin 12 of port 0.

D1: (R) Port 1 (channel B) DSR
This bit is the inverted state of pin 6 of port 1.

S1: (R) Port 1 (channel B) SPEED
This bit is the inverted state of pin 12 of port 1.

2.1.2.6.4 SCC Circuit Connections

TABLE II-18. SCC Circuit Connections

DB-25 Pin	EIA-232 Name	V.35 Name	SCC Pin Name
1	AA	101	GND
2	BA	----------	TxD
3	BB	----------	RxD
4	CA	105	RTS
5	CB	106	CTS
6	CC	107	*
7	AB	102	----------
8	CF	109	DCD
11	----------	114+^	RTxC
12	CI	----------	*
13	----------	115+	TRxC
14	----------	115-	TRxC
15	DB^	----------	RTxC
15	----------	103+	TxD
17	DD	----------	TRxC
17	----------	103-	TxD
18	----------	114-^	RTxC
19	----------	104+	RxD
20	CD	108	DTR
25	----------	104-	RxD

* Pins 6 and 12 do not enter the SCC.
They may be read using the EIA status register.
^ The TxC signal is disconnected from RTxC on the SCC on port 1 when in diagnostic mode.

2.1.2.6.5 SCC Baud Rate Table

The diagnostic port on the SCC (port 1) supports asynchronous baud rates of 1200 and 9600. To achieve these baud rates, the Diagnostic Port Clock Select bit in the Control/Status Register must be reset and the SCC must be programmed according to the table below:

TABLE II-19. SCC Baud Rate Table

Baud Rate	Clock	Clock Mode	Time Constant
1200	RTxC	x64	50
9600	RTxC	x32	11

2.1.2.7 Coax Microcontroller Interface

Most communication between the 80C186 and the Coax Microcontroller uses the dual port RAM. I/O ports are used for two functions: CMC interrupts to the 80C186 and 80C186 control of the Coax Microcontroller. The CMC sends interrupt vector information to the 80C186 through a FIFO buffer. Any data in the FIFO generates an interrupt to the 80C186 on INT1. The 80C186 reads the 8-bit vector information through an I/O port. The 80C186 control of the Coax Microcontroller covers resetting and halting as well as downloading the 8Kx16 program store. All of these functions are accomplished using the I/O ports described below.

2.1.2.7.1 FIFO (0x22c0)

A 64x8 bit FIFO is placed between the CMC and the 80C186 for CMC interrupts to the 80C186. This FIFO is writable by the CMC and readable by the 80C186. Any data in the FIFO will generate an interrupt to the 80C186 on INT1. This data may be read and removed from the FIFO by reading address 0x22c0. The FIFO may not be written to by the 80C186, and should only be read when INT1 is active, that is, it should only be read when there is data available in the FIFO.

2.1.2.7.2 Instruction Bus (0x2290)

In order to monitor and control the CMC program store, the 80C186 must have access to the CMC instruction bus, which is the data bus for the CMC program RAM. An I/O port is assigned to this bus. A read of this port will yield the current contents of the CMC instruction bus. The bus should only be read when the CMC is halted (see below for information on how to halt the CMC) to insure that the bus is not in transition when it is read. A write to this port latches data to be presented to the instruction bus under control of the ILON and ILOFF ports (see below for definition). The port address is 0x2290.

2.1.2.7.3 Address Bus (0x22b0)

The 80C186 may also read the CMC address bus, which is the address bus for the CMC program RAM. Due to the fact that the two processors run asynchronously, this bus should only be read when the CMC is halted (see below for information on how to halt the CMC) to insure that the bus is not in transition while it is being read. The CMC address bus port address is 0x22b0. This port is read only; it may not be written to.

2.1.2.7.4 Control Method

Several I/O ports are used by the 80C186 to control the CMC. In addition to the registers described above, there are 11 other registers listed below. These are all 8-bit registers which may be read or written to, but the data is not significant. Their function is accomplished

simply by accessing them, either as a read or as a write. They are grouped into 5 functional pairs plus one. Accessing one address in the pair turns a function on; accessing the other address turns that function off. Functions remain in the state they were last set to unless a system reset sets them all to the values indicated below. Using these registers and the ones described above in the proper sequence enables the 80C186 to download and control the operation of the CMC. Algorithms for control are described below.

TABLE II-20. Control Registers

Address		Register	Description
0x2280	*	ResetOn	Toggles the CMC hardware reset
0x2281		ResetOff	
0x2282	*	HaltOn	Toggles the CMC Halt input
0x2283		HaltOff	
0x2284	*	StepOff	Used to single step the CMC
0x2285		StepOn	
0x2286	*	ILOff	Enables or disables the Instruction Latch
0x2287		ILOn	
0x2288	*	PSOn	Enables or disables the output of the CMC Program Store
0x2289		PSOff	
0x22a0		WritePS	Strobes data on the Instruction Bus into the CMC Program Store

*** indicates the reset state of the function**

Note: IL and PS should never be on at the same time. One should be turned off before the other is turned on.

2.1.2.7.4.1 CMC Modes

For ease in the discussion of CMC control procedures, there are defined below 4 "modes" that the CMC may be in based upon the states of the 5 pairs of control registers described above.

TABLE II-21. CMC Modes

Mode	Requirements
Reset	ResetOn
Halt	ResetOff, HaltOn
Step	ResetOff, HaltOff, StepOn
Run	ResetOff, HaltOff, StepOff, ILOff, PSOn

Transitions between modes are all legal providing no undefined modes are entered during transition. For example, to go from Halt Mode to Run Mode, first issue StepOff, ILOff, and PSOn, if they are not issued already, and then issue HaltOff. Otherwise, for a short time the

CMC would be in neither Run Mode nor Halt Mode, and the results could be problematic.

2.1.2.7.4.2 Algorithm for Single Stepping

From Halt Mode, go to Step Mode (StepOn, if not on already, then HaltOff), then back to Halt Mode. The single step is done immediately after HaltOff is issued. The instruction that is on the Instruction Bus at that time will be executed. The CMC must return to Halt Mode to rearm the single step mechanism.

2.1.2.7.4.3 Algorithm for Jumping to an Address

Forcing the CMC to jump to an address is accomplished by halting the CMC, turning off the program store, placing a jump instruction on the instruction bus, and single stepping the CMC. From Halt Mode issue PSOff followed by ILOn. Write a JMP address command for the desired address to the Instruction Latch (form of command illustrated below). Single step the CMC to execute this jump instruction. At this point the CMC is ready to fetch an instruction from the desired address; go to Run Mode to run.

TABLE II-22. CMC JMP address Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Address to jump to											

2.1.2.7.4.4 Algorithm for Writing Program RAM

Jump to the desired address. Do not issue ILOff. Write data for program RAM to the Instruction Bus. Issue WritePS.

2.1.2.7.4.5 Algorithm for Reading Program RAM

Jump to the desired address. Issue ILOff, then PSOn. Read the Instruction Bus to read the desired data.

2.1.3 Hardware Interrupts

Because INT0 is set up in cascade mode, there are a total of four types of hardware interrupts possible to the 80C186. They are NMI, INT0, INT1, and INT3. Each one and its sources are described below.

2.1.3.1 NMI

NMI is not driven by any of the devices on the base board. It will only be driven if there is an option card present that uses it. See the option card section (section 8) to see which option cards use NMI.

2.1.3.2 INT0

INT0 receives vectored interrupts from the SCC on the base card. Devices on the option card may be added to the daisy chain after the SCC. See the option card section (section 8) to see which option cards use INT0.

2.1.3.3 INT1

INT1 is used exclusively by the CMC FIFO buffer. Any data in the FIFO causes INT1 to be held active until the 80C186 reads all of the data from the FIFO. See section 2.1.2.7.1 for details.

2.1.3.4 INT3

INT3 has several devices ORed together, any of which can use the interrupt. The Control/Status Register shows which of the possible devices is requesting an interrupt. The possible devices are the Floppy Disk Controller, the Control Panel Switches, and any device on an option card that may use this interrupt. The following sections provide further detail:

TABLE II-23. Interrupt 3 Cross Reference

Section	Topic
2.1.2.3	Control/Status Register
2.1.2.5	Floppy Disk Controller
2.1.2.4	Control Panel
8	Option Cards

2.1.4 Romhelp Overview

In addition to the hardware resources described above, the 80C186 programmer has at his disposal a small library of ROM based routines called "romhelp routines." These include routines to access the microfloppies, routines to download code to the CMC, and a routine that calls the ROM-based self-test code. The romhelps are described in more detail in section 3.3.

2.1.5 Reset Procedure

The following actions should be taken immediately after a reset:

- Reprogram UMCS and other chip selects (sec. 2.1.2.1.2)
- Program watchdog timer (timer 0) (sec. 2.1.2.1.4)
- Program RAM refresh unit; init. RAM (sec. 2.1.2.1.3)
- Set up interrupt system (sec. 2.1.2.1.5)
- Read and clear control panel (sec. 2.1.2.4)
- Read Control/Status register (sec. 2.1.2.3)

2.2 CMC Programming

The CMC peripheral devices and programming methods are described below.

2.2.1 CMC Internals

The CMC is intended to run in its highest speed mode in this design. Mode select flags F1 and F2 of register 15 should therefore be set to zero.

2.2.2 Status Register

TABLE II-24. CMC Status Register

7	6	5	4	3	2	1	0
FR	CP	X	X	X	X	X	X

Address: Read Strobe 0

FR: (R) FIFO Ready, Active Low

A zero in this position indicates that the FIFO may be written to. A one indicates that the FIFO is either full or is still recovering from the previous write.

CP: (R) Coax Expansion Card Present, Active Low

A zero in this position indicates that the system contains a Coax Expansion Card. If the Coax Expansion Card is present, the CMC may access 8 coax ports. If the Coax Expansion Card is not present, the CMC may access only 4 coax ports.

2.2.3 FIFO Buffer

The FIFO buffer may be accessed using Write Strobe 0. To prevent loss of data, the CMC must wait for the FIFO Ready bit of the Status Register is active before writing to the FIFO.

2.2.4 Port Select Register

Any of the coax ports in the system may be connected to the CMC receiver and transmitter through an external multiplexing scheme. Once this is done, the CMC may transmit to and receive from the selected port. The Port Select Register controls the multiplexing.

TABLE II-25. CMC Port Select Register

7	6	5	4	3	2	1	0
LB	X	X	X	X	A2	A1	A0

Address: Write Strobe 4

A0-A2: Port Select Address

These three bits determine which coax port the CMC transmitter and receiver are connected to. Values from 0 through 3 select the four ports on the base card. Values from 4 through 7 select the four ports on the Coax Expansion Card, if present.

LB: Loopback, Active High

Normally, the line receiver is disabled when the transmitter is active, preventing an external loopback. If this bit is set, however, the line receiver stays enabled while the transmitter is active, allowing the CMC to perform an external loopback.

2.2.5 RAM Access Procedure

Five CMC ports are used to access the dual port RAM. These ports and their addresses are shown below, followed by procedures for reading and writing to the dual port RAM.

2.2.5.1 Address High, Write Only

TABLE II-26. CMC Address High Register

7	6	5	4	3	2	1	0
X	X	X	A12	A11	A10	A9	A8

Address: Write Strobe 3

A8-A12: (W) Dual Port RAM Address, High Byte

The 13-bits of address required to address the 8K of dual port RAM are written in 2 registers. This register holds the upper 5 bits of the 13-bit address.

2.2.5.2 Address Low, Write Only

TABLE II-27. CMC Address Low Register

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Address: Write Strobe 2

A0-A7: (W) Dual Port RAM Address, Low Byte

The 13-bits of address required to address the 8K of dual port RAM are written in 2 registers. This register holds the lower 8 bits of the 13-bit address.

2.2.5.3 RAM Data, Read and Write

Data from the RAM is read using Read Strobe 1. Data going to the RAM is written using Write Strobe 1.

2.2.5.4 Read RAM Request, Read Only

Read Strobe 3 is used in the process of reading dual port RAM to issue a Read RAM Request. No valid data is obtained by this read; it merely issues a command to the RAM control logic.

2.2.5.5 Dual Port RAM Read Procedure

The following procedure must be used to read dual port RAM:

(1) Write high byte of address. This step may be skipped if the last value written to the high byte of the address is the desired value.

(2) Write low byte of address. This step may be skipped if the last value written to the low byte of the address is the desired value.

(3) Issue Read RAM Request.

(4) Wait a minimum of one CMC instruction cycle.

(5) Read data.

2.2.5.6 Dual Port RAM Write Procedure

The following procedure must be used to write dual port RAM:

(1) Write high byte of address. This step may be skipped if the last value written to the high byte of the address is the desired value.

(2) Write low byte of address. This step may be skipped if the last value written to the low byte of the address is the desired value.

(3) Write Data.

(4) Wait a minimum of 2 CMC instructions before any more dual port RAM operations.

2.3 Option Cards

One of the available option cards may be installed in a 6542 system. The characteristics of each of these are described in section 8. In order to use the information in section 8, however, there must be a method for determining whether an option card is present, and, if so, what type of option card it is. This function is accomplished through the use of the Card Type Register. This register is common to all of the option cards. The value in the register indicates what type of card is present. If no card is present, there will be a watchdog timeout when the Card Type Register is read. The following section gives the value in the card type register for each of the option cards.

2.3.1 Card Type Register (0x2300)

This is an 8-bit read only register. If no option card is present, a read of this register will yield a watchdog timeout. If there is no watchdog timeout, the relationship between this register's

value and the option card type is as detailed below:

TABLE II-28. Card Type Register Values

Range of Values	Type of Option Card
0x00 - 0x0f	CDB Development Option Card
0x10 - 0x1f	Asynchronous Port Option Card

3. FIRMWARE OPERATION SUMMARY

3.1 Firmware Overview

The 6542 firmware can be broken into 4 functional blocks: Initialization, Self-Test, Bootload, and Software Support. The initialization code is the first program control after every system reset. It has 3 functions: initialization of 186 registers; quick processor, RAM, and ROM tests; and determining which block to execute next. If the Self-Test button on the control panel was the source of the reset, then the self-test block is executed next; otherwise, the bootload block is executed immediately. The self test block performs a detailed test of the 6542 hardware. The results are reported through the Test LED on the control panel. The Test LED will flash during the test. At the end of the test the LED will stay on if the controller has passed. If the controller fails, the LED will go out. At the end of the test, the processor enters an infinite loop (unless it is in the special continuously testing loopback mode discussed below). The loop may be exited by pushing a button on the control panel. The Self-Test or Program Load buttons will generate hardware resets which will transfer control to the Initialization block. The On-Line button will generate an interrupt which will transfer control to the bootload block without a hardware reset. The bootload block attempts to read code from the microfloppies. It will keep trying until it finds some code or a hardware reset interrupts it. When it finds code, it will place it in RAM and then transfer control to that code. From this point on, the 6542 is under software control. The only function the firmware serves is software support through the romhelp routines. These are a set of ROM based routines made available to application programs. They include floppy control routines, CMC download routines, and the self-test block of code. Self-test works the same way from romhelp except that at the end it goes directly to bootload without waiting for a button to be pressed on the control panel.

3.2 Loopback Mode

If the loopback bit in the Control/Status register is tied low by a hardware strap, the 6542 is in loopback mode. Loopback mode causes the 6542 to run self-test repeatedly as soon as power is applied. The test will continue to run until a fatal error occurs or power is removed. (Errors considered fatal by the self test code are RAM and ROM errors, because both prevent the test code from being executed reliably. These errors cause an immediate halt of the processor with no results reported.) The self-test used during loopback mode is a more extensive test than the usual self-test. Because it attempts to test the EIA interface all the way to the connector, external loopback plugs are required on all EIA ports. These loopback plugs must make the following connections:

TxD (pin 2)	to	RxD (pin 3)		
DTR (pin 20)	to	DSR (pin 6)	and	DCD (pin 8)
RTS (pin 4)	to	CTS (pin 5)	and	SPEED(pin 12)

After each pass through the self test code, the results of that pass will be transmitted out the diagnostic port at 9600 baud. If there were any errors, the error table (described below) will be transmitted. If there were no errors, all that will be transmitted will be the word "PASS". The loopback test mode is intended for R&D use only.

3.3 Romhelp

Several "romhelp routines" are provided by the 6542 firmware. These are subroutines in EPROM that are made available for software use. They are accessible using a software interrupt in the following fashion: All arguments to be passed to the routine are placed on the stack. The routine number is placed in the AX register of the 80C186. A software interrupt 0x6e is executed, transferring control to the EPROM based code. Upon return from the software interrupt, the value to be returned will be in the AX register. Use of any of these routines requires that vector 0x6e in the 80C186 vector table is not changed after the firmware sets it following a reset. A sample C-callable assembly-language routine to call the romhelp routines is illustrated below:

```
romhelp:
        pop     %si             / adjust stack
#ifdef  B16TV
        pop     %dx             /
#endif
        pop     %ax             / get top of stack in %ax
        int     0x6e            / transfer control to EPROM
        push    %ax             / push result for caller
#ifdef  B16TV
        push    %dx             / long return to caller
        push    %si             /
        lret                    /
#else
        jmp     *%si            / return to caller
#endif
```

Using this routine, romhelp routines could be called using a C call of the form:

romhelp(routine#, arg1, arg2, arg3, ..., argn);

Each romhelp routine is briefly described below:

3.3.1 Card Type

C-calling sequence: romhelp(1)
Arguments passed: none
Results returned: 6542's card type
Description: Returns a value to indicate the type of hardware (6542)

3.3.2 Self Test

C-calling sequence: romhelp(3)
Arguments passed: none
Results returned: never returns; redownloads when it is done
Description: Causes the MINI to jump to its firmware selftest routine.

3.3.3 Error Array Location

C-calling sequence: romhelp(4, segment, offset)
Arguments passed: segment, offset
Results returned: none in AX
Description: Caller passes the segment and offset of a structure that is to be filled with the segment and offset of the 32 byte error array. This structure is two words long; the first word will contain the offset, the second will contain the segment of the error array.

3.3.4 Switch Settings

C-calling sequence: romhelp(5)
Arguments passed: none
Results returned: The value of the control panel switch register read during the reset sequence.
Description: see results returned above

3.3.5 Format

C-calling sequence: romhelp(22, drive)
Arguments passed: drive - the drive that contains the diskette to be formatted.
Results returned: non-zero = Pass = Format successful, zero = Fail = Format failed
Description: Formats the diskette in the specified drive.

3.3.6 Recalibrate

C-calling sequence: romhelp(24, drive)
Arguments passed: drive - the drive number.
Results returned: non-zero = successful, zero = unsuccessful
Description: Position the drive's R/W head on track zero.

3.3.7 Seek

C-calling sequence: romhelp(25, drive, track)
Arguments passed: drive = the drive number, track = the track number to seek to.
Results returned: non-zero = successful, zero = unsuccessful
Description: Force the selected drive to seek to the desired track.

3.3.8 Read

C-calling sequence: romhelp(26, drive, head, track, starting_sect, num_of_sect, segment, offset)
Arguments passed: drive - the drive number to read from.
head - the side of the diskette to read from.
track - the track number to read from.
starting_sect - the sector to start reading from.

num_of_sect - the total number of sectors to read.
segment - the segment to transfer data to.
offset - the offset to transfer data to.
Results returned: non-zero = successful, zero = unsuccessful
Description: Perform multi-sector read from the micro-floppy drive.

3.3.9 Write

C-calling sequence: romhelp(27, drive, head, track, starting_sect, num_of_sect, segment, offset)
Arguments passed: drive - the drive number to write to.
head - the side of the diskette to write to.
track - the track number to write to.
starting_sect - the sector to start writing to.
num_of_sect - the total number of sectors to write.
segment - the segment to transfer data from.
offset - the offset to transfer data from.
Results returned: non-zero = successful, zero = unsuccessful
Description: Perform multi-sector write to the micro-floppy drive.

3.3.10 CMC Download

C-calling sequence: romhelp(28, seg, off, dest, count)
Arguments passed: seg - segment for source of data to be downloaded
off - offset for source of data to be downloaded
dest - destination in control store where data will go
count - number of instruction words to download
Results returned: non-zero = successful, zero = unsuccessful
Description: Transfer data from the 80186 memory space to the CMC program store.

3.3.11 CMC Run

C-calling sequence: romhelp(29, start_adr)
Arguments passed: start_adr - location to start the CMC
Results Returned: none
Description: Start the CMC running at the specified address.

3.3.12 Set CMC Break Point

C-calling sequence: romhelp(30, brk_adr)
Arguments passed: brk_adr - address at which to set break point
Results returned: none
Description: The instruction at the specified address will be replaced with a jump to self infinite loop.

3.3.13 Remove CMC Break Point

C-calling sequence: romhelp(31, instr, do_rtrn)
Arguments passed: instr - instruction word to execute
do_rtrn - determines how function exits
0 = keep break point and go to single step mode
1 = write instruction to control store and then run
2 = keep break point but run.
Results returned: none
Description: Continues from a break point.

3.3.14 Read CMC Register

C-calling sequence: romhelp(32, reg)
Arguments passed: reg - the number of the requested register
Results returned: the value of the requested register
Description: Reads one of the CMC's internal registers.

3.3.15 Write CMC Register

C-calling Sequence: romhelp(33, reg, val)
Arguments passed: reg - the number of the requested register
val - the value assigned to that register
Results returned: none
Description: Writes a value to one of the CMC's internal registers.

3.4 Self-Test Result Codes

The results of self test are stored and reported as 32 16-bit words of data. Each test is assigned a bit in one of these words. If the test is passed, the bit is reset; if the test is failed, the bit is set. The table below associates these bits with the sections of hardware that they represent.

TABLE II-29. Self-Test Result Codes

Word	Device Tested	Bit	Error Type
1	Timer 1	0	Control register read/write error
		1	Count register read/write error
		2	Max. count register read/write error
		3	Timer is not counting
		4	Timer is not counting
		5	Timer interrupt failed
2	Timer 2	0	Control register read/write error
		1	Count register read/write error
		2	Max. count register read/write error
		3	Timer is not counting
		4	Timer is not counting
		5	Timer interrupt failed
3	DMA Channel 0	0	Data corrupted or not transferred
		1	Data corrupted or not transferred
		2	Data corrupted or not transferred
		3	Data corrupted or not transferred
		4	Data corrupted or not transferred
		5	Data corrupted or not transferred
		6	DMA interrupt failed
4	DMA Channel 1	0	Data corrupted or not transferred
		1	Data corrupted or not transferred
		2	Data corrupted or not transferred
		3	Data corrupted or not transferred
		4	Data corrupted or not transferred
		5	Data corrupted or not transferred
		6	DMA interrupt failed
5	Timer 0	0	Timer is not counting
		1	No ready from SCC
		2	No ready from FDC
		3	No ready from page register
		4	No ready from CMC
		5	Timer interrupt failed
6	Main RAM	0	Stuck data bits
		1	Read/write error

Word	Device Tested	Bit	Error Type
7	Paged RAM	0	Stuck data bits
		1	Read/write error
		2	Low window uniqueness test failed
		3	High window uniqueness test failed
		4	Low window wraparound failed
		5	High window wraparound failed
		6	Number of page that failed
		7	
		8	
		9	
		10	
8	Dual Port RAM	0	Stuck data bits
		1	Read/write error
9	Floppy Disk Controller	0	Command not completed
10	Coax Microcontroller	0	CMC instruction bus error
		1	CMC address bus error
		2	CMC download error
		3	FIFO cannot be cleared
		4	CMC will not run
		5	CMC internal test failed
		6	CMC dual port RAM test failed
		7	Aux. present dispute
		8	CMC lost
11	Coax Port 0	0-3	1: receiver time out
			2: receiver malfunction
			3: receiver error bit set
			4: RXDAV bit stuck high
			5: data bits don't match
			F: not tested or not present
		4-7	Number of test that failed
12	Coax Port 1	0-7	Same as port 0
13	Coax Port 2	0-7	Same as port 0
14	Coax Port 3	0-7	Same as port 0
15	Coax Port 4	0-7	Same as port 0
16	Coax Port 5	0-7	Same as port 0
17	Coax Port 6	0-7	Same as port 0
18	Coax Port 7	0-7	Same as port 0
19	CMC Status Port	0	Stuck bit

Word	Device Tested	Bit	Error Type
20	CMC FIFO	0	FIFO never ready
		1	FIFO says ready when full
21	186 FIFO	0	No FIFO interrupt
		1	FIFO data error
22	Synchronous Port	0	Transmit buffer empty bit error
		1	Receive buffer full bit error
		2	Data error
		3	DMA on xmit: transmit buffer empty bit error
		4	DMA on xmit: data error
		5	DMA on rcv: receive buffer full bit error
		6	DMA on rcv: data error
		7	Int mode: transmit buffer empty bit error
		8	Int mode: interrupt did not occur
23	Diagnostic Port	0	DMA on xmit: transmit buffer empty bit error
		1	DMA on xmit: data error
		2	DMA on rcv: receive buffer full bit error
		3	DMA on rcv: data error
		4	Ext loopback: DTR,RTS,DSR, or SPEED error
		5	Ext loopback: DTR,RTS,DCD, or CTS error
24	Option Card Test #1	all	See section 8
25	Option Card Test #2	all	See section 8
26	Option Card Test #3	all	See section 8
27	Option Card Test #4	all	See section 8
28	Option Card Test #5	all	See section 8
29	Option Card Test #6	all	See section 8
30	Option Card Test #7	all	See section 8
31	Option Card Test #8	all	See section 8
32	Option Card Test #9	all	See section 8

4. HARDWARE ORGANIZATION

This subsection describes the hardware operation in detail. Frequent reference is made to the circuit card schematic diagrams by page number. (See section 7.1 for information on procuring copies of the schematics for the base, expansion, and option cards.)

4.1 Reset Logic

Based upon their sources, the reset signals serving to initialize the 6542 hardware may be grouped into three overlapping sets: power supply initiated resets, control panel initiated resets, and software initiated resets. The control panel resets are a subset of the power supply resets, and the software resets are a subset of the control panel resets. This allows the power supply to initiate all of the hardware on power up, while the control panel initializes everything but itself. The software may reset the 80C186 peripherals.

4.1.1 Power Supply Initiated Reset

The +5V output of the power supply is monitored by a Texas Instruments TL7705A supply voltage supervisor, as shown on page B9. When the supply voltage is below the reference voltage of the 7705 (approx. 4.55V) it drives POR# low. When the supply voltage rises above the reference voltage, the 7705 will hold POR# low for a time determined by an external capacitance and then release POR# to be pulled inactive by the 4.3kohm pull-up resistor. The two 4.7 microfarad capacitors will keep POR# active for approximately 120 milliseconds after the +5V supply is within range. The 0.1 microfarad capacitor is intended to prevent false triggering due to power bus transients. The 7705 also provides a reference voltage for the thermal shutdown circuit (see below).

The POR# signal is used on page B10 to trigger the CLRPANEL# signal to clear the control panel switch latches. It is also used on page B11 to reset the 555 timer used for control panel resets. The above devices are not reset by control panel or software initiated resets. POR# is also used to create RESET, RESET#, and RES186. These three signals are shared with the control panel reset, so they are described in the next section.

4.1.2 Control Panel Initiated Reset

The Program Load and Self-Test buttons on the control panel, if they are not masked (see section 2.1.2.4.4), generate a hardware reset when pressed. As the control panel section which follows (section 4.3.6.3) describes, when not masked these buttons will drive the output of the LS38 on page B11 (location G6) low and latch it in that state until the control panel latches are cleared. This low output is AC coupled through the 1200pF capacitor to the trigger input of the 555 timer, also on page B11. The effect will be a pulse on the trigger input, with the width determined by the R-C time constant of the 1200pF capacitor and the 10kohm resistor. A pulse is required, rather than a constant low voltage, to prevent the 555 from retriggering indefinitely. An open collector gate was chosen to drive the trigger input in order to guarantee a large voltage swing on the high-to-low transition, which is necessary to ensure that the trigger input reaches a low enough voltage to cause a reset. Because this signal is AC coupled, when the control panel latches are cleared, the LS38 output will go from low to high, but the trigger input will go from 5V to nearly 10V! The circuit will not be ready for another reset until this signal has exponentially decayed down to the neighborhood of 5V. If the Program Load or Self-Test buttons are pressed before this time, there is potential for not only missing the reset, but also locking out subsequent reset requests. This is the reason for the software requirement that after clearing a Program Load or Self-Test switch closure, the switch must be checked 50 microseconds later (approximately 4 time constants) to be sure that it has not been pressed during the critical period of time following the clear.

The output of the 555 will be a pulse of approximately 50ms duration. The length of this pulse is determined by the time constant of the 100kohm resistor and the 0.47microfarad capacitor. The 555 output is inverted and called LKPOR# (the LK prefix is used for historical consistency,

the meaning behind it being forgotten), which drives RESET, RESET#, and RES186. RES186 is the hardware reset input to the 80C186. A separate signal was created for the 80C186 because it requires reset to reach 3.0V before it is considered high. This specification was met by adding a pull-up resistor, as shown on page B9. RESET initializes the dual port RAM control PAL. RESET# initializes the LEDs, the RAM control PAL, and the FIFO. It also clears the writable bits in the Control/Status register and in the F259 on page B40, which activates all of the software controlled resets described below.

4.1.3 Software Initiated Reset

The Control/Status register has three bits allocated for hardware resets. One runs directly to the option card; this bit is called MAINIORES# on the schematics (page B8) and RO (reset option) in section 2.1.2.3 of this document. FDCRES#, or RF (reset floppy), runs to the WD37C65/B Floppy Disk Controller. SCCRES#, or RS (reset SCC), runs to the SCC PAL and causes the PAL to hold ZRD# and ZWR# active simultaneously, inducing a reset in the SCC. The reset width and reset recovery times of these devices determine the constraints given in section 2.1.2.3. The CMC may also be reset under software control by using the ResetOn control register as described in sections 2.1.2.7.4. and 2.1.2.7.4.1. This is wired directly to the CMC reset input.

4.2 Thermal Stress Warning

A thermistor is used as a temperature sensing device to issue a warning if the temperature inside the 6542 cabinet becomes too high. The circuitry for this sensor is shown on page B9. The thermistor and resistor form a voltage divider, while the LM239 compares the resulting voltage with the reference supplied by the TL7705 (typically 2.53V). As the thermistor heats, its resistance drops and the voltage that it presents to the comparator increases. When that voltage crosses the reference voltage, the LM239 output switches and an interrupt is generated to the 80C186 via INT3. The thermistor is situated on the board close to both the fan and one of the power resistors to maximize its efficiency in detecting a fan failure. In the event of a fan failure, its temperature should rise faster than that of the rest of the board, allowing it to give an early warning of impending problems. The unit should be turned off and serviced as soon as possible to avoid excessive thermal stress which will shorten the component lives.

4.3 80C186 @ 12.5 MHz

The 6542 uses an 80C186-12, a 12.5 MHz CMOS version of the earlier NMOS 80186. Most of the design was done with an eventual upgrade to a 16 MHz part in mind. The clock input is provided by an oscillator, rather than a crystal, because the oscillator was deemed more tolerant of physical abuse. Both of the DMA channels and all of the interrupts are used, as well as one of the timers. The upper memory chip select and 6 of the 7 peripheral chip selects are used. Both SRDY and ARDY are used in a normally-not-ready scheme. One or the other is pulsed active to complete a bus cycle, rather than holding them inactive to lengthen a cycle as in a normally-ready-scheme. The HOLD input is not used. The TEST input is tied to the reset output to put the 80C186 into enhanced mode so that the RAM refresh logic may be used.

4.3.1 Watchdog Timer

One of the internal timers of the 80C186 is used as a watchdog timer to prevent erroneous memory or I/O accesses from halting the system. If a read or write is attempted to an unmapped area of the 80C186 memory or I/O space, none of the peripheral devices will return a ready. To prevent the processor from waiting forever for a ready in this case, a "watchdog timer" monitors the bus cycles. The watchdog timer is implemented using one of the 80C186 internal timers, timer 0. This is accomplished by running ALE into TMRIN0, the external input for timer 0, to reset the timer at the beginning of each bus cycle. The timer is set to delay for a period of time longer than any valid bus cycle. For the 6542, 10 microseconds is sufficient to outlast any valid bus cycle. On an invalid bus cycle which does not receive a ready, timer 0 will reach terminal count, pulsing TMR0OUT# low for one clock period. This pulse is latched in a set of cross-coupled NAND gates, shown on page B4, and sent on as WDRDY# to activate ARDY. The ALE of the next bus cycle, in the form of ALESHIFT#, will clear the latch, resetting the external components of the watchdog circuit. There is a danger, in watchdog circuits of this type, of a false ready being returned if the normal ready signal occurs at a time close to the watchdog timeout. This is due to the synchronization delays of the timer circuitry inside the 80C186 which allow the timer output to trigger after the input has pulsed to reset the timer. While the input is being synchronized, the output may still go active. In the case of the watchdog timer, this has the effect of providing a false ready for the following bus cycle. If the following bus cycle required any wait states, this could result in erroneous data. For this reason, the watchdog timer period is required to be approximately 10 microseconds, clearly longer than the longest normal 80C186 bus cycle. The timer period should not be much longer than 10 microseconds to prevent problems with the RAM refresh scheme, as described in section 4.2.4.

4.3.2 Latched Address Bus

Pages B5 and B6 show three F373's that are the source of the LA bus and the LS (latched status) signals. They are controlled by DALE (delayed address latch enable), a signal derived from ALE in a manner shown on page B3. The F74 delays the rising edge of ALE until the falling edge of the 80C186 system clock. The falling edge of ALE is delayed only one gate delay. Use of DALE allows the latched addresses to remain valid for a longer time at the end of a cycle, but it does not delay the time for the new address to become valid. The outputs of the F74 used to create DALE are called ALESHIFT. Both ALESHIFT signals are replicas of ALE delayed on both edges to coincide with negative clock edges. This signal is easier to synchronize for use in PALs. Also on this page BALE is created as a buffered version of ALE.

4.3.3 EPROM

Two 27128 EPROMs are placed directly on the LA bus, enabled by the UCS# signal coming out of the 80C186. Their outputs run onto the 80C186 AD bus using LS244s as buffers for timing reasons. The outputs of the EPROMs do not go to a high impedance state fast enough after an access; therefore the 244s are used to isolate them from the AD bus.

4.3.4 RAM Banks

The 6542 will support either three or four RAM banks, each consisting of 512K of RAM in four 256Kx4 DRAM chips arranged in a 16-bit wide configuration. The data leads of the RAMs are connected to the AD bus through a set of 22 ohm damping resistors. One set of damping resistors serves all of the RAM banks. The address leads of the RAMs come from the LA bus

through F257 2 to 1 multiplexers followed by 22 ohm damping resistors. Bank 1, the non-paged memory, has one set of address multiplexers using only LA signals as shown on page B16. Banks 2 through 4 share a set of address multiplexers, shown on page B18, which substitute outputs of the page register for some of the address leads to implement the paging function. The page register is shown on page B17. Its 10 bits are contained in one LS374 pack and one LS74 pack. The LS244s are there to allow the value of the page register to be read. The outputs of the page register are multiplexed through the F257s using LA17 as the select. As can be seen from the memory map (section 2.1.1), LA17 is the bit that distinguishes between the low page and the high page; therefore it is used to select one of the two page addresses. Because each page covers 128K of memory but can be placed on 64K boundaries, it is necessary to add the page address with the lower bits of the address put out by the 80C186. This addition is accomplished using the LS283 shown on page B18. The highest bits are added using the 16L8 PAL to determine which bank should be used. The BANK[1:4] outputs of this PAL determine which bank gets a CAS. Only one of these outputs will be valid at a time, and only that bank will get a CAS and complete the cycle. The other banks will go through a RAS only refresh cycle. This PAL uses inputs from the adder and the page register to determine which bank to activate. Because the top of paged memory wraps around to the bottom of paged memory, the PAL must have some indication of how much memory is present. The EXTRARAM# input serves this purpose by going active if a RAM expansion card is installed. The LA19 and LA18 inputs are used to determine whether the access is to main RAM, paged RAM, or some other memory range. If it is not intended for RAM, none of the BANK outputs are enabled, thus preventing CAS from reaching any of the RAM banks. BPCS4#, BRD#, BWR#, LA5, and LA6 are used by the PAL to create RDPGR# and WRPGR#, the page register control signals. The VALIDPG# output is not used. The RAM control signals originate on page B14. The 16R4D PAL contains the state machine that controls RAS, CAS, and ready timing. The MUX signal is used as a select input to the address multiplexers. The SRDY signal goes directly into the 80C186 because the RAM is the only peripheral using SRDY. CASEN is another CAS qualifier used on page B15. Both CASEN and BANKn must be present to allow CAS to be generated for a particular bank. Because BANKn is not generated for non-DRAM address ranges, it performs the CASEN function rendering CASEN unnecessary. LBHE and LA0# enable CAS for the high and low bytes, respectively, to allow both byte and word accesses. The integrated DRAM Refresh Control Unit in the 80C186 is used to generate refresh cycles. Because the 80C186 leaves both LA0 and BHE# high during the refresh cycles, neither the low nor the high bytes will get a CAS, which makes a RAS-only refresh cycle for all banks simultaneously. The refresh cycle, in the absence of a hold condition, may be delayed a maximum of one bus cycle. In this system, the length of the longest bus cycle is defined by the watchdog timer to be approximately 10 microseconds. Because the refresh timer continues to count even if the refresh bus cycle is delayed, a delay of greater than one bus cycle will result in a missed refresh address. For this reason the watchdog timeout period must remain significantly shorter than the refresh period.

4.3.5 Peripheral Data Bus (BD Bus)

The AD bus coming out of the 80C186 is buffered by a set of F245 transceivers to create the buffered data bus (BD Bus), as shown on page B7, which serves as the data bus for all 80C186 peripherals except for the RAM and EPROM. The transceiver enable signal, TCEN#, is generated on page B3. The transceiver must be enabled for accesses to all devices on the BD bus. These include all I/O ports and the dual port RAM. The memory space that is reserved for future applications also must use the BD bus, because any future RAM will have to be on the option card, which uses only the BD bus. The F00 at location B4 on page B3 selects the range of addresses for which the transceiver is to be enabled. The lower input, LS2, enables TCEN# for any I/O access. The upper input from the F10 enables TCEN# for addresses above

the paged RAM windows that are not in the region where UCS# is enabled. For other bus cycles, the transceiver is not enabled. The basic shape of the TCEN# pulse is determined by the ALESHIFT# input. This is used instead of DEN# so that the transceiver will remain enabled for a longer time at the end of a write cycle, which is required by devices which require a long data hold time, such as the SCC. The F10 at location C4 exists for the purpose of disabling TCEN# earlier during the read cycles to avoid a bus contention problem. The LS1 input holds the output of the F10 high for the write case so that it has no impact on the timing. The BRD# input disables TCEN# when BRD# goes inactive. The ORed combination of DEN# and BINTA0# is intended to cut off TCEN# at the end of an interrupt acknowledge cycle. BRD# and BINTA0# are required because the data bus float time is specified relative to these signals rather than relative to DEN#. DDT/R# is also generated on page B3; it is switched in the middle of the clock cycle that ALESHIFT# is low so that the direction will change while the transceiver is disabled.

4.3.6 Control Panel

The control panel section of the logic includes both the physical user interface and the Control/Status register.

4.3.6.1 Address Decodes

Page B10 shows the address decodes for the control panel section of the logic. The address bits are fed into an F138 decoder. The decoder is enabled by the combination of BALE and BPCS4#. The chip select is required to be buffered to ensure that it will not go active before BALE from the previous cycle goes high, because that could cause a glitch on the select lines. (In this case, the glitch would not be a problem because all of the outputs are gated with either BRD# or BWR# before they are used.) For the same timing reason, BALE is used rather than any of the other ALE derivatives. This is the reason for the buffers on some of the PCS lines. They are buffered to take advantage of the minimum delay that the FAST gates provide rather than for loading reasons.

4.3.6.2 Control/Status Register

The Control/Status Register is shown on page B8. The writable bits are stored in the LS174, clocked in by the WRCOMMAND# signal from the address decodes on page B10. Only 5 of the 6 bits are used. The RDCOMSTAT# signal enables the LS244s to gate the contents of the register onto the BD bus. The 4.3kohm pull-up on the input to the BD5 buffer is for a loopback bit. This is normally inactive; it may be pulled active by an external strap to ground. The other pull-up is for the interrupt coming from the option card (INT3MAINIO#) so that if no option card is present, the signal will be held inactive.

4.3.6.3 Control Panel Switches

The four control panel switches are not shown in the schematics because they are part of the separate control panel board. They are all normally open SPST switches with one contact connected to Vcc. The other contacts are shown on page B11 of the schematics where they come off of the control panel connector. They are given active-high names corresponding to the switches which they are connected to: OFF-LINE, ON-LINE, PROGRAM-LOAD, and SELF-TEST. The OFF-LINE and ON-LINE signals are run through an R-C network, which, in conjunction with the input hysteresis of the LS244, is intended to remove the contact bounce

noise. The time constants of these networks were set to be as long as possible within the constraints of the 244 input leakage and the largest available capacitor, which was 47 microfarads. The outputs of the 244 corresponding to these two switches are used as clocks for two LS74s. This arrangement allows the LS74s to be cleared while the buttons may still be held down; the buttons must be released and depressed again to set the flip-flops. This was necessary because the outputs of the flip-flops for these two switches are used to create the CPINT# signal, which is one of the components of INT3. The other two switches do not drive interrupts, so they are latched using simple cross-coupled NAND gates. The mess of logic between the 244 and the cross-coupled NAND gates implements the masking function described in section 2.1.2.4.4. The function can be described by a boolean equation such as the one which follows for the Program Load switch:

```
LATCH = PROGRAM-LOAD*!MASKRESET*!OFFLINE#
      + PROGRAM-LOAD*OFF-LINE*!MASKRESET
      + PROGRAM-LOAD*ON-LINE
```

"!" is used as the negation operator. LATCH being a one implies that the program load latch is set; the other names are signals from the schematics. A similar function is valid for the Self-Test switch:

```
LATCH = SELF-TEST*!MASKRESET*!OFFLINE#
      + SELF-TEST*OFF-LINE*!MASKRESET
      + SELF-TEST*ON-LINE
```

If either of these two latches are set, a one is presented to the input of the LS38 at location G6 which results in a system reset as explained in section 4.1.2. The state of any of these latches may be read using the LS244 at location C8. This is enabled by the RDPANEL# strobe. The latches may be cleared using the CLRPANEL# strobe. Both of these strobes come from the control panel address decoder on page B10.

4.3.6.4 Control Panel LEDs

The LED drivers are shown on page B12. The Power LED is driven by a resistor to ground because it is intended to be on continuously. The Test and Off-Line LEDs are turned on and off through a simple two-bit register (that is roughly the cost of the register also). The Active LED, which is required to stay on for 500ms after each time it is strobed, requires a more complex circuit. The STRBACTVLED# signal is pulsed low to strobe the Active LED. This clears the counter and drives the ripple carry out (RCO) signal low, which puts a high on the parallel enable (ENP) input to the counter as well as starting a trigger pulse to the first 555 timer. When the STRBACTVLED# goes high again, the counter begins to count. When it reaches 15, the RCO signal goes active, which removes the ENP and ends the trigger pulse to the 555. This method was used to provide a long enough trigger pulse (1 microsecond) to the 555 without using a series capacitor, which has the problem described in section 4.1.2. The first 555 is used to create a pulse long enough to enable the transistor to discharge the 4.7 microfarad capacitor; the second 555 provides the 500 ms delay after a trigger pulse.

4.3.7 Floppy Disk Controller (WD37C65)

The floppy controller address decodes are shown on page B34. The ready signal, FDCRDY#, is a negative logic AND of BPCS2# and BALE. This function could have been accomplished using only BPCS2# and saving a gate. A separate address is provided for DMA accesses to the data

register in the floppy controller because the WD37C65 uses DACK# as a separate chip enable not to be active at the same time as FDCCS#. Using two addresses saves hardware. DACK# is also used to mask the DMA request because the DMA request does not go inactive fast enough. Masking it during the DMA access prevents the 80C186 from executing two DMA cycles when only one was requested. Page B33 shows the WD37C65 itself. Resistors are used on its data bus because it is very sensitive to voltage undershoot. Pull-downs are used on the FDRQ and FDCINT leads because these leads may be set to a high impedance state. DRD# and DWR# are used instead of the usual BRD# and BWR# to insure that the setup times for address before read or write strobes required by the 37C65 are met. All floppy interface signals run directly to the floppy drives. The F74 is used to create an 8MHz clock for the diagnostic port on the SCC to use as a baud rate clock.

4.3.8 Serial Communications Controller (Z8530)

The control logic for the SCC interface is shown on page B24. Because the SCC timing requirements are so different from those of the 80C186, a PAL is used to create appropriate interface signals. This PAL runs three types of cycles: Read, Write, and Interrupt Acknowledge. It is activated by PCS0 or PCS1, using BRD#, BWR#, and BINTA0# to determine the type of cycle to be run. INTA0 is buffered to provide sufficient hold time for the PAL. PCLK, the clock for the SCC, is generated externally, as is DZINTACK#, in order to meet the unreasonably tight setup and hold times of interrupt acknowledge with respect to PCLK when the 80C186 is running at 16 MHz. The PAL provides for the recovery time between SCC accesses so that programmers do not need to worry about violating it. It also holds ZRD# and ZWR# low when a reset condition is indicated by SCCRES# being active. It does not, however, provide for the recovery time required by the SCC after reset. Both the SCC on the base card and the SCC on the Asynchronous Port Option Card use the same PAL for control signals. The base card SCC uses addresses under PCS0, while the optional SCC uses PCS1#. The SCC is shown on page B25. LA6 is gated with BPCS0# so that half of the addresses under PCS0 may be allocated to the EIA Status Register. The F32 and two F00s on the RTxCB input act as a multiplexer under control of the Control/Status Register to either allow synchronous operation or send the 8-MHz ASYNCHCLK to be presented as a baud clock. The pull-ups on the DMA request lines prevent false requests when these lines are in a high impedance state. The F245 is used as a buffer on the data bus because the SCC does not have enough drive to use the BD bus directly. Pages B26 through B31 show the drivers and receivers for the EIA and V.35 ports. The connectors marked "EIA" and "V35" are the jumper connectors used to set the option for the synchronous port. In the EIA mode, adjacent pins in the EIA connectors on the schematic are connected. In the V.35 mode, adjacent pins in the V35 connectors on the schematic are connected. Page B31 shows the status register. This allows monitoring of external interface signals not supported by the SCC. Page B32 shows the driver for the transmit and receive LEDs on the control panel. TxD-0 is buffered here because of the number of loads on it. TxD-1 does not need to be buffered, but it is anyhow.

4.3.9 Dual Port SRAM Control

The dual port RAM section of the schematics includes the dual port RAM chip, the surrounding buffers, and the associated control logic. The SRAM chip is shown on page B36. It contains 8Kx8 of memory; only 4K was required, but the 8K chip was the smallest available SMT part at the time of the design. The bus structure connecting the surrounding buffers yields some insight into the operation of the RAM controller. The address buffers are shown on page B37. Two sets of buffers are used: one for the CMC address, and one for the 80C186 address. The 80C186 address, taken off of the LA bus, uses the F244s as buffers. Because the 80C186 waits for the

RAM to be ready, the buffers do not need to store the address, only gate it on and off. The CMC buffers, however, need to latch the address, as well as gate it on and off. This is because CMC can only write 8-bits of data at a time and has no dedicated address bus. CMC must write the address and then write or read the data. The dual port RAM control will gate either address onto the SRAM address bus (DPA0-12) using the control signals AECMC# and AE186#. Page B38 shows the data buffers. The two 646s for the 80C186 are set up to operate as transceivers, but latching the data going toward the 80C186 because the RAM does not hold it long enough. The 646 for the CMC is set up to latch data in both directions. Data going toward CMC is latched on both reads and writes to simplify the control logic. This 646 can be used as a register to hold data last read from RAM, but the data will be erased by the next read or write to RAM. Because the SRAM is only 8 bits wide, only one of the 80C186 646s is used at a time, depending upon whether an odd or even address is used. Control of the dual port RAM is accomplished using the PALs and discrete logic shown on page B35. The 16R8D PAL implements the state machine for the RAM cycles. Running off of the 80C186 clock, it will support speeds of up to 16MHz completing one RAM read or write in three clock cycles. To run at such a high speed, the 16L8D PAL is needed to govern the signal transitions. By satisfying the hold times for the various interrelated signals asynchronously, the RAM cycle time is reduced from 4 cycles to 3 cycles. A lower speed design could get by without the 16L8 PAL. Dual port RAM cycles for the 80C186 are initiated by the DPRAM# address decode and appropriate status signals for memory read, memory write, or instruction fetch. CMC cycles are initiated by the CMCREQ signal. CMCWRITE is also present if a write cycle is being initiated. CMCREQ is synchronized within the PAL, while CMCWRITE does not need to be synchronized. In order to keep DPRAMRDY, the ready signal to the 80C186, from running into the next 80C186 cycle, it is latched outside of the PAL using the F08 and F32 and cleared by the ALESHIFT of the following cycle.

4.4 Coax Micro-Controller

The coax line interface for the 6542 is handled by a Coax Micro-Controller, or CMC. The CMC is shown on page B39. It uses an 18.867 MHz clock frequency, because this is 8 times the data rate on the coax lines. CMCCLK, the CMC system clock, runs at one quarter the crystal frequency, or 4.72 MHz. Because this configuration requires no lengthened cycles, the CMC will execute one instruction every CMCCLK period, or an instruction every 212 ns. Three of the four read strobes and five of the five write strobes are used. The halt input is used, but the interrupt is not used. The receiver is set up to use the TTL input because the comparator function is done externally. Only two of the transmitter driver outputs are used because external drivers are used.

4.4.1 CMC Control

Page B40 shows the logic that the 80C186 uses to download and control the CMC. Because the CMC requires a RAM access time of 60 ns in its program memory, no buffers were placed in series with the RAM on either the address or the data side. The 80C186 may read the CMC address bus through the 244 buffer shown on page B42, but may not write the CMC address bus because the CMC address drivers may not be placed in a high impedance state. The instruction bus is buffered to the 80C186 side with 646s, shown on page B41, because it may be read or written, due to the output control available on the 8Kx8 SRAMs. The F138 on page B40 has decodes for reading and writing to the instruction bus, as well as reading the address bus,

writing the program store (actually WRPS# merely strobes the contents of the instruction bus into the program RAM), and reading the FIFO. It also has a decode running to the F259 addressable latch. This latch controls the reset and halt inputs to the CMC, as well as the RAM output enable (PSON#) and the 646 output enable (ILE#). The two F174s and the F74 are used to create a single step feature. This is accomplished by removing CMCHALT# for one CMCCLK cycle. The procedure for using the single step is outlined in section 2.1.2.7.4.3.

4.4.2 Dual Port RAM Interface

The CMC sees the dual port RAM as a set of 5 registers:

TABLE II-30. CMC Dual Port RAM Registers

Strobe Name	Register	Type	Name
WRADRLOW#(WS2)	24	write	Address Low
WRADRHI#(WS3)	25	write	Address High
WRDATA#(WS1)	23	write	Data (write)
RDRAMRQ#(RS3)	24	read	Read Request
RDDATA#(RS1)	22	read	Data (read)

The RDRAMRQ# and WRDATA# strobes are latched for interpretation by the dual port RAM control PAL as shown on pages B37 and B38. When RDRAMRQ# goes active, it sets the CMCREQ signal. When WRDATA# goes active, it sets the CMCWRITE signal as well as the CMCREQ signal. Because CMCWRITE is set at the same time as CMCREQ, synchronizing one guarantees the other in the dual port RAM control PAL. Both of these latches are cleared by the RAM control PAL.

4.4.3 CMC Status Register

Read strobe 0, called RDSTAT#, is used to read the CMC Status Register. It is implemented using two bits of an F244 buffer, as shown on page B43. The AUXPRESENT# signal is tied high through a resistor on the base card, and grounded on the Coax Expansion Card if it is present. The FIFRDY# signal is an AND combination of the input ready outputs of the two FIFO chips. It is synchronized using an F174 on the rising edge of CMCCLK to avoid metastable states within the CMC.

4.4.4 Coax Interface

The CMC receiver and transmitter are multiplexed between the four or eight coax ports based upon the value written to the multiplexer register shown on page B45. The lower three bits in the register run to both an LS259 decoder and an LS251 multiplexer. The LS251 multiplexer connects one of CXIN[0:7], the inputs from the 8 coax ports, to RCVDAT, the TTL coax input to the CMC. The LS259 has pin 15 tied low to configure it as a decoder. It creates two sets of select signals: SEL[0:7] and TSEL[0:3]. (TSEL[4:7] are created on the coax expansion card) The TSEL signals, which are enabled only when TXACT is valid, that is, when the CMC transmitter is active, enable the output drivers to the coax ports. They must be enabled only when the transmitter is active so that the line does not acquire a DC offset due to the inability of the line transformer to couple DC. The receivers require both their respective SEL input and the

general RCVSEL signal to be active before they will be enabled. RCVSEL is active when TXACT is inactive to enable the receiver only when the 6542 is not transmitting. For loopback testing, this feature may be bypassed using the high bit in the multiplexer, called LPBACK. The receivers are enabled individually to lessen the amount of noise that will be present on the base board in the presence of noisy lines. Pages B46 and B47 show the coax transformers with the line receivers and drivers. The "black box" resistor packs hold the resistors for the receiver hysteresis biasing as well as the transmitter signal level control. The transmitter is used in a one-to-one configuration for transmitting, and in a one-to-two configuration for receiving. The impedance is matched for either coax or twisted pair cabling using the switching capabilities of TPC connectors. The receiver provides approximately 12mV of hysteresis for noise immunity without excessive signal distortion.

4.4.5 FIFO Buffer Interface

Though the access to the FIFO seems simple from a programming perspective, using only WS0 to write to the FIFO as to a register, the actual hardware is a bit more complex. The FIFO is too slow to keep up with CMC, so a buffer is used to interface the two parts, as shown on page B43. WRFIF is generated from WRFIF#, going active when WRFIF# goes inactive. This provides a write strobe for the FIFO that meets the setup and hold times required by the FIFO.

4.5 Option Card Connector

The following signals are available on the Option Card Connector:

TABLE II-31. Option Card Connector Pinout

Pin	Direction	Name
1	POWER	VCC
2	OUTPUT	LA0
3	OUTPUT	LA1
4	OUTPUT	LA2
5	OUTPUT	LA3
6	OUTPUT	LA4
7	OUTPUT	LA5
8	POWER	GND
9	OUTPUT	LA6
10	OUTPUT	LA7
11	OUTPUT	LA8
12	OUTPUT	LA9
13	OUTPUT	LA10
14	OUTPUT	LA11
15	POWER	VCC
16	OUTPUT	LA12
17	OUTPUT	LA13
18	OUTPUT	LA14

Pin	Direction	Name
19	OUTPUT	LA15
20	OUTPUT	LA16
21	OUTPUT	LA17
22	POWER	GND
23	OUTPUT	LA18
24	OUTPUT	LA19
25	OUTPUT	BALE
26	OUTPUT	BDT/R#
27	OUTPUT	BRD#
28	OUTPUT	BWR#
29	POWER	VCC
30	INPUT	INT3MAINIO#
31	I/O	BD0
32	I/O	BD1
33	I/O	BD2
34	POWER	+12V
35	I/O	BD3
36	I/O	BD4
37	I/O	BD5
38	I/O	BD6
39	I/O	BD7
40	INPUT	NMI
41	POWER	GND
42	OUTPUT	LS2
43	OUTPUT	LS1
44	OUTPUT	LS0
45	OUTPUT	PCS6#
46	OUTPUT	PCS1#
47	OUTPUT	MAINIORES#
48	POWER	GND
49	OUTPUT	BCLKOUT
50	INPUT	MAINIODRQ0#
51	INPUT	MAINIODRQ1#
52	INPUT	MAINIORDY#
53	OUTPUT	ZRD#
54	OUTPUT	ZWR#
55	POWER	-12V
56	OUTPUT	DZINTACK#
57	INPUT	EXSCCINT#
58	OUTPUT	EXINTEN
59	OUTPUT	PCLK

Pin	Direction	Name
60	POWER	GND

5. INTERCONNECTION INFORMATION

The potential connectivity of the 6542 hardware is outlined below. Actual devices supported will depend on software support.

5.1 Coaxial Ports

The coaxial port hardware available on the base card and Coax Expansion Card will support all devices equivalent to IBM 3270 type A devices. Software will support a subset of these devices.

5.1.1 Cabling

The coax ports will support device attachment through up to 5000 feet of RG62A/U coaxial cable, as described in section V. Alternately, up to 1000 feet of Type 3 wiring may be used with an appropriate balun.

5.1.2 IBM Cabling System Compatibility

The 6542 will perform to the standards set forth by IBM for their controllers connecting to type I devices through coax, type 1, or type 2 wiring using either baluns or DPC connectors as described in the following IBM documents: "Using the IBM Cabling System with Communication Products" (GA27-3620-1), "IBM Cabling System Planning and Installation Guide" (GA27-3361-06), and "IBM Cabling System" (GA23-0206-1). Additionaly, the 6542 will support the IBM coax-to-twisted-pair adaptor as described in "IBM/ROLM 3270 Coax-to-Twisted-Pair Adaptor" (GA27-3722-02).

5.2 EIA Ports

The EIA ports on the 6542 conform to the AT&T Computer Standard 1.3 - AT&T RS-232 except that the connector sex on the 6542 conforms to the de facto industry standard rather than the AT&T specification.

5.2.1 Modem Cables

5.3 PDS Compatibility

6. POWER SUPPLY UNIT

An ASTEC SA70-X400 70-Watt switching power supply is used to meet the power requirements of the 6542 in both the United States and European countries.

6.1 Safety Standards

The 6542 complies with the following safety standards:

TABLE II-32. Safety Standards

Organization	Standard
UL (Underwriters Labs)	478
CSA (Canadian Stds Assoc.)	C22.2 No. 220
IEC (Int. Electrotechnical Comm.)	380(DIN IEC 380/VDE 0806)
IEC	435(DIN IEC 435/VDE 0805)

6.2 EMI Standards

The 6542 complies with the following EMI standards:

TABLE II-33. EMI Standards

Organization	Standard
FCC (Federal Communications Comm.)	Part 15 Subpart J Class A
DBP (West German Post Office)	Vfg.523/1969 (VDE 0871 Part 2 Class A)

6.3 Input Power Requirements

The 6542 power supply may be optioned for either U.S. or European input voltages. This is a factory-set option. Input requirements for each voltage range are outlined below:

TABLE II-34. Power Requirements

Option	Voltage Range	Frequency Range	Current
115VAC(US)	85 - 135 VAC	47 - 400 Hz	1.5A RMS
230VAC(Europe)	170- 270 VAC	47 - 400 Hz	0.75A RMS

6.4 Outputs

The ASTEC SA70-X400 provides the following output voltages at the given current levels:

TABLE II-35. Power Supply Output Voltages

Voltage	Tolerance	Current	Ripple
5.1V	3%	1-8A	50mV p-p
-5V	5%	0-0.7A	50mV p-p
12V	5%	0.5-3.5A	100mV p-p
-12V	5%	0-1A	50mV p-p

6.5 General Characteristics

Operating Temperature:
0 - 50 degrees C.

Efficiency:
70% minimum at full load.

Overvoltage Protection:
+5V output trip voltage: 5.9V to 7.0V.

Overcurrent protection:
All outputs short circuit protected.

Temperature Regulation:
0.02% per degree C.

Hold-up Time (115VAC):
>24ms at full load.

Insulation Resistance:
50Mohm minimum from input to ground and from input to output. 10Mohm minimum from output to ground.

MTBF:
Greater than 50,000 hours at full load at 25 degree C ambient temperature.

Storage Temperature:
-20 degree C to 85 degree C.

Inrush Current:
20A (115VAC) or 40A (230VAC) at 25 degree C ambient cold start.

7. ASSOCIATED DOCUMENTS

Documents described below may be referred to for further information on the 6542 Mini Controller.

7.1 Schematics

7.1.1 Base Card Schematics

7.1.2 Asynchronous Port Option Card Schematics

7.1.3 Coax Port Expansion Card Schematics

7.1.4 RAM Expansion Card Schematics

7.2 Board Drawings

7.2.1 Base Card Circuit Board Drawing

7.2.2 Asynchronous Port Option Card Circuit Board Drawing

7.2.3 Coax Port Expansion Card Circuit Board Drawing

7.2.4 RAM Expansion Card Circuit Board Drawing

7.3 Assembly Drawings

7.3.1 Base Card Assembly Drawing

7.3.2 Asynchronous Port Option Card Assembly Drawing

7.3.3 Coax Port Expansion Card Assembly Drawing

7.3.4 RAM Expansion Card Assembly Drawing

7.4 VLSI Integrated Circuit Specifications

7.4.1 80C186 Specification

7.4.2 80C186 Programmer's Reference Manual

7.4.3 CMC Specification

7.4.4 Serial Communications Controller Specification

7.4.5 Floppy Disk Controller Specification

7.4.6 Floppy Disk Controller Application Notes

7.4.7 Microfloppy Disk Drive Specification

7.5 PAL Descriptions

7.5.1 DRAM PAL

7.5.2 Bank Select PAL

7.5.3 SCC/ZBUS PAL

7.5.4 Dual Port RAM PAL I

7.5.5 Dual Port RAM PAL II

7.6 Interface Specifications

7.6.1 AT&T RS-232

7.6.2 EIA-232-D

7.6.3 CCITT V.35

7.6.4 IBM 3174/3274 Control Unit to Device Product Attachment Information

7.7 Program Document/Listing

7.8 Control Panel Print

8. OPTION CARDS

8.1 Asynchronous Port Option Card

8.1.1 General

The Asynchronous Port Option Card adds two I/O ports to the 6542 system. Both of these ports are set up for EIA-232 operation. No additional processing power is added with this card; it contains only 80C186 peripheral devices.

8.1.2 Reset

The Asynchronous Port Option Card is reset by the SCC Reset bit in the Control/Status register. The Option Card Reset bit has no effect on this option card.

8.1.3 Programming Information

The Asynchronous Port Option Card adds devices to the 80C186 I/O space. It provides no additional memory.

8.1.3.1 Serial Communications Controller

The Asynchronous Port Option Card uses an 8 MHz Z8530 Serial Communications Controller (SCC) to control its two EIA-232 ports. Both ports are set up for asynchronous operation only at a wide variety of baud rates.

8.1.3.1.1 SCC Interrupts

The SCC uses INT0 of the 80C186 in cascade mode. It is placed in the daisy chain after the base card SCC, which gives it a lower priority interrupt. The SCC must be programmed to provide the interrupt vector during the interrupt acknowledge cycle.

8.1.3.1.2 SCC Register Addresses

The four 8-bit registers within the SCC are accessed using the following addresses:

TABLE II-36. SCC Registers

Address	Register
0x2080	Channel B Command
0x2082	Channel B Data
0x2084	Channel A Command
0x2086	Channel A Data

8.1.3.1.3 EIA Status Register (0x20c1)

TABLE II-37. EIA Status Register (0x20c1 read only)

7	6	5	4	3	2	1	0
X	X	X	X	S1	D1	S0	D0

Address: 0x20c1 (Read only)

D0: (R) Port 0 (channel A) DSR
This bit is the inverted state of pin 6 of port 0.

S0: (R) Port 0 (channel A) SPEED
This bit is the inverted state of pin 12 of port 0.

D1: (R) Port 1 (channel B) DSR
This bit is the inverted state of pin 6 of port 1.

S1: (R) Port 1 (channel B) SPEED
This bit is the inverted state of pin 12 of port 1.

8.1.3.1.4 SCC Circuit Connections

TABLE II-38. SCC Circuit Connections

DB-25 Pin	EIA-232 Name	SCC Pin Name
1	AA	GND
2	BA	TxD
3	BB	RxD
4	CA	RTS
5	CB	CTS
6	CC	*
7	AB	GND
8	CF	DCD
12	CI	*
20	CD	DTR

* Pins 6 and 12 do not enter the SCC.
They may be read using the EIA status register.

8.1.3.1.5 SCC Baud Rate Table

Both ports of the SCC support a wide variety of asynchronous baud rates based on a 3.6864 MHz clock coming in on the RTxC pin. The following clock modes and time constants are recommended for producing the different baud rates. The T/R column gives the EIA RS-404 performance category for the transmitter and receiver, respectively.

TABLE II-39. SCC Baud Rate Table

Baud Rate	T/R	Clock	Clock Mode
50	1/A	RTxC	x64
75	1/A	RTxC	x64
110	1/A	RTxC	x64
134.5	1/A	RTxC	x64
150	1/A	RTxC	x64
300	1/A	RTxC	x64
600	1/A	RTxC	x64
1200	1/A	RTxC	x64
1800	1/A	RTxC	x64
2000	2/B	RTxC	x32
2400	1/A	RTxC	x64
3600	1/A	RTxC	x64
4800	1/A	RTxC	x64
7200	1/A	RTxC	x64
9600	1/A	RTxC	x64
19200	1/A	RTxC	x32

8.1.3.2 Card Type Register (0x2300)

This is a read-only register that will identify the option card as an Asynchronous Port Option Card. This register should not be written to unless the card is being used as a CDB Development Option Card (see below).

TABLE II-40. Card Type Register (0x2300 read only)

7	6	5	4	3	2	1	0
0	0	0	1	X	X	X	X

Address: 0x2300 (Read only)

8.2 Self-Test Information

The following table shows the tests done on the Asynchronous Port Option Card and the location of their results in the error table.

TABLE II-41. Self-Test Result Codes

Word	Device Tested	Bit	Error Type
24	Port A	0	Transmit buffer empty bit error
		1	Receive buffer full bit error
		2	Data error
		3	Int mode: transmit buffer empty bit error
		4	Int mode: interrupt did not occur
25	Port B	0	Transmit buffer empty bit error
		1	Receive buffer full bit error
		2	Data error
		3	Ext loopback: DTR,RTS,DSR, or SPEED error
		4	Ext loopback: DTR,RTS,DCD, or CTS error
26	Not Used		
27	Not Used		
28	Not Used		
29	Not Used		
30	Not Used		
31	Not Used		
32	Not Used		

8.3 CDB Development Card

The CDB Development Card is built on the same board as the Asynchronous Port Option Card. The only difference is that the CDB card has an option strap soldered on to cause the Card Type Register to return a different value. The CDB card also has the NMI Register (described below). This register is present on the Asynchronous Port Option Card but is not mentioned in the above section because it is not intended for use on that card.

8.3.1 Card Type Register

This is a read-only register that will identify the option card as a CDB Development Card.

TABLE II-42. Card Type Register (0x2300 read only)

7	6	5	4	3	2	1	0
0	0	0	1	X	X	X	X

Address: 0x2300 (Read only)

8.3.2 NMI Register

TABLE II-43. NMI Register (0x2300 write only)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	N

Address: 0x2300 (Write only)

N: NMI Enable, Active Low

A zero in this position causes the SCC interrupt to be directed to the NMI input to the 80C186 instead of INT0. INT0 is not used in this case. When the Option Card Reset bit of the Control/Status Register is active, the NMI Enable bit is set to a one.

SECTION III

ADJUSTMENTS AND LUBRICATION

1. ADJUSTMENTS

No adjustments are required for the controller.

2. LUBRICATION

No lubrication is required for the controller.

SECTION IV

MANUFACTURING INFORMATION

1. ASSEMBLY

All parts of the 6542 controller are to be manufactured as specified in MR2029.

1.1 FCC Part 15J Compliance

No special parts or procedures are required for compliance to FCC Part 15J Regulations governing EMC.

1.2 Base Unit

The 6542 base unit is to be assembled using the parts listed in the CPR for comcode 501009120 as shown in drawing 501009120 (56C801AAA).

1.3 RAM Expansion Card

The RAM Expansion Card for the 6542 is to be assembled using the parts listed in the CPR for comcode 501009112 as shown in drawing 524104197.

1.4 Coax Expansion Card

The Coax Expansion Card for the 6542 is to be assembled using the parts listed in the CPR for comcode 501009104 as shown in drawing 524104189.

1.5 Asynchronous Port Option Card

The Asynchronous Port Option Card for the 6542 is to be assembled using the parts listed in the CPR for comcode 501009138 as shown in drawing 524104171.

2. TESTING

2.1 Burn-in Requirements

The 6542 is to be manufactured per MR2029 as a group 3 unit. All 6542 controller components shall be burned in per MR2029 prior to assembly. Controllers failing system test mat be repaired using replacement assemblies which have been burned in per MR2029. Following system test, randomly selected 6542 controllers shall receive an additional burn in. Samples will be taken from production each week and burned in for 96 hours at room temperature. Sample sizes and acceptable failure rates will be determined by current production levels in accordance with the corporate Reliability Test Plan dated March 5, 1985. (???)

2.2 Initial Operability and Failure Rate

The initial operability of the base unit as shipped shall not be less than 99% (minimum long term average). The initial operability of the expansion and option cards as shipped shall not be less than 99.5%. The quality assurance organization will audit the product for conformance to this specification by an appropriate statistical sampling plan.

2.3 System Test

A complete test of the 6542 and peripheral cards will include the ROM-based self-test, a test of the floppy drive interface, and a test of the external I/O ports.

2.3.1 Self-Test

The ROM-based self-test is entered by pressing the self test button or by placing the controller in loopback test mode using a hardware strap (see section II.3.2) before power up. This will test most of the hardware on the base and option cards and report the results through the test LED and the diagnostic port. If the test fails, the self-test LED is turned and the error table is transmitted out the diagnostic port asynchronously at 9600 baud.

2.3.2 Floppy Drive Interface

The ROM-based self test does not read and write to the floppy. To test this interface, an additional test must be devised. Reading, writing, and formatting should be tested over the entire range of tracks.

2.3.3 EIA Ports

The control-panel-initiated self test tests only up to the SCC. Loopback self test, which requires special loopback plugs (see section II.3.2), will test out to the DB-25 connectors, but does not test the transmit and receive clocks. Either EIA or V.35 operation will be tested for the synchronous port, depending on the position of the jumper. To test both, the test must be executed twice. A complete test must include a test of the transmit and receive clocks for both EIA and V.35 operation. This test will be devised by the testing organization.

2.3.4 Coax Ports

The coax ports on the base card and the coax expansion card are not completely tested by self test. To completely test them, a test must be devised which requires each port to transmit and receive through 5000 feet of coaxial cable (RG62A/U) or an attenuator which will simulate the effect of this length of cable. The test should also exercise the TPC connectors by transmitting and receiving through 2000 feet of IBM type 1 twisted pair cable.

2.3.5 Asynchronous Ports

The ports on the Asynchronous Port Option Card are completely tested by the ROM-based self test in loopback mode using appropriate loopback plugs because these ports have no clock leads.

SECTION V

INSTALLATION INFORMATION

1. BASE UNIT

1.1 Cabling

Cables attached to the 6542 base unit must comply with the following rules.

1.1.1 EIA Cables

The 6542 base unit EIA ports use male DB-25 connectors set up as DTE. See Table II-18 for pinouts. A maximum of 50 feet of cable is allowed on either EIA port.

1.1.2 V.35 Cables

The synchronous host port on the 6542 base unit may be configured for V.35 operation using a jumper plug on the base board, as shown in Figure V-1. See Table II-18 for pinouts. When configured for V.35, an adaptor cable must be used. The part number of the adaptor cable is XXXXXXXXX. The maximum length of V.35 cable is 100 feet.

1.1.3 Coaxial Cables

Coaxial cabling schemes must meet the following specifications.

1.1.3.1 Type

Coaxial cabling must be of the RG62A/U type.

1.1.3.2 Length

Up to one mile (5280 feet) of coaxial cable is allowed.

1.1.3.3 Power Line Separation

Coax cabling must not be run in the same conduit as power lines. Coaxial cables should be separated from power lines as shown in the table below.

TABLE V-1. Coaxial Cabling and Power Lines

Power Line Voltage	Coax and/or Power Lines		
	Neither in grounded conduit	One in grounded conduit	Both in separate grounded conduits
< 2 kVA	5 inches	2.5 inches	1.2 inches
2 - 5 kVA	12 inches	6 inches	3 inches
> 5 kVA	24 inches	12 inches	6 inches

1.1.3.4 Lighting Fixture Separation

Coaxial cable should remain at least 5 inches from all lighting fixtures.

1.1.3.5 Grounding

The coaxial cable's outer conductor or shield must not be grounded, and must not be connected to the shield of any other coaxial cable. This means that when two cables are spliced (i.e. connected together with a BNC metal adapter), the BNC adapter and connector must not be grounded. They must be protected with a plastic type sleeve. If the BNC is brought to a patch panel, the panel must be a non-conductive type.

1.1.3.6 Cable Network

There should only be one coaxial cable, with a maximum of 13 splices, connected between the device and the controller. There should not be tee connection and there should not be any unterminated cables.

1.1.3.7 Cable Connections

All splices and patches must maintain a low resistance path on both the center conductor and the shield conductor. The resistance between the center conductor and shield must be maintained at greater than 100kohms.

1.1.3.8 Loop Resistance

With the shield and center conductor shorted together at the far end, the D.C. resistance looking down the cable at the near end (between center conductor and shield) should be approximately 47 ohms/1000 feet of cable.

1.1.3.9 Minimum Radius

The coaxial cable should not be bent to a radius smaller than 10 times the diameter of the cable.

1.1.3.10 Heat Dangers

The coaxial cable should not be installed in close proximity to 'hot spots', such as steam or exhaust pipes.

1.1.3.11 Crimped Connections

Use of crimped connections on coaxial cable is highly recommended. If the shield is improperly crimped to the BNC, an intermittent connection can occur, which could increase the system error rate.

2. EXPANSION CARDS

2.1 RAM Expansion Card

The RAM Expansion Card should be installed as shown in Figure IV-1.

2.2 Coax Expansion Card

2.2.1 Installation

The Coax Expansion Card should be installed as shown in Figure IV-2.

2.2.2 Coax Cabling

The coax cabling for the Coax Expansion Card must meet the same specifications as the coax cabling for the base unit.

3. OPTION CARDS

3.1 Asynchronous Port Option Card

3.1.1 Installation

The Asynchronous Port Option Card should be installed as shown in Figure IV-3.

3.1.2 Cabling

Cabling for the Asynchronous Port Option Card must meet the same specifications as the EIA cabling for the base card.

Figure V-1. Jumper Plugs for EIA/V.35 Selection

Figure V-2. RAM Expansion Card Installation

Figure V-3. Coax Expansion Card Installation

Figure V-4. Asynchronous Port Option Card Installation

SECTION VI

SERVICING INSTRUCTIONS

1. FIELD REPLACEABLE ITEMS

The following table lists the 6542 components that are considered field replaceable. These items may be required in field repair of the units.

TABLE VI-1. Field Replaceable Items

Part Name	Comcode
Power Supply	523483493
Floppy Drive	
Base Card	
RAM Expansion Card	501009112
Coax Expansion Card	501009104
Asynch Option Card	501009138
Fan	
Door Assembly	
AC Line Cord	
Power Switch	
Line Filter	
Base Board Power Cable	
Floppy Power Cable	
Floppy Data Cable	

2. DIAGNOSTIC PROCEDURE

The following procedure may be used to identify and correct problems with the 6542 controller.

2.1 Check Power

Plug the unit in and turn on the power switch. Look at the power LED on the outside of the door. If it is on, go to 2.2. If it is off, go to 2.1.1.

2.1.1 Check Power Supply Output

Remove cover from unit. Using voltmeter, check voltage on the power supply output connector between the +5V and ground pins, being careful to not touch other parts of the power supply

which may contain dangerous voltages. If the reading is between 4.75 and 5.25 volts, go to 2.1.2. If any other voltage, go to 2.1.1.1.

2.1.1.1 Check Input Voltage

Using voltmeter, check voltage at input to power supply. If the voltage is the expected power line voltage, go to 2.1.1.2. If the voltage is any other value, go to 2.1.1.1.1.

2.1.1.1.1 Check Power Source

Check voltage at wall outlet and at cabinet input. Replace either line cord or power supply as required.

2.1.1.2 Check Power Supply

Disconnect power cable from base card and plug into spare base card. Check power supply output again. If output is between 4.75 and 5.25 volts, go to 2.1.1.2.1. If output is any other value, replace power supply.

2.1.1.2.1 Check Base Card

Disconnect control panel, option cards, and all cables from base card. Plug power cable back into base card. Measure power supply output voltage. If output is not between 4.75 and 5.25 volts, the base card has a power short and must be replaced. If the output is between 4.75 and 5.25 volts, the power short is on one of the peripherals. Plug them back in one at a time until the voltage goes out of range. Replace the device that drives the voltage out of range.

2.1.2 Check Power Cable

Check voltage between the same wires at the other end of the cable on the base card. If the voltage is between 4.75 and 5.25 Volts, go to 2.1.3. If the voltage is any other value, replace the power cable.

2.1.3 Check Control Panel

Because +5V is good on the base card and the power LED is not on, there must be a problem with either the base card or the control panel. Replace Control Panel. If the Power LED comes on, this was the problem. If the LED does not come on, replace the base card.

2.2 Run Self Test

Push the self test button on the control panel. The Test LED should begin flashing and flash through the entire test (at least 1 minute). If the LED does not flash, go to 2.2.1. At the end of the test, the light will either stay on or stay off to indicate a pass or a failure, respectively. If self test fails, go to 2.3. If self test passes, go to 2.4.

2.2.1 If self test does not run...

If the LED does not flash after the self test button is pressed, replace the control panel. If trouble persists, either the base card is failing in such a way that it cannot even begin the test, such as failing the initial RAM or ROM tests, or it is not starting the test. Both point to base card problems, or possibly a power supply problem. Replace base card and/or power supply.

2.3 Self Test Fails

If self test has failed, the Test LED will remain off after self-test has been executed. When the controller is in this state immediately after self test, before powering down or pushing any other buttons, push the Off-Line button to request a report of which cards failed. After the Odd-Line button has been pushed, the Test LED will flash a number of times to indicate which card has failed. If several cards have failed, each time the Off-Line button is pushed one of the failed cards will be reported. To see all of the failures, repeat the procedure of pushing the button and counting the flashes until the first failure is reported again. The controller will continue to cycle through the failures as the button is pressed. The following table shows the failures indicated by the flashing Test LED.

TABLE VI-2. Field Error Reporting

No. of Flashes	Cards Failing
0	Test error: Control Panel or Base Card or Power Supply
1	Base Card
2	Base Card or RAM Expansion Card
3	Base Card or Coax Expansion Card
4	Base Card or Option Card
>4	Test error: Base Card or Power Supply

2.4 Self Test Passes

Self Test does not test everything in the system. Problems with the EIA and coax connecters will not be detected by the normal self test. If the customer complaint involves specific ports, it is likely that either they are bad or the customers cabling is bad. Customer cabling problems may be detectable by connecting their cables to known working ports. Replace card with offending ports as necessary. If the customer complaint involves intermittant operation or a fan fail warning, check that the fan is working. If not, replace fan or power supply as necessary.