22

DATA SYSTEMS
STATION
DATA TEST SET NO. 911NA

CHANGES

B. Changes in Apparatus (Components)

B.1 Added

Capacitor C69,
KS-20676, L1, 560 pF,
App Fig. 1

Lamp DS1,
Marco Oak 22-35380-6P19-211,
Equipped with A1B Neon Lamp,
Option Y, App Fig. 1

Resistor R2,
KS-20289, L6C, 68.1 Kilohms,
Option Y, App Fig. 1

Terminals TP1 through TP4,
Cambion Corp 571-4115-1-0519,
Option X,
App Fig. 1

B.2 Removed

Diode CR8,
HP 5082-4882,
Option Z, App Fig. 1

B.3 Superseded	Superseded by
Diodes CR1 through CR7 and CR9 through CR25, HP 5082-4882, Option Z, App Fig. 1	Diodes CR1 through CR7 and CR9 through CR25, 541A, Option Y, App Fig. 1
Cord PWR, Belden 17239, App Fig. 1	Cord PWR, KS-20340, L1, App Fig. 1
Jacks J7 through J10, Switchcraft L111, App Fig. 1	Jacks J7 through J10, KS-21546, L1, App Fig. 1
Terminals E3 through E17 and E20, Cambion Corp, 571-4115-1-0519, App Fig. 1	Terminals E3 through E17 and E20, Cambion Corp, 1511-1-01-10, App Fig. 1

D. Description of Changes

D.1 The 120V ac power ON indicator was powered by the output of the rectifier. This arrangement is replaced by a neon lamp indicator switched directly across the ac line when power is turned on. Option Y is assigned to the new arrangement and option Z is assigned to the previous arrangement. Option Z is rated Mfr Disc.

D.2 The ac line power cord is changed to PVC yellow cord for improved strength and visibility.

D.3 In Note 205, the following is added: Wiring to test points TP1 through TP4 (option X) shall be No. 24 AWG, or heavier.

D.4 In Note 206, the following is added: (f) Resistor R2 and Lamp DS1.

D.5 In Note 206, paragraph (c), remove reference to terminals E15 and E17. These terminals do not require insulation.

D.6 Note 207 is changed as follows:

207. All spare leads on connectors J1 through J8, as shown in App Fig. 1, shall be left at original length, taped, and stored.

D.7 On CP1, capacitor C69 is added at the output of IC25. All units manufactured are equipped with capacitor C69.

D.8 The connector table on App Fig. 1 is changed to indicate spare and unequipped terminals.

D.9 Shielded cables are replaced by twisted wires. Option V is assigned to the new arrangement and option W is assigned to the previous arrangement. Option W is rated Mfr Disc.

D.10 Note 202 is changed as follows: Polarity information for CR1 through CR25 (option Z) is as follows:....

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DEPT 3116-PE-JES

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DATA SYSTEMS STATION DATA TEST SET NO. 911NA

CHANGES

B. Changes in Apparatus (Components)

B.1	Superseded	Superseded By
	Jacks J7 through J10, Switchcraft N111, App Fig. 1	Jacks J7 through J10, Switchcraft L111, App Fig. 1
	Y2 Oscillator, Vectron Lab. Inc. CO-231, See Note 105, CPS3	Y2 Oscillator, Vectron Lab. Inc. 231-2405, 180.000 KHz, CPS3
	Y3 Oscillator, Vectron Lab. Inc. CO-231, See Note 105, CPS3	Y3 Oscillator, Vectron Lab. Inc. 231-2405, 105.000 KHz, CPS3

D. Description of Changes

D.1 On FS1, sheet B3, remove the word "OPTIONAL" from XTAL OSC Y2 and Y3. Frequency information is added to the Y2 and Y3 XTAL OSC.

D.2 On CPS3, sheet J3A, change function designation on pins 4 and 6 of connector P5.

D.3 On FS1, sheet B3, remove function designation from pins 13, 14, and 22 of connector P5.

D.4 On FS1, sheet B3, change function designation on pins 4, 6, 17, and 18 of connector P5.

D.5 On FS1, sheet B5, change wiring of the BAUD switch.

D.6 On FS1, sheet B5, remove ground from shielded cables.

D.7 Remove Note 105 from sheet D1.

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DEPT 3116-PE-JES

DATA SYSTEMS
STATION
DATA TEST SET NO. 911NA

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The 911NA data test set is a portable electronic set designed to provide an accurate source of data test signals, with precise control of the type and amount of distortion, as required, and a means of accurately measuring data signal degradation of Baudot and ASCII (American Standard Code for Information Interchange) codes from 45.5 to 1800 baud with a variety of input and output modes of operation.

1.02 The set combines integrated circuitry including read-only-memories. Light-emitting diodes are used for information displays. Several new functions in addition to the features provided by the existing 911A data test set are provided.

2. GENERAL DESCRIPTION OF OPERATION

GENERAL

2.01 The test set is a portable electronic test instrument 10 inches high, 12 inches wide, and 6 inches deep, and weighs under 20 pounds. It is equipped with a self-contained power supply operating from 105 to 135 volts at 50 to 60 Hz.

2.02 The cover provides storage for patch cords which are supplied with the set and contains an information plate which displays 5- and 8-level code charts and a baud rate table for the BAUD switch. In addition, this cover provides storage for the 911P EIA test adapter.

2.03 The test set provides 5-element Baudot code with stop-pulse lengths of 1.0, 1.42, or 1.5 elements, or 8-element even parity ASCII code with stop-pulse lengths of 1.0 or 2.0 elements. Thirteen selectable crystal-controlled speeds are provided ranging from 45.5 to 1800 baud. Tables A and B show the baud rates and codes provided by the test set. Provision has been included for two additional baud rates as determined by customer-provided clocks and for using an external clock source.

TABLE A

BAUD SWITCH

Switch Position	Baud	Switch Position	Baud
1	45.5	11	1050.0
2	56.9	12	1200.0
3	61.12	13	1800.0
4	74.23	14	Spare
5	75.0	15	Spare
6	110.0	16	Spare
7	134.46	17	Optional
8	150.0	18	Optional
9	300.0	19	*
10	600.0	20	External Clock

*Position 19 is strapped to position 20.

TABLE B

CODES

Code	Description
5/7.0	5-element code with 1.0-bit stop pulse.
5/7.42	5-element code with 1.42-bit stop pulse.
5/7.5	5-element code with 1.5-bit stop pulse.
8/10	8-element code with the eighth information bit coded for even parity and with 1.0-bit stop pulse.
8/11	8-element code with the eighth information bit coded for even parity and 2.0-bit stop pulse.
8/11M	8-element code with the eighth information bit kept marking and 2.0-bit stop pulse.

To reduce the size and cost and to simplify its operation, the BAUD and CODE switches are common to the transmitting and receiving sections of the test set. Thus the generating and measuring sections are always set for the same code and speed.

2.04 The test set will generate and measure marking, spacing and switched bias, marking, spacing and switched end distortion and combination switched distortion ranging from 0 to 49 percent in 1-percent increments.

2.05 The receiving circuit output is digitally displayed on a 2-digit light-emitting diode numeric display. One digit is used for units and the other for tens. An indication of the type of distortion is displayed on light-emitting diodes.

TRANSMITTING SECTION OF CIRCUIT

2.06 For Baudot code, the following 80-character per line test sentence is generated.

THE QUICK BROWN FOX JUMPED OVER A LAZY DOGS BACK 1234567890 A1A TESTING

The sentence is preceded by four nonprinting characters:

LETTERS, CARRIAGE RETURN, LINE FEED, LETTERS.

The A1A character sequence is used to check the teletypewriter's ability to shift from the letters mode, to the figures mode, to the letters mode at line speed.

2.07 For ASCII code, three selectable line lengths of test message are provided.

(a) A short 38-character per line test sentence (S) is generated. This line length is intended to be used for testing sprocket-feed teletypewriters which print a limited number of characters per line,

such as machines used to prepare customer service orders. The characters printed are:

THE QUICK BROWN FOX JUMPED OVER A

(b) A normal 77-character per line test sentence (N) is generated.

THE QUICK BROWN FOX JUMPED OVER A LAZY DOG'S BACK 1234567890 TESTING 0123.

(c) A long 137-character per line test sentence (L) is generated. This line length is provided for testing teletypewriters equipped with wide platens.

THE QUICK BROWN FOX JUMPED OVER A LAZY DOG'S BACK 1234567890 TESTING 0123 THE QUICK BROWN FOX JUMPED OVER A LAZY DOG'S BACK TEST 0123.

The sentences are preceded by four nonprinting characters:

DELETE, CARRIAGE RETURN, LINE FEED, DELETE

2.08 A selectable 1-, 2-, or 3-character message for testing selective calling stations in either Baudot or ASCII code may also be generated. Selection is made via the manual setting of three groups of eight switches. In addition, SKIP switches are provided for the second and third characters. Appropriate positions of the switches are easily determined by referring to the code charts provided inside the cover of the test set.

2.09 In the idle or stop state, the generator output is marking (STEP-STOP-START switch in STOP position). A space condition may be generated by pressing the nonlocking SPACE switch.

2.10 Output distortion of the following types may be generated in 1-percent steps from 0 to 49 percent, as controlled by the DIST 1 percent and DIST 10 percent switches and the TYPE DIST switch.

(a) Marking bias (MB) distortion is generated when the space-to-mark transitions are displaced before their proper time occurrence in relation to the beginning of the start pulse.

(b) Spacing bias (SB) distortion is generated when the space-to-mark transitions are displaced after their proper time occurrence in relation to the beginning of the start pulse.

(c) Switched bias (SWB) distortion is generated by alternating the MB and SB distortion every other character.

(d) Marking end (ME) distortion is generated when the mark-to-space transitions are displaced after their proper time occurrence in relation to the beginning of the start pulse.

(e) Spacing end (SE) distortion is generated when the mark-to-space transitions are displaced before their proper time occurrence in relation to the beginning of the start pulse.

(f) Switched end (SWE) distortion is generated by alternating the ME and SE distortion every other character.

(g) Switched combination (SWC) distortion is generated by alternating the MB, SB, ME, and SE distortion in each sequence of four characters.

2.11 Output status of the generator is displayed on the SIGS (signals) light-emitting diode (LED). The LED is lit when the output is marking, extinguished when the output is spacing, and flickers when the set is transmitting signals.

2.12 The RESET switch, when activated, clears all counters and prepares the test sentence generator to transmit the 3-character selectable messages or fox sentences from the beginning.

2.13 Stepped or continuous outputs are provided by the STEP-STOP-START switch. When in the START position and generating fox signals, the circuit will transmit continuously; or when generating the selectable message, the generator will stop at the end of 1-, 2-, or 3-character selected message depending on the position of the SKIP switches. The circuit will transmit one character at a time each time the switch is activated to the STEP position.

2.14 The REPEAT switch, when operated to the ON position, disables the address counters and causes the generator, if generating fox signals, to transmit the same character repeatedly; or if generating the selectable message, to generate the message repeatedly.

2.15 Element (EL) and character (CH) framer pulse appearances are provided on the front panel to provide synchronization with other test equipment, as required by the user.

2.16 Output information from the generating section of the set is in the form of LV hub or EIA voltage which appears at VOLT OUT (LV hub or EIA) jack. A solid-state keyer is provided for keying polar and neutral loops up to 260 volts at 62.5 milliamperes. The keyer should not be used above 150 BAUD of operation. The neutral loop output appears at LP driver T- and T+ jacks. T- has a negative battery on the tip and T+ has a positive battery on the tip.

2.17 The INPUT switch, when set to the TST position, will internally connect the send and receive sides of the test set together on a voltage basis, thus elminiating the necessity of a patch cord for making back-to-back tests. When transmitting to an external circuit, this switch position will permit the monitoring of the transmitted signals as may be required by the user.

RECEIVING SECTION OF CIRCUIT

2.18 The measuring portion of the test set will recognize either odd or even parity errors. The receipt of a parity error will, under control of the PARITY switch, light the PARITY ERROR LED. The LED may be extinguished by momentarily setting the PARITY ON-OFF switch to the OFF position or by depressing the RESET switch.

2.19 The DISCR % switch is used to determine the operating point of the type of distortion LEDs. Only an amount of distortion exceeding the 0-, 3-, 5-, 7-, 10-, or 15-percent setting of the switch will light the appropriate distortion LED. This switch has no effect on the numeric display.

2.20 The FILTER switch, when placed in the IN position, prevents spurious impulses, such as those introduced by contact bounce, from being recognized as actual distortion in the incoming signal, and being displayed as such. Any transient shorter than approximately 0.1 millisecond is thus disregarded by the measuring set.

2.21 The test set will measure both synchronous and asynchronous (start/stop) data signals as determined by the ASYNC/SYNC switch. In the SYNC position, the 911NA measures distortion on a bit-by-bit basis instead of on the character-by-character basis used for asynchronous measurements. Since the clock rate required by the test set is 100 times the baud rate, clock pulses from a synchronous type data set cannot be used as a source of external clock signals.

2.22 A character recognition feature will indicate, on a LED display, the state (mark or space) of each element of successive characters as they are received, to provide character identification. When receiving Baudot code, one character is displayed, and for ASCII code, both present and immediately preceding characters are shown. Code tables provided inside the cover of the set will assist in translating the display to discrete characters.

2.23 The type of information displayed on the 2-digit light-emitting diode DISPLAY is determined by the setting of the DISPLAY switch. When set to PK, the highest percent of received signal distortion is displayed and held until manually reset. In the AUTO PK position, the DISPLAY will be automatically reset for each 16 characters received. In the COUNT PK position, the set will count overall distortion hits above the percentage level as determined by the setting of the DIST PKS switch. The PK CNT position will program the set to count only end distortion hits above the setting of the DIST PKS switch. In the PAR CNT position, the set will count the number of parity errors received. In the count positions, the set will count to a maximum of 99 and must be manually reset via the RESET switch.

2.24 The INPUT switch is used to select the proper circuitry for compatibility with the input signal. Voltage signals in the form of high voltage hub (No. 2 hub) or EIA are received via the VOLT INPUT jack. The EIA LOW position is used for normal EIA signals while the EIA HIGH position provides a high impedance input for bridging on circuits without signal interference. Neutral current signals of 4, 10, 20, or 60 milliamperes may be measured via current input T- (negative on tip) or T+ (positive on tip) jacks. In the TST position, the measuring set circuitry is disconnected from the input interface and connected to the VOLT OUT EIA jack on the transmitting side of the test set for making back-to-back tests without the use of a patch cord. Input protection for the current inputs provides a short circuit and lights the OVERLOAD LED when the input current exceeds approximately 90 milliamperes.

2.25 Input status of the measuring set is displayed on the SIGS (signals) LED. The LED is lit for a marking input, extinguished for a spacing input, and flashing when the receiver is receiving signals.

SECTION II - DETAILED DESCRIPTION

1. TEST SENTENCE GENERATOR (CP1)

CHARACTER FRAMER

1.01 $\overline{\text{Clock}}$ input on pin 21 is passed via gate IC57C to the element and character framer circuit. Assuming the cascaded up/down counters IC32 and IC33 and the JK flip-flop IC55A have been previously reset, clock pulses pass through gate IC56D to the count-up input of the counters. The output of the counters produces a negative transition pulse for counts of 0, 42, and 50 clock pulses at the outputs of gates IC31, IC30, and IC29 respectively. The 50 pulse, via gate IC56C and inverter IC27C, clocks the JK flip-flop IC55A, reversing its output state which disables gate IC56D and enables gate IC56B, transferring the clock to the count-down input of the two counters. As the counters count down past 42, a second 42 pulse is produced by IC30. When the count reaches 0, the 0 pulse from gate IC31, via gate IC56C and inverter IC27C, will again clock the JK flip-flop IC55A restoring its output to the original state, disabling gate IC56B and enabling gate IC56D. Thus, the counting cycle starts again with output pulses being produced for a count of 0, 42, 50, 42, 0, 42..., etc, clock pulses, and a 0 pulse being generated for each 100 clock pulses. The interval between 0 pulses corresponds to the length of one bit.

1.02 Character length is determined by the character framer counter IC59. The counter is used as a programmable divider by being preset to a predetermined number by outputs 1, 7, and 14 of the diode matrix IC51 and, employing the 0 pulse as a clock (element pulse) will produce a max/min (high) output when sequences to the maximum count of 15. The CODE switch position, diode matrix output, and preset numbers are shown in Table C.

TABLE C

Code	Diode Matrix Terminal No.								Preset Number
	1	7	14	12	10	9	13	8	
7.0	L	L	L	H	L	H	L	L	8
7.42	H	H	H	H	L	L	H	L	7
7.5	H	H	H	H	L	L	L	H	7
8/10	H	L	H	L	H	H	L	L	5
8/11	L	L	H	L	H	H	L	L	4
8/11M	L	L	H	L	H	H	L	L	4

1.03 The max/min (high) output combined with a 0, 42, or 50 pulse via gate IC52D, produces a negative transition corresponding to the length of one character (character pulse). The selection of a 0, 42, or 50 pulse is determined by outputs 9, 13, and 8 of diode matrix IC51 which controls gates IC53B, IC53A respectively. The negative pulse triggers a pulse-forming circuit consisting of flip-flops IC54A and IC55B and gate IC58B. The output consists of a negative pulse of one-half clock pulse duration. This pulse, referred to as a reset pulse, appears at the end of each character. The pulse also appears in inverted form via inverter IC28A and buffer IC44F. The transition is employed throughout the circuit for synchronization purposes.

1.04 The element and character framer pulses appear at the E1 and CH jacks on the front panel via buffer gates IC70D and IC70F.

STEP-STOP-START CIRCUIT

1.05 Circuit character generation is controlled by the STEP-STOP-START switch and the associated flip-flops employed to overcome switch bounce. When operated to either the START or STEP position, the circuit will generate a reset pulse to synchronize the circuit in addition to enabling character generation. In the STOP position, the output of the D flip-flop IC54B is low, disabling gate IC57C. The output of gate IC53D is high. When operated to the STEP position, the output of gate IC56A goes high triggering multivibrator IC61. The 7-millisecond negative pulse clocks the D flip-flop IC54B, whose output changes to high enabling gate IC57C and allowing the passage of clock pulses to the element and character framer circuits. The negative pulse of IC61 output also triggers IC62, whose 1-microsecond negative transition via inverter IC53D resets the circuit prior to the generation of the character. The circuit is stopped during the stop pulse by the max/min pulse if generating odd stop-pulse codes or by a delayed max/min pulse (developed via IC50C and IC50D gates) if generating unit length stop-pulse codes via lead W, thus triggering multivibrator IC60. Its 15-microsecond positive-output pulse, via gate IC58C, sets flip-flop IC54B disabling gate IC57C and preventing the passage of clock pulses to the element and character framer circuits.

1.06 When operated to the START position, circuit operation performs as explained above except there is a low input to gate IC58C from flip-flop IC49A, and IC49B prevents the passage of the positive pulses from IC60 until the switch is restored to the STOP position. This will enable gate IC58C, allowing the pulse from IC60 to set IC54B as previously described.

CHARACTER GENERATION

1.07 Character generation is performed by the read-only-memory IC3. Its output is determined by the eight inputs from the binary counters IC1 and IC2. The information stored in the read-only-memory is

permanently programmed into the device at the time of its manufacture. Once the information is entered it cannot be changed; it can however, be read out as often as desired. Each alphanumeric character is represented by a binary number. Table D describes the generation of the "Quick Brown Fox" test message.

TABLE D

Address (Binary Input)	Output
1-81	80-character per line Baudot code
88-126	38-character per line ASCII code, called the short message (S)
88-165	77-character per line ASCII code, called the normal message (N)
88-225	137-character per line ASCII code, called the long message (L)

Test sentence selection is determined by the LINE LENGTH switch as well as the CODE switch. For those codes generating the Baudot code, a ground via lead F from diode matrix IC51 disables gates IC11, 12, 13, and 14, permitting circuit operation via gates IC69B and IC14B. Max/min pulses, via gate IC52C and lead G, clock counters IC1 and IC2 resulting in the binary output programming of the read-only-memory. When a count of 81 is reached, gate IC69B is enabled. The negative transition of its output clears the D flip-flop IC68B, applying a ground via Q4 transistor to diode matrix IC15. The matrix output programs counters IC1 and IC2 for the binary number 1. The output of diode matrix IC15 is shown in Table E.

TABLE E

Input	Diode Matrix Terminal Numbers							
	Output							
	1	7	14	8	13	9	12	10
6	L	L	L	H	H	L	H	L
4	L	L	L	H	H	L	H	L
11	L	L	L	H	H	L	H	L
2	H	L	L	L	L	L	L	L

In addition, the negative output of gate IC69B via driver IC10B, plus an inverted clock pulse, produces a negative spike at the output of the D flip-flop IC9A. This negative spike loads the binary number into counters IC1 and IC2. The reset pulse at the end of the 81st character sets the D flip-flop IC68B. Subsequent max/min pulses sequence the counters until a count of 81 is reached again. The program counters are again reset to 1 and the generation of the Baudot test message begins again. The RESET switch is also used to reset the circuit by simulating a count of 81 via gate IC14B, which is in parallel with gate IC69B and in addition creates the negative spike necessary to reload the program counters. Generation of ASCII code disables gates IC69B and IC14B and enables gates IC11 and IC12, or IC13 and IC14, depending upon the position of the LINE LENGTH switch. The program counters will therefore be reset to a count of 88 from a count of 125 via gate IC11, 165 via gate IC13, or 225 via gate IC12. The circuit may also be reset as previously described. The REPEAT switch, when operated to the ON position, disables gate IC52C, inhibiting the counting sequence of counters IC1 and IC2. The fixed output from the counters maintains the same program input to the read-only-memory, thus generating a repeated character.

1.08 The output of the read-only-memory is passed via gates IC4A through IC5B to the shift registers IC6 and IC7. Parallel input is clocked out serially via lead A. The 0 pulse, via inverter IC26B and gate IC52A, is used as the clock signal input via lead C. Gate IC52A disables the clock pulse at the step-to-start transition of the generated signal by a blanking pulse formed by the D flip-flop IC39B. The reset pulse, via lead D, is employed instead to determine the end of the character transition and to load the next character into the shift registers.

1.09 The selectable 1-, 2-, or 3-character message is selected by placing the FOX-CHAR switch in the CHAR position which inhibits the read-only-memory output by disabling gates IC4A through IC5B, and enables gates IC65A, IC65B and IC65C. Delayed max/min pulses on lead W clock the 1, 2, or 3 counter consisting of JK flip-flops IC63A and IC63B, and gates IC64B, IC64C, and IC64D. The count is dependent upon the position of the SKIP switches which, when operated to the SKIP position, disable their associated gates. Character sequence is controlled via gates IC65A, IC65B, and IC65C and buffers IC44B, IC44D, and IC44C, respectively. The outputs of these buffers control three groups of diodes, CR2-CR25. Switches 1-1 through 1-8, 2-1 through 2-8, and 3-1 through 3-8, when

operated to position M, provide marking bits at the inputs of the shift registers IC6 and IC7 via diodes CR2-CR25. Upon completion of counting, a negative pulse output clears the counters and via inverter IC8B and gate IC58A sets flip-flop IC54B.

PERCENT DISTORTION GENERATION

1.10 The percent of output distortion is determined by the settings of the DIST 0-9 and DIST 0-40 switches which control diode matrices IC16 through IC20, their associated gates, gate IC25, and inverter IC26D to produce a positive pulse one-half a clock pulse in width. This pulse will appear either between 0 percent to 49 percent during the count-up sequence, or 49 percent to 0 percent during the count-down sequence of counters IC32 and IC33, as determined by the input on lead I and the position of the two switches. The diode matrix output for the DIST 0-9 switch is shown in Table F. Table G shows the diode matrix output for the DIST 0-40 switch.

TABLE F

Percent	Terminal Numbers															
	IC16				IC17				IC18				IC19			
	1	7	14	8	1	7	14	8	1	7	14	8	1	7	14	8
0	H	L	H	L	H	L	H	L	L	L	L	L	L	L	L	L
1	L	H	H	L	H	L	H	L	L	L	L	L	L	L	L	L
2	H	L	L	H	H	L	H	L	L	L	L	L	L	L	L	L
3	L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	L
4	H	L	H	L	L	H	H	L	L	L	L	L	L	L	L	L
5	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L
6	L	L	L	L	L	L	L	L	H	L	L	H	L	H	H	L
7	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	L
8	L	L	L	L	L	L	L	L	H	L	H	L	H	L	L	H
9	L	L	L	L	L	L	L	L	L	H	H	L	H	L	L	H

TABLE G

Percent	Terminal Numbers					
	IC20					
	13	9	14	8	1	7
0	H	L	H	L	H	L
10	H	L	H	L	L	H
20	H	L	L	H	H	L
30	H	L	L	H	L	H
40	L	H	H	L	H	L

This pulse locates the displaced transition necessary to generate the type of distortion selected. A count-down pulse is employed for the generation of the space-to-mark transitions for marking bias, and the mark-to-space transitions for spacing end distortion. A count-up pulse is used for the space-to-mark transition for spacing bias and the mark-to-space transition for marking end distortion.

GENERATION OF THE VARIOUS TYPES OF DISTORTION

1.11 Two outputs from shift register IC7 are used to allow the generation of the various types of distortion while maintaining a constant character length. Output A on terminal 10 (lead A) is a signal having a ground for a marking bit and a positive voltage for a spacing bit. Output B on terminal 11 (lead B) has the same polarity as on output A except that output B is advanced by one bit. Output B thus acts as an "anticipator" since it provides information as to the state (marking or spacing) of the next bit on output A. The generation of the various types of distortion is under control of TYPE DIST switch. The TYPE DIST switch positions and diode matrix are shown in Table H.

TABLE H

Switch Position	Terminal Numbers											
	IC34						IC35					
	7	1	13	14	9	8	7	1	13	14	9	8
MB	L	H	L	L	L	L	H	L	L	H	L	H
SB	L	H	L	L	L	H	L	H	H	L	H	L
SWB	L	H	L	H	L	H	H	H	L	L	H	H
ME	H	L	L	L	L	H	H	L	H	L	H	L
SE	H	L	H	L	L	H	L	H	L	H	L	H
SWE	H	L	H	H	L	H	H	H	H	H	L	L
SWC	H	H	H	H	H	H	H	H	H	H	H	H

1.12 With the TYPE DIST switch in the marking bias (MB) position, ground is applied to terminal 2 of diode matrices IC34 and IC35. Outputs (terminals) 7, 8, 9, 13, and 14 of IC34 are grounded and outputs (terminals) 1, 9, and 13 of IC35 are grounded. Ground on these outputs of IC34 disables gates IC38B, IC42B, IC45B, IC37A, IC43C, IC43D, IC41A, IC66C, and IC66D. Signals from the shift register IC7, output A, [low (0) for mark and high (1) for space] are applied to terminal 13 of gate IC38A via inverter IC26E. The output from gate IC38A is applied to terminal 12 of flip-flop IC9B. The outputs from flip-flop IC9B are delayed by one-half clock pulse in reference

to output A of shift register IC7. The outputs from flip-flop IC39A are delayed by one clock pulse in reference to output A of shift register IC7.

1.13 The inputs of gate IC40D are derived from flip-flop IC9B and IC39A. The output of gate IC40D, terminal 11, has a negative spike of one-half clock pulse width for every positive transition at output A of shift register IC7. This spike is thus delayed by one-half clock pulse in reference to output A of IC7 which will provide the undistorted transition for character generation.

1.14 Ground on outputs 1, 9, and 13 of IC35 disables gates IC36A, IC36C, and IC46C. Gates IC46A and IC46B are enabled which causes gate IC37C to be disabled. Since gates IC36C and IC46C are disabled, this allows the pulses from flip-flop IC55A, terminal 13, to pass through gate IC37D. This pulse is applied to gate IC25 where the digital time delay is derived. This time delay is used to displace transitions for generating various amounts of distortion. Since this pulse is low during the first half of the bit (0-49), and it is high during the second half of the bit (49-0), the only count-down pulse (during the second half of the bit) will be passed through gate IC25. The output of gate IC25 is applied to gate IC42A via inverter IC26D. Since gate IC36A is disabled and gate IC36B is enabled, signals from the shift register IC7, output A, are passed to the input of gate IC42A. Since gate IC41A is disabled and gate IC41B is enabled, inverted signals from shift register IC7, output B, are passed to the input of gate IC42A. The inputs at gate IC42A are as follows.

(a) The input on terminal 1 is a positive spike for every bit and occurs during the last half of the bit. The position of the spike in reference to output A of the shift register IC7 is determined by the amount of distortion being generated.

(b) The input on terminal 13 is the output A of the shift register (mark-0 and space-1).

(c) The input on terminal 2 is the inverted output B of the shift register and is advanced by one bit in reference to output S of the shift register.

Assume that the DIST % switches are set to 25 percent through the description of this section. The output of gate IC42A will be a negative spike which occurs 25 percent sooner than the negative transition of the shift register, output A. The output of this gate is transferred via gate IC66A and inverter IC8E to the input of gate IC40B.

1.15 The output of gate IC40D is a negative spike for each negative transition of the shift register, output A, which is transferred without delay via gates IC40A and IC40B (gates IC40A and IC40B form a flip-flop) to the input of gate IC45A. Since gate IC45B is disabled, the output of gate IC45A has all positive transitions advanced by 25 percent, and all negative transitions occurring without delay, in respect to the shift register inverted output A. The signal at the output of gate IC45A has 25 percent of marking bias (mark-1 and space-0).

1.16 With the TYPE DIST switch in the spacing bias (SB) position, ground is applied to terminal 12 of diode matrices IC34 and IC35. Outputs (terminals) 7, 9, 13, and 14 of IC34 and outputs (terminals) 7, 8, and 14 of IC35 are grounded. Ground on outputs 7, 9, 13, and 14 of IC34 performs the same functions as described in paragraph 1.12 except that gate IC37A is enabled since ground from output 8 of IC34 is removed. The output of gate IC40D is the same as described in paragraph 1.12 of this section. Ground on outputs 7, 8, and 14 of IC35 disables gates IC36B, IC46A, and IC46B. Gates IC36C and IC46C are enabled, which causes gate IC37D to be disabled. Since gates IC46A and IC46B are disabled, this allows pulses from flip-flop IC55A, terminal 12, to pass through gate IC37C. This pulse is applied to gate IC25. The operation of gate IC25 is the same as described in paragraph 1.12 except that the only count-up pulse during the first part of the bit will be passed through this gate. The output of gate IC25 is applied to gate IC42A via inverter IC26D. Since gate IC36A is enabled and gate IC36B is disabled, inverted signals from the shift register IC7, output (A) are passed to the input of gate IC42A. Gate IC41A is disabled and gate IC41B is enabled and therefore, inverted signals from shift register IC7, output (B), are passed to the input of gate IC42A. The inputs at gate IC42A are as follows.

(a) The input at terminal 1 is a positive spike for every bit and occurs during the first half of the bit.

(b) The input on terminal 13 is the inverted output A of the shift register.

(c) The output on terminal 2 is the same as described in 1.12.

1.17 The output of gate IC42A will be a negative spike which occurs 25 percent later than the negative transition of the shift register, output A. The output of this gate is transferred via gate IC66A and inverter IC8E to the input of gate IC40B. The output of gate IC40D is the same as described in 1.12, and its transferral to the output of gate IC45A is also the same. Since gate IC45B is disabled, the output of gate IC45A has all positive transitions delayed by 25 percent and all

negative transitions occurring without delay in respect to the shift register inverted output A. The signal at the output of gate IC45A has 25 percent of spacing bias.

1.18 With the TYPE DIST switch in the switched bias (SWB) position, ground is applied to terminal 3 of diode matrices IC34 and IC35. Outputs (terminals) 7, 9, and 13 of IC34 are grounded and outputs (terminals) 13 and 14 of IC35 are grounded. Grounding these outputs disables gates IC38B, IC41A, IC42B, IC43C, IC43D, IC45B, IC46A, and IC46C. The output of gate IC40D is the same as described in 1.12. The inputs to gate IC42A will alternate for every character. One character will have the same inputs as described in 1.12 for marking bias, and the next character will have the same inputs as described in 1.16 for spacing bias. The switching of the inputs of gate IC42A is under control of flip-flop IC48B. This flip-flop is switched once every character by the output of gate IC58B at the beginning of the start pulse. The outputs from flip-flop IC48B are applied to the inputs of gates IC66C and IC66D. The output of gate IC66C controls gates IC36A, IC37A, and IC36C. The output of gate IC66D controls gates IC36B, IC46B, IC46C, and IC66B. Since gate IC45B is disabled, the output of gate IC45A has 25 percent of switched bias.

1.19 With the TYPE DIST switch in the marking end (ME) distortion position, ground is applied to terminal 11 of diode matrices IC34 and IC35. Outputs (terminals) 1, 9, 13, and 14 of IC34 are grounded, and outputs (terminals) 1, 8, and 14 of IC35 are grounded. Ground on these outputs of IC34 disables gates IC38A, IC45A, IC41B, IC41A, IC43C, IC43D, IC66C, and IC66D. Signals from the shift register IC7, output A, are applied to terminal 4 of gate IC38B. The output from gate IC38B is applied to terminal 12 of flip-flop IC9B. The outputs of flip-flops IC9B and IC39A have the same delays as described in 1.12, in reference to output A of the shift register IC7. The inputs to gate IC40D are derived from flip-flops IC9B and IC39A. The output of gate IC40D has a negative spike of one-half clock pulse width for every negative transition at output A of the shift register. This spike is thus delayed by one-half clock pulse in reference to output A of the shift register, which will provide the undistorted transition for character generation. Ground on outputs 1, 8, and 14 of IC35 disables gates IC36A, IC46A, and IC46B. Gates IC36C and IC46C are enabled which causes gate IC37D to be disabled. Because gates IC46A and IC46B are disabled, pulses from flip-flop IC55A, terminal 12, are allowed to pass through gate IC37C. This pulse is applied to gate IC25. The operation of gate IC25 is the same as described in 1.12 except that only a single count-up pulse during the first part of the bit will be passed through this gate. The output of gate IC25 is applied to gate IC42A via inverter IC26D. The inputs at gate IC42A are as follows.

(a) The input at terminal 1 is a positive spike for every bit and occurs during the first half of the bit.

(b) The input on terminal 13 is the output A of the shift register.

(c) The input on terminal 2 is high since both gates IC41A and IC41B are disabled.

1.20 The output of gate IC42A will be a negative spike which occurs 25 percent later than the positive transition of the shift register, output A. In marking end distortion, all mark-to-space transitions are delayed except the start-pulse transition. In order to have the start pulse undistorted, a reset pulse, D, is applied to the input of gate IC66A via gate IC42B. The output of gate IC66A is applied to the input of gate IC40B via inverter IC8E. The input at gate IC40B is the same as the output of gate IC42A except that it will also have a negative pulse of one-half clock pulse width at the end of the stop pulse. Since gate IC45A is disabled, the output of gate IC45B has all positive transitions delayed by 25 percent, except the start pulse transition, and all negative transitions occurring without delay in respect to the shift register, inverted output A. The signal at the output of gate IC45B has 25 percent of marking end distortion (mark-1 and space-0).

1.21 With the TYPE DIST switch in the spacing end (SE) distortion position, ground is applied to terminal 4 of diode matrices IC34 and IC35. Outputs (terminals) 1, 9, and 14 of IC34 and outputs (terminals) 7, 9, and 13 of IC35 are grounded. Ground on these outputs of IC34 disables gates IC38A, IC45A, IC41B, IC43C, IC43D, IC66C, and IC66D. The output of gate IC40D is the same as described in 1.19. Ground on outputs 7, 9, and 13 of IC35 disables gates IC36B, IC36C, and IC46C. Since gates IC36C and IC46C are disabled, this allows the pulses from flip-flop IC55A, terminal 13, to pass through gate IC37D. These pulses are applied to gate IC25. The operation of gate IC25 is the same as described in 1.12. The output of gate IC25 is applied to gate IC42A via inverter IC26D. The inputs at gate IC42A are as follows.

(a) The input at terminal 1 is a positive spike for every bit and occurs during the last half of the bit.

(b) The input at terminal 13 is the inverted output A of the shift register.

(c) The input at terminal 2 is the output B of the shift register and is advanced by one bit in reference to output A of the shift register.

The output of gate IC42A will be a negative spike which occurs 25 percent sooner than the negative transition of the shift register, output A. In spacing end distortion all mark-to-space transitions are advanced except the start-pulse transition. In order to have the start pulse undistorted, a reset pulse, D, is applied to the input of gate IC66A via gate IC42B. The output of gate IC66A is applied to the input of gate IC40B via inverter IC8E. The input at gate IC40B is the same as the output of gate IC42A except that it will have in addition a negative pulse at the end of the stop pulse. Since gate IC45A is disabled, the output of gate IC45B has all positive transitions advanced by 25 percent except the start pulse transition, and all negative transitions occurring without delay in respect to the shift register, inverted output A. The signal at the output of gate IC45B has 25 percent of spacing end distortion.

1.22 With the TYPE DIST switch in the switched end (SWE) distortion position, ground is applied to terminal 10 of diode matrices IC34 and IC35. Outputs (terminals) 1 and 9 of IC34 are grounded, and outputs 8 and 9 of IC35 are grounded. Ground on these outputs disables gates IC38A, IC45A, IC41B, IC43C, IC43D, IC46B, and IC36C. The output of gate IC40D is the same as described in 1.19. The inputs to gate IC42A will alternate for every second character. One character will have the same inputs as described in 1.19 for marking end distortion, and the next character will have the same inputs as described in 1.21 for spacing end distortion. The switching of the inputs of gate IC42A is under control of flip-flop IC48B. This flip-flop is switched once every character by the output of gate IC58B, at the beginning of the start pulse. The outputs from flip-flop IC48B are applied to the inputs of gates IC66C and IC66D. The outputs of these gates control which type of distortion (marking or spacing end distortion) is applied to the input of gate IC45B. The output of gate IC45B has 25 percent of switched end distortion.

1.23 With the TYPE DIST switch in the switched combination (SWC) distortion position, ground is applied to terminal 5 of diode matrices IC34 and IC35. All outputs (terminals) of IC34 and IC35 are high. Gates IC66C and IC66D control the one character sequence type of distortion or bias while gates IC43C and IC43D control two character sequences of switched end distortion or switched bias. The switched combination distortion is composed of four basic types of distortion generated in a repetitive cycle of four characters; the first character has MB, the second character has SB, the third character has ME distortion, and the fourth has SE distortion. This is accomplished by switching flip-flop IC48B every character at the beginning of the start pulse. The 9 output of flip-flop IC48B switches flip-flop IC48A every two characters. The outputs of these two flip-flops are applied to gates IC66C, IC66D, IC43C, and IC43D which control the type of distortion applied to the inputs of gate IC45A or IC45B. The outputs of these two gates will have 25 percent of switched combination distortion.

1.24 The output of gate IC45A or IC45B is connected to the EIA driver IC47. The signal output of gate IC45A or IC45B is also connected via inverter IC8F and buffer IC70A to SIGS lead which in turn is coupled to the SIGS light-emitting diode (LED). The LED will be on for a marking output, extinguished for a spacing output, and will flicker at the bit rate when signals are being generated.

1.25 Depressing the nonlocking SPACE switch applies a ground via lead SS to the input of the EIA driver IC47 to simulate a steady spacing output.

2. DISTORTION MEASURING SET (CP2)

UNITS AND TENS DISTORTION COUNTER

2.01 The units and tens distortion counter consists of gates IC52A, IC52B, and IC52C, flip-flop IC53A, and up/down decode counters IC54 and IC55. In the idle condition, both counters are cleared by flip-flop IC63B, causing the output of gate IC60 to go low and the output of IC59 to go high. Gate IC60 detects 0 count, while gate IC59 detects 50 count. Counters IC54 and IC55 are enabled at the first mark-to-space transition (start pulse) of the incoming signals. These counters, which start counting from 0 to 50, are triggered by a low-to-high transition of the clock pulse. When a count of 50 is reached, gate IC59 goes low causing the output of gate IC58A to go high. This toggles flip-flop IC53A through gate IC52A. These counters now start to count from 50 to 0. The output of gate IC59 is used to trigger the character-framer binary counter IC61 and flip-flops IC3C and IC3D. The outputs of counters IC54 and IC55 are used for stores IC18 and IC19 and for distortion discriminator circuit IC6, IC7 and for gate IC9.

CHARACTER FRAMER

2.02 The character framer consists of 4-bit binary counter IC61, gate IC62B, and flip-flop IC63B. The input to IC61 is applied from gate IC59 (count 50). The counter is arranged to divide by 7 or 10 depending on the position of the CODE switch. For Baudot codes (5/7.0, 5/7.42, and 5/7.5) the counter is arranged to divide by 7 and for ASCII codes (8/10, 8/11, and 8/11M) the counter is arranged to

divide by 10. During the idle condition (mark), the 1 side of flip-flop IC63B is low which clears counters IC54 and IC55, and flip-flop IC53A. Flip-flop IC63B is set at the first mark-to-space transition (start pulse) of the incoming signal causing the 1 side of this flip-flop to go high. This enables flip-flop IC53A, counters IC54 and IC55, and gate IC58D. The character framer is required for synchronizing the measuring set with the incoming signals.

2.03 If flip-flop IC63B gets stuck in the set condition (0 side low) due to noise impulses, the counters IC54 and IC55 will get out of synchronization with the incoming signals. This would prevent these counters from reaching the 50 count. Since counter IC61 is triggered from the 50 count gate (IC59), counters IC54 and IC55 would never be cleared to start the proper count. When this unusual condition occurs the 4-bit binary counter IC56 is enabled. After 16 transitions from flip-flop IC53A or 8 transitions from flip-flop IC53B the output D of counter IC56 will go low. This will clear flip-flop IC63B which in turn will clear counters IC54 and IC55 thus synchronizing the measuring set with the incoming signals.

2.04 When synchronous signals are measured, operate ASYNC-SYNC switch to SYNC position. This transfers outputs from flip-flop IC63B to the outputs of monopulser IC4. Every transition of the incoming signal causes a positive pulse (one-half clock width) at the output of the exclusive OR gate IC2C which triggers the monopulser. The outputs of the monopulser are approximately 1.5-microsecond pulses which provide similar functions as flip-flop IC63B on a bit-by-bit basis.

UNITS AND TENS DISTORTION STORES AND COMPARATORS

2.05 The units and tens distortion stores consist of two 4-bit bistable latches IC18 and IC19. These latches are ideally suited for use as temporary storage for binary information. The outputs from the units and tens counters are present at the D inputs of both stores. The information is transferred to the Q outputs of both stores when the load pulse E is high. The Q outputs will follow the data inputs as long as the load pulse remains high. When the load pulse goes low, the information (that was present at the time the transition occurred) is retained at the output of the stores until the load pulse is permitted to go high again.

2.06 The units and tens comparators are composed of two 4-bit magnitude comparators IC26 and IC27. These circuits are used to compare two 4-bit words (A and B); word A is associated with input A and word B is associated with output B. The comparators determine their relative magnitude with the result being indicated by high-level voltage at the A>B, A<B, or A=B output. The comparators compare the information from the units and tens counters to the information located in the stores. If the magnitude of the data present at the input of the units and tens counters is greater than the information of the store (A>B), the output of store IC27 is high. This enables gate IC23B which causes load pulse L to go through gate IC28A, inverters IC36B and IC37D providing load pulse E for clocking stores IC18 and IC19. This load pulse E will load the information to both stores. The load pulse L is derived from the incoming signal by the flip-flops IC1A and IC1B and gate IC2C. The output gate IC2C will have a positive pulse of one-half clock pulse width for each transition of the incoming signal. If the information in the store is equal or less than the information from the units and tens counters, gate IC23B is disabled. When gate IC23B is disabled, it provides a no-load pulse E at the inputs of the stores; therefore, the information in the store remains unchanged. The information in the store is the amount of distortion present in the incoming signals. The information in the stores is in the form of binary-coded decimal (BCD) and it is applied to the numerical display on the control panel.

DISTORTION ANALYZER

2.07 The distortion analyzer circuit consists of gates IC11A, IC11B, IC12A, IC12B, IC13A, 4-bit store IC14, inverter IC8C, buffers IC15A, IC15B, IC15E, IC15F, and flip-flops IC16A and IC16B. The distortion measuring set detects and displays the peak distortion of incoming signals. In practice, this distortion is made up of a certain amount of each of the four basic types of distortion: marking bias, spacing bias, marking end distortion, and spacing end distortion.

(a) A marking bias (MB) corresponds to a transition from space-to-mark occurring before the end of the element.

(b) A spacing bias (SB) corresponds to a transition from space-to-mark after the end of the element.

(c) A marking end (ME) distortion corresponds to a transition from mark-to-space occurring after the end of the element.

(d) A spacing end (SE) distortion corresponds to a transition from mark-to-space occurring before the end of the element.

2.08 When the incoming signal has MB, the 1 side of flip-flop IC53A is high during the time interval. This time interval is the second half of each bit where

the units and tens counters are counting from 50 to 0. The MS1 signal (high for mark and low for space) causes gate IC11A to go low. The output of gate IC11A is applied to the input of store IC14. This information is transferred to the output of the store by the load signal L via gates IC3B and IC3A. Gates IC3C and IC3D are used to block the first mark-to-space (M-S) transition (start pulse) from being transferred to the store. This transition is a reference point for measuring all distortion and therefore it is not necessary to transfer it to the store. When the output of gate IC11A is low, except the first M-S transition, the output 1Q of store IC14 will also go low. This causes the MB LED to light on the control panel via buffer IC15E.

2.09 When the incoming signal has SB, the 0 side of flip-flop IC53A is high during the time interval. This time interval is the first half of each bit when the units and tens counters are counting from 0 to 50. The inputs to gate IC11B are high from flip-flop IC53A and from the MS1 signals causing the output of this gate to go low. This information is transferred to store IC14 in a similar manner to that described in 2.08. The output 2Q of the store goes low causing the SB LED to light on the control panel via buffer IC15F.

2.10 When the incoming signal has ME distortion, the 0 of flip-flop IC53A is high. The $\overline{MS1}$ signal is high for space, and since the 0 side of flip-flop IC53A is also high, this causes the output of gate IC12B to go low. The information is transferred through the store IC14 via flip-flop IC16A and buffer IC15B to the ME LED on the control panel, and causes the ME LED to light.

2.11 When the incoming signal has SE distortion, the 1 side of flip-flop IC53A is high The $\overline{MS1}$ is high for space, and since the 1 side of flip-flop IC53A is also high, this causes the output of gate IC12A to go low. The information is transferred through the store IC14 via flip-flop IC16B and buffer IC15A to the SE LED on the control panel, and causes the SE LED to light. Flip-flops IC16A and IC16B are used for ME and SE distortions only. Without these flip-flops the ME and SE LEDs would light momentarily and for higher baud rates, and they would not provide sufficient brightness.

PARITY CHECK

2.12 Some codes, such as the ASCII code, provide an eighth bit for checking the parity of a received character. This parity bit, which is usually the eighth information bit, makes the number of marking information bits always an even number if even parity is used, or always an odd number if odd parity is used.

2.13 When no parity is desired, flip-flop IC39B is held in the clear condition by grounding the clear terminal of this flip-flop via the PARITY (ON-OFF) switch. This PARITY switch also applies ground to either the CLEAR or SET terminal of flip-flop IC39A, depending on whether an even or an odd parity check is made. When a parity check is desired, operation of the PARITY switch to its ON position removes ground from flip-flops IC39B (CLEAR terminal) and IC39A (CLEAR or SET terminal) depending on the position of the PARITY (EVEN-ODD) switch.

2.14 For an even parity check, flip-flop IC39A is held in the set state during the stop pulse by gate IC64A. This allows flip-flop IC39A to change its state in the middle of every marking bit except during the stop pulse of the received character. If the number of marking bits of the incoming character is even, flip-flop IC39A will be in the set state. In this case there will be no change in the state of flip-flop IC39B. During the start pulse, flip-flop IC39A is cleared via gates IC2D and IC38C. If the number of marking bits of the incoming character is odd, flip-flop IC39A will be in a clear state during the second half of the stop pulse. If the stop pulse consists of two bits, flip-flop IC39A will be cleared during the second half of the first bit of the stop pulse. When flip-flop IC39A clears, it enables gate IC38A which sets flip-flop IC39B. This causes PAR LED on a control panel to light via inverter IC37B, indicating that a parity error has occurred. The PAR LED can be extinguished either by operating the PAR ON-OFF switch to OFF, or by depressing the RESET switch.

2.15 For an odd parity check, flip-flop IC39A is held in the clear state during the stop pulse by gate IC64A. The flip-flop IC39A will operate in a manner similar to that described in 2.14. If the number of marking bits is odd, flip-flop IC39A will be in the set state and flip-flop IC39B remains in its clear state. If the number of marking bits of the incoming characters is even, flip-flop IC39A will be in a clear state. This causes flip-flop IC39B to set, lighting the PAR LED on the control panel, indicating that a parity error has occurred.

DISPLAY CHARACTERS

2.16 Provision is made for displaying the information bits of the last two characters received for ASCII code and the last character received for Baudot code. This feature is under control of the DISPLAY CHAR switch, which has three positions (OFF, 5, and 8). Position OFF is used when display characters are not required. Position 5 is used for Baudot code, and position 8 is used for ASCII code. The circuit consists of buffer amplifiers IC42, IC46, and

IC51, gates IC43, IC49, and IC50, two 8-bit shift registers IC44 and IC47, and one 5-bit shift register IC48. All shift registers perform serial-to-parallel conversion. The output of these shift registers will be low for the marking bits and high for the spacing bits of the received characters.

2.17 The clocking signal for all shift registers is provided from the output of gate IC43C. The output of this gate provides sampling in the middle of every bit of the received character to determine whether the bit is marking or spacing. Data at the inputs of the shift register may be changed while the clocking signal is high, but only information meeting the setup requirements will be entered. Clocking (output of gate IC43C) occurs on the low-to-high level transitions.

2.18 For receiving ASCII code characters, shift register IC48 is held clear by the CODE switch. When the first character of an ASCII code is received, its information bits are shifted serially into the shift register IC44. The start pulse is shifted from IC44 to flip-flop IC45B. The outputs from IC44 are connected to DISPLAY CHAR LEDs 1-1 through 1-8 on the control panel via buffer amplifiers. Lighted DISPLAY CHAR LEDs represent a marking bit of the received character, eg, if second and fifth bits of the first received character are marking, LEDs 1-2 and 1-5 will be lit. When the second character is received into the shift register IC44, the first-character information which was formerly stored, is transferred into the second-shift register IC47. The outputs of the second-shift register are connected to DISPLAY CHAR LEDs 2-1 through 2-8 via buffer amplifiers. The information of the first character is displayed on LEDs 2-2 and 2-5. The information of the second character received is displayed on LEDS 1-1 through 1-8.

2.19 For receiving Baudot code characters, shift registers IC44 and IC47 are held clear by the CODE switch. All DISPLAY CHAR LEDs are extinguished by the DISPLAY CHAR switch except LEDs 2-1 through 2-5. When a character is received, its information bits are shifted serially into the shift register IC48. The outputs from IC48 are connected to DISPLAY CHAR LEDs 2-1 through 2-5 via exclusive OR gates IC50 and IC49B, and via buffer amplifiers.

DISTORTION DISCRIMINATOR CIRCUIT

2.20 This circuit consists of diode matrix IC5, inverters IC6, IC7, and IC8 and gates IC9 and IC10. The DISCR % switch is provided to suppress any type of distortion beneath a predetermined threshold level from the distortion display. This level is determined by the position of the DISCR % switch. The DISCR % switch has five positions (0, 3, 5, 10, and 15 percent). If the DISCR % switch is set to position 5, any distortion less than 5 percent will not illuminate a LED. Most teletypewriter signals contain more than one type of distortion. The use of the DISCR % switch will provide a general breakdown as to the contribution of the different types of distortion in the signal.

2.21 When DISCR % switch is set to a particular threshold level, gates IC10C and IC10D will be controlled by gate IC9 and flip-flop IC53A. Some inputs of gate IC9 are connected directly to the units and tens counters and some inputs are connected to the counters via inverters, which are under control of diode matrix IC5. For example, when the DISCR % switch is set to the 5 position, ground is applied to terminal 11 of diode matrix IC5. The outputs 7, 14, 13, and 10 of diode matrix IC5 are grounded. These outputs are connected via inverters IC7D, IC7E, and IC6E to the inputs of gate IC9 under control of the diode matrix. Gate IC9 will be low for a time interval of 5 percent of every transition of the received character. This causes gate IC10C to go low which disables gates IC11A, IC11B, IC12B, and IC12A. These gates will blank out any display of the distortion of the received character of 5 percent or less thus preventing LEDs MB, SB, ME, and SE from lighting. When the amount of distortion of the received character is higher than the setting of the DISCR % switch, gate IC10C will go high. This will allow the display of the proper type of distortion by the LEDs on the control panel. The procedure for other settings of the DISCR % switch is similar and can be easily traced.

DISPLAY CIRCUIT

2.22 The DISPLAY switch has five positions: PK, AUTO PK, PK CNT, END CNT, and PAR CNT. When the DISPLAY switch is set to the PK position, ground is applied to terminal 3 on diode matrices IC40 and IC41. Outputs 13 and 14 of IC40, and outputs 8, 13, and 14 of IC41 are grounded. Ground on terminal 13 of IC40 disables gate IC33A, which causes its output to go high. This enables gate IC28A via buffer IC29C, which will allow the load pulse L to pass when the output A>B of comparator IC27 is high. The output of gate IC28A provides the load pulse E to stores IC18 and IC19 via inverters IC36B and IC37D. This will allow the highest percent of received signal distortion to be displayed on the DISPLAY LEDs of the control panel.

2.23 When the DISPLAY switch is set to the AUTO PK position, ground is applied to terminal 5 on diode matrices IC40 and IC41. Outputs of IC40 and 41 are the same as for PK, except that terminal 13 of IC40 is high. This enables gate IC33A. The input 2 to gate IC33A is derived from 4-bit binary counter IC32, flip-flop IC34B, and

gates IC33C, IC33D, and IC33B. The output of gate IC33B will go high for every sixteenth character. The display units and tens on the control panel will be automatically reset for every sixteenth character.

2.24 When the DISPLAY switch is set to the PK CNT position, ground is applied to terminal 4 on diode matrices IC40 and IC41. Outputs 8, 9, and 13 of IC40, and outputs 7, 8, and 9 of IC41 are grounded. Ground on terminals 8 and 9 of IC40 disables gates IC20, IC21, IC22B, IC22C, IC22D, IC23A, IC23C, and IC23D. This blocks the information from the stores IC18 and IC19 to display units and tens on the control panel. Ground on terminal 13 of IC40 disables gate IC33A. Ground on terminal 7 of IC41 disables inverter IC37D. This blocks the load signal derived from comparator IC27 via gates IC23B and IC28A. Ground on terminal 8 of IC41 disables inverter IC36E which enables gate IC35A. Terminal 14 of IC41 is high which enables inverter IC37E. This will pass the load signal L independently of comparator IC27 via inverters IC36A and IC37E to stores IC18 and IC19. The DIST PKS switch provides, in 5-percent steps from 5 to 40 percent, a threshold distortion to the comparators IC26 and IC27. When the distortion from stores IC18 and IC19 is above the setting of the DIST PKS switch, the output A<B of comparator IC27 goes high. This causes gate IC13C to go low; its output is connected to the input of gate IC35A via buffer IC15D, and inverters IC36C and IC36F. Output of gate IC35A goes high which causes the counters IC30 and IC31 to advance by one count for any type of distortion, counting total distortion hits. These counters are arranged to count a maximum of 99. After a count of 99, the counters will lock up and must be manually reset by the RESET switch.

2.25 When the DISPLAY switch is set to the END CNT position, ground is applied to terminal 2 of IC40 and IC41. Outputs 8, 9, and 13 of IC40 are grounded in the same manner as the PK CNT position. Outputs 7, 8, and 13 of IC41 are grounded in the same manner as the PK CNT position, except that output 13 is grounded. Output 13 of IC41 disables gate IC13A. This enables gate IC13B which allows the counting of end distortion hits above the setting of the DIST PKS switch. Counting of these hits is the same as described in 2.24. When the DISPLAY switch is set to the PAR CNT position, ground is applied to terminal 11 of IC40 and IC41. Outputs 7, 8, and 13 of IC40 are grounded in the same manner as the PK CNT position. Outputs 1, 13, and 14 of IC41 are grounded. Grounding output 13 of IC41 is performed in the same manner as counting end distortion hits as described in this paragraph. Ground on terminal 1 of IC41 disables inverter IC36F, which enables gate IC35A. Ground on terminal 14 of IC41 disables inverter IC37E. Output 8 of IC41 is high, which enables inverter IC36E. When a parity error is received, flip-flop IC34A will clear for every error. Normally, flip-flop IC34A is set by the first M-S transition. When flip-flop IC34A is cleared, its 0 side is low which disables gate IC35A via inverters IC36D and IC36E. Output of gate IC35A goes high which causes the counters IC30 and IC31 to advance by one count. The counters will count the number of parity errors received up to a maximum of 99. The counters can be manually reset by the RESET switch.

3. CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS (CP3)

CLOCK CIRCUIT

3.01 To generate and receive the various characters of a test message, an accurate clock is necessary since errors in the clock rate will cause the total distortion for some characters to be as much as nine times the distortion of one bit. Thus, a clock frequency many times higher than the baud rate is chosen so that, when divided to the desired frequency, the error rate is proportionally divided.

3.02 The crystal controlled oscillator Y1 has a square-wave output of 9.6 MHz. This output is divided to a frequency of 100 times the desired baud rate and distributed to both the generating and receiving portions of the test set. Table I indicates the clock output frequency for each position of the BAUD switch.

3.03 For positions 1 through 13 of the BAUD switch, the 9.6-MHz clock frequency is passed via gate IC8C to flip-flops IC7A and IC7B where an initial 4-to-1 division takes place. The 2.4-MHz output is then further reduced by counters IC17, IC18, and IC19 whose frequency division is determined by the inputs from the BAUD switch controlled diode matrices IC13, IC14, IC15, and IC16. The negative spike outputs from the counters are further reduced and formed into a symmetrical square wave by flip-flop IC11A. The square-wave output is then passed via gates IC8B and IC10 to the clock output via gate IC9C, and in inverted form (clock) via inverter IC5F.

3.04 Switch positions 17 and 18 apply ground to inverters IC5C and IC5A which disables gates IC8C or IC8B and IC4C or IC4B, respectively. Disabling gate IC8C stops the Y1 oscillator clock output from entering the flip-flop IC7A. The customer-provided clock is obtained now from Y3 oscillator via gate IC4C or from Y2 oscillator via gate IC4B depending on the position of the BAUD switch. The output of gate IC4C or IC4B is passed to the input of gate IC1D as described in 3.03. Since there is no frequency division associated with these gates, the crystal-controlled clock frequency should be 100 times the desired baud rate.

TABLE I

Position	Baud Rate	Frequency Division of Counters IC17, 18, and 19	Clock Output (IC9C) Frequency in KHz
1	45.5	263	4.563 ±2 Hz
2	56.9	211	5.687 ±2 Hz
3	61.12	196	6.122 ±3 Hz
4	74.23	162	7.407 ±3 Hz
5	75.0	160	7.500 ±3 Hz
6	110.0	109	11.009 ±3 Hz
7	134.46	89	13.483 ±4 Hz
8	150.0	80	15.000 ±4 Hz
9	300.0	40	30.000 ±4 Hz
10	600.0	20	60.000 ±4 Hz
11	1050.0	11	109.091 ±4 Hz
12	1200.0	10	120.000 ±5 Hz
13	1800.0	7	171.429 ±5 Hz
14	Spare		
15	Spare		
16	Spare		
17	Optional		
18	Optional		
19	*		
20	External Clock		

*Position 19 is strapped to position 20.

3.05 Positions 19 or 20 are selected when employing an external frequency source. These positions of the BAUD switch disable gates IC8C and IC8B and enable gate IC9B to permit the introduction of the external clock via the EXT CLK jack and transistor stage Q1. The clock source must be a square wave of 45 to 55 percent duty cycle, at a potential from ground to +5 ±0.5 volts. The BAUD switch positions and diode matrix output are shown in Table J.

INTERFACE CIRCUITS

3.06 The neutral loop interfaces are polarized solid-state circuits operating from the loop battery, and are designed for protection against excessive loop current and improper loop voltages. The T+ and T- designations on the jacks indicate the voltage polarity on the tip side of the loop to accommodate the interface requirements.

TEST SENTENCE GENERATOR EIA INTERFACE

3.07 Driver IC47 consists of two EIA drivers which convert data signals (+5 volts and ground) to standard EIA signal levels. This driver has two outputs. Output signals from driver IC47A are normal EIA, and from driver IC47B are inverted EIA. These signals are coupled via NORM-REV switch to the EIA VOLT OUT jack. Resistor R1 and capacitor C1 (on control panel) form a wave-shaping network at this point to add the necessary slope to the output signals as required by EIA standards.

3.08 The lead INT1 is coupled to CP3 from the NORM-REV switch. Assuming that the NORM-REV switch is in normal position and that the loop is patched into jack J7 (T+ LP DRIVER), the lead INT1 will have EIA signals of approximately -12 volts per mark, and approximately +12 volts per space. The loop must have the proper polarity, positive on the tip and negative on the sleeve, in this application.

3.09 Transistor Q22 and its associated circuit, in conjunction with the primary windings 1-10 and 2-9 of transformer T1, and windings 1-10 and 2-9 of transformer T2, forms a Hartley oscillator. This oscillator oscillates at approximately 80 kHz, and is coupled to the secondary windings of

TABLE J

Switch Position	Terminal Numbers																							
	IC13						IC14						IC15						IC16					
	1	7	14	8	13	9	1	7	14	8	13	9	1	7	14	8	13	9	1	7	14	8	13	9
1	H	H	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H
2	H	L	L	L	H	L	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H
3	L	H	H	L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
5	L	L	L	L	L	H	H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
6	H	L	L	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
7	H	L	L	H	L	L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
8	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
9	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	L	L	L	L	L
10	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	H	L	L	L	L	L	L
11	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	H	L	L	L	L	L	L	L
12	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	H	L	L	L	L	L	L	L
13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L

both transformers. This arrangement provides complete isolation from ground since the loop voltage can range from +130 volts to -130 volts in some cases. The EIA signals are coupled to the bases of transistors Q5 and Q16. A marking signal turns on transistors Q16 and Q18 and turns off transistor Q5. Transistor Q18 shorts out the secondary winding 3-8 of transformer T2. The shorted-out winding of transformer T2 turns off transistor Q19. Since transistor Q5 is turned off, winding 3-8 of transformer T1 is open. This couples the oscillator frequency from primary winding 2-9 of transformer T1 into its secondary winding 5-6, on transistors Q6 and Q8. Transistor Q6 closes the loop via resistor R42 (130 ohms) and via jack J7 (T+ LP DRIVER), sending a marking signal into the neutral loop. Since transistor Q8 is on, capacitor C17 charges through resistor R46 and through transistor Q6 toward a positive potential at the junction of resistor R42 and cathode C of transistor Q6. When a spacing signal is received at the bases of transistors Q5 and Q16, it turns off transistors Q16 and Q18 and turns on transistor Q5. Transistor Q5 shorts out primary winding 3-8 of transformer T1. The shorting of winding T1 is coupled into its secondary winding 5-6 as a short circuit which removes signals from gate G of transistor Q6 and turns off transistor Q8. Since transistor Q6 is a 4-layer device, it will stay on. The primary winding 3-8 of transformer T2 is open since transistor Q18 is off. This allows coupling the oscillator frequency from primary winding 2-9 of transformer T2 to its secondary winding 5-6. This turns on transistor Q19, which causes capacitor C17 to discharge through transistor Q19, turning off transistor Q6. When transistor Q19 turns off it opens the loop, thus sending a spacing signal.

3.10 Operation of transistors Q9, Q20, and Q23 is the same as previously described for transistors Q19, Q8, and Q6, respectively, except that the marking and spacing signals are reversed. Transistor Q6 is on for marking signal while transistor Q23 is on for a spacing signal. Transistor Q23 keys the loop associated with jack J8 (T- LP DRIVER). The tip of this jack must be at a negative potential and the sleeve at a positive potential. The loop driver provides a transfer equivalent to that of relay contacts for sending polar signals.

DISTORTION MEASURING SET INTERFACE CIRCUIT

3.11 When current input is used, the set is inserted in series with the loop via the current input jack J9 or J10. Care must be taken to observe the voltage polarity of the loop (+ or - on the tip) and use of the appropriate jack. The current input circuit consists of resistor R34 and optical coupler OC1 via input leads A1 and B1. Overload protection is performed by transistors Q3 and Q4 and their associated circuit components. Current flow in the circuit creates a voltage drop across resistor R34. When this voltage drop exceeds the breakdown voltage of zener diode CR6 (8.2 ±.5 volts), transistor Q3 conducts, lighting the overload LED CR25 and shorting the input via diode CR4. The overload current is approximately 90 milliamperes. Once activated, input current must be reduced to 0 to deactivate the overload protection. Capacitor C15 acts as a filter to prevent hits (current peaks) from operating the overload feature. Protection against improper polarity is afforded via diode CR8 which acts as a short circuit across the input. If the current exceeds the 90-milliampere overload trigger point, transistor Q4 will operate and act as an additional short circuit. Since this is an improper operating procedure, an overload lamp and filter capacitor has not been incorporated into the circuit design.

3.12 Input signals are coupled via the optical coupler OC1 to the operational amplifier IC20. The proper input bias is determined by the setting of the INPUT switch and the factory-adjusted potentiometers (R53 through R56). The output of amplifier IC20 is coupled via lead J to the reverse (R) position of the INPUT switch and lead R to the buffer amplifier Q21, or the output of amplifier IC20 is coupled via inverting stage Q15, lead K to the normal (N) position of the INPUT switch and lead R to the buffer amplifier Q21.

3.13 EIA input signals at the VOLT INPUT jack are coupled via lead IN1, resistor R29, lead I and the EIA LO position of the INPUT switch to the buffer amplifier Q21. For bridging purposes, the EIA signals are coupled via lead IN1, resistors R29 and R30, lead H, and the EIA HI position of the INPUT switch to the buffer amplifier Q21.

3.14 High voltage hub No. 2 signals at the VOLT IN jack are coupled via IN1, resistors R29, R30, R31, inverting stage Q2, lead G, and the HV HUB position of the INPUT switch to the buffer amplifier Q21.

FILTER CIRCUIT

3.15 If the FILTER switch is in the OUT position, the output of the buffer amplifier Q21 (lead IN2) is coupled via the FILTER switch to the lead B input of the distortion measuring set (DMS) (CPS2).

3.16 If the FILTER switch is in the IN position, the output of the buffer amplifier Q21 (lead IN2) will be connected to the lead A2 input of the filter and output of the filter (lead B2) will be connected to the lead B input of the DMS. The filter consists of an integrating network formed by capacitor C19 and resistor R49, followed by a Schmitt trigger circuit consisting of transistors Q12 and Q13. Resistors R50 and R51 determine the slicing level of transistor Q12. Transistors Q10 and Q11 are arranged in a complementary emitter-follower configuration. When a positive voltage is applied at terminal 5 (filter input), transistor Q10 turns on and transistor Q11 turns off. This causes capacitor C19 to charge exponentially toward +12 volts. When the voltage at the base of transistor Q12 exceeds the voltage of the emitter, the transistor turns on. The voltage of the emitter is determined by the Q14 transistor and its associated circuit. Turning on transistor Q12 reduces the voltage on the base of transistor Q13 which turns on. Transistor Q13 inverts the signal which then appears as the filter output on terminal 4. When ground is applied to the bases of transistors Q10 and Q11, transistor Q10 turns off, and transistor Q11 turns on causing capacitor C19 to discharge toward ground. The voltage at the base of transistor Q12 decreases exponentially and when the voltage drops below the emitter voltage, the transistor turns off. This causes transistor Q13 to turn off. The signal at the output of the filter is delayed by approximately 0.1 ms. This will prevent the set from responding to transitions less than 0.1 ms, such as contact bounce or signal noise, regardless of where it occurs in the signal. The distortion between the input and the output of the filter can be minimized by the factory adjustment of resistor R52.

4. POWER SUPPLY CIRCUIT (CP4 AND REAR PANEL)

4.01 The +12, -12, and +5 volt regulators (IC1, IC2, and IC3 with their associated components) and the full-wave rectifier (CR1) are mounted on CP4. The power transformer, filter capacitors, power transistor (Q1), and full-wave rectifier (CR26) are mounted on the rear panel (power supply) as shown on sheet B5. The power transformer (T1) has a primary winding and two secondary windings. The primary winding is tied to 120 volts ac via a 3-prong ac cord. Secondary winding (3 and 5) derives ±19 volts ac and has a center-tap ground (4) which is tied to the full-wave rectifier (CR1) via terminals 3T1 and 5T1. The output of CR1 at terminals +V and -V is +18.5 and -18.5 volts (±0.5 Vdc) respectively. Secondary winding 6 and 7 derives +14 volts (±0.5 Vdc) which is tied to full-wave rectifier CR26. The output + of CR26 (+13.5 volts) is tied to the collector of transistor Q1.

4.02 IC1 is a voltage regulator for the +12 volt supply. The output voltage at terminal 4 is capable of supplying up to 300 mA with ±0.5 volt regulation. Resistors R1 and R2 are arranged as a voltage divider, which determines the output voltage at terminal 4 of IC1. Resistor R3 provides a voltage drop under output short-circuit conditions. The regulator detects the voltage drop across resistor R3 and turns off. Resistor R4 is provided to eliminate any VHF instability problems resulting from excessive lead lengths at the regulator output.

4.03 IC2 is a voltage regulator for the -12 volt supply. The output voltage at terminal 6 is capable of supplying up to 300 mA with ±0.5 volt regulation. Resistors R6 and R7 form a voltage divider, which determines the output voltage at terminals 6 and 8 of IC2. Resistor R5 provides an output short-circuit detection which turns off the regulator under this condition.

4.04 IC3 is a voltage regulator for the +5 volt supply. Resistors R8 and R9 form a voltage divider which determines the output voltage at terminal 4. Resistor R10 provides the same function as resistor R5 in 3.19. Resistor R11 provides detection of the output voltage level.

4.05 Transistor Q1 is arranged as a constant current emitter-follower. Terminal 4 of regulator IC3 provides the bias voltage for transistor Q1, which can provide up to 3 amperes dc. Capacitors C1 through C6 on the rear panel are filter capacitors. Capacitors C7 and C8 on the rear panel are transient filters. Capacitors C1, C2, and C4 on CP3 are used for reducing noise. Capacitors C2 and C3 are used to prevent high-frequency oscillations.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 105 to 135 volts at 50 to 60 Hz.

1.02 Baud rate maximum is 9600.

2. FUNCTIONAL DESIGNATIONS

None.

3. FUNCTIONS

3.01 To provide for the generation and measurement of data signals of either Baudot or ASCII codes at baud rates from 45.5 to 1800 baud. The ASCII test sentence is available in three different lengths.

3.02 To provide for an external clock and accommodations for customer-provided crystal clocks.

3.03 To generate a 1-, 2-, or 3-character selectable message in either Baudot or ASCII code.

3.04 To generate and measure marking bias, spacing bias, switched bias, marking end distortion, spacing end distortion, switched end distortion, and combination switched distortion from 0 to 49 percent in 1-percent steps.

3.05 To provide for continuous, one-character-at-a-time, or repetitive-character transmission.

3.06 To provide for manual resetting of the test sentence and distortion displays.

3.07 To provide a local test for back-to-back testing of the transmitting and receiving portions of the test set.

3.08 To provide for EIA, hub, polar, and neutral modes of operation.

3.09 To check both odd and even parity.

3.10 To count odd or even parity errors.

3.11 To provide a means of generating a steady spacing output.

3.12 To provide a filter to eliminate the effect of short transients (approximately 100 microseconds) in the received signal.

3.13 To count distortion hits above a predetermined level.

3.14 To provide a display of characters as they are received.

4. CONNECTING CIRCUITS

None.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are specified in X-78827.

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SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 The drawing is reissued to correct the BAUD rate information, bring the codes of integrated circuits up to date, to remove the part of a power supply from CP3 and add these removed components to a new CP4. Additional components have been added and codes changed to improve the operating margins of the set. These changes were done on a NO RECORD basis since no equipment has been manufactured. All of the changes will be included in the manufactured units.

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3

DATA SYSTEMS STATION EIA TEST ADAPTER NO. 911P FOR USE WITH RS-232A, B, OR C INTERFACE CONNECTORS

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The EIA Test Adapter No. 911P is designed as an aid in testing data set modems and associated terminal equipment which use the standard RS-232A, B, or C interface connectors.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The EIA Test Adapter No. 911P is a small unit which may be carried in the cover of either the 911A or the 911NA data test set (DTS). The adapter is mounted in a metal box which measures 4-3/4 inches high, 2-1/2 inches wide, and 1 inch deep. Attached to the box are two 8-inch cords, terminating in 25-pin connectors, which allow the 911P test adapter to be connected in series with the data set and the terminal equipment. Pin jacks and switches are provided to enable several functions to be checked and measurements to be made with either a 911A or a 911NA DTS. Pin jacks are also provided which enable voltage measurements to be made on the +V, -V, and CF leads and for testing the secondary channel of the data sets 202 type.

SECTION II - DETAILED DESCRIPTION

1. MONITORING INCOMING AND OUTGOING SIGNALS

1.01 The 911P test adapter provides monitoring access to the EIA signals between the data set and the terminal equipment. To prevent the loss of any messages during insertion of the adapter, traffic is stopped momentarily on the circuit to be tested. The female connector on the cord interconnecting the terminal equipment and the data set is removed from the socket, and the adapter is connected in series with the circuit (as shown in Information Note 302). With all switches on the adapter in the NOR (down) position, the circuit is connected through on a lead-by-lead basis so traffic can be restored. As shown on FS1, the pin jacks (BA-T and BA-DS) associated with lead 2 enable the 911 DTS to monitor and measure transmission from the terminal toward the data set. Similarly, the pin jacks (BB-T and BB-DS) associated with lead 3 enable the monitoring and measuring of the incoming signals between the data set and the terminal. Cords coded P1N which are equipped with pin plugs can be used to connect from either the BA (outgoing) or BB (incoming) pin jacks to the VOLT-IN jack [VOLT-IN (911A), VOLT-INPUT (911NA) with input switch on the EIA position] of the 911 DTS and to connect between the circuit ground on the AB pin jack, associated with lead 7 of the adapter, and the 911 DTS ground (GRD). Since this monitoring and/or measurement is done on a high impedance basis, it has no effect on the signals being transmitted or received, thus enabling the checks to be made on a normal operating basis.

2. VOLTAGE MEASUREMENTS OF +V, -V, AND CF

2.01 With the series connections made as discussed in SECTION II, 1.01, voltage measurements of +V, -V, and CF can be made by connecting a voltmeter (10,000 ohms per volt, or higher) or an oscilloscope between the pin jacks on leads 8, 9, and 10 and the circuit ground AB pin jack on lead 7.

3. TRANSMISSION OF SIGNALS FROM THE 911 DTS

3.01 Once the adapter has been connected in series as described in SECTION II, 1.01, signals can be transmitted from the 911 DTS to the data set or the terminal equipment. To transmit from the 911 DTS to the data set, operate the BA switch to the OPEN (up) position, thus opening the path between the terminal and the data set. Connect the 911

DTS VOLT-OUT jack [VOLT-OUTPUT (911A) with output switch on the EIA position, VOLT-OUT EIA (911NA)] to the BA-DS jack and the ground of the 911 DTS to the AB pin jack of the adapter. Asynchronous signals can then be transmitted to (and through) the data set from the 911 DTS.

3.02 The 911NA data test set can be used to transmit through the data set to an outlying selective calling-type station (eg, 85 or 86) by using the three programmable characters to transmit the desired codes. The measuring portion of the 911NA can be used to monitor the answer-back or other signals received from the outlying station. The incoming signals will be shown on the LED display of the 911NA DTS. The correctness of the received characters, parity errors, and the amount of distortion received can thus be checked at one time. The BB switch should be operated to the OPEN (up) position for this test to prevent the incoming signals from going to the terminal. The VOLT-IN pin jack of the 911 DTS should be connected to the BB-DS pin jack in order to monitor the incoming signals.

3.03 If loop-back is available at the outlying station, the method discussed in 3.02 can be used to check transmission through the outlying data set. If the outlying data set is not equipped for loop-back operation, but an EIA test adapter is available at the outlying station, loop-back operation can be obtained as covered in 4.

3.04 To transmit from the 911 DTS to the terminal equipment, operate the BB switch to the OPEN (up) position, thus opening the path between the terminal and the data set. Connect the 911 DTS VOLT-OUT jack [VOLT-OUTPUT (911A), VCLT-OUT EIA (911NA)] to the BB-T pin jack and the ground of the 911 DTS to the AB pin jack of the adapter. Signals can then be transmitted from the 911 DTS to the terminal.

3.05 In a manner similar to that previously described, monitoring and measurement of signals from the terminal can be made simultaneously by connecting the measuring portion of the 911 DTS to pin jack BA-T of the adapter. Any signals being transmitted from the equipment can be blocked or allowed to go to an outlying data set by operating the BA switch to OPEN (to block) or leaving it in the nonoperated (NOR) position to pass the signals. With the BA switch in the nonoperated position, any signals returned from the outlying station may be monitored in the BB-DS jack of the adapter.

4. LOOP-BACK OPERATION

4.01 With the EIA test adapter connected in series as previously discussed, loop-back operation of the data set can be obtained by operating switches BA and BB to the OPEN (up) position and switch LB to the LB (loop-back) position. The looped-back transmission can be measured at the data set by monitoring in either the BA-DS or the BB-DS jack.

4.02 This method of looping back a data set through the use of the EIA test adapter does not require the use of a 911 data test set.

5. OPERATION OF THE CA+, CA-, AND CD SWITCHES

5.01 In normal operation of the data sets, the CA lead (4) is low if tne terminal is not ready to send and high if the terminal is ready to send. Similarly, lead 20 is low or high depending on whether the terminal is not ready or ready. The CA+ and CD switches provide the capability of simulating the ready condition (high) on these leads when operated to the ON (up) position.

5.02 In a similar manner, the operation of the CA- switch to the OFF (up) position opens the CA lead (4) toward the terminal equipment and connects it to -V (lead 10).

6. TESTING THE SECONDARY CHANNEL OF THE DATA SETS 202 TYPE

6.01 Pin jacks CB, CC, CE, SCA, and SCF provide access for making measurements on leads 5, 6, 22, 11, and 12, respectively. The SC switch in the OPEN (up) position opens paths from the terminal equipment on leads 11 and 12 in a manner similar to that of switches BA and BB on leads 2 and 3.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 Provides monitoring access of the EIA signals between the data set and the terminal equipment.

3.02 Provides access for the 911 DTS for transmitting signals to the data set or to the terminal equipment.

3.03 Provides loop-back operation.

3.04 Provides the capability of making voltage measurements on EIA control leads.

3.05 Provides low potential if the terminal is not ready to send and high potential if the terminal is ready to send.

3.06 Provides access for testing the secondary channel of the data sets 202 type.

4. CONNECTING CIRCUITS

4.01 None.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The requirements covered herein apply to the EIA Test Adapter No. 911P Circuit per J79911.

5.02 Sufficient checks shall be made to assure that the wiring of the EIA Test Adapter No. 911P is in agreement with SD-73112-01.

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