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INSTRUCTION MANUAL
FOR
TELEGRAPH SIGNAL ANALYZER
DIGITECH MODEL DT-603-3

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CHANGE NO.

ERRATA FOR INSTRUCTION MANUAL
FOR
TELEGRAPH SIGNAL ANALYZER
DIGITECH MODEL DT-603-3

DRAWINGS

Figure 8A - Change 5R6, 680 ohms to 700 ohms

Figure 10 - Fgl-2, Correct Resistor Value R1 & R28 from 3900 ohms to 1800 ohms.

Fgl-2, Correct Transistor Value Q1 & Q2 from 2N404 to 2N1300

Fal-2, Correct Capacitor Value C21 from 83 mmf to 150 mmf

Figure 16 - Ge4-2, Correct Transistor Value Q2 from 2N404 to 2N1300

Figure 17 - Add C26, 150 mmf across R24

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DIGITECH, INC.
8/3/66
Revision #1

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Chapter 1

INTRODUCTION

1-1. Scope:

This instruction manual describes the Telegraph Signal Analyzer, Model DT-603-3 and covers its installation, operation, and alignment.

For variations of the DT-603-3 operating on other or additional speeds and inputs, an attachment sheet is provided, noting these changes.

1-2. Purpose and Use:

The DT-603-3 is a high quality, portable, transistorized telegraph signal analyzer operating on the digital principle.

It uses digital techniques to measure all types of telegraph distortion on all or individually selected transitions within a character, and displays the result on an easy to read linear scale meter.

1-3. Description:

Refer to Figure 1. The DT-603-3 is housed in a portable case measuring approximately 9" high by 7¼" wide by 9¼" deep. A carrying handle is provided at the top of the case.

A door is provided on the right side of the unit for access to all non-operating adjustments.

A 3-wire line cord extends from the rear of the unit. The signal input jack is located on the front panel.

1-4. Technical Description:

The DT-603-3 is completely semi-conductor in design, making full use of digital circuitry to create a test instrument for the analysis of telegraph signals.

The DT-603-3 measures all types of distortion on all or individually selected transitions within a character. Bias and End distortion as well as Total Peak, Early Peak, and Late Peak are displayed on an easy to read meter, permitting even an untrained operator to make accurate, unambiguous measurements. Peak readings are displayed with full instrument accuracy and remain displayed until reset manually.

The use of the digital principle makes possible distortion measurements to an accuracy of 2% without any warm-up period or operator adjustments. Long term accuracy is essentially independent of component aging and drift.

A most important feature of the digital principle is that it makes the instrument operation and accuracy independent of speed to an upper limit. Standard operating speeds of 45.5, 50, 61.1, 74.2, 75 and 150 Bauds are supplied internally with provision on the rear panel for using an external oscillator for operating speeds up to 1200 bauds.

The DT-603-3 will measure distortion on start/stop telegraph and data signals of 5,6,7, or 8 level codes, without regard to the length of the stop interval. (With Synchronizer Adapter SA-3 Option it will also phase lock its timing to that of the incoming signal to measure distortion on synchronous signals.)

Measurements may be made on a current basis without interrupting traffic for neutral telegraph signals of 20 or 60 ma and polar signals of 20 or 30 mas. In addition, measurements may be made on a voltage basis using the Hi Z input.

The capabilities of the DT-603-3 described above enable its use in the complete analysis of a telegraph signal to determine the amount and type of bias or end distortion it may contain. The use of EARLY and LATE PEAK distortion measurements enable an operator to determine the amount of fortuitous or cyclic distortion in the signal, while TOTAL PEAK indicates the largest amount of distortion in the signal under test. The instruments ability to measure all transitions or to select each bit individually is an aid in isolating the cause of distortion and can be used to measure speed errors.

1-5. Technical Characteristics:

Types of Distortion Measured:	Marking and Spacing Bias Marking and Spacing End Total Peak Early Peak Late Peak
Display:	Meter readout with indicating lights for Marking and Spacing.
Speeds:	1. Speeds are 45.5, 50, 56.8, 74.2, 75, 150 and EXTERNAL. 2. An external oscillator may be used to operate the instrument at speeds up to 1200 bauds.
Codes:	Operates on standard 5, 6, 7, and 8 level start/stop codes with any length stop interval. Operates on Synchronous signals when Synchronizing Adapter SA-3 option is provided.

Inputs:	1. Isolated 20 ma. (200 ohms) and 60 ma. (67 ohms) neutral, and 30 ma. (200 ohms) polar loops. 2. Hi Z INPUT (High impedance input) operating on a voltage basis with a signal of -5 volts or more for Mark and Gn. or a positive voltage for Space. This input will operate the DT-603-3 on either a neutral or polar basis, presenting an impedance of approximately 50K ohms for negative signals and a higher impedance when the signal goes positive.
Peak Reset:	Peal readings are maintained at full level until manually reset.
Distortion Accuracy:	2%
Bit Transition Selection:	All or individual selected transitions may be measured.
Signal Indicator:	A light indicates the condition of the loop. (lights on Mark)
Character Sync:	A sync pulse occurring once per character is supplied.
Operating Temperature:	0°C to 50°C
Power:	The self contained power supply operates from 115 volts a-c 50 to 400 cps, using approximately 15 watts of power.
Physical:	The unit is portable, fitting in a case 9" high by 7¼" wide and 9¼" deep, weighing approximately 8 pounds.

Chapter 2

UNPACKING AND INSTALLATION

2-1. Unpacking and Checking

Remove the DT-603-3 from its shipping container. While doing so check the outside of the case for possible damage incurred during shipment.

2.2. Installation

The DT-603-3 is a self contained portable instrument so no special installation procedures are required.

The line cord should be plugged into a 3 wire receptical of 115v A.C. 60 cycles.

A standard telephone jack is required to patch into the input loop.

When in use, the DT-603-3 should be placed on its rubber feet on a horizontal surface. Operation of the unit on its side or back will result in loss of meter accuracy.

EXTERNAL OSCILLATOR

If an external oscillator is to be used a Cinch Jones plug CJP302CCT must be obtained and wired to the external timing source. Pin 1 (wide) should contain the 10 volt RMS. signal while Pin 2 (narrow), the groud.

SECTION 3
OPERATION

3-1. Chart of Operating Controls, Indicators and Connectors

Control, Indicator or Connector	Position	Function
Power (DPDT Slide Sw)	ON	Connects both side of line cord to equipment and turns on power.
Power (Neon Lamp)		Lights when ac power is applied.
Signal Indicator (lamp)	Flash	Lights when the input signal is a MARK.
INPUT (phone jack)		Provides connection to INPUT circuits.
Input Polarity (DPDT Slide Sw)	+	Connects tip of jack to positive side of input.
	-	Connects tip of jack to negative side of input.
Speed-Bauds	Selected	Sets analyzer operating speed to the indicated rate in bauds or for use with an external oscillator.
Transition Select (Rotary Sw)	ALL	For the analysis of all transition positions in a character as determined by the AVERAGE-PEAK switch.
	1 through 9	For the selection of individual transition positions in a character.
Average-Peak (Rotary Sw)	Bias	For the measurement of average distortion on the space to mark (S/M) transitions.
	End	For the measurement of average distortion on the mark to space (M/S) transitions.
CODE-Levels (Rotary Sw)	5,6,7,8	For the selection and measurement of 5,6,7, or 8 level Start/Stop signals.
	Sync.	For use when the Synchronizing Adapter (option) SA-3 is supplied.

Control, Indicator or Connector	Position	Function
	Total (Peak)	For the measurement of Peak distortion on both S/M and M/S transitions occurring both earlier and later than.
	Early (Peak)	For the measurement of peak distortion on both S/M and M/S transitions occurring earlier than normal.
	Late (Peak)	For the measurement of peak distortion on both S/M and M/S transitions occurring later than normal.
INPUT MA (Lever Sw)	20N	For use with 20 milliamp neutral loops.
	60N	For use with 60 milliamp neutral loops.
	30P	For use with polar loop having from 5 ma. to 30 ma. of current.
Meter Reset (Lever Sw)	OFF	No reset is generated in this position.
	ON	Resets meter to zero-(must be used when making peak readings.)
	Cal (40)	Causes meter to read 40 percent for meter calibration purposes.
Meter		Indicates the magnitude of distortion on the input signal from 0 to 50 percent.
Marking (lamp)		Lights when average distortion is of the marking type.
Spacing (lamp)		Lights when average distortion is of the spacing type. NOTE: Both lights are not when measuring peak distortion.
Loop Fuse	1/10 Amp 8AG	Lo impedance input protection.

Control, Indicator or Connector	Position	Function
Test Points	Gnd.	Connects to circuit ground.
	SIG.	Connects to internal circuit side of the input isolator (Positive on mark)
	SYNC.	Provides a once per character synchronizing pulse.
Filter (Side Sw)	IN	Causes removal of small holes in input signal before analysis on Speeds up to 75 Bauds only.
	OUT	Removes filter from the circuit.
Ext. Osc. (2 Pin Socket)		Provides means for connecting an external Timing source.
Hi Z INPUT		Provides connection to high impedance input circuit.

3-2. Operation:

The DT-603-3 may be used by unskilled operators for measuring average and peak distortion on telegraph lines. With a more skilled operator it may be used as a laboratory instrument for the complete analysis of such signals.

a. Initial Steps: Plug the a-c line cord into a source of 115v, 60 cps power and turn the power switch to ON. The power indicator should light.

Set the Speed-Baud switch to the rate of the signal to be measured.

Set the Input MA switch to the current condition of the signal to be measured.

Plug the analyzer in series with the loop. If the SIG IND light does not flash, reverse the INPUT Polarity Switch.

Make sure the TRANSITION SELECT switch is on the ALL position.

NOTE: A check of the meter accuracy can be made by using the METER RESET switch in the CAL (40) position to produce a reading of 40 on the meter. If an adjustment is necessary see Chapter 4. (Such adjustment should not be necessary under normal operating conditions.)

b. Bias Distortion (See Figure 4)

Distortion in telegraph is defined as the time displacement of a signal transition from its correct position. On shaped signals, the time of a transition is taken as the half current point for neutral signals and as the zero cross-over point for polar signals.

Bias distortion is defined as an average displacement of the space to mark (S/M) transitions from the correct position. It is marking bias if the resulting mark interval is lengthened (transition occurs early), and it is spacing bias if the preceding space interval is lengthened (transition occurs late).

To measure bias distortion on the DT-603-3 set the center switch to the BIAS position. The amount of bias will register on the meter, with the lights indicating whether it is marking or spacing.

A signal containing zero distortion and operating at the same speed as the analyzer will cause the meter to read zero and the marking and spacing lights to blink alternatively.

c. End Distortion (See Figure 4)

End distortion is defined as an average displacement of the mark to space (M/S) transitions relative to the first M/S transition (start pulse). It is called marking end if the preceding mark interval is lengthened (transition occurs late), and it is called spacing end if the resulting space interval is lengthened (transition occurs early).

To measure end distortion on the DT-603-3 set the center switch to the END position. The amount of end distortion will register on the meter, with the lights indicating whether it is marking or spacing.

d. Total Peak Distortion

Total Peak distortion on the DT-603-3 is defined as the highest amount of distortion occurring on a signal. It may occur on M/S or S/M transitions, either early or late. A single transition is sufficient to give the peak distortion with full accuracy. The reading will be maintained indefinitely until it is changed by a higher one or reset to zero. In short, a Total Peak measurement, provides a reading of the highest amount of distortion in a signal from any cause.

To make a Total Peak measurement on the DT-603-3 set the center switch to the TOTAL position and reset the meter. The meter reset switch should then be used to destroy the old peak reading before taking new ones.

For all PEAK settings of the center switch the Marking and Spacing lights are made inoperative. This is due to the fact that both type of transitions are measured simultaneously and the definition of Marking and Spacing changes with the type of transition.

e. Early and Late Peak Distortion

When the center switch is set to Early Peak the DT-603-3 measures the maximum distortion of both M/S and S/M transitions occurring earlier than the correct time.

When the center switch is set to Late Peak the DT-603-3 measures the Maximum distortion of both M/S and S/M transitions occurring later than the correct time.

This ability to display separately peak distortions which occur early and those which occur late, enables the operator to measure the maximum amount of random fortuitous distortion prevalent when transmitting teletype over radio circuits.

f. Transition Selection

The DT-603-3 will measure distortion for all transition times in a character restricted only by the center switch (for example on Bias only S/M transitions are measured). In addition, the TRANSITION SELECT switch may be used to restrict the measurement to any one of the intervals one half baud either side of a correct transition location.

This feature is useful in locating defective segments on commutators and locating distortion sources which are evident only in certain bits of a character. It is further useful in detecting distortions due to small speed errors in the signal. NOTE: DO NOT USE FOR SYNCHRONOUS OPERATION.

g. Measuring Speed Error

Small differences in speed between the DT-603-3 and the incoming signal can be determined through use of the TRANSITION SELECT. On a random signal pattern the distortion measurement on each successive transition will increase. A faster incoming signal will introduce Marking Bias, shile a slower input signal will introduce Spacing Bias. The amount of speed error in percent is one-fifth (1/5) of the increase in distortion reading from transition 1 to transition 6. For example a 5% increase of Marking Bias from position 1 to position 6 would indicate that the incoming signal speed is 1% fast.

h. Front Panel Test Points

There are three test points located to the right of the front panel for use in observing the incoming signal on an oscilloscope.

The GND point provides access to the internal circuit ground.

The Sync point provides a once per character synchronizing signal. It is negative going one-half bit into the STOP interval and positive going at the beginning of a character. It is approximately 13 volts in amplitude.

The SIG point provides a reproduction of the input signal at the output of the input loop isolation circuits. This reproduction is a true one with no changes in the shaping on the original signal. The resulting signal measures about 2 volts and is referenced to the internal signal ground. Marks are shown positive and Spaces are negative. No signal is seen at this point when the Hi Z input is used.

i. FILTER Switch

On the front panel of the unit is a two position slide switch for the insertion of a filter in the input circuit chain. It will remove from the signal noise due to contact bounce and atmospheric conditions as wide as ½ milisecond in time duration. For normal use, this filter should be left out of the circuit. It must be left out at operating speeds above 75 Bauds.

j. EXTERNAL Oscillator

On the rear panel of the unit is a two pronged jack provided for inserting an external oscillator at 200 times the desired operating speed in bauds, up to a maximum of 1200 bauds. See Chapter 2, Installation for details in connecting this signal.

The signal may be sine or square wave at an amplitude equivalent to 10 volts RMS. The signal may remain connected to the unit while the DT-603-3 is used on its internal speeds and will operate at the external speed only when the SPEED-BAUDS switch is set to the EXT position.

k. Input Polarity

The input polarity switch is used to connect the incoming loop signal to the polarity sensitive isolator circuit. When in the + position it connects the Tip of the INPUT jack to the + side of the isolator, when in the - position it connects the tip of the INPUT jack to the - side of the isolator. If the DT-603-3 is plugged into a loop and the SIG IND light does not flash, reverse the POLARITY switch. The polarity switch does not affect the HI Z input.

l. Signal Indicator

The SIG IND light is a long life incandescent lamp introduced into the circuit in such a way as to light when the loop is on Mark.

m. Code Levels

The Code Level switch is used to select the proper timing interval within the Analyzer for 5,6,7, or 8 level code signals. A level is defined here as an intelligence bit. For example: Baudot code is 5 level while IBM 10.42 Code is 8 level.

The Sync. position of this switch is used only when the Synchronizing Adapter (option) SA-3 is provided. It then causes the DT-603-3 timing to lock onto that of the incoming sy chronous signal, providing the speeds of the incoming signal and the internal timing are within 0.1% of each other.

n. HiZ Input

Access to the HI Z (high impedance voltage bridging) input is made by using the orange HI Z pin jack and the black GND pin jack. The incoming signal must be a minimum of 5 volts in amplitude and connected so that the signal to the HI Z pin jack is negative for the Mark condition and ground (or positive) for the Space condition.

o. Input (Low Impedance)

The low impedance series input is available through the phone type jack. This input is designed to operate in conjunction with the current levels selected on the INPUT MA switch by inserting the DT-603-3 in series with the incoming loop. Resistance is provided across the jack to prevent an opening of the operating loop while inserting the plug.

CHAPTER 4

OPERATOR MAINTENANCE AND ALIGNMENT

4-1. Fuse Sizes and Locations:

For access to the two line fuses, which are 3/8 Amp Slo-Blo the case cover must be removed. This is done by removing the three #6 x 3/8" screws on each side of the cover and lifting it off the base. The fuses are visible on the top of the frame.

A 100 ma. 8AG fuse is provided on the front panel to protect the input isolator from current overloads.

4-2. Crystal Frequencies:

No adjustments are required in the Crystal oscillator of the DT-603-3.

The crystal frequencies and baud speeds relationships are as follows:

SPEED-BAUD	FREQUENCY AT 3ETP1 (CPS)	CRYSTAL FREQUENCY (Kc)
* 37.5	7500 ± 2	120.000
45.5	9100 ± 2	145.622
50.0	10000 ± 3	120.000
* 56.8	11378 ± 3	182.045
61.1	12224 ± 3	195.652
74.2	14840 ± 4	118.720
75	15000 ± 4	120.000
150	30000 ± 8	120.000
*1200	240,000 ± 30	240.000

*These speeds are not supplied in the standard unit

4-3. Adjusting the Meter:

The meter adjustment for the DT-603-3 is made by setting the METER RESET switch to the CAL position and adjusting the miniature rheostat labeled M until the meter reads 40 as seen from the normal viewing position. This rheostat is the one closest to the front of the unit as viewed through the access door.

This adjustment is made at the factory and should only be made as it becomes necessary.

To mechanically adjust the pointer to zero, remove Assembly 1 at the top of the unit to provide access to the adjustment screw on the meter. Adjust the meter to zero with the power ON and the Meter Reset in the ON position.

4-4. Adjusting the Input Circuits:

The remaining three rheostats are used in adjusting the input circuits. They are adjusted at the factory and need only to be checked on an annual basis.

a. 60 MA Threshold Adjust (3ER6)

The rheostat designated 60B is used to adjust the threshold point of the input circuits to operate when the input current of a 60 ma loop exceeds 30 ma.

Set the Input MA switch to 60 MA and adjust the steady mark current in the loop for 30 MA. Key the loop and adjust the 60B rheostat until the SIG IND light on the front panel passes from an off condition to the point where it begins to flash. This sets the input circuits to threshold at 30 MA.

b. 20 MA Threshold Adjust (3ER5)

The rheostat designated 20B is used to adjust the threshold point of the input circuits to operate when the input current on a 20ma. loop exceeds 10ma.

Set the INPUT MA switch to 20 MA and adjust the steady mark current in the loop to 10 ma. Key the loop and adjust the 20B theostat until the SIG IND light on the front panel passes from an off condition to the point where it begins to flash.

c. Filter Adjust (3ER4)

The rheostat designated FIL is used to adjust the input circuits so that no distortion is introduced by the addition of the internal filter.

A steady source of signal having no variation in distortion (though it may have a fixed amount) must be available for this adjustment.

The technique used for adjusting the Filter circuit is to adjust the FIL rheostat so that the DT-603-3 gives the same readings whether the filter is IN or OUT of the circuit.

This represents all of the adjustments in the DT-603-3.

CHAPTER 5

THEORY OF OPERATION

5-1. General:

a. Introduction

The DT-603 uses computer logic curcuit techniques to measure time displacements of signal transitions from a reference and to display the result as a percent distortion on a meter.

The majority of circuits are repetitive and fall into two main classes, bistables (flip-flops) and gates. A detailed analysis of these circuits is provided here and should be used for reference when consulting the remainder of the theory.

b. Bistables (flip-flops)

A typical flip-flop is shown in figure 3. The circuit is called bistable because it has two stable states. The circuit is in a stable state with Q1 conducting (on) and Q2 non-conducting (off) or vice-versa. Assume Q1 on and Q2 off. The collector of Q2 will be at a negative potential close to the supply voltage. This negative voltage causes current to flow through R6 to the base of Q1 to saturate it. Some of the current flows through base resistor R3 to the +15 volts supply, to maintain a negative base to emitter voltage capable of saturating Q1. The saturation current of Q1 causes a voltage drop across R1 which places the collector of Q1 near ground (approx. -.2v). The voltage divider formed by R2 and R7 from ground to positive 15 volts places the base of Q2 positive thereby insuring turn-off. Resistors R3 and R7 absorb collector leakage current Icbo during the off condition to insure that either transistor can be reverse biased up to temperatures of 50° Centigrade. The resulting condition is stable since Q1 - is forced by Q2 - off to remain that way and Q2 - off is forced by Q1 - on and the positive bias from R7 to remain that way. The circuit operation is identical with Q1 turned off and Q2 turned on.

A change in condition is usually accomplished by triggering the "ON" transistor off. The regenerative action of the circuit then turns the "OFF" transistor on. For example to turn Q1 off a positive pulse is applied to C1 where it is differentiated by C1R4. The resulting positive spike passes through CR1 to the base of Q1 to turn it off. Capacitors C2 and C4 help to speed up the regenerative action which then tales place while Q1 is turning off and Q2 is turning on. When the flip-flop is used in a counting function, input capacitors C1 and C3 are tied together. The input pulse is steered to the off transistor by the differentiating resistors R4 or R8. The collector of the Q1, the "ON" transistor, is at ground thereby allowing the trigger to go positive at the junction of C1R4 while the collector of Q2 is at -9 volts keeping the trigger at C3R8 at a net negative potential. This system is called collector steering.

When a flip-flop is not used for counting, but rather as a storage element resistors R4 and R8 may be returned either to the collectors or to external steering signals. Several trigger circuits consisting of a capacitor, resistor, and diode combination may be used for each transistor of the flip-flop.

c. Gates

Two types of logical gates are used in this unit, the transistor NOR gate and the diode AND gate. The most frequently used gate is the transistor "NOR" gate shown in figure 3b. It consists of a transistor Q1, its collector resistor R1, a base biasing resistor R2 (mainly for operating at elevated temperatures) and a number of input resistors which may range from one to six. The gate operates so that a single negative input will cause Q1 to saturate and bring its collector to ground. On the other hand all inputs must be positive (ground potential) to cause Q1 to turn off and provide a negative output. Thus the gate will go negative when there is positive coincidence on <u>all</u> inputs, a characteristic which makes it an AND gate, or the gate will go positive when any of the inputs goes negative, a characteristic which makes it an OR gate. The circuit then is used to perform both the AND and the OR logical functions by proper choice of input signals.

Capacitor C1, a small capacitor, is sometimes used to speed up the operation of a gate during the turn-off time.

The diode AND gate shown in figure 3c. is another form of the logical AND gate. Unlike the transistor gate described above it does not invert the signal. <u>Any</u> negative signal on one of the inputs will cause a negative output through a forward biased diode regardless of the signals on the other three. If <u>all</u> the inputs are positive (ground) then the output will go positive.

The diode gate in figure 3d. is also an AND gate but operates in such a way that any positive (gnd) signal on one of the inputs will cause a positive output through a forward biased diode regardless of the signal on the other input. If <u>all</u> inputs are negative, then the output will go negative.

The choice of which type of diode AND gate type is used depends on the polarity of the desired output.

<u>5-2. Block Diagram Theory of Operation</u>:

Refer to figure 5, a Block Diagram of the DT-603-3

NOTE: See Chapter 7 PARTS LIST for an explanation of submodule and component reference designations and locations.

The heart of the unit is a crystal controlled Pierce Oscillator operating at several hundred times the desired rate in bauds, operating into a four stage binary divider (9AF, 3AF, 3BF, and 3CF). Switch 5S4 selects the proper crystal for the oscillator and selects an output from the binary divider at 200 times the operating rate in bauds. The selected divider output passes through gates 3KGQ1 and 3KGQ2.

The squared up timing signal is then applied to 3J603-S2 Q1 where

its passage through this gate is controlled by a stop pulse generated by the combination of the timing chain and the input signal being measured.

When the timing signal is allowed to pass through 3J603-S9 it is divided in half by 3LF and further divided into one hundred parts by two decades in cascade to produce a timing signal at 1JF which completes one full cycle per bit. The position of the timing chain starting with binary 1AF and ending with binary 1JF has therefore, one hundred states or counts per bit of input signal. It is this count which determines distortion in the input signal. The input signal transition creates a transfer pulse to transfer the count from this timing chain into a Register where it is stored, decoded, and appears as a reading on the meter.

The counter formed by binaries 1EF, 1FF, 1LF, and 3FF and gates 8BG 8CG Q1 and 8CG Q2 determine character timing. Assume that gate 3J603-S9 Q1 is closed and the timing chain is not operating. The next M/S (mark to space) transition of the input signal will cause 8CG Q2 to go positive, thereby resetting binaries 1AF, 1BF, 1CF, 1DF, 1IF 1EF, 1FF, 1LF, and 3FF to a "one" state. The change in 1EF causes 8BG Q1 to saturate (gnd.) and thereby open 3J603-S9 A1 allowing timing signals to pass through. When six and one-half bits have been counted gate 8BG Q1 turns off (negative) stopping the timing cycle. Measurements are possible then during the first 6½ bits of a telegraph signal on 5 level operation. For 6 level operation the circuit times out 7½ bits; for 7 level, 8½ bits; and for 8 level, 9½ bits.

The outputs of the character timer (1EF, 1FF, 1LF, and 3FF) are selected through the TRANSITION SELECT switch 5S3 as inputs to a diode AND gate on Assembly 3. Its output is always positive on the ALL position and is positive for one bit only, starting ½ bit before and ending ½ bit after a properly timed selected transition. Its output is used to limit the generation of a transfer pulse to the selected time interval.

The input telegraph signal is connected through a polarity reversing switch 5S7 to an Isolator 3GI allowing the DT-603-3 to be inserted anywhere in series with the telegraph loop without concern for grounds. The output of the Isolator is biased for the selected loop current and is connected to a threshold circuit consisting of the amplifiers of 3H603-S4 before being squared up in Schmitt Trigger 3IT. A noise filter may be introduced into the threshold circuit by switch 5S8. Since the threshold circuit is adjusted to provide snap action at the mid-current points of the incoming signal, the output of 3IT provides a squared replica of the incoming signal with the transitions occurring at the mid-current points of the incoming signal. The output from 3IT is further reproduced in binary 3DF, one side of which operates the SIGNAL INDICATOR Lamp 5DS3 when the incoming signal is a Mark.

When the Hi Z voltage input is used the isolator 3GI is completely bypassed and the signal is amplified by gate 3J603-S9 Q2 before entrance to going to the threshold circuit of 3H603-S4.

The transitions from 3DF are used to generate transfer pulses at 8AF as selected by the AVERAGE-PEAK switch, 5S5. When measuring Bias distortion, only the S/M (space to mark) transitions are allowed to generate transfer pulses. When measuring END distortion, only the M/S transitions are allowed to generate transfer pulses. When measuring PEAK distortion both the S/M and M/S transitrons provide outputs at 8AF, where potential transfer pulses begin. The selected input signal transitions are used to set binary 8AF. The binary is then reset within 1/100th of a bit by an output timing signal from binary 3LF so as to insure that a transfer will not occur during the short time interval that the timing chain is in the process of changing.

The transfer pulses generated in binary 8AF are a-c coupled into gates 8DG Q1 and 8DG Q2 where a number of restrictions are placed on their passing through. The first restriction allows transfers which occur later than the correct time to pass only through 8DG Q2, while those occurring earlier than the correct time are allowed to pass only through 8DG Q1. A second restriction allows no transfer to pass for the Start pulse, since this is the reference for all timing in a Start-Stop telegraph signal and has, by definition, no distortion. A third restriction is from the TRANSITION SELECT which may limit the passage of transfers to a selected time interval during a character. The fourth restriction comes from the EARLY and LATE PEAK positions of 5S5 which allow only the selected type of transition to pass by saturating 8DG Q2 for EARLY PEAK and 8DG Q1 for LATE PEAK. The fifth and final restriction is active when peak measurements are being made. The output of the Peak Logic circuits prevents a transfer from passing unless it represents a higher distortion than that already stored in the Register.

Thus the surviving transfer pulses, representing incoming signal transitions to be measured are generated and passed through inverting driver gates 8EG Q1 and 8EG Q2 where they are used to transfer the count in the timing chain for storage in the Register.

The Register is made up of binaries 2AF, 2BF, 2DF, 2EF, 2LF, 2KF, 2IF, and 2HF. The outputs of each binary of the two decades of the timing chain is connected to a corresponding stage in the Register in such a way that either the number in the timing chain or its one's complement can be transfered. The Late transfer signal transfers the number directly while the Early transfer signal transfers the one's complement of the number in the timing chain. This reversal of numbers provides for counts of 0 to 49 during the position of a bit when transitions are Late and from 49 to 0 during the position of a bit when transitions may be Early. The number transfered into the register at the time of a signal transition becomes numerically the percent distortion. The decision as to type is made by the selector switch 5S5 and the MARKING and SPACING lights. These lights operate from the eighth stage of the Register indicating whether the transition occurred earlier or later than normal.

The number stored in the first seven stages of the Register are decoded by a precision resistor network into a heavily damped meter to display the magnitude of distortion in percent.

The peak Logic circuitry made up of sub-modules 2C603-S1, 2F603-S1, 2JG and 2GF compare continuously the number in the Register with that of the timing chain decades. A gating signal is formed in 2GF which is positive only for those numbers where the timing chain count is equal or greater

than the number in the Register. This peak gating signal when selected by 5S5 becomes one of the restriction of the passing of transfer signals through 8DG Q1 and 8DG Q2.

Meter Reset switch 5S2 is used to manually reset the Register to zero or in the Cal. (40) position to set it to 40. The meter is provided with a variable shunt resistor 3ER7 for adjusting it to read 40 in the CAL position of 5S2.

5-3. Assembly 1 - Timing Counters:

Refer to figures 6A, 6B, and 9A

Assembly 1 contains the two Decade Counters of the Timing Countdown and three of the four stages of the Bit Counter.

A timing signal at a frequency of 100 times the rate in bauds coming from Q2 of 3LF (3LF output) is used to trigger the first stage of the first decade counter made up of binaries 1AF, 1BF, 1CF, 1DF and gate 1KG Q1. The decades used in the DT-603-3 use a 1-2-4-2 weighting on the binary stages as shown in the wave forms of figure 6a. When a count of 0010 (4) is reached 1KG Q1 turns off (negative). At the next count its output goes positive changing the count to 1101 (5). Stage 2 (1BF) is reset to a 1 while the last two stages are reversed by triggering 1CF to a zero which in turn triggers 1DF to a 1 state. The output of 1DF has a frequency of 10 times the rate in bauds.

The second decade, made up of binaries 1GF, 1HF, 1IF, 1JF and gate 1KG Q2. Its operation is identical to that of the first decase described above.

The remainder of the assembly is taken up by binaries 1EF, 1FF, and 1LF which together with binary 3FF make up the Bit Counter (Character timer). The "0" output of 1JF is used instead of the "1" output to trigger the first stage of the counter, providing a one-half bit offset at the beginning of a character. The outputs of these four binaries are decoded by switch 5S3 TRANSITION SELECT to provie on Assembly 3 a gating output one bit wide beginning one-half bit before and ending one-half bit after a correct input signal transition.

The output of these binaries is also connected to Assembly 8 where a count of 6½, 7½, 8½, or 9½ is detected before a STOP pulse is generated in 8BG Q1 to prevent further oscillator signals from entering the counting chain.

The TIMING RESET signal is caused by the telegraph signal Start transition and resets the decades and the Bit Counter stages to all "1" 's. This destroys the coincidence of the stop gate 8BG Q1 Assembly 8 allowing the oscillator signals to enter the timing chain for another character interval up to ½ bit into the stop pulse.

5-4. Assembly 2 - Register and Peak Logic:

Refer to figures 7A and 7B.

Assembly 2 contains two major sections, the Register and the Peak Logic Circuits.

a. The Register

The Register is made up of eight binaries corresponding on a stage for stage basis with the eight binaries of the two timing decades of Assembly 1. The trigger networks of these stages are connected to the decades in the manner shown in Figure 7A so that when a Late transfer command pulse occurs, the binary state of each stage of the decade counter is transferred into the corresponding Register stage. When a Early Transfer command pulse triggers the Register the inverse of the binary state of each stage in the decade counter (except the Last-1JF) is transferred into it.

The "0" (pin 12) output of each of the first seven Register stages are connected through a silicon diode for isolation between stages to pin 2 then to a precision resistance decoding network. The output of the resistance network provides a current signal proportional to the digits in the Register. The meter is heavily shunted to provide a damping action and is calibrated directly in percent distortion.

The first seven stages provide current in the ratio of 1.2.4.2.10.20.40 to the meter. When the transistor Q1 is saturated the precision resistor associated with that stage conducts current through the now forward biased silicon diode into the meter. When the Q1 transistor is "OFF", the silicon diode is reverse biased and less than one microampere of current flows through the resistor.

The reverse biasing of the silicon diode is made possible by using the unregulated side of the -15 volt power supply (at a level of about -20 volts) to power all stages on Assembly 2.

The register is reset to zero distortion by clamping each Q2 stage of the Register to ground through a diode (CR27) by means of switch section 5S2A. A calibration signal for the meter at 40% is accomplished by grounding Q1 of the 40% Register stage 2IF in conjunction with the zero reset by means of switch section 5S2B.

The eight the Register stage is used to operate the MARKING and SPACING indicator lights on the front panel for BIAS and END distortion measurements. The state of counter stage 1JF in Assembly 1 changes each half bit (Early and Late). It is this information which is transferred to 2HF. When measuring BIAS, transitions occurring EARLY have MARKING bias while those occurring LATE have SPACING bias. The reverse is true for END ditortion. Switch sections 5S5F and 5S5G provide for the reversing of these lights when switching from BIAS to END.

b. Peak Logic Circuits

The peak logic circuitry is made up of the diode AND gates on sub-modules 2C and 2F (both are special sub-modules type 603-S1 figure 15 gates 2JG Q1 and 2JG Q2 and binary 2GF).

Sub-module type 603-S1 contains seven dual input diode AND gates, the outputs of which are tied together through seven 16K ohm resistors to provide a single current output. The current output from 2C provides signal to the base of 2JG Q1 while that of 2F provides it to the base of 2JG Q2. Gate 2JG Q1 is allowed to pass signals only during the period of Early transitions while 2JG Q2 is allowed to pass signals only during the period of Late transitions.

Consider the operation of the seven diode AND gate group. The "0" output of the first seven counter stages are connected to one of the two inputs of the seven AND gates. The second input of these gates is connected to the Register outputs. On sub-module 2C the "0" outputs of the Register stages control the passage of counter stage outputs so that when the number in the counter equals the 1's complement of the number in the Register the collector of 2JG Q1 goes negative. When it is "less than" 2JG Q1 stays positive, and when it is "greater than" 2JG Q1 follows the counter output. For this reason the first negative output of 2JG Q1 is used to trigger binary 2GF.

On sub-module 2F the "1" outputs of the Register stages control the passage of the counter stage outputs so that when the number in the counter equals the number in the Register the collector of 2JG Q2 goes negative, resetting binary 2GF.

The output of 2GF connects to switch section S5E and provides a gating signal for the transfer pulses on Assembly 8 which on PEAK measurements only allows transfer of a number in the counter to the Register when the telegraph signal transition has a distortion greater than that already stored in the Register.

Note the binary 2GF uses negative triggering and requires a positive voltage for the steering diodes. This voltage is provided by resistors 2R8 and 2R9.

5-5. Assembly 3 - Timing Divider - Input Circuits - Selected Transition:

Refer to figure 8A and 8B.

Assembly 3 contains, the Timing Divider, the Input circuitry, the SELECTED TRANSITION gate, and all adjustments for the DT-603-3.

a. Timing Divider

The timing divider is made up of binaries 3AF, 3BF, 3CF and 9AF on Assembly 9. The function of the timing divider is to divide down the relatively high frequency signal from the crystal oscillator to a frequency 200 times the desired operating rate in bauds. The four stages operate as a straight binary divider on all speeds except 50 baud. The Q1 output

of each binary is selected by switch 5S4C to provide the proper input to timing countdown circuits of the analyzer.

When 50 baud operation is selected switch section 5S4B provides a ground to the reset trigger resistor of binary 3BF to shorten the count from a normal 16 to a count of 12. This allows for the use of a single crystal for operating speeds of 50, 75, 150 etc.

The square wave signal from the squaring gates 3KG is connected to a timing control gate 3J603-S9 Q1 where it is allowed to pass through and trigger 3LF, the first stage of the timing countdown. The flow of signal through 3J603-S9 Q1 is prevented during the "stop" interval which begins 6½ bits (5 level) after the Start of a character and lasts until the Start of the next character.

The output (pin 17) of 3LF is used to trigger the decade counters on Assembly 1. The "0" output (3LF) is used to reset binary 8AF on Assembly 8 after it has been set by an incoming telegraph transition.

b. Input Circuits

The input circuitry is made up of an Isolator, Threshold Detector, Filter, and a Schmitt Trigger.

The input telegraph signal is electrically isolated from the DT-603-3 circuitry through the use of a standard Royer type DC to DC converter. The isolator presents a low impedance (67 ohms on 60 ma and 200 ohms on 20 ma, and 30 ma input positions of 5S1) current input which may be inserted anywhere in series with the telegraph loop.

Refer to figure 14, The input isolator 3GI is made up of a push-pull type oscillator operating between one and two megacycles in frequency. On a MARK condition loop current flows between pins 3 and 6 of sub-module 3GI and the resulting voltage causes the oscillator formed by Q1, Q2, R4 R5, and transformer T1 to oscillate. The filter formed by L3 and C2 prevent the oscillations from appearing on the loop. The oscillator output is coupled through a secondary of T1 to a full wave rectifier made up of CR20 and CR22, and a filter made up of L24, C27, and R28. The result is a positive DC voltage across R28 for mark inputs and, since the oscillator does not operate on space inputs, zero voltage across R28 on space. Thus the telegraph signal is reproduced across R28 isolated electrically from the input loop. It is this signal (pin 24) which is brought to the front panel test point 5TP1 (SIG) for viewing the input.

The other end of R28 (pin 27) is connected through the INPUT MA switch to appropriate adjustable bias voltages for 60 and 20 ma. neutral operation and ground for 30 ma. polar operation.

The output of the isolator, properly biased is connected to the threshold detector 3H603-S4 (see figure 17). Q1 is biased on through resistor R3 and is turned off when the positive signal of the isolator causes the input diode CR5 to conduct, thereby making the base of Q1 positive and

turning the transistor off. The bias voltages are adjusted so that this action takes place at the mid-current level of the telegraph signal.

The output of Q1 drives the Filter circuit made up of capacitors 3C10, 3C11 and the amplifier made up of R24, R25, Q2, and R28 on 3H603-S4 and 3R5. Two filter capacitors are used because the low output impedance of switching transistors allows shaping only on turn off. Thus capacitor 3C10 shapes the S/M transitions only. In order to retain this shaping it is necessary that Q2 operate as a linear amplifier. Two types of negative feedback are provided to insure this condition: current feedback through emitter resistor 3R5 and voltage feedback through R25. Capacitor 3C11 shapes the M/S transitions.

The ground returns for capacitors 3C10 and 3C11 are provided through switch 5S8 FILTER IN-OUT and interlocked with the Speed switch 5S4 to prevent its use on speeds higher than 75 bauds. When inserted into the circuit the Filter helps reduce false starts and errors due to short duration (about ½ miliseconds or less) noise in the input signal.

When the High impedance Input is used gate 3J603-S9 Q2 becomes the input circuit. It presents an impedance of approximately 50K ohms to the line. A negative 5 volts signal on its input will be interpreted by the DT-603-3 as a Mark and a ground signal will be interpreted as a space. The output of 3J603-S9 Q2 connects to the second diode input of threshold gate 3H603-S4. As long as no signal is being applied to the current input 5J1 the Isolator output will not interfere with the operation of the Hi Z INPUT and as long as no signal is being applied to the Hi Z INPUT gate 3J603-S9 Q2 will not interfere with the Isolator output.

The output of 3H603-S4 Q2, either shaped or square, drives a Schmitt Trigger 3IT to provide a good reshaped replica of the telegraph signal with transitions occurring at the half-current points. FILTER Adj. resistor 3ER4 connected between the emitters of the two stages of the Trigger provides a means of adjusting the level at which 3IT changes state. In this way the output of 3IT can be adjusted to be the same with or without the Filter circuit.

The outputs of 3IT are used to trigger binary 3DF andform aregenerated replica of the input signal. Transistor 3DF Q1 drives the SIG IND lamp 5DS3, turning it on when the input signal is in a marking condition.

The outputs of 3DF go to Assembly 8 to form transfer pulses for the Register.

C. SELECTED TRANSITIONS:

Module 3 also contains the diode gate which detects the count in the Bit Counter to produce the selected one bit timing interval for measuring SELECTED TRANSITIONS. Switch 5S3 connects the outputs of the Bit Counter

stage of Assembly 1 and binary 3FF to the input of a diode gate formed by diodes 3CR1 through 3CR4 and resistor 3R1 except in the ALL position when it grounds these inputs. Grounding the inputs of the diode gate provides a positive output thereby neutralizing the effect of this circuit on gate 8DG. When a time interval is selected, however, the diode gate only grounds during the period ½ bit before and ½ bit after the proper transition time for the SELECTED TRANSITION, thereby allowing the gates on 8DG to pass a transfer pulse only during this interval.

Sub-module 3E contains the FILTER adjust network 3ER1 and 3ER4, the 20 MA. (20B) bias network 3ER2 and 3ER5, the 60 MA. (60B) bias network 3ER3 and 3ER6, and the Meter (M) shunt adjust 3ER7.

5-6. Assembly 8 - Transfer Pulses - Character Timing:

Refer to figure 9A and 9B.

Assembly 8 contains the circuitry for transforming telegraph signal transitions into transfer pulses for the Register (8AF, 8DG, and 8EG) and the circuitry which detects character timing (8BG and 8CG).

All Transfer pulses are formed in binary 8AF. Diodes 8CR4 and 8CR5 are electrically connected across Resistors 8AFR6 and 8AFR11 to permit rapid recovery of the trigger circuits of 8AF at operating speeds of 1200 bauds. Switch 5S5 provides a ground steering voltage for allowing

M/S transitions on BIAS
S/M transitions on END
Both M/S and S/M transitions on PEAK

to set 8AF to "0". A timing signal, 3LF, resets the binary within a time of 1/100 of a bit or less. The time of reset, which occurs only when the Decade counters are static, becomes the beginning of a transfer pulse. The output of 8AF is AC coupled to gates 8DG Q1 and Q2. The passage of the Transfer through these gates is then controlled by five factors:

1. Q1 will pass only Transfers occurring EARLY -(input $\overline{1JF}$)
   Q2 will pass only Transfers occurring LATE -(input 1JF)

2. No transfer will pass for the Start transition (first M/S in a character) - the inhibiting signal comes from 8BG Q2.

3. The TRANSITION SELECT may restrict passage of transfers to a selected time interval.

4. On EARLY PEAK position of 5S5 no late transfer pulses will pass through Q2.
   On LATE PEAK position of 5S5 no early transfer pulses will pass through Q1.

5. On all PEAK positions of 5S5 the output of 2GF (PEAK Gate Signal) will prevent transfers from passing through Q1 or Q2, unless they represent a distortion higher than that already stored in the Register.

The surviving Transfer pulses represent those transitions selected to be measured. They are passed through the inverter driver gates 8EG Q1 and Q2 before going to Assembly 2 to trigger the Register.

The character timing is detected by gate 8BG-Q1 from the signals connected to it from the Bit Counter through sections A to D of CODE LEVELS switch 5S9. Gate 8BG-Q1 produces a negative Stop pulse 6½, 7½, 8½ or 9½ bits from the Start transition for settings of 5,6,7, or 8 level respectively on the CODE LEVELS switch. This negative stop pulse is used to prevent timing signals from reaching binary 3LF of the timing countdown during the Stop interval.

The negative stop signal is inverted in gate 8CG Q1 to prime gate 8CG Q2. The S/M signal from binary 3DF, the 2nd input to 8CG Q2 is also positive during the Stop period. Gate 8CG is therefore turned off (negative) from the time the stop pulse begins until the S/M signal from 3DF goes negative. This occurs at the beginning of the next character and causes 8CG Q2 to saturate (positive). The output is used to reset the Decade and Bit Counters, removing the negative Stop signal of timing gate 3J603-S9 Q1 and allowing another character cycle to take place.

Gate 8BG-Q2 detects the count 11 from the last two stages only of the Bit Counter to produce a negative signal beginning at the start of a Character and lasting ½ bit. Its output is used to prevent the Start transitions from causing an effective Transfer.

Diode 8CR3 uses the positive Stop signal from gate 8CG Q1 to reset binary 8AF. This reset is necessary since no timing signals are available from binary 3LF to reset 8AF during the stop interval.

5-7. Assembly 6 and 4 Power Supply:

Refer to figure 9A.

The DT-603-3 is operated from two zener diode regulated dc voltages and one unregulated voltage. The first secondary voltage of transformer 4T1 (pin 5-6) is rectified by a bridge and filtered by a Pi type RC filter before being connected to a 15 volt, 10 watt zener diode 4CR1. This provides the negative 15 volt dc supply. The unregulated voltage at junction of 6R1 and 6C2 (approx. 20 volts) is used to power Assembly 2 (Register and Peak Logic).

The second secondary voltage of 4T1 (7-8) is half wave rectified and filtered by capacitor 6C3 before being dropped in resistor 6R2. The zener regulator for the resulting +15 volts dc supply 3CR3 is located on Assembly 3 and provides a regulated +15 volts. The need for regulation on the +15 volts is occasioned only by the Filter Adjust of Trigger 3IT which is sensitive to significant voltage changes between the -15 volts and the +15 volts levels.

5-8. Assembly 9 - Crystal Oscillator:

The basic timing is produced by a transistor Pierce Oscillator consisting of transistor 9Q1 and its associated biasing networks. Any one of four crystals are switched into the circuit by switch section 5S4A. (Space is provided for 2 additional crystals and load capacitors for special speeds).

Transistor 9Q2 acts as an emitter follower to provide load isolation for the oscillator. Binary 9AF is used as the first stage of the timing divider used to divide the oscillator frequency to 200 times the desired operating rate in bauds.

Chapter 6

CORRECTIVE MAINTENANCE

6-1. General:

a. Component Replacement

The use of printed circuit boards in this unit requires caution in the replacement of defective components. Printed circuit boards are easily damaged by excessive heat during soldering. Use a small iron (25 watts to 35 watts) and apply the hot iron tip to the lead of the component to be removed. DO NOT APPLY IRON TO FOIL. As soon as the solder melts remove the iron and brush excessive solder away. Straighten leads and, if necessary, reheat and pull the lead out. Do not force or twist the leads to remove them as this may result in damage to the foil.

Never attempt to save the component at the expense of damaging the printed circuit board. Cutting out of the component and subsequent removal of the remaining portion of the leads is the preferred method of component removal.

Before inserting the new component, clear all holes of solder. This may be accomplished by briefly heating the area of the hole and, when the solder is soft, tap the board. Mount the component on the p - c board, gently pushing the leads through the holes. Bend the leads close to the foil and clip them to about 1/8" in length. Apply flux to the joints and solder. Remove the iron as soon as the solder flows into the joint. Clean the joint of excess flux with alcohol and the repair is complete.

b. Repair of Printed Circuit Conductor

If the foil conductor is damaged it must be replaced with a physical wire conductor. Remove the defective portion of the conductor. Drill two holes one at each end of the break alongside the foil. Insert either buss wire or insulated wire from the side of the board opposite that of the broken conductor, and bend the ends of the wire across the foil. Apply flux and solder. Check with an ohmmeter for continuity.

6-2. Test Equipment Required:

The following test equipment is required for maintenance, and trouble shooting of the DT-603:

Oscilloscope - Tektronix Model 535A or equivalent.
Frequency Counter - Hewlett-Packard Model 523B or equivalent.
Multimeter - Simpson Model 260 or equivalent.
Telegraph Signal Generator - Digitech Model DT-101B, Model DT-103 or equivalent unit capable of generating a telegraph signal with controlled amounts of distortion.

6-3. Assembly Locations:

The DT-603-3 is made up of nine assemblies. See figure 2 for a view showing their location within the unit.

ASSEMBLY NUMBER	LOCATION	DESCRIPTION
1	Top	PC-191 Timing
2	Bottom	PC-161 Register & Peak Logic
3	Right Side	PC-189 Timing Divider Input Circuits
4	Left Side	Power Fuses and Transformer
5	Front & Rear	Front Panel & Chassis Components
6	Inside	PC-170 Power Supply
7		Case and Cover
8	Rear	PC-190 Transfer Circuits & Character Timing
9	Inside	PC-188 Crystal Oscillator

6-4. Trouble Shooting Procedures:

a. General

The DT-603-3 is made up of six functional logic sections as outlined in figure 5, Block Diagram. In this diagram the reference designation for the logic blocks supplies locating information. For example 1AF refers to Assembly 1 location A and designates a flip-flop type of circuit.

The first step in servicing a defective unit is to localize the fault to a particular section of the unit, then to a particular sub-module before locating the defective component. In most cases it will not be necessary to remove any of the module assemblies to replace a component. If it should become necessary, however, always turn the ac power off while doing so. Since the circuits other than the oscillator are constructed in the form of sub-modules containing, with few exceptions, either a complet binary or two (2) gates, a trouble shooting procedure for these logic elements will be discussed here.

b. Trouble Shooting a Binary (flip-flop) Figure 10:

There are two types of check which can be made to isolate a defective component in the flip-flop circuit. The first type of check is to determine whether the circuit is dc stable. Ground the base lead of Q1 to turn it off. The collector of Q1 should go negative and the collector of Q2 should go to ground. If Q1 does not turn off, (1) it may have an internal collector to emitter short, or (2) the collector is grounded somewhere in the external circuit. If Q2 does not turn on, going to ground, it may have a base to emitter open or a base to collector open in the transistor. Open circuits between collector of Q1 to base of Q2 are another possible cause. Next, reverse this procedure grounding the base of Q2. The dc check, therefore, will locate faulty transistors, resistors or connections within the flip-flop circuit.

If the flip-flop circuit is dc stable, grounding the bases of Q1 and Q2 alternately will cause the circuit to flip back and forth between its two stable states. The second type of check involves the ac trigger circuits each consisting of a capacitor, resistor, diode combination. There is at least one trigger circuit connected to each transistor base in a flip-flop. With a signal on each input, check the collectors of Q1 and Q2 to determine which one is at ground and doesn't turn off. The trigger circuit associated with that transistor is suspect. The most probable cause of trouble is a defective diode. This may be checked with the Volt-Ohm-meter in the circuit. Forward resistance of a good diode will be under 20 ohms on the RX1 scale, while the reverse resistance will normally be in the range 200 K to 400K on the RX 10,000 scale. Input trigger diodes are located on sub-modules in position 7, 9, 20, and 22.

c. Trouble Shooting Gates - PNP (Figure 11).

Transistor gates are rather simple to trouble shoot in that they contain only two component types, transistors and resistors. If a gate is found to be not operating check the base wave form on the Oscilloscope. For the transistor to saturate the base must be negative about -0.2 volts with respect to the emitter and to be cut-off the gate must be positive (and to about 3 volts). If either one of these conditions exits steadily then the gate collector will stay at the appropriate voltage (gnd. or negative) without changing and the inputs to the gate should be checked. A base voltage significantly more negative than -0.2 volts with respect to its emitter indicates an open circuit.

To determine whether a transistor which is saturated is defective, short the base to the emitter; this should cut the transistor off, producing a negative voltage at the collector.

If the defect keeps the gate always cut-off, check the forward resistance on the transistor base to emitter and base to collector junctions for an open circuit condition.

d. Trouble Shooting a Schmitt Trigger -(Figure 12)

Since a trigger has two stable states controlled by the input signal level, the first check outlined for the binary (Para. 6-4b) is also applicable.

6-5. Trouble Shooting:

a. General

Trouble shooting the DT-603 requires the use of the test equipment listed in paragraph 6-2.

The Telegraph Signal Generator is necessary to key the Input circuits of the DT-603-3 and thereby provide Transfer pulses for known amounts and types of distortion.

The Oscilloscope is necessary for viewing waveforms to determine the faulty circuit. Once the trouble has been isolated to a faulty circuit, use of the ohmmeter portion of a Multimeter for checking diode and transistor forward and back resistances will locate the defective component.

The Frequency Counter is necessary only for checking the oscillator speeds. There are no adjustments for the crystal oscillator.

The trouble shooting procedure is given in the form of a discussion aided by a trouble chart where it seemed useful for each major circuitry section in the unit. A single General Chart is provided to make use of the various visual indicators in directing the maintenance personnel to the proper sections of the unit.

Refer to paragraphs 6-1, and 6-3 for specific information on component replacement, and how to trouble shoot the logical circuits found on individual sub-modules. Sub-module identification and location of components may be found in the Parts List, Chapter 7 and the figures associated with each Assembly or Module.

a. To service the DT-603-3 it must first be removed from its protable case. The case is made in two parts, a base and a cover. The cover is removed by removing three screws on each side of the unit and lifting. In this condition, however, access to Assemblies 2,3 and 9 are not possible. Removal of the two bottom screws on the front panel and two screws in the rear of the L-shaped base will allow the main unit to be removed from the base. Assemblies 1,2,3,8, and 9 containing all of the "active" circuitry are now accessible from the outside of the unit. To gain access to assemblies 4,5, 7 and 9 removal of one or all of the outside assemblies is necessary.

Before starting to trouble shoot make sure ac power of 115 volts 60 cps is applied to the unit, that the power switch is ON, and the neon indicator glows. Failure of the neon to light warrants a check of the ¼A. Slo Blo fuses located on Assembly 4. They are accessible from the top of the unit.

b. Finding the Faulty Section

For purposes of trouble shooting, the DT-603-3 is made up of 6 major circuitry sections. These are:

PARAGRAPH	SECTION	LOCATION
6-5C	Power Supply	Assembly 6 and 4
6-5d	Timing	Assembly 3,1,8, and 9
6-5e	Input	Assembly 3
6-5f	Transfer	Assembly 8
6-5g	Register	Assembly 2
6-5h	Peak Logic	Assembly 2

Use the following chart of visual symptoms to isolate the source of trouble to one of the major sections. When more than one section is listed, they should be checked in the order in which they are listed.

In some cases the chart will list directly a sub-section, sub-module, or switches to be checked.

	SYMPTOM	FAULT SECTION
1.	Power Indicator doesn't light	Power Supply
2.	Mark and Space Lights are both out when S5 is on BIAS or END	a. Power Supply b. Register
3.	Meter doesn't give any indication on CAL (40)	Power Supply
4.	Sig Ind doesn't flash	a. Polarity Switch in wrong position. b. Input MA Switch in wrong position. c. Input
5.	Constant error in Meter reading	a. Small Speed Difference between telegraph signal and DT-603-3 timing. b. Timing (Decades) c. Register
6.	SiG Ind flashes but Meter doesn't read	a. Transfer b. Register
7.	Unit operates normally on Average, but will not hold Peak reading.	a. Peak Logic b. Transfer (8DG)
8.	Operates on one or more speeds but not on others	a. Timing
9.	Operates on ALL Transistions but not on a SELECTED TRANSITION.	a. Check Gate 3FG Q1 & Q2 on Assembly 3. b. Switch 5S3

The following reminders may be helpful in trouble shooting a unit.

1. To make measurements with the DT-603-3 the METER RESET switch 5S2 must be in the OFF position.

2. When, after inserting an input signal, the SIG IND doesn't flash, always check the position of the INPUT POLARITY and the INPUT MA switches.

3. When making PEAK measurements or when using the TRANSITION SELECT the METER RESET should be used to verify the readings.

4. When checking signals for END distortion, and use is made of the TRANSITION SELECT there can be no measurement for the 1st and last transistion of a character. This is due to the fact that these two can only be S/M (space to mark) transitions, while END distortion is a displacement of M/S transitions.

c. Power Supply

Check dc supply voltages with a 20K ohm/volt meter. The voltage wires are color coded: Black for ground, Yellow for -15 volts (and -20 volts on Assembly 2), and Red for +15 volts.

Use the front panel GND test point TP3 for ground reference. Check the -15 volts at the anode (stud) end of the 10 watt zener diode CR4 located at the left rear underside of Assembly 4. (-15 volts may also be checked at any sub-module pins 1 and 28 on Assembly 1). Check the +15 volts on Assembly 3 at the cathode end of zener diode 3CR3. (+15 volts may also be checked at any sub-module pins 4 and 25 on Assembly 1). These two voltages should measure between 13 and 17 volts. There are no dc fuses. A short circuit on the +15 volts will cause no damage and the voltage will return to normal after the short is removed. A short circuit on the -15 volts may blow the ac fuse after a period of time.

Damage may result to resistor 6R1 on Assembly 6 for a direct short on the -15 volts supply that remains for several hours. The -15 volts will recover from short term direct short circuits. In case of a direct short circuit on one of the dc voltages (use an ohmmeter to check), determine which Assembly has the short by removing dc voltage leads to each Assembly until the short disappears. Then locate the short circuit on that assembly.

SYMPTOM	PROBABLE CAUSE
A-C Indicator doesn't light	Fuses 4F1 or 4F2 open (Replace. If fuse persists in blowing check for short in transformer secondary circuit).
-15 Volts reads 0 volts	1. Zener diode 4CR1 shorted. Check diode with an ohmmeter. 2. External circuit is shorted. See discussion preceding this chart.
-15 volts reads low	1. Capacitor 6C1 or 6C2 defective 2. Resistor 6R1 increased in value
+15 volts reads 0 volts	Zener diode 3CR3 shorted External circuit shorted
+15 volts reads high	Zener diode 3CR3 open
+15 volts reads low	Capacitor 6C3 defective Resistor 6R2 increased in value.

d. Timing Circuits

The Timing circuits are located on Assemblies 3,1,8, and 9. The oscillator, located on Assembly 9 is made up of 9Q1 and 9Q2 and its associated components, the shaping gates 3KG, gate 3J603-S9 Q1 and the first stage of countdown binary 3LF are located on Assembly 3. The last stage of the Bit Counter 3FF is also located on Assembly 3. The first and second Decade Counters, and the 1st three stages of the Bit Counter are located on Assembly 1. The generation of the STOP interval as detected from the Bit Counter takes place in 8BG and the priming signal (Timing Reset) is generated in 8CG Q2. Switch 5S4 (Speed-Bauds) selects the proper timing components for the oscillator.

The test point on sub-module E (3ETP1) provides a view of the timing signal at 200 times bauds from the collector 3KG Q2. If no signal is visible at this point check the timing divider stages 3CF, 3BF, 3AF and 9AF for an output. No signal output of all divider stages indicates a problem in the crystal oscillator itself, check 9Q1 and 9Q2 for shorted or open junctions.

SYMPTOM	PROBABLE CAUSE
No Signal at 9Q1 or 9Q2	1. 9Q1 or 9Q2 defective 2. Speed-Bauds switch on EXT. position.
No Signal at 9AF, 3AF, 3BF or 3CF	Check each stage according to para. 6.4
No Signal at 3KG	1. Check 3KG (see para. 6-4).

Since no timing signals will pass through gate 3J603-S9 Q1 unless the unit is being keyed by a loop signal and the timing chain is operating, it is suggested that the Stop signal input to this gate (pin 9) be grounded. (This may best be done by grounding the collector on gate 8BG Q1.) Timing signals will then be allowed to pass through to trigger the timing chain starting with binary 3LF, and in turn to the stages on Assembly 1.

If the signal stops or disappears anywhere in the timing chain, then the stage at which this happens is suspect and should be checked according to paragraph 6-4b.

If the signal does not disappear, but the resulting bit timing is at too low a frequency, it is an indication that the reset functions within the first or second decades is faulty.

SYMPTOM	PROBABLE CAUSE
Fist Decade divides by 16	Gate 1KG Q1 defective or Diodes CR7 on 1CF and CR22 on 1BF are both open.
Fist Decade divides by 14	Diode CR7 open on 1CF
First Decade divides by 12	Diode CR22 open on 1BF
Second Decade divides by 16	Gate 1KG Q2 defective or Diodes CR7 on 1IF and CR22 on 1HF are open.
Second Decade divides by 14	Diode CR7 open on 1IF
Second Decade divides by 12	Diode CR22 open on 1HF

If the decades divide properly and the timing signal progresses through the Bit Counter stages 1EF, 1FF and 1LF remove the ground placed on 8BG Q1 and key the telegraph loop. Check for a signal at 8CG Q2 going positive at the start of a character (Timing Reset). For this to happen the signal at 8BG Q1 should be negative, and at 8CG Q1 it should be positive (gnd). The second input to 8CG Q2 coming from the Input circuits (3DF) should be changing. If this is not the case check the deficient stage for defective components.

Assuming, however, that the positive going signal is present at 8CG Q2 but the Bit counter stages 1EF Q2, 1FF Q2, 1LF Q2 and 3FF Q2 (on 8 level code) don't reset, then check the triggering circuit on these binaries. The trigger circuits are made up of capacitor C21, diode CR22, and resistor R23.

This Timing Reset signal is also used to reset all four stages of the 1st Decade and the 3rd stage of the 2nd Decade. Failure to reset any of these stages will result in a constant timing error at the beginning of a character and a resulting error in the Meter reading. The amount of error shown in the Meter reading will indicate the stage involved.

METER READING ERROR	SUB-MODULE	TRIGGERING COMPONENT
1%	1AF	C21, CR22, R23
2%	1BF	(on Module) 1C1, 1CR1, 1R1
4%	1CF	C8, CR7, R6
8%	1DF	C21, CR22, R23
40%	1IF	C8, CR7, R6

Note: Meter reading errors can also be caused by faulty Register stages. See paragraph 6-5g.

e. Input Circuits

The Input circuits are located on Assembly 3 at the right side of the unit. They are made up of the Isolator 3GI, the threshold amplifiers on 3H603-S4, the Schmitt Trigger 3IT, Binary 3DF and the adjustments on sub-module 3E.

The operation of the Input circuits are affected by the level of current in the telegraph loop, the adjustments of potentiometers 3ER4, 3ER5 and 3ER6, and the setting of switches 5S1 (INPUT MA), 5S7 (POLARITY), and 5S8 (FILTER).

NOTE: When the Hi Z (high impedance) input is used, transistor Q2 of 3J603-S9 becomes the input amplifier for this mode of operation. A negative 5 volt signal is required for Mark and a ground signal is required for Space on this input.

To check the Isolator 3GI set the input telegraph loop to steady mark. Oscillations at a frequency of one to two megacycles at an amplitude of 8 to 10 volts peak to peak should be observed at the collectors of Q1 and Q2. (The input side of the Isolator is of course isolated from the DT-603 circuit ground. To view the collector signals, therefore, a ground must be provided at the emitters of these transistors.) If no oscillations occur, transistors Q1 or Q2 may be defective or transformer T1 has a shorted base to collector winding. If the oscillations are very sinusoidal and high in amplitude, this is an indication that the transformer secondary is not being loaded. Diodes CR20 or CR22 may be open.

The voltage at R28 and C27 (SIG, TP1) should be positive, the amount depending on the setting of the 20B or 60B Bias Adjust (3ER5 and 3ER6). Keying the input loop should produce a replica of the loop signal at this point. See Chapter 4 for alignment of the Bias and Filter adjustments for the Input circuits.

The progress of the signal should be checked through Q1 and Q2 of 3H603-S4 and finally at the trigger 3IT and binary 3DF. The signals at Q1 and Q2 of 3H603-S4 will be sharp when switch 5S8 FILTER is OUT and will be shaped when it is IN. There will be no noticeable change in the output of trigger 3IT when the Filter is inserted providing FIL adjust 3ER4 is properly adjusted. If this control is badly mis-adjusted, trigger 3IT will not operate from the signal out of 3H603-S4 Q2.

f. Transfer Circuits

The transfer circuits are located on Assembly 8 at the rear of the unit. They are made up entirely of 8AF, 8DG and 8EG.

Apply a 10% switched bias signal to the DT-603 and observe the results when trying to measure BIAS. The following Symptoms assume that the SIG IND light flashes.

SYMPTOM	PROBABLE CAUSE
Meter doesn't read and MARKING and SPACING lights do not blink alternately.	No Transfers are being generated in 8AF on S/M transitions. Check transistors and diodes.
Reads Marking Bias only. No reading on Early Peak	Gate 8DG Q1 or 8EG Q1 defective.
Reads Spacing Bias only. No reading on Late Peak.	Gate 8DG Q2 or 8EG Q2 defective.

g. Register Circuits

The Register circuits are located on Assembly 2 at the bottom of the unit. They are made up of the eight binaries 2AF, 2BF, 2DF, 2EF, 2LF, 2KF, 2IF, and 2HF, and the precision resistor network formed by 2R1 through 2R7. Refer to figure 18 for a schematic diagram of a Register stage.

The type of trouble caused by a fault in the Register circuits will generally fall into the catagory of a constant numberical error in the meter reading. The error may add or subtract from the correct reading depending on whether the faulty Register stage stays in the ON or the OFF condition. The amount of error is a clue to which stage may be faulty.

NOTE: A constant numberical error may also result from trouble in the Timing Circuits (See paragraph 6-5d.).

ERROR	SUB-MODULE	ERROR	SUB-MODULE
1%	2AF	10%	2LF
2%	2BF or 2EF	20%	2KF
4%	2DF	40%	2IF

The MARKING and SPACING lights are controlled by 2HF.

The stages operate independently of each other and depend on steering signals from the corresponding counter stage on Assembly 1 and the Early and Late Transfer pulses from gates 8EG Q1 and Q2.

It is suggested that a check of all diodes automatically be made with an ohmmeter in any suspected stage.

Inability to obtain a zero reading on the meter when using the METER RESET (No telegraph signal applied) suggests a defective diode CR27 in one of the Register stages.

A check of the precision resistor network may be made by first resetting the meter to zero and grounding the Q1 collector of each stage of the Register in sequence to determine whether the reading increases by the proper amount.

h. Peak Logic Circuits

The Peak Logic circuits are located on Assembly 2 at the bottom of the unit. They are made up entirely of 2C603-S1, 2F603-S1, 2JG, and 2GF.

Use the Telegraph Signal Generator to apply a switched bias signal of known distortion, and set the DT-603 to read Total Peak.

If the meter does not give a steady indication of the amount of distortion but kicks downwards occasionally, check for operation on Early Peak and on Late Peak. The condition will repeat on one of these conditions only. If it is Early Peak use an ohmmeter to check the diodes on 2C603-S1, if it is Late Peak check the diodes on 2F603-S1.

If the Peak readings will not hold when the distortion is reduced, check for outputs on 2JG Q1 and Q2 and binary 2GF.

Remember that binary 2GF uses negative triggering and if replacement of CR9 or CR20 becomes necessary, the new unit must be installed with the cathode at the top.

Chapter 7

PARTS LIST

7-1. General:

The DT-603-3 is constructed of nine main assemblies. These are:

ASSEMBLY NUMBER	LOCATION	DESCRIPTION	PART NO.
1	Top	PC-191 Timing	6033-A1
2	Bottom	PC-161 Register & Peak Logic	6033-A2
3	Right Side	PC-189 Timing Divider-Input Circuits	6033-A3
4	Left Side	Power Fuses and Transformer	6033-A4
5	Front & Rear	Front Panel & Chassis Components	6033-A5
6	Inside	PC-170 Power Supply	6033-A6
7		Case and Cover	6033-A7
8	Rear	PC-190 Transfer Circuits & Character Timing	6033-A8
9	Inside	PC-188 Crystal Oscillator	6033-A9
10	Rear	Synchronizing Adapter	SA-3

Assemblies 1,2,3,8, and 9 make use of submodular construction using standard logic circuits. For these assemblies the parts list catalogs the components directly on the main assembly and for the submodules only their type. A schematic diagram, component layout, and component description for each submodule type is given in figures 10 through 17. Paragraph 7-2 describes the submodule designations and component part numbers.

Assemblies 4,5 and 6, do not use any submodules. For these assemblies, the parts list describes all replaceable components.

In some instances, resistors listed as ¼ watt will be found to be ½ watt types in the unit. In some units germanium diodes 1N270 are replaced by germanium diodes 1N636. Transistors SC150 and 2N404 may be used interchangeably. These substitutions will in no way affect the performance of the DT-603-3.

7-2. Submodule Designations:

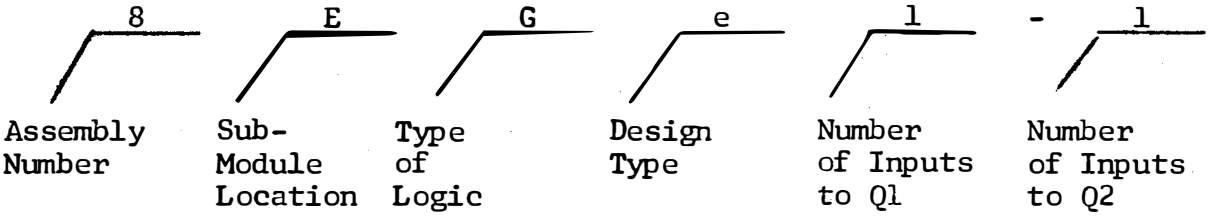
The submodule reference designators are designed to provide both locating and circuit identification information.

Example #1, 1AFa1-2

1	A	F	a	1	-	2
Assembly Number	Sub-Module Location	Type of Logic	Design Type	Number of Inputs to Q1		Number of Inputs to Q2

Thus 1AFa1-2 refers to a submodule located in position A of Assembly 1. This submodule is a binary (flip-flop) of the "a" circuit design and has a "set one" input as well as the standard count inputs. Figure 10 provides all information on this submodule type; schematic diagram component layout and Bill of Material.

Example #2, 8EGe1-1

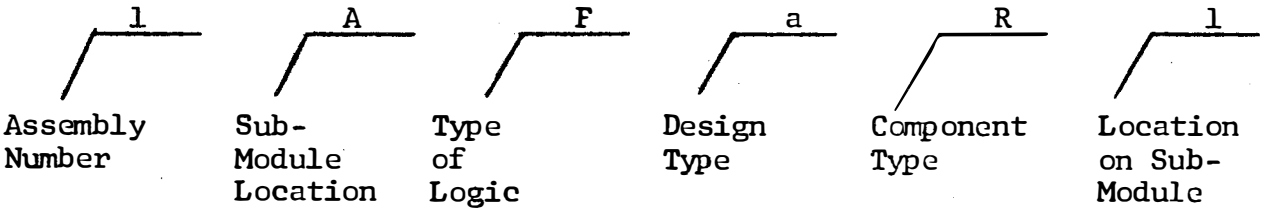


Thus 8EGe1-1 refers to a submodule located in position F of Assembly 3. This submodule is a double gate of the "e" circuit design. One input resistors are provided for the gate whose output is submodule pin 12. One input resistor is provided for the gate whose output is submodule pin 17. Figure 11 provides all information on this submodule type; schematic diagram, component layout, and bill of material.

Part Numbers For Submodule Components

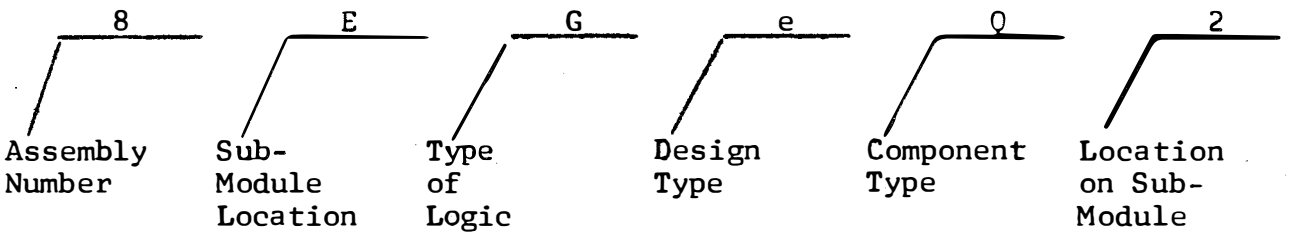
The component part numbers are designed to provide locating as well as circuit parameters.

Example #1, 1AFaR1



Thus 1AFaR1 refers to a resistor located in position number one of submodule A in assembly number 1. Refer to Binary (flip-flop) submodule reference drawing figure 10. It shows that the resistor is used as the collector resistor of transistor Q1 and is a ¼ watt composition type with a tolerance of ± 5%. From the chart in figure 10, the "a" design value of R1 is 3900 ohms.

Example #2, 8EGeQ2



Thus 8EGeQ2 refer to a transistor located in mounting clip number two of submodule E in module number 8. Referring to the Double Gate submodule reference drawing, figure 11, show that the transistor is used in the second gate and for the "e" design is an SC150.

For Submodules Type F, with inputs other than shown on reference drawing figure 10, refer to Fa column for number of components used and appropriate logic column for the component values.

EXAMPLE, Fg 1-2, refer to Fa1-2 column for number of components and Fg2-2 for the component values.

7-3. List of Parts:

A. Assembly 1 (Timing) 6033-A1

Component Designator	Description	Part Number
1C1	Capacitor Mica, dipped 82mmfd, 500V, 5%	6033-C1
1CR1	Diode, germanium, 1N270	6033-CR1
1R1	Resistor, fixed composition, 3900ohms, ½W, 5%	6033-R1

Sub-Module Position	Sub-Module Type	Part Number	Notes
1A	Fg1-2	1AFg1-2	R1 & R28 = 1800 ohms
1B	Fg1-2	1BFg1-2	R1 & R28 = 1800 ohms Q1 & Q2 are 2N1300
1C	Fg2-2	1CFg2-2	R1 & R28 = 1800 ohms Q1 & Q2 are 2N1300
1D	Fg1-2	1DFg1-2	
1E	Fa1-2	1EFa1-2	
1F	Fa1-2	1FFa1-2	
1G	Fa1-1	1GFa1-1	
1H	Fa1-2	1HFa1-2	
1I	Fa2-2	1IFa2-2	
1J	Fa1-1	1JFa1-1	
1K	Ga3-3	1KGa3-3	Capacitor C8, 22mmfd added
1L	Fa1-2	1LFa1-2	

B. Assembly 2 (Register & Peak Logic) 6033-A2

Component Designator	Description	Part No.
2R1	Resistor, fixed deposited Carbon 68.1K ohms, ½W, 1%	6033-R2
2R2	Resistor, fixed deposited Carbon 34K ohms, ½W, 1%	6033-R3
2R3	Resistor, fixed deposited Carbon 13.7K ohms, ½W, 1%	6033-R4
2R4	Resistor, fixed deposited Carbon 6.81K ohms, ½W, 1%	6033-R5
2R5	Resistor, fixed deposited Carbon 137K ohms, ½W, 1%	6033-R6
2R6	Same as 2R1 68.1K	
2R7	Resistor, fixed deposited Carbon 3.4K ohms, ½W, 1%	6033-R7
2R8	Resistor fixed composition 470 ohms ¼W, 1%	6033-R8
2R9	Same as 1R1 - 30K	

Submodule Position	Submodule Type	Part Number	Notes
2A	Fa2-2	2AFa2-2*	CR2 (1N456A) anode to collector CR27 (1N270) cathode to collector
2B	Fa2-2	2BFa2-2*	
2C	603-S1	2C603-S1	See Figure 14
2D	Fa2-2	2DFa2-2*	
2E	Fa2-2	2EFa2-2*	
2F	603-S1	2F603-S1	See Figure 14
2G	Fa1-1	2GFa1-1	Diodes CR9, CR20 installed reversed.
2H	Fe2-2	2HFe2-2	R1 & R28 = 330 ohms
2I	Fa2-2	2IFa2-2*	
2J	Ga2-2	2JGa2-2	R4, R25 = 120K ohms R11, R18 = 100 ohms
2K	Fa2-2	2KFa2-2*	
2L	Fa2-2	2LFa2-2*	

* These binaries all have diode CR2 (1N456A) tied anode to the collector of Q1 and diode CR27 (1N270) tied cathode to the collector of Q2. R6, R11, R18 - change to 10K ±5%

C. Assembly 3 Timing Dividers - Input Circuits) 6033-A3

COMPONENT DESIGNATOR		PART NO.
3CR1	Same as 1CR1 (1N270)	6033-CR1
3CR2	Same as 1CR1 (1N270)	6033-CR1
3CR3	Same as 1CR1 (1N270)	6033-CR1
3CR4	Same as 1CR1 (1N270)	6033-CR1
3CR5	Diode, zener, 1N965A, 15 volt, 10%	6033-CR2
3R1	Resistor,fixed,composition 160K ¼W, ±5%	6033-R1
3R2	Resistor,fixed,composition 30K ohms,¼W, 5%	6033-R1
3R3	Resistor,fixed,composition, 110 ohms,½W, 5%	6033-R9
3R4	Resistor,fixed,composition, 1K ohms, ½W, 5%	6033-R10

On Sub-Module 3E the following parts are listed:

3ER1	Resistor, fixed composition 6200 ohms ¼W, 5%	6033-R11
3ER2	Resistor, fixed composition 1800 ohms ¼W, 5%	6033-R12
3ER3	Same as 3ER2	6033-R12
3ER4	Resistor, variable, wire wound 2000 ohms Bourns 3607P-1-202.	6033-R13
3ER5	Resistor, variable, wire wound 200 ohms Bourns 3607P-1-201.	6033-R14
3ER6	Same as 3ER5	6033-R14
3ER7	Same as 3ER5	6033-R14
3TP1	Testpoint Sealectro SKT-102PC	6033-3TP1

SUB-MODULE POSITION	SUB-MODULE TYPE	PART NUMBER	NOTES
3A	Fal-1	3AFal-1	
3B	Fal-2	3BFal-2	C21 = 150 mmf
3C	Fal-1	3CFal-1	
3D	Fel-1	3DFel-1	C10,C19 = .005 MFD R1 = 330 ohms
3F	Fel-2	3FFel-2	
3G	I	3GI	Isolator (Figure 13).
3H	603-S4	3H603-S4	See Figure 17.
3I	Tb	3ITb	Trigger(Fig.12) C26=150MMF
3J	603-S9	3J603-S9	Gate (Figure 16).
3K	Ge4-2	3KGe4-2	Q1 & Q2 are 2N1300 Gate (Figure 16)
3L	Fdl-2	3LFdl-2	

D. Assembly 4 (Side Panel) 6033-A4

COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
4CR1	Diode, Zener, 15v, 10% 10W., 1N2979A	6033-CR3
4F1	Fuse, 3AG, 3/8 Amp Slo-Blo	6033-F1
4F2	Same as 4F1	
4T1	Transformer, Power	B1081
4XF1	Fuseholder, Littlefuse 342.004	6033-XF1
4XF2	Same as 4XF1	

E. Assembly 5 (Front & Rear Panel) 6033-A5

COMPONENT DESIGNATOR	DESCRIPTION	PART NUMBER
5DS1	Lamp, GE #344	6033-DS1
5DS2	Same as 5DS1	
5DS3	Same as 5DS1	
5DS4	Lamp, Neon, Eldema #189-5093	6033-DS2
5J1	Jack, Telephone Switchcraft L12A	6033-J1
5J2	Jack - 2 Pin Cinch-Jones CJS302-AB	6033-J2
5J3	Connector Cannon DA-15S	6033-J3
5M1	Meter - Ideal 0-50ua EPI-C	6033-M1
5R1	Resistor, fixed, deposited carbon 24 ohms, ½W,1%	6033-R15
5R2	Resistor fixed composition, 3900 ohms ¼W, 5%	6033-R16
5R3	Same as 5R1	
5R4	Same as 5R1	
5R5	Resistor, fixed composition 220K ohms ¼W, 5%	6033-R17
5R6	Resistor, fixed wirewound, 700 ohms, 5W, 5%	6033-R18
5S1	Switch, Lever, 2 Pole, 3 Pos. N.S. CRL #1454	6033-S1
5S2	Switch, Lever, 2 Pole, 3 Pos. N.S. Spring Return CRL #1467	6033-S2
5S3	Switch, Rotary, 3 Pole, 11 Pos. N.S. CRL PA#1009	6033-S3
5S4	Switch, Rotary, 6 Pole, 7 Pos.N.S. Digitech A1193	6033-S4
5S5	Switch, Rotary, 8 Pole, 5 Pos.N.S. CRL PA #1027	6033-S5
5S6	Switch, Slide, DPDT H.H. Smith #518	6033-S6
5S7	Same as 5S6	
5S8	Same as 5S6	
5S9	Switch, Rotary 6 Pole, 5 Pos. CRL #PS-115	6033-S9
5TP1	Test Point, Selectro #SKT-10 - Green	6033-TP2
5TP2	Test Point Sealectro #SKT-10 - Yellow	
5TP3	Test Point, Selectro #SKT-10 - Black	6033-TP3
5TP4	Test Point, Sealectro #SKT-10 - Orange	6033-TP4
5XDS1	Lampholder, Dialco #101-3830-937	6033-XDS1
5XDS2	Same as 5XDS1	
5XDS3	Same as 5XDS1	
5F1	Fuse 1/10 Amp 8AG or AGX	6033-F2
5XF1	Fuseholder Littlefuse 342.001	6033-XF2

F. Assembly 6 (Power Supply) 6033-A6

COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
6C1	Capacitor, Electrolytic 500MFD, 50 V, Ind.Cond. #1B1307-RMV	6033-C2
6C2	Same as 6C1	
6C3	Capacitor, Electrolytic, 200 MFD, 50V, Ind.Cond. #1B1393-RMV	6033-C3
6CR1	Diode Silicon 1N3253	6033-CR4
6CR2	Same as 6CR1	
6CR3	Same as 6CR1	
6CR4	Same as 6CR1	
6CR5	Same as 1CR1	
6R1	Resistor, fixed, wire wound 15 ohms 3W, 10%	6033-R19
6R2	Resistor, fixed, composition 470 ohms ½W, 5%	6033-R20

G. Assembly 7 (Case and Cover) 6033-A7

Description	Part Number
Case Bottom Pan	C1158
Case Cover Assembly	C1159

H. Assembly 8 (Transfer Circuits & Character Timing) 6033-A8

COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
8C1	Capacitor Mica, 470 mmfd. 500 V 5%	6033-C4
8R1	Resistor, fixed, composition 10K ohm, ¼W,5%	6033-R21
8R2	Same as 1R1 (30K)	6033-R1
8CR1	Diode 1N270	6033-CR1
8CR2	Diode 1N270	6033-CR1
8CR3	Diode 1N270	6033-CR1
8CR4	Diode 1N270	6033-CR1
8CR5	Diode 1N270	6033-CR1
8C2	Capacitor, DISC .01 MFD 50V	6033-C5
8CR6	Diode, 1N270	6033-CR1

SUB-MODULE POSITION	SUB-MODULE TYPE	PART NUMBER	NOTES
8A	Fe2-1	8AFe2-1	Diode across R18
8A	Fe2-1	8AFe2-1	C8, C10 are 220 mmf.
8B	Ga4-2	8BG4-2	Gate (Figure 16).
8C	Ga1-2	8CGa1-2	C19=82mmf.R20=43K R25=120K
8D	Ga6-6	8DGa6-6	C10, C19 are 22 mmf.,Q1 & Q2 are 2N1300
8E	Ge1-1	8EGe1-1	C10, C19 are 220 mmf.

I. Assembly 9 - Crystal Oscillator

NOTE: In the DT-603-3,this part uses PC-188 and has part #6033-A9. In the DT-613-3, this part uses PC-245 and has part #6133-A9.

SUB-MODULE POSITION	SUB-MODULE TYPE	PART NUMBER	NOTES
9A	Fa1-1	9AF1-1	C10, C19= 150 MMF Diode CR9, CR20 installed.

COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
C1	Capacitor, Disc Ceramic .47 mfd, 3V Sprague HY-130	6033-C6

COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
C2	Capacitor, Dipped Mica, 2000 mmf, ± 5%	6033-C7
C3	Not Used	
C4	Capacitor, Dipped Mica, 560 mmf, ± 5%	6033-C8
C5	Capacitor, Dipped Mica, 680 mmf, ± 5%	6033-C9
C6	Capacitor, Dipped Mica, 470 mmf, ± 5%	6033-C4
C7	Same as C5	
C8 and C9	Factory Select (Used on non-standard units only)	
C10 thru C15	Capacitor, Dipped Mica, 30 mmf, ± 5%	6033-C10
R1	Resistor, Fixed Composition, 22 Ohms, ½W, ± 5%.	6033-R22
R2	Resistor, Fixed Composition, 1K, ½W, ± 5%.	6033-R10
R3	Resistor, Fixed Composition, 4300 ohms, ½W, ± 5%.	6033-R23
R4	Resistor, Fixed Composition, 43K ohms, ½W, ± 5%.	6033-R24
R5	Resistor, Fixed Composition, 7500 ohms, ½W, ± 5%.	6033-R25
R6	Same as R2	
Q1	Transistor Germanium PNP Type 2N1224	6033-Q1
Q2	Transistor Germanium PNP Type 2N404	6033-Q2
Y1	Crystal type CR-37/U 145.622 KC	6033-Y1
Y2	Crystal type CR-37/U 120.000 KC	6033-Y2
Y3	Crystal type CR-37/U 195.652 KC	6033-Y3
Y4	Crystal type CR-37/U 118.720 KC	6033-Y4
XY1 thru XY6	Crystal Holder, Augat #800-AG9	6033-XY1

Chapter 8

SYNCHRONIZING ADAPTER MODEL SA-3 Pat.Pend.

(OPTION)

8-1. Purpose and Use:

The Synchronizing Adapter, Model SA-3 is designed for use with Telegraph Signal Analyzer, Model DT-603-3 and DT-613-3 to add to them the capability for analyzing synchronous telegraph signals by phase locking the DT-603-3 or DT-613-3 timing signal to the incoming telegraph signal.

Synchronous signals are defined as a continuous binary stream of data in which only information bits are transmitted. The source of synchronizing information in the signal is the fact that the interval between transitions is, on a perfect signal, an integral number of bits, and the frequency of transmission is accurate and stable (usually to 1 part in 10^6).

There are two ways in which these signals may be analyzed for distortion content. Method #1 assumes a very low amount of fortuitous distortion in the signal, and treats it the same as a Start-Stop type of signal. Method #2 (the only acceptable method when fortuitous distortion is high, such as on radio circuits) involves the use of a synchronizer to lock the Analyzer timing to that of the incoming signal.

METHOD #1

Analysis of synchronous signals on a Start-Stop basis may be made under most conditions where transmission is not over a radio path. The Analyzer operates by using the first mark to space (M/S) transition to initiate the timing of a character. Measurements are then made during the next 6½ bits (on 5 level code operation) after which the Analyzer timing stops. A new measurement cycle begins on the next M/S transition in the signal. Thus, accurate measurements are made for all but one transition in each equivalent character time interval.

METHOD #2

Analysis of synchronous signals on a continuing basis requires that the internal timing of the Analyzer be "locked" in phase with the incoming signal. The correction to the internal timing must be sufficiently damped, however, so that fortuitous or random distortion in the input signal will not cause the relative phasing between it and the Analyzer timing to change.

The Telegraph Signal Analyzer Model DT-603-3 may be operated to make measurements by Method #1 and, with the addition of the Synchronizing Adapter, Model SA-3, by Method #2. To use Method #2 it is necessary that the uncorrected bit rate of the Analyzer timing be within 0.1% of the bit rate of the incoming signal. For this reason crystal oscillators are used as the basic timing source in the DT-603-3 and DT-613-3.

The Synchronizing Adapter, Model SA-3 may be added to DT-603-3 or DT-613-3 at initial purchase, or, if the need for it does not develop until later, it may be added at that time. Addition of the SA-3 increases the depth of the DT-603-3 to 12 1/8". On the DT-613-3 the physical size is not affected.

8-2. Theory Of Operation:

Refer to the logic diagram Figure 20, and the waveforms diagram Figure 20B. The synchronizer is made up of two monostable multivibrators 10D603-S7 and 10H603-S8 and four binaries 10CF, 10EF, 10FF and 10GF.

The 200 X bit rate timing signal from the Analyzer is routed through Monostable 10D603-S7 for both types of operation, start-stop and synchronous, when the SA-3 is supplied. This signal provides the basic timing for the Analyzer.

In order to lock the internal timing signal of the Analyzer to the phase and frequency of the incoming synchronous signal, timing pulses are either added or subtracted from the 200 X bit rate timing signal. The synchronizer is designed to track only the S/M transition of the incoming signal. Whenever the S/M transitron is not in phase with the bit rate timing a correction is made in the 200 X bit rate timing signal. If the transitron is early a pulse is subtracted by 10GF to delay the internal timing; and if the transitron is late (relative to the internal bit rate signal) a pulse is added by 10H603-S8. In this way, the internal timing of the analyzer is adjusted to that of the incoming signal. To be effective, however, the baud rate of the incoming signal must be within approximately 0.1% of that of the internal baud rate of the Analyzer.

Adding A Pulse (line 3,4, and 6 through 10 Of Figure 20B)

A replica of the input signal which has a positive polarity (gnd) on Space and a negative polarity on Mark is connected to a voltage divider made up of 10R1 and 10R2. Capacitor 10C1 provides equalization, so as to maintain a good rise time on the signal. The output of the voltage divider is used to trigger binaries 10EF and 10FF. Which of these two binaries will be triggered by the M/S transition of the incoming signal depends on the condition of the Early and Late bit rate timing signals at the time of the M/S trigger. The Late timing signal, positive during the first half of a bit, is connected to the trigger resistors R11 and R18 of Binary 10EF. When the internal timing is late, the incoming M/S transition causes 10EF to change state.

Every second change of 10EF triggers Binary 10CF to produce a positive output at pin 12. This positive output conditions trigger resistor 10R3 to enable the Oscillator timing (200 X bit rate) signal ($\overline{OSC}$) to trigger Monostable 10H603-S8. The trigger occurs 180° out of phase with the OSC signal which triggers monostable 10D603-S7. The Q2 output (pin 17) of the monostable triggers the second input to monostable 10D603-S7, thereby adding a pulse to the 200 X timing signal midway between the normal pulse outputs. The Q1 Output (pin 12) of monostable 10D603-S7 resets binary 10CF to prepare it for the next ADD command from binary 10EF.

This process of adding pulses is continued until the internal timing is no longer occurring late with respect to the M/S transition.

Subtracting A Pulse (lines 5, 11 through 15 of Figure 20B)

The Subtract circuitry consists of Binaries 10FF and 10GF and gate 3J603-S9 Q1.

When the internal timing is Early with respect to the M/S transition of the data signal, Binary 10FF is triggered. Every second change in state of 10FF produces a trigger for binary 10GF, causing 10GFQ2 to go negative. This negative signal is connected to one input of stop gate 3J603-S9Q1 and prevents timing signals to pass through the gate. This prevention lasts for one count only since the Q1 output of 10D603-S7 resets binary 10GF to eliminate the negative signal at Q2. This reset occurs as shown in Figure 20b line 14, and results in the deletion of one and only one pulse from the 200 X bit rate timing signal for each positive excursion of binary 10GF.

The maximum correction rate is 1/400 bit per bit and occurs only for a dot cycle pattern. The average correction rate on an information containing signal will be 1/800 bit per bit.

When the analyzer timing has been locked onto the input signal, both add and subtract pulse will be generated in the synchronizer to maintain the synchronization.

8-3. Installation:

When the SA-3 is not factory installed a jumper is provided on Assy. 3 (see Figure 8A). To operate the SA-3 this jumper must be removed.

The SA-3 is attached to the rear of the portable case on the DT-603-3 by means of three screws. The SA-3 cover must be removed to provide access to the mounting holes.

Connection of the SA-3 to the DT-603-3 is made by plugging connector 10P1 of the SA-3 to connector 5J3 on the rear panel.

Installation of Assy. 10 (SA-3) of the DT-613-3 is made by mounting the module to the chassis by means of four each #4 screws and connecting plug 10P1 to connector 5J3 in the wiring harness. Remove the jumper from Assy. 3 as indicated in Figure 8A.

8-4. Maintenance:

The following table will be useful in locating troubles within the SA-3. Before consulting the table check that the OSC and $\overline{\text{OSC}}$ timing signals are present at the white and purple wires on Assy. 10.

SYMPTOM	PROBABLE CAUSE
Analyzer doesn't operate on Start-Stop as well as Sync.	1. Timing signals are not being repeated by monostable 10D603-S7. Check for defect. 2. Binary 10GF is defective resulting in a constant negative output from Q2 which prevents timing signals from passing through gate 3J603-S9 Q1. Binary 10CF is defective resulting in a sonstant ground at Q1. This causes pulses to be added continuously to the Osc. 200 X signal and make the Analyzer operate at double speed.
Synchronizer will not Add, but will Subtract allright.	1. Check binaries 10EF and 10CF. 2. Check monostable 10H603-S8. 3. Check diode CR9 on 10D603-S7.
Synchronizer will not Subtract, but will Add allright.	1. Check binaries 10FF and 10GF.

In general, if the circuitry seems to produce signals, but the unit will not synchronize, a check should be made of the wiring through connector 10P1 to the proper assemblies within the Analyzer.

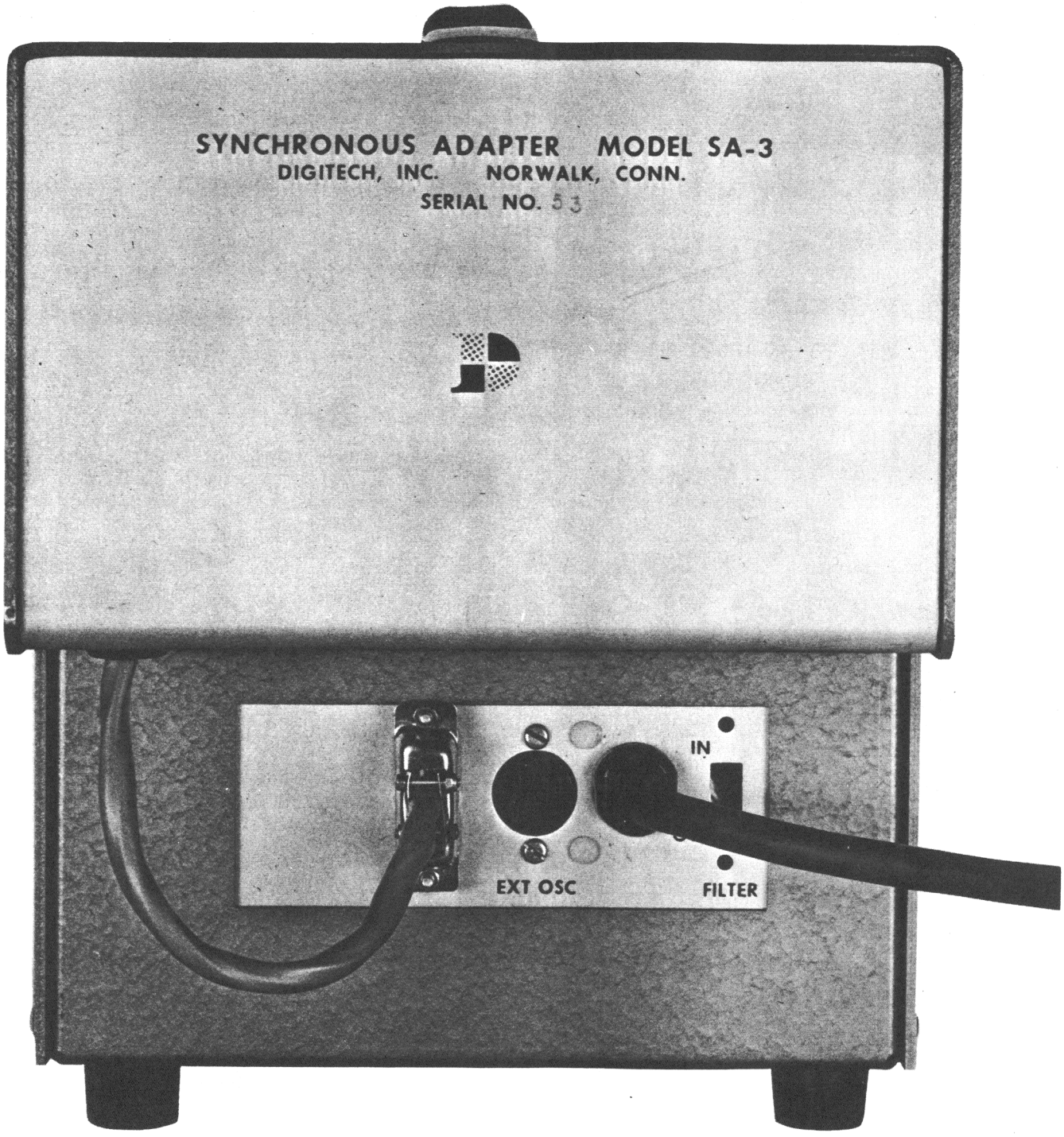
Note that synchronization will be impossible if the input signal speed differs from the Analyzer speed by more than 0.1%. The synchronizer will always add or always subtract without ever locking in.

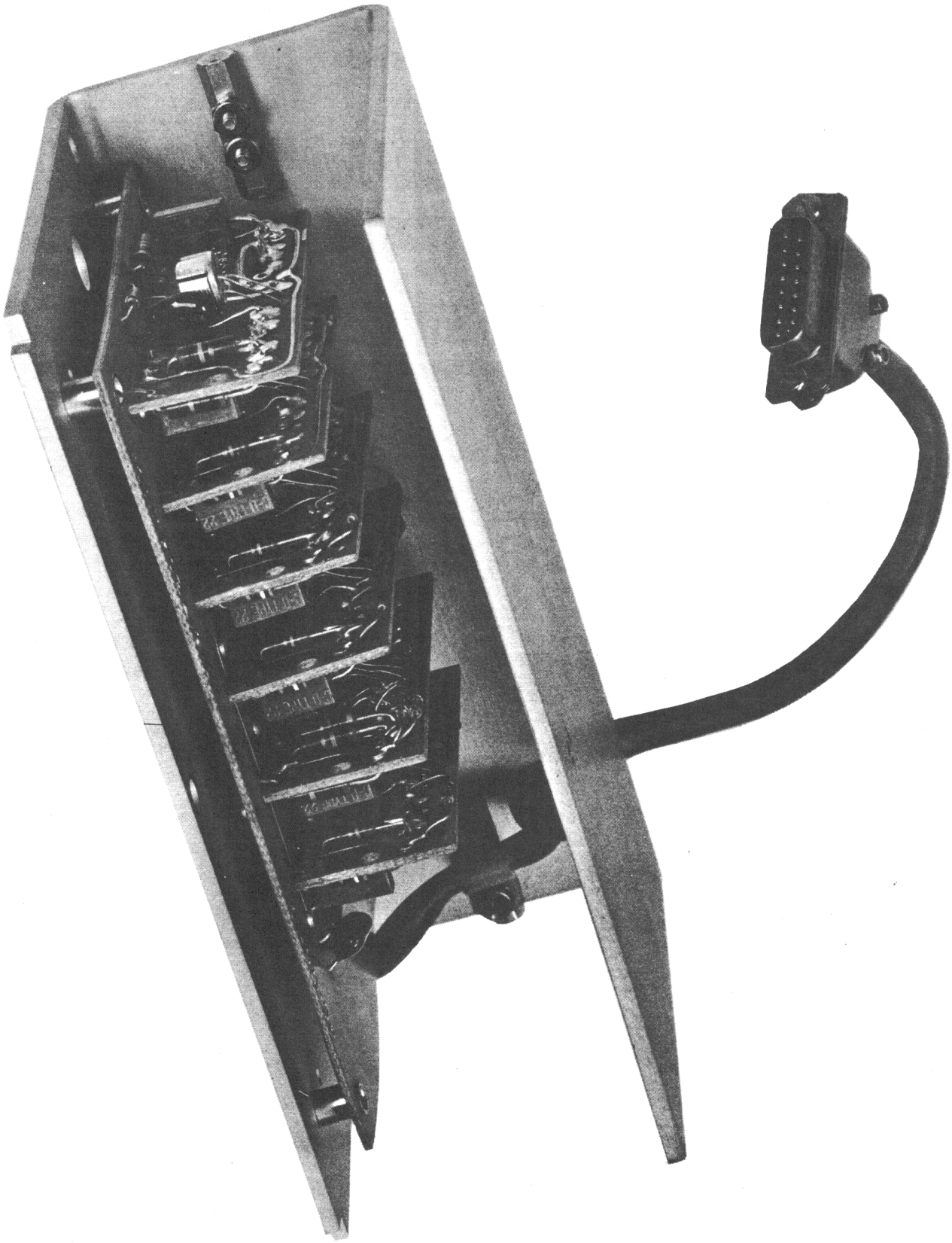
8-5. Parts List:

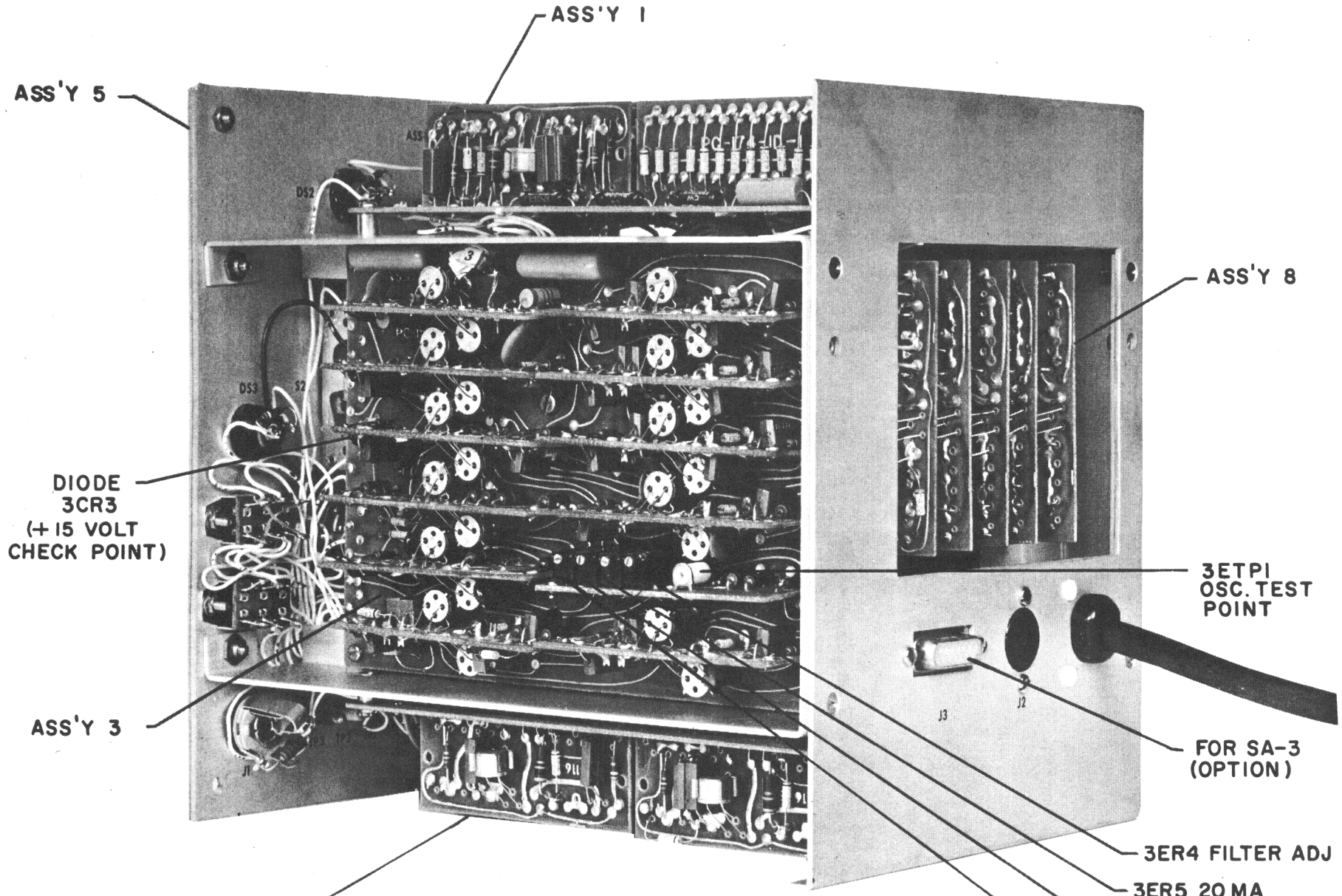
COMPONENT DESIGNATION	DESCRIPTION	PART NUMBER
10R1	Same as 5R2	6033-R16
10CR1	Same as 1CR1	6033-CR1
10R1	Same as 5R2	6033-R16
10R2	Same as 5R2	6033-R16
10R3	Same as 1R1	6033-R1
10P1	Connector 10P1 Cannon DA-15P Shell is Cannon DA J/S (19678-1)	6033-P1

SUB-MODULE POSITION	SUB-MODULE TYPE	PART NUMBER	
10A	Not Used		
10B	Not Used		
10C	Fal-1	10CFal-1	Add Speed up diode at CR9 and CR20.
10D	603-S7	10D603-S7	
10E	Fal-1	10EFal-1	R29, R30 added
10F	Fal-1	10FFal-1	R29, R30 added
10G	Fal-1	10GFal-1	
10H	603-S8	10H603-S8	


TELEGRAPH SIGNAL ANALYZER
MODEL DT-603-3
DIGITECH, INC. NORWALK, CONN.
PAT. PEND.
MARKING
SPACING
PERCENT DISTORTION
10 20 30 40 50
20N
INPUT MA
60
30F
AVERAGE
PEAK
TOTAL
END
EARLY
BIAS
LATE
CAL. (40)
OFF
ON
METER RESET
SIG IND
61.12
74.2
75
50
150
45.5
EXT
SPEED-BAUDS
4
5
3
6
2
7
1
8
9
ALL
TRANSITION SELECT
+
–
INPUT POLARITY
IN
OUT
FILTER
6
7
8
5
SYNC
ON
POWER
CODE LEVELS
SIG.
SYNC.
GND
HI Z INPUT
INPUT
SERIAL NO.

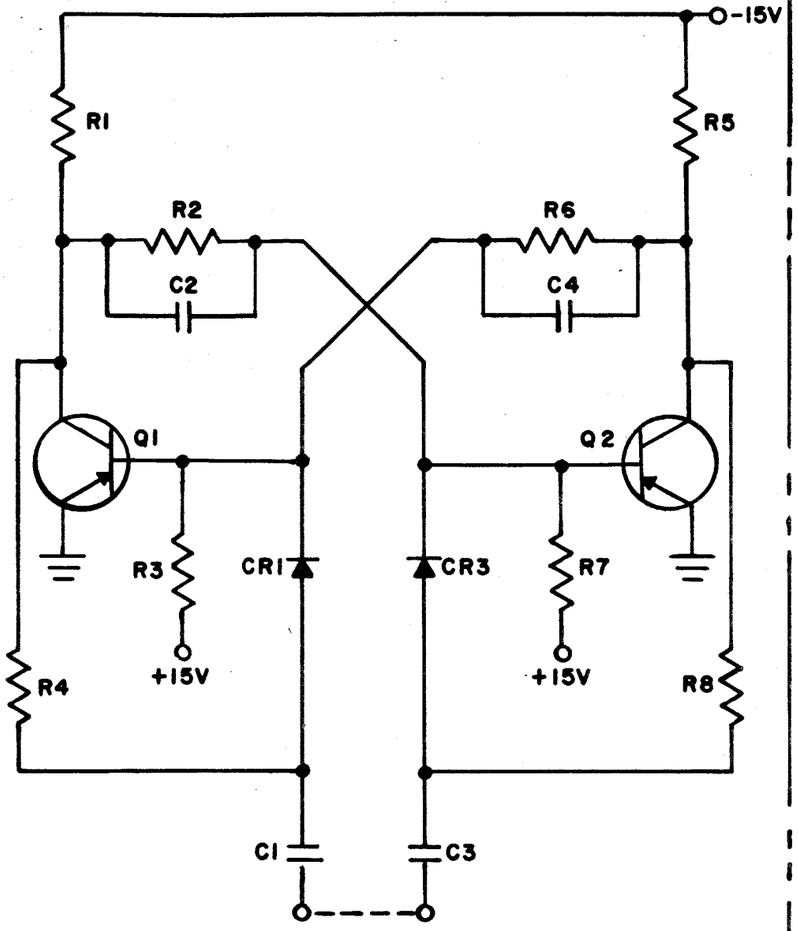

SYNCHRONOUS ADAPTER MODEL SA-3
DIGITECH, INC. NORWALK, CONN.
SERIAL NO. 53
IN
EXT OSC
FILTER





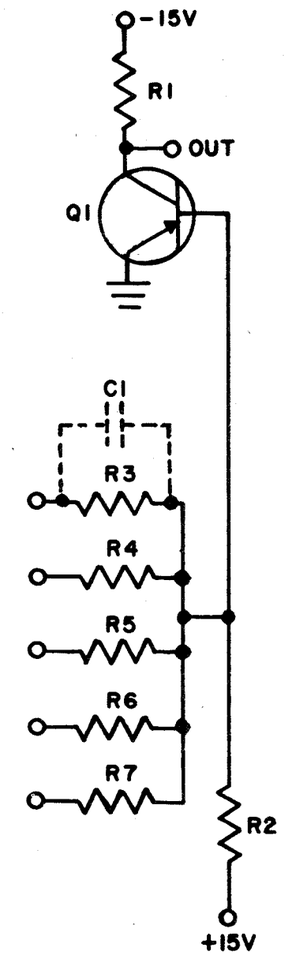
ASSEMBLY LOCATIONS

FIGURE 2



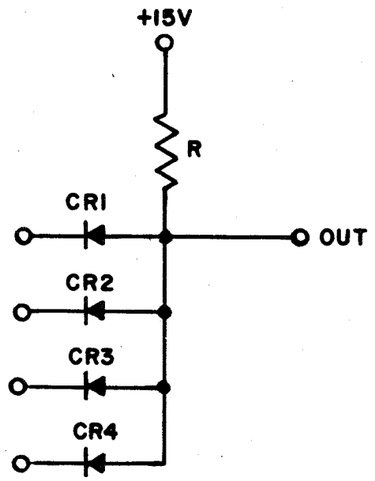
BINARY (FLIP-FLOP)

FIG. 3A



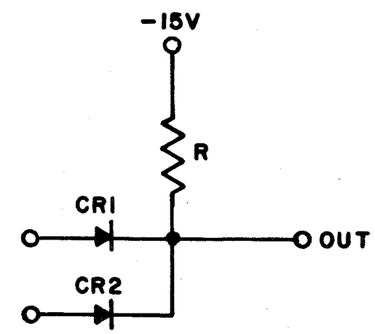
TRANSISTOR
"NOR" GATE

FIG. 3B



DIODE "AND" GATE

FIG. 3C

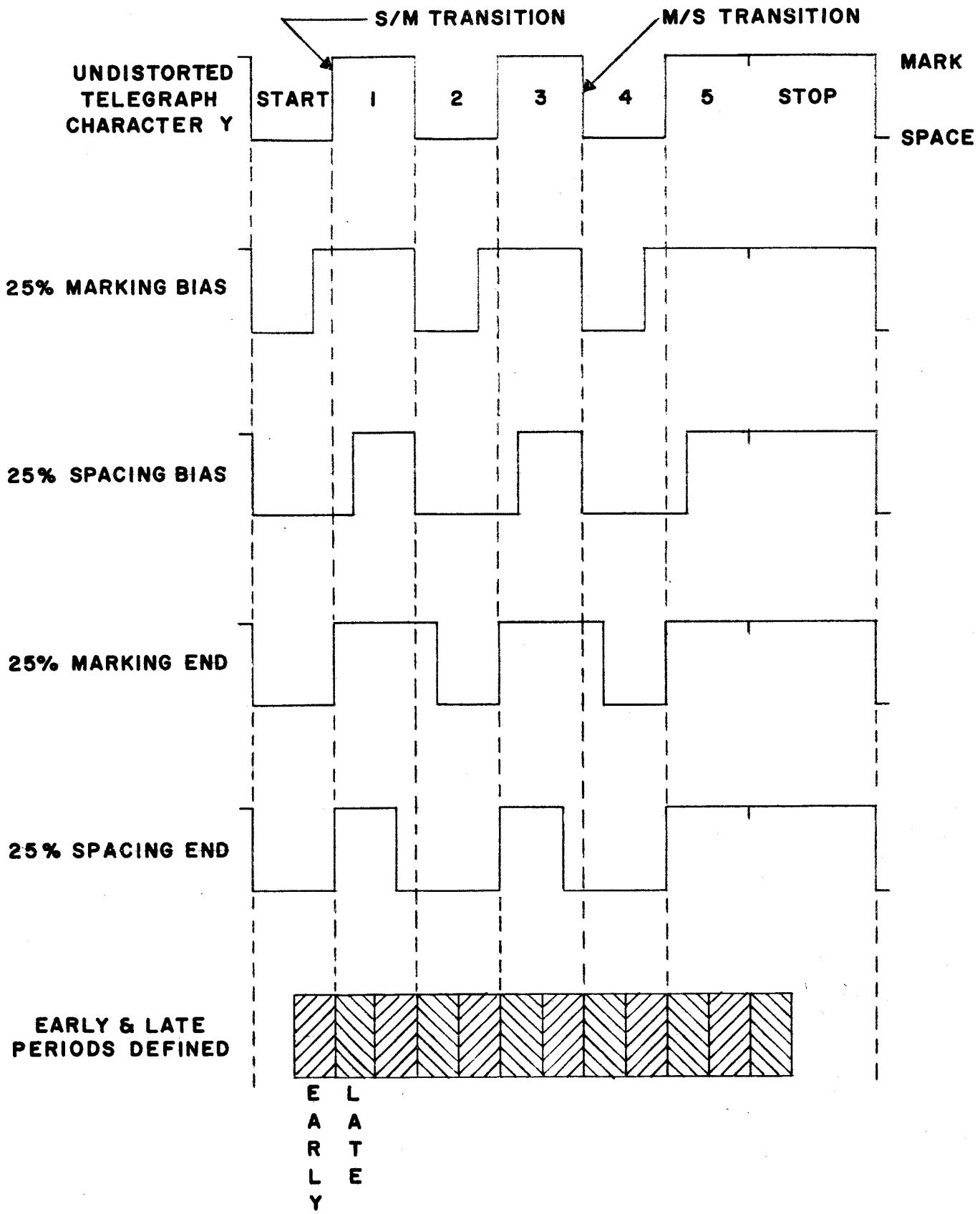


DIODE "AND" GATE

FIG. 3D

TYPICAL LOGIC CIRCUITS

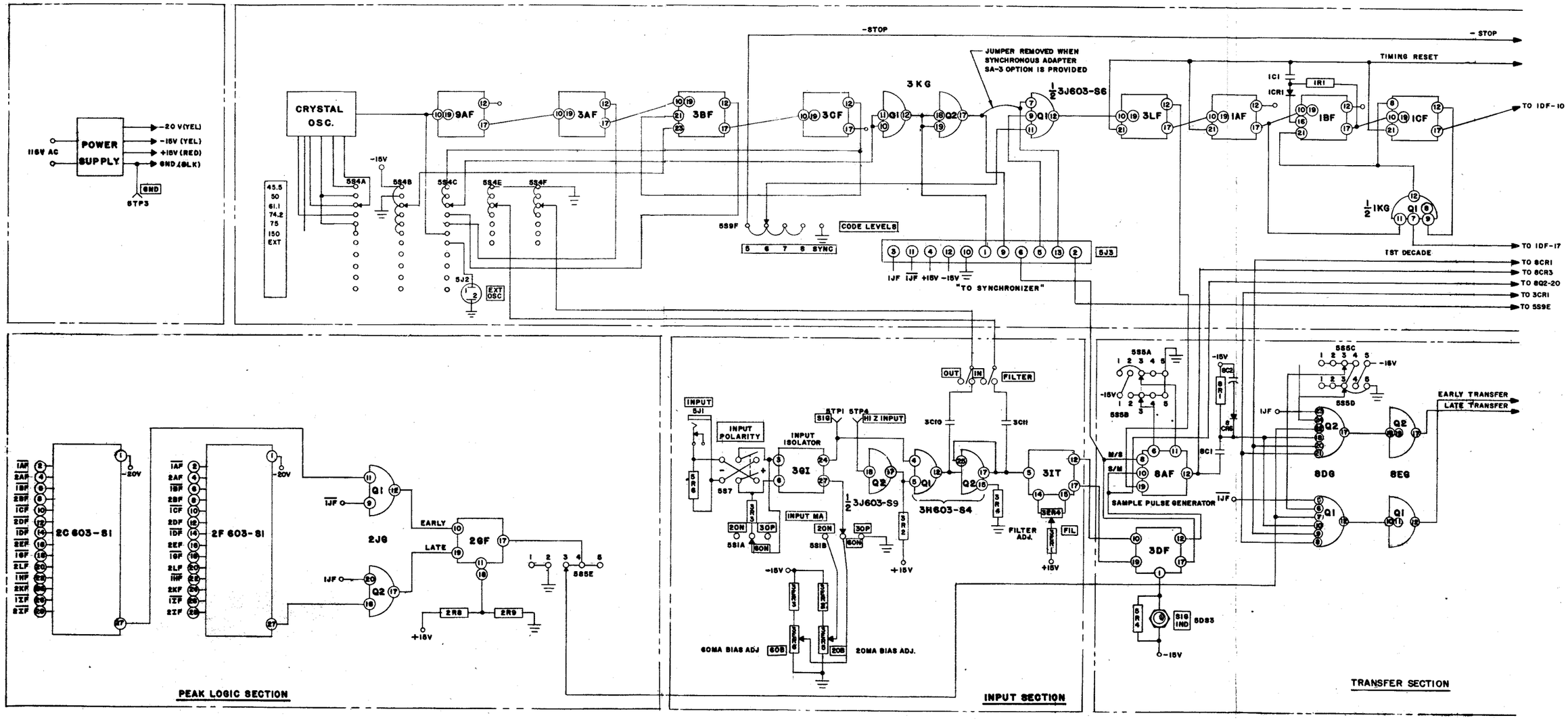
FIGURE 3A,B,C&D



TYPES OF DISTORTION

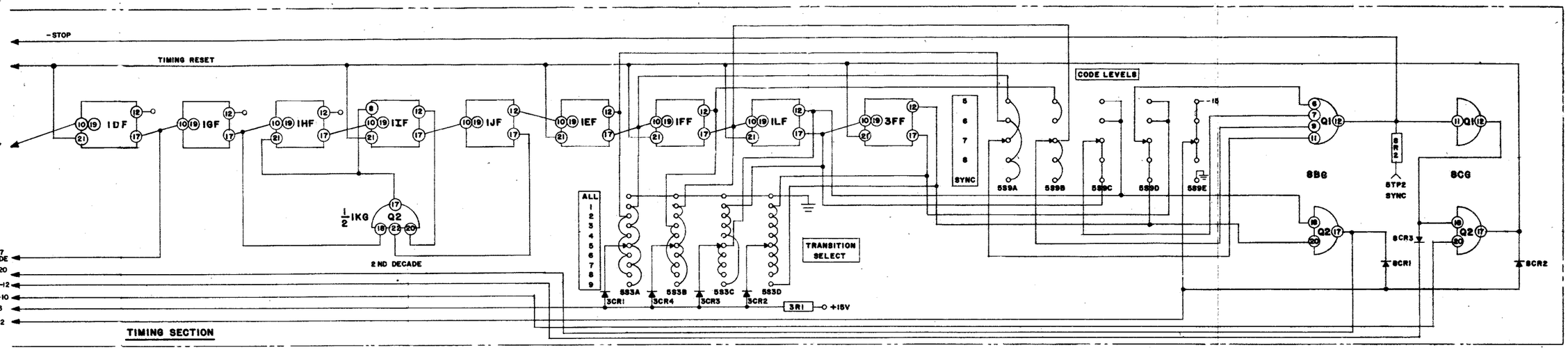
B1926

FIGURE 4

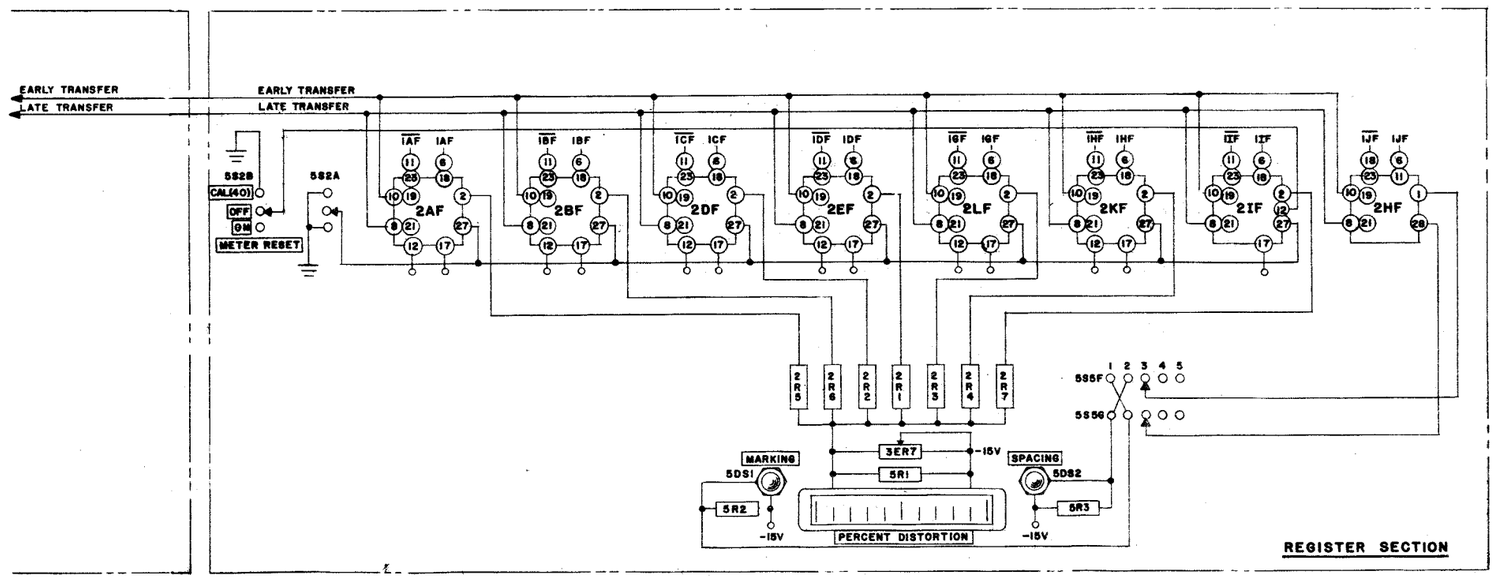


BLOCK DIAGRAM, DT-603-3

D1934
FIGURE 6
SHEET 1 OF 2



TIMING SECTION



REGISTER SECTION

NOTES:

1- ▭ DESIGNATIONS WHICH ARE ENCLOSED IN A RECTANGLE CORRESPOND TO ACTUAL MARKINGS ON THE UNIT ITSELF.
2- ○ DESIGNATIONS WHICH ARE ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.
3- FRONT PANEL MARKINGS FOR THE SWITCH DESIGNATED AS 5S5A, 5S5B, ETC. ARE ABBREVIATED AS FOLLOWS.

ABBREVIATION	ACTUAL	
5S5	AVERAGE	PEAK
1	BIAS	
2	END	
3		TOTAL
4		EARLY
5		LATE

4- DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS.

3LF
ASSEMBLY NUMBER
LOCATION ON ASSEMBLY
TYPE OF CIRCUIT (SEE NOTE No 5)

5- DESIGNATIONS OF CIRCUIT TYPES ARE ABBREVIATED AS FOLLOWS.

F = FLIP-FLOP
G = GATE
T = TRIGGER
I = ISOLATOR
S = SPECIAL

6- DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS.

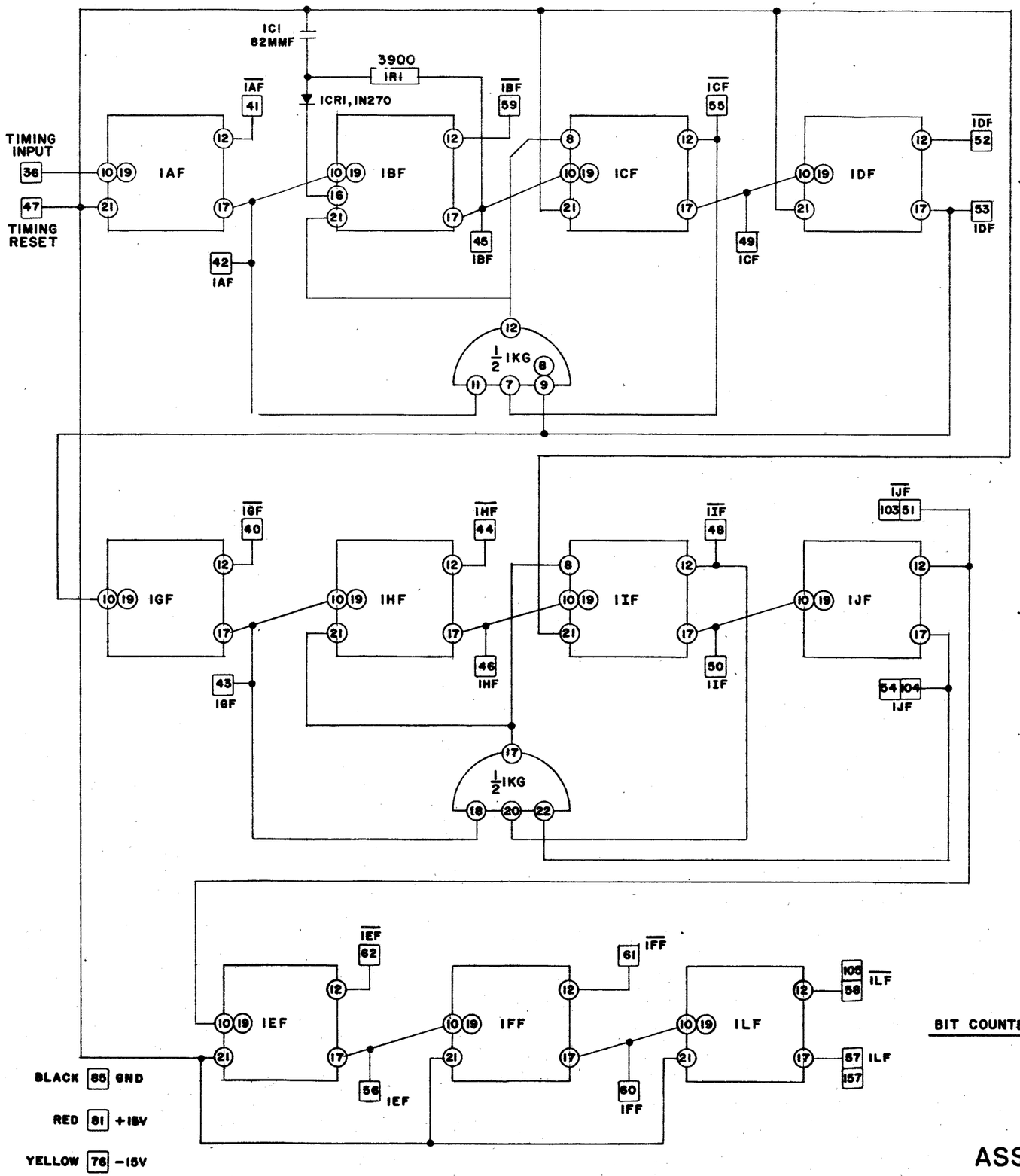
ASSEMBLY NUMBER → 3
SUB-ASSY. POSITION (IF ANY) → E
COMPONENT TYPE → R
COMPONENT NUMBER → 5
(IN THIS EXAMPLE A RESISTOR)

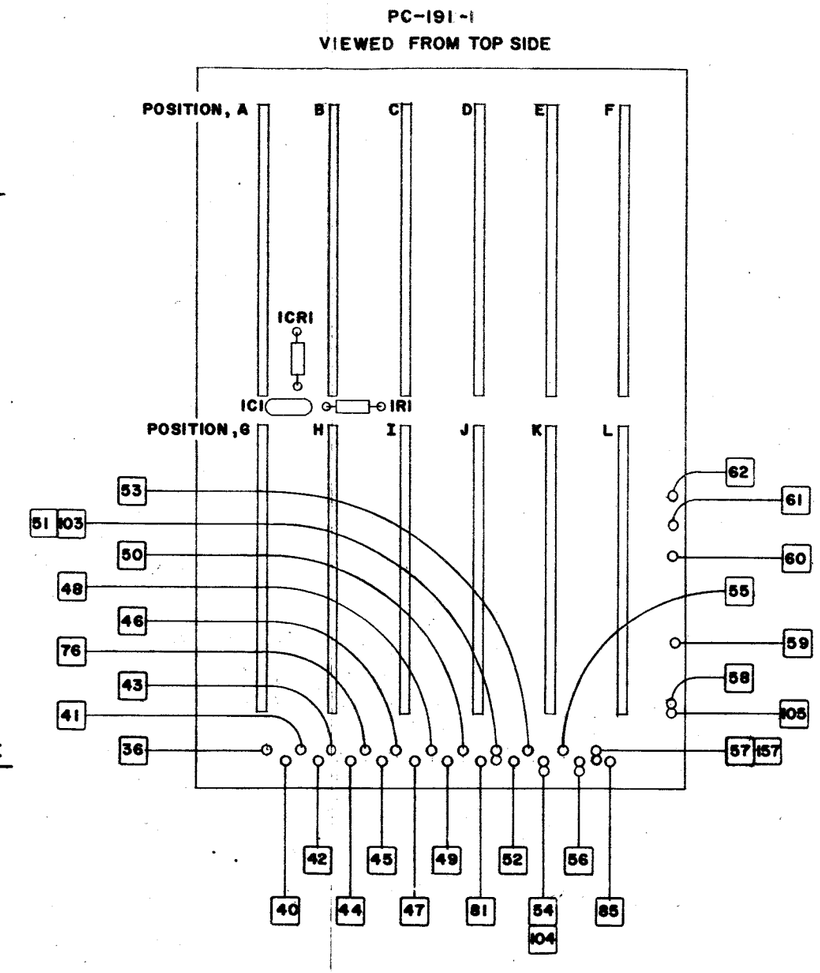
7- BINARY OUTPUT DESIGNATIONS;
ON FLIP-FLOPS THE "0" OUTPUT (PIN 12) IS DESIGNATED WITH A BAR OVER THE DESIGNATOR. WHILE THE "1" OUTPUT (PIN 17) USES THE PLAIN DESIGNATOR. EXAMPLE: FOR BINARY 1BF THE "0" OUTPUT (PIN 12) IS DESIGNATED $\overline{1BF}$ WHILE THE "1" OUTPUT (PIN 17) IS DESIGNATED 1BF.

BLOCK DIAGRAM, DT-603-3

D 1934

FIGURE 6
SHEET 2 OF 2





NOTES:

1- DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,

IAF

ASSEMBLY NUMBER
POSITION ON ASSEMBLY
TYPE OF CIRCUIT, F=FLIP-FLOP G=GATE

2- ☐ DESIGNATIONS ENCLOSED IN A SQUARE INDICATE WIRE NUMBERS.

3- ◯ DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

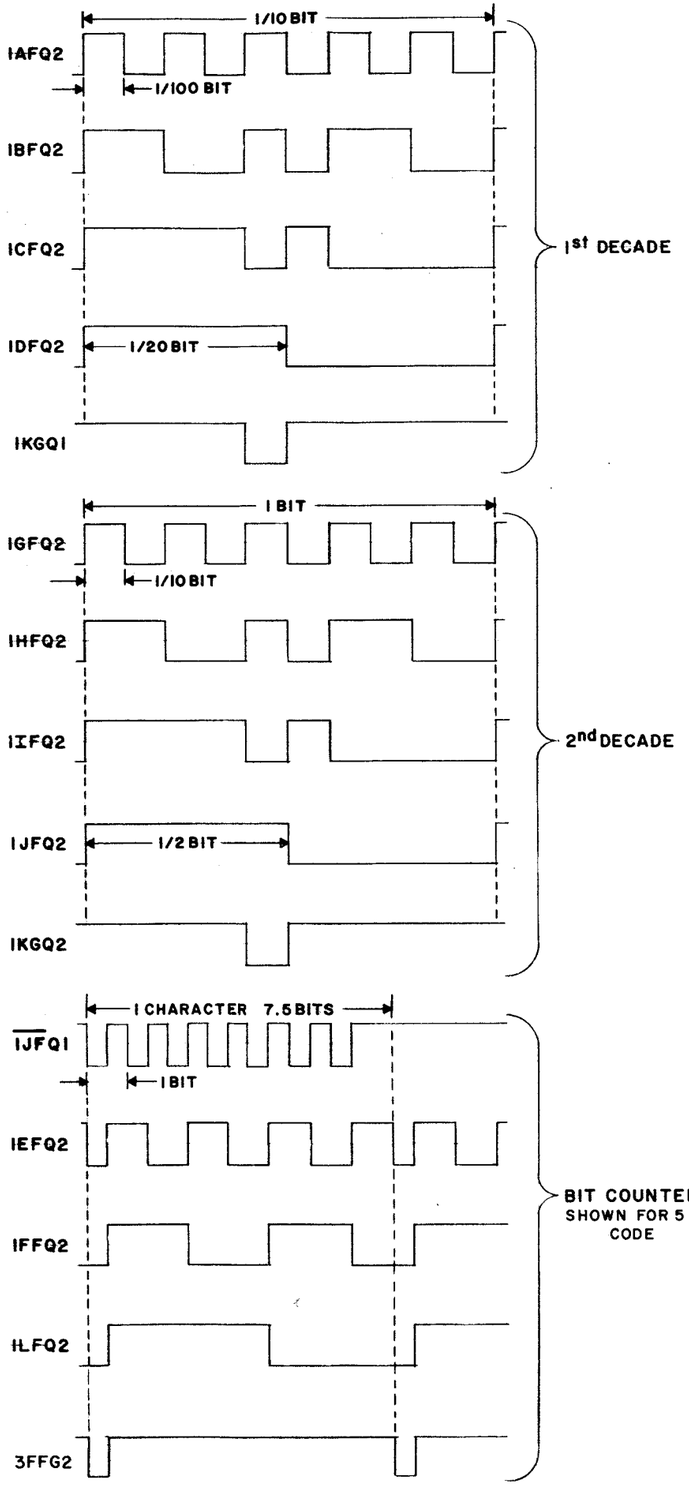
4- DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS.

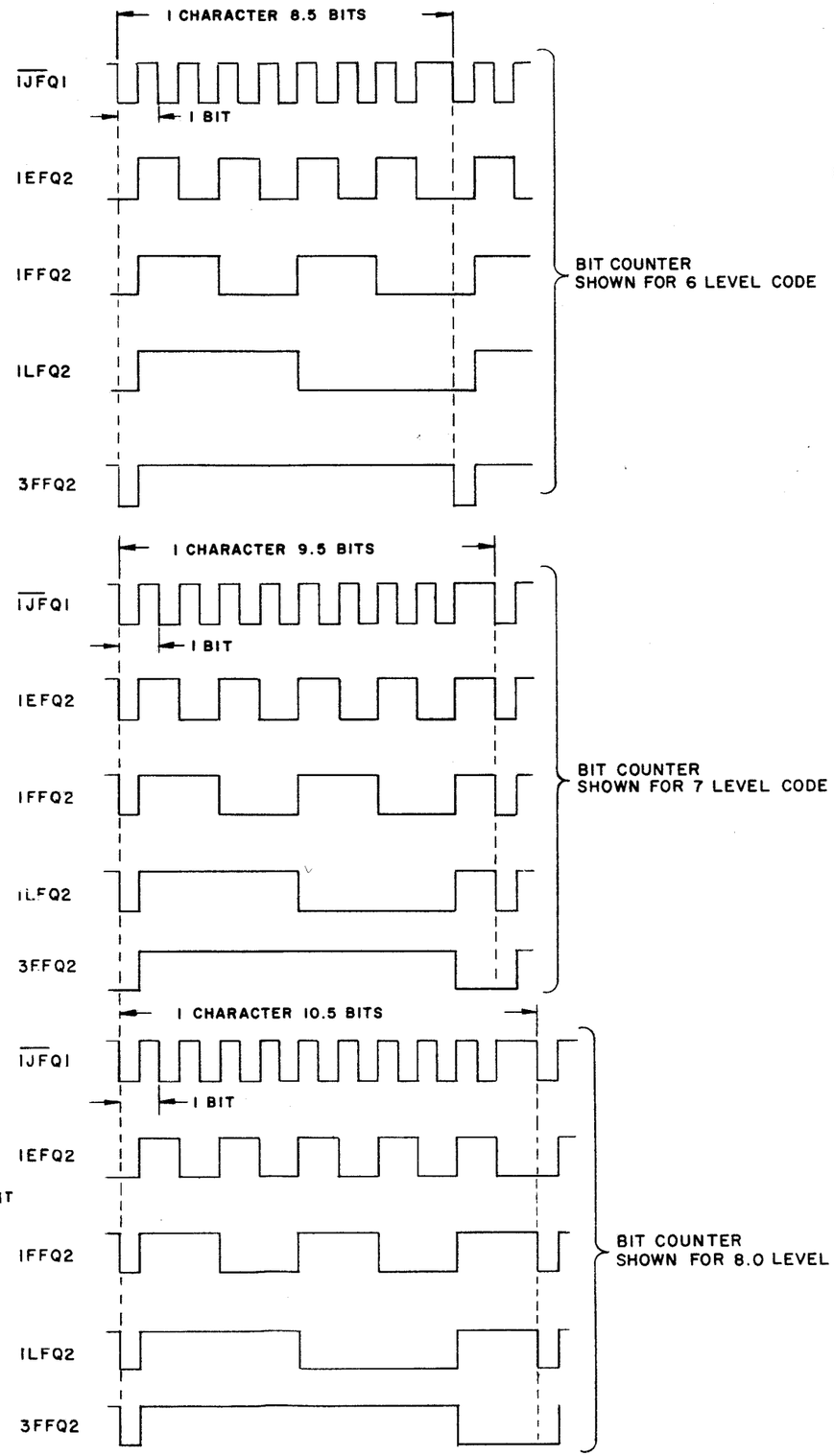
ICRI

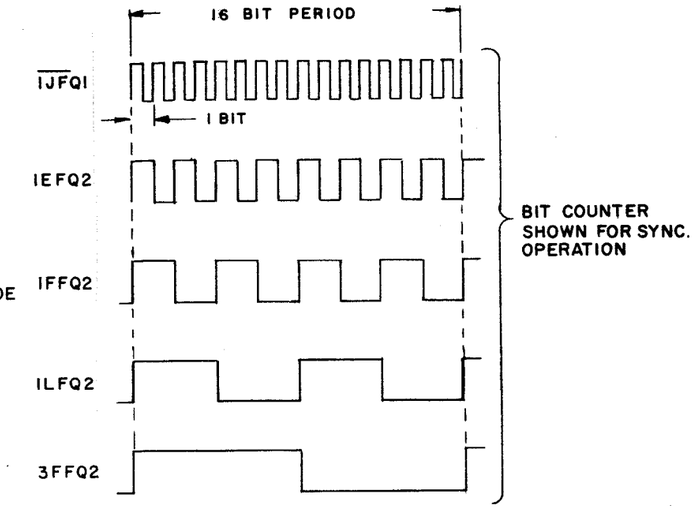
ASSEMBLY NUMBER
COMPONENT TYPE
COMPONENT NUMBER

ASSEMBLY Nº 1 DIAGRAM, DT-603-3

D1935
FIGURE 6A



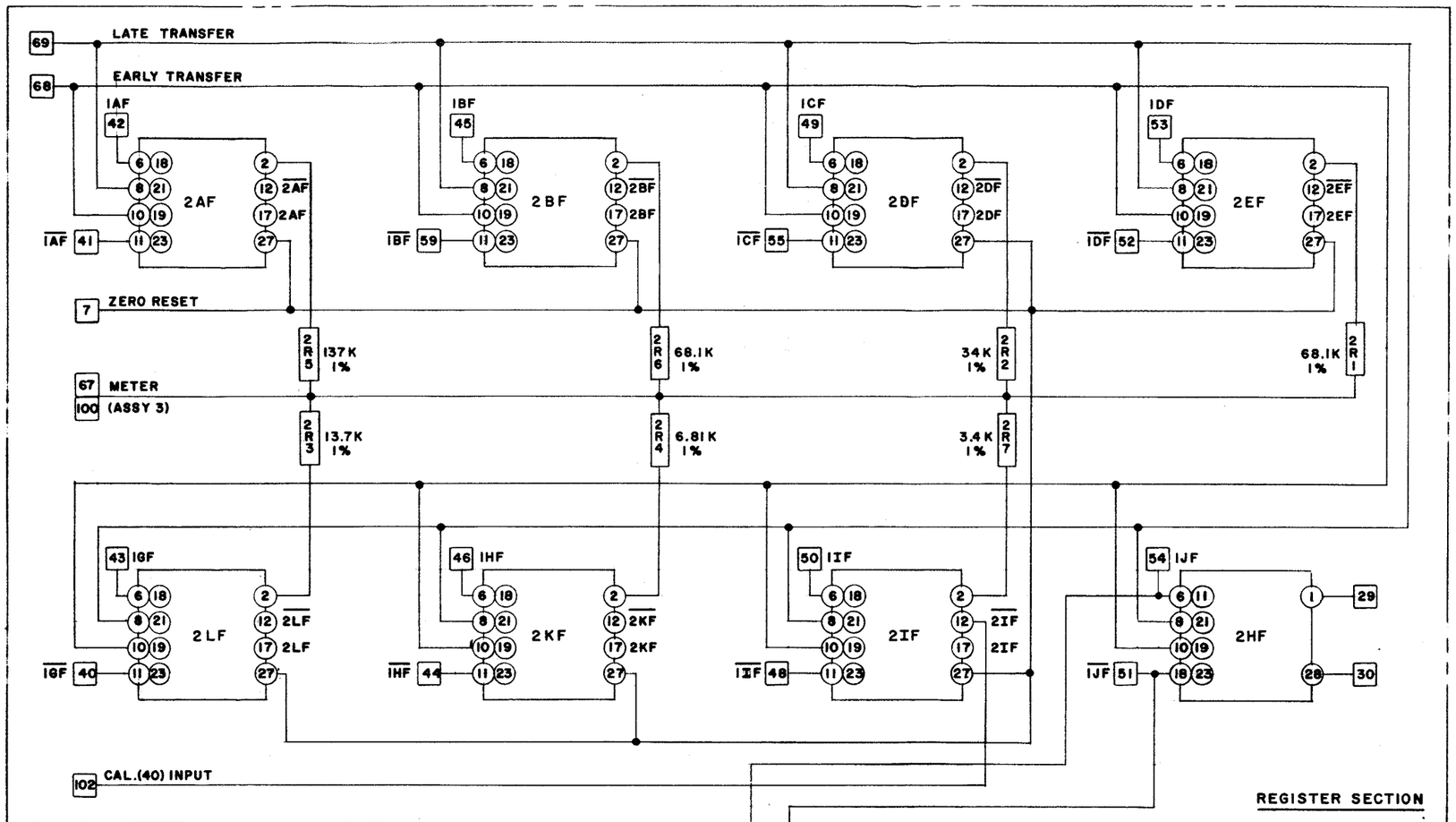


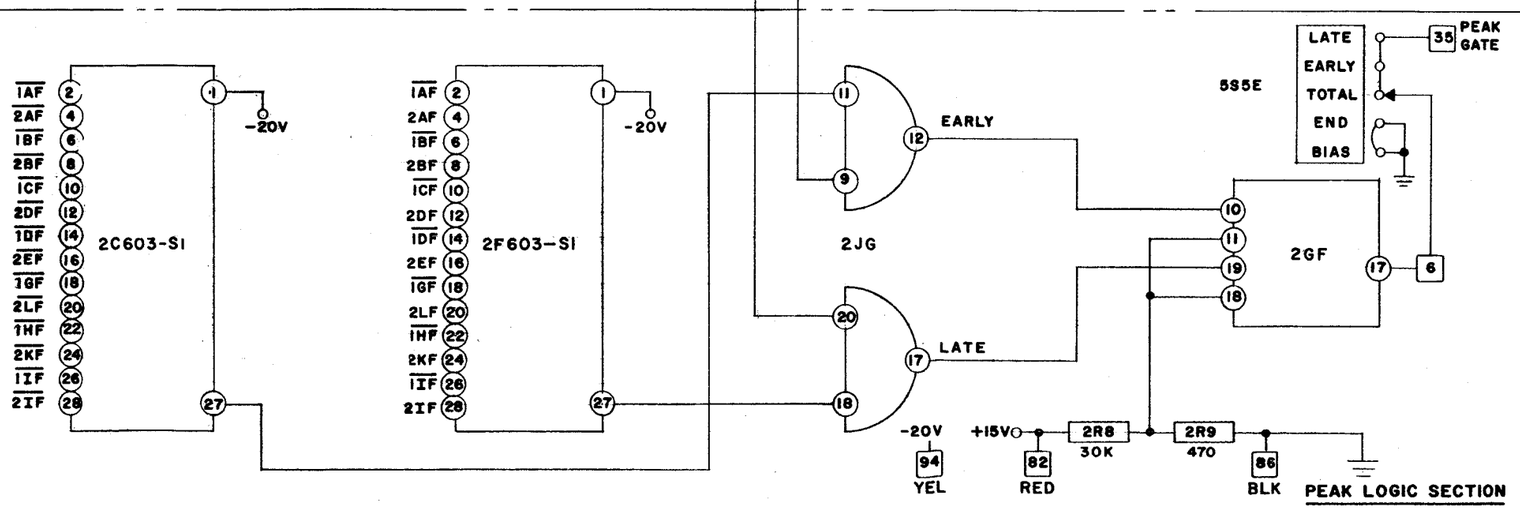


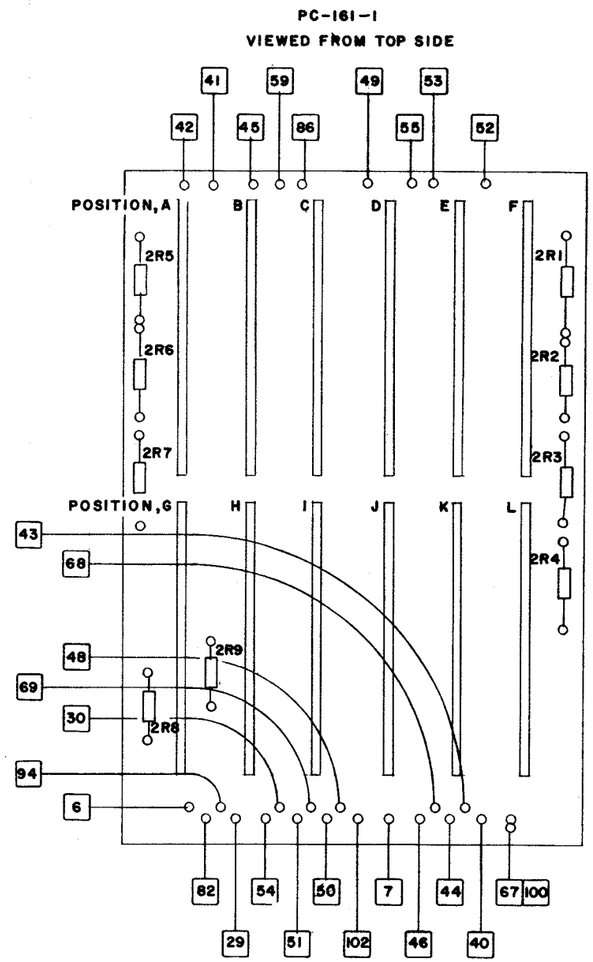
WAVEFORMS, ASSEMBLY NO. 1
DT-603

D1939

FIGURE 6B







NOTES:

1- DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,

2 AF — 2 = ASSEMBLY NUMBER, POSITION ON ASSEMBLY; AF = TYPE OF CIRCUIT, F = FLIP-FLOP, G = GATE

2- ☐ DESIGNATIONS ENCLOSED IN A SQUARE INDICATE WIRE NUMBERS.

3- ◯ DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

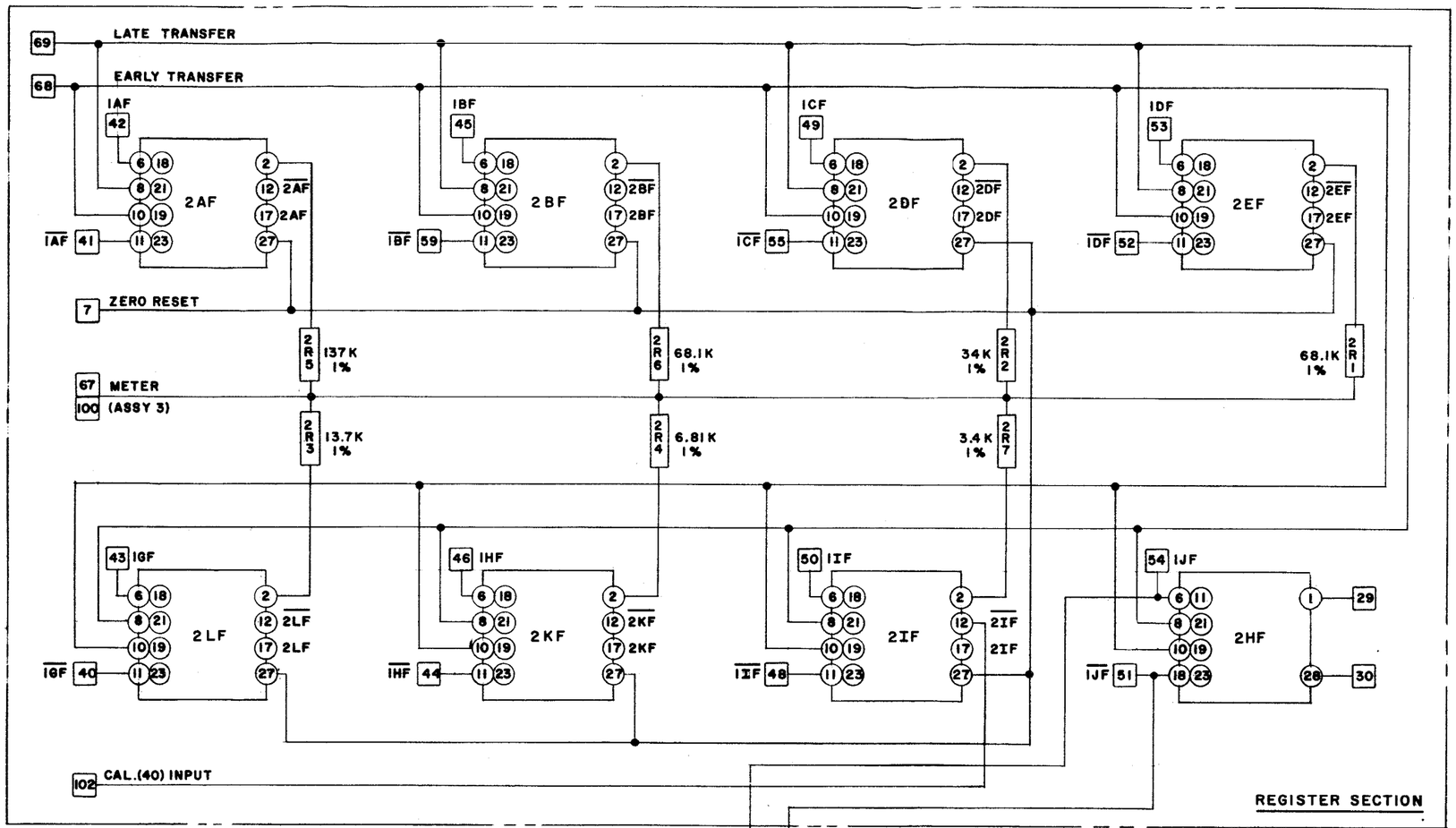
4- DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS.

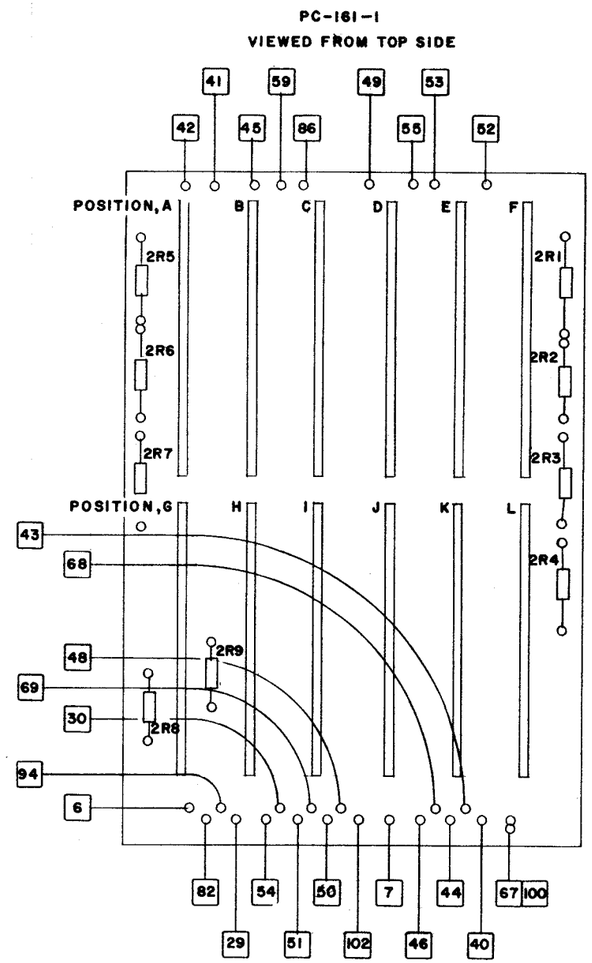
2R7 — 2 = ASSEMBLY NUMBER, R = COMPONENT TYPE; 7 = COMPONENT NUMBER

ASSEMBLY Nº 2 DIAGRAM, DT-603-3

D1937

FIGURE 7A





NOTES:

1- DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,
2AF — 2 = ASSEMBLY NUMBER, A = POSITION ON ASSEMBLY, F = TYPE OF CIRCUIT, F = FLIP-FLOP, G = GATE

2- [ ] DESIGNATIONS ENCLOSED IN A SQUARE INDICATE WIRE NUMBERS.

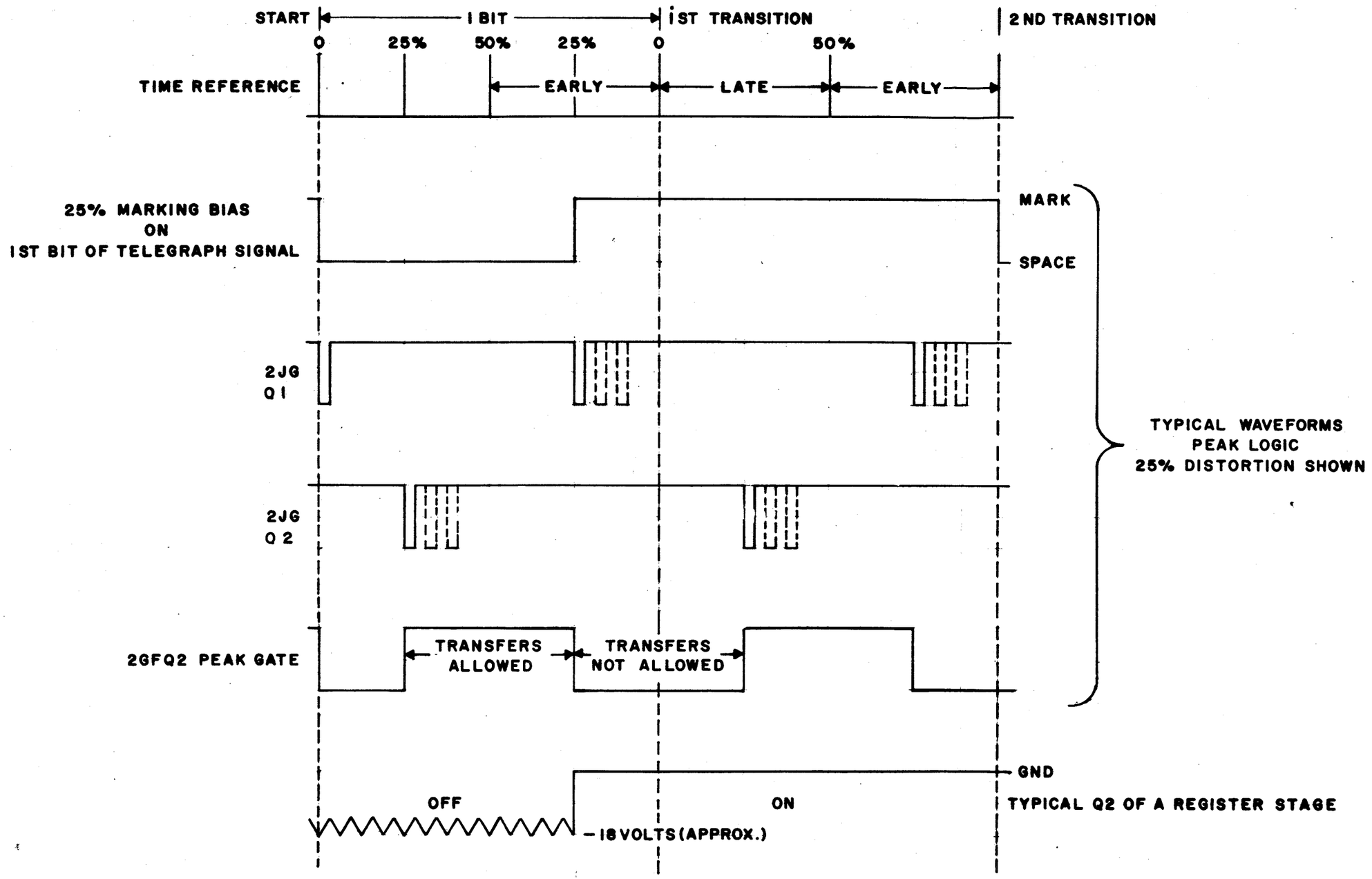
3- ( ) DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

4- DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS.
2R7 — 2 = ASSEMBLY NUMBER, R = COMPONENT TYPE, 7 = COMPONENT NUMBER

ASSEMBLY Nº 2 DIAGRAM, DT-603-3

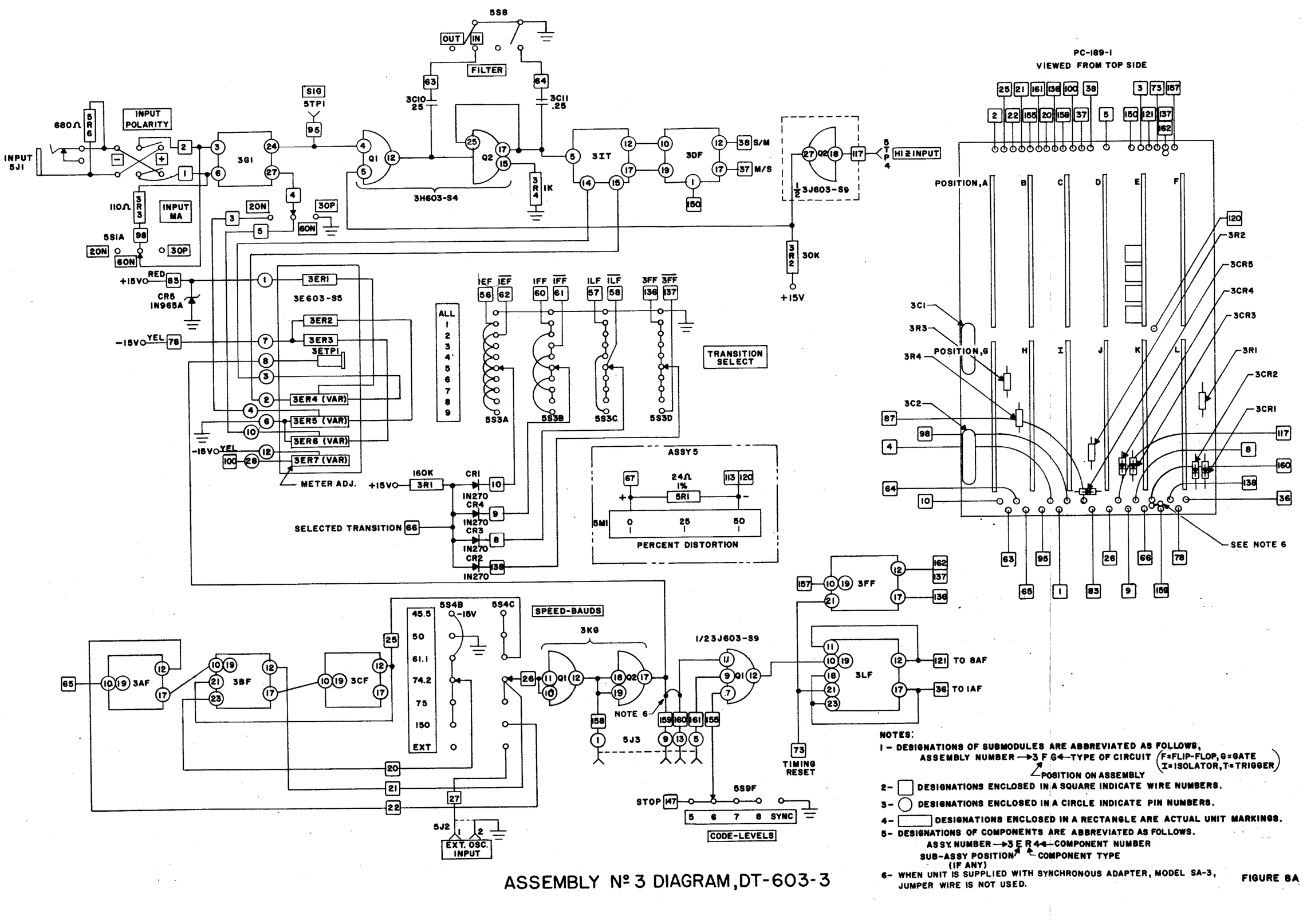
D1937

FIGURE 7A



WAVEFORMS, ASSEMBLY Nº 2

FIGURE 7B



NOTES:

1 – DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,
ASSEMBLY NUMBER → 3 F G ← TYPE OF CIRCUIT (F=FLIP-FLOP, G=GATE I=ISOLATOR, T=TRIGGER)
POSITION ON ASSEMBLY

2 – ☐ DESIGNATIONS ENCLOSED IN A SQUARE INDICATE WIRE NUMBERS.

3 – ○ DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

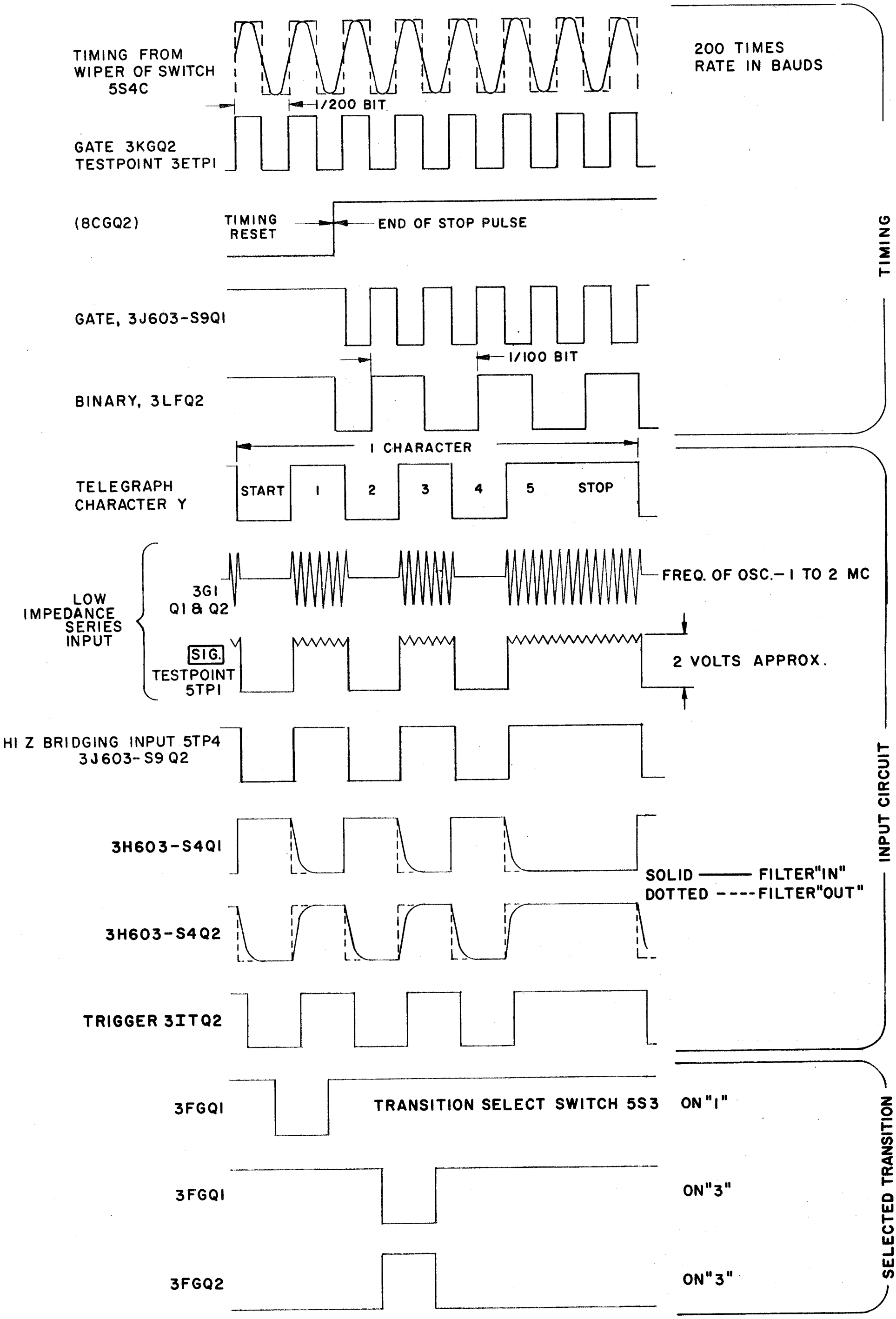
4 – ▭ DESIGNATIONS ENCLOSED IN A RECTANGLE ARE ACTUAL UNIT MARKINGS.

5 – DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS.
ASSY. NUMBER → 3 E R 4 ← COMPONENT NUMBER
SUB-ASSY POSITION (IF ANY)
COMPONENT TYPE

6 – WHEN UNIT IS SUPPLIED WITH SYNCHRONOUS ADAPTER, MODEL SA-3, JUMPER WIRE IS NOT USED.

ASSEMBLY Nº 3 DIAGRAM, DT-603-3

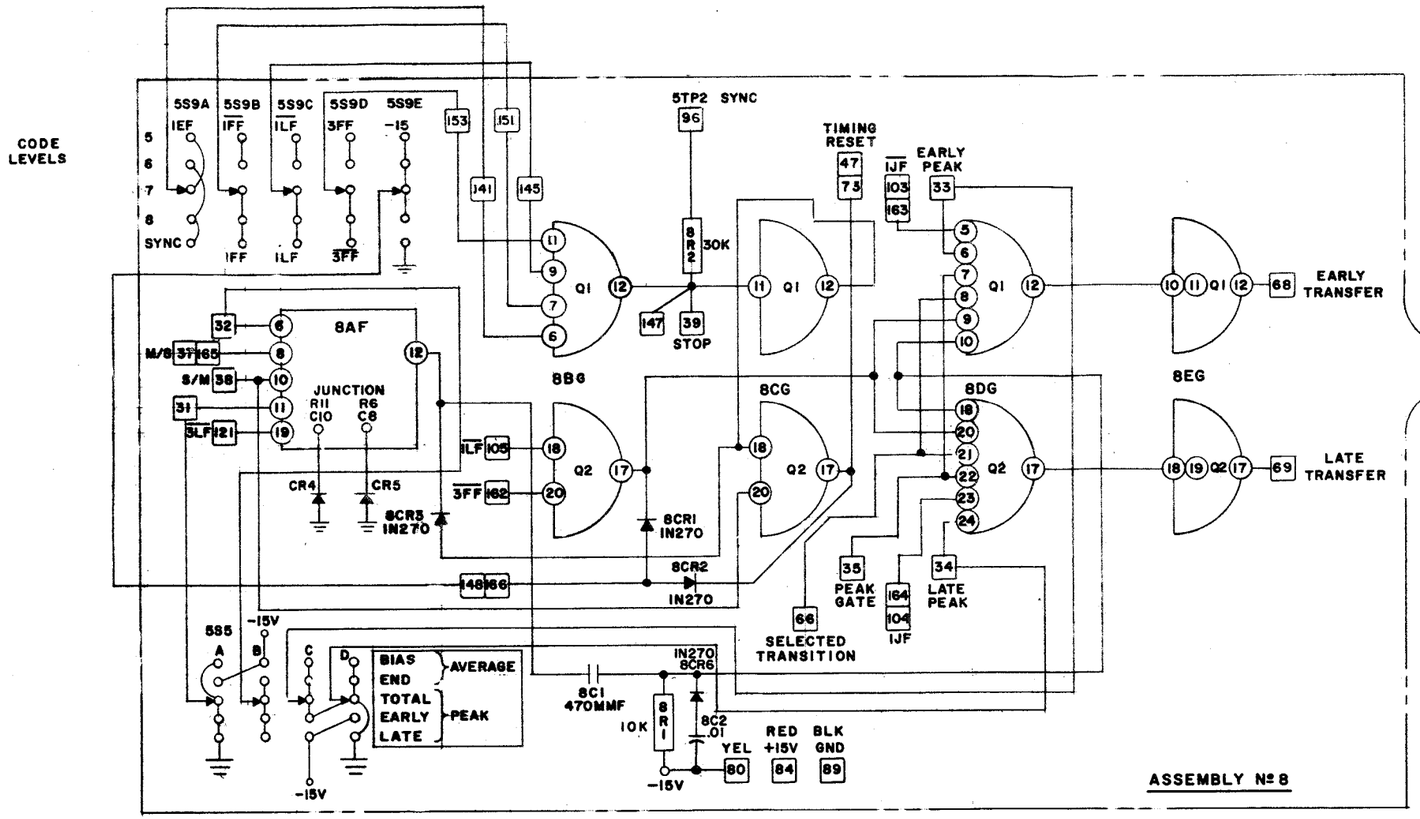
FIGURE 8A D1938



B1929

WAVEFORMS, ASSEMBLY Nº 3

FIGURE 8B



NOTES:

1 – DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,

8AF
ASSEMBLY NUMBER
POSITION ON ASSEMBLY
TYPE OF CIRCUIT, F = FLIP-FLOP, G = GATE, S = SPECIAL

2 – ☐ DESIGNATIONS ENCLOSED IN A SQUARE INDICATE WIRE NUMBERS.

3 – ◯ DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

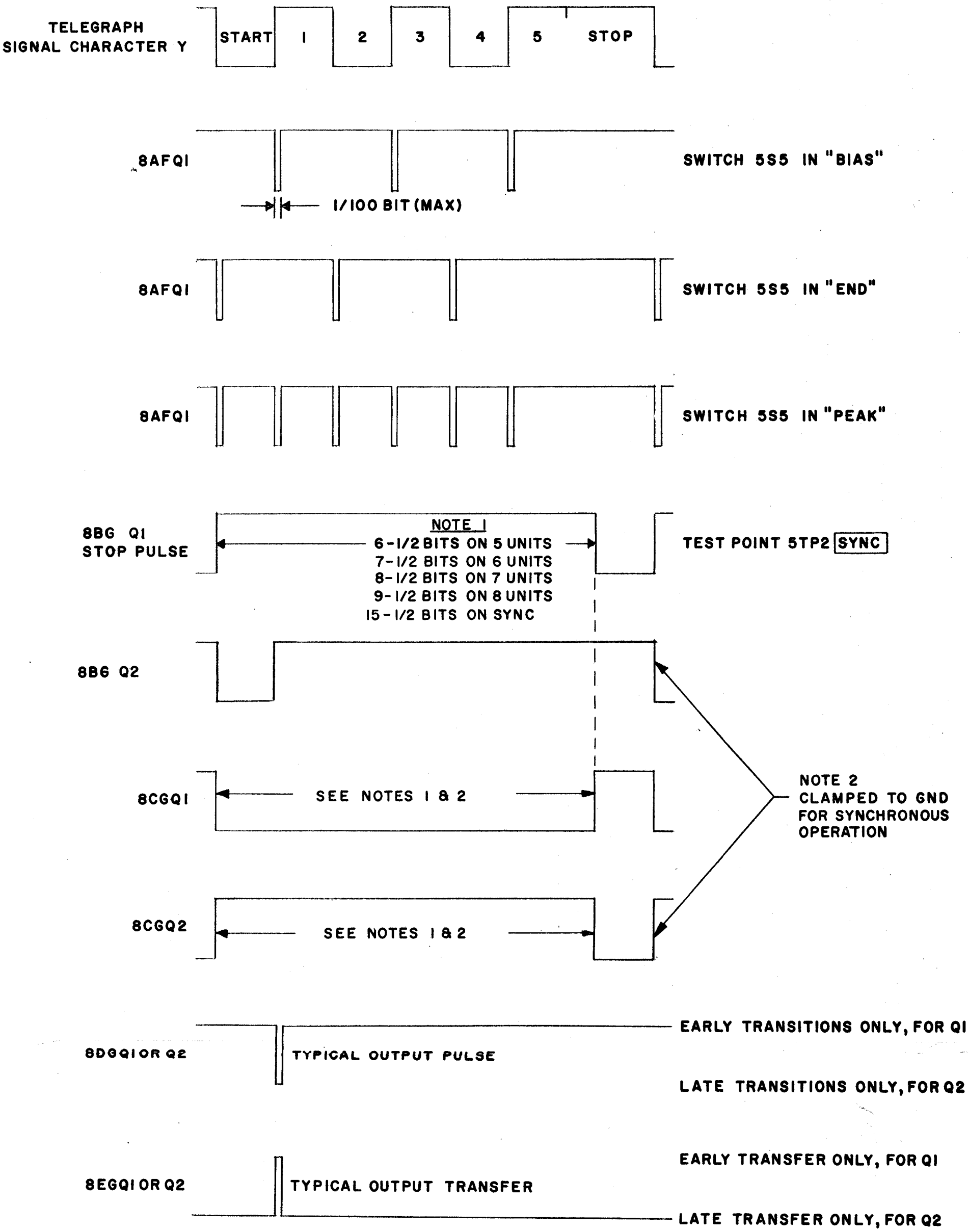
4 – DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS,

8R2
ASSEMBLY NUMBER
COMPONENT TYPE
COMPONENT NUMBER

D1936

ASSEMBLY Nº 8, Nº 6 & Nº 4 DIAGRAM, DT-603-3

FIGURE 9A

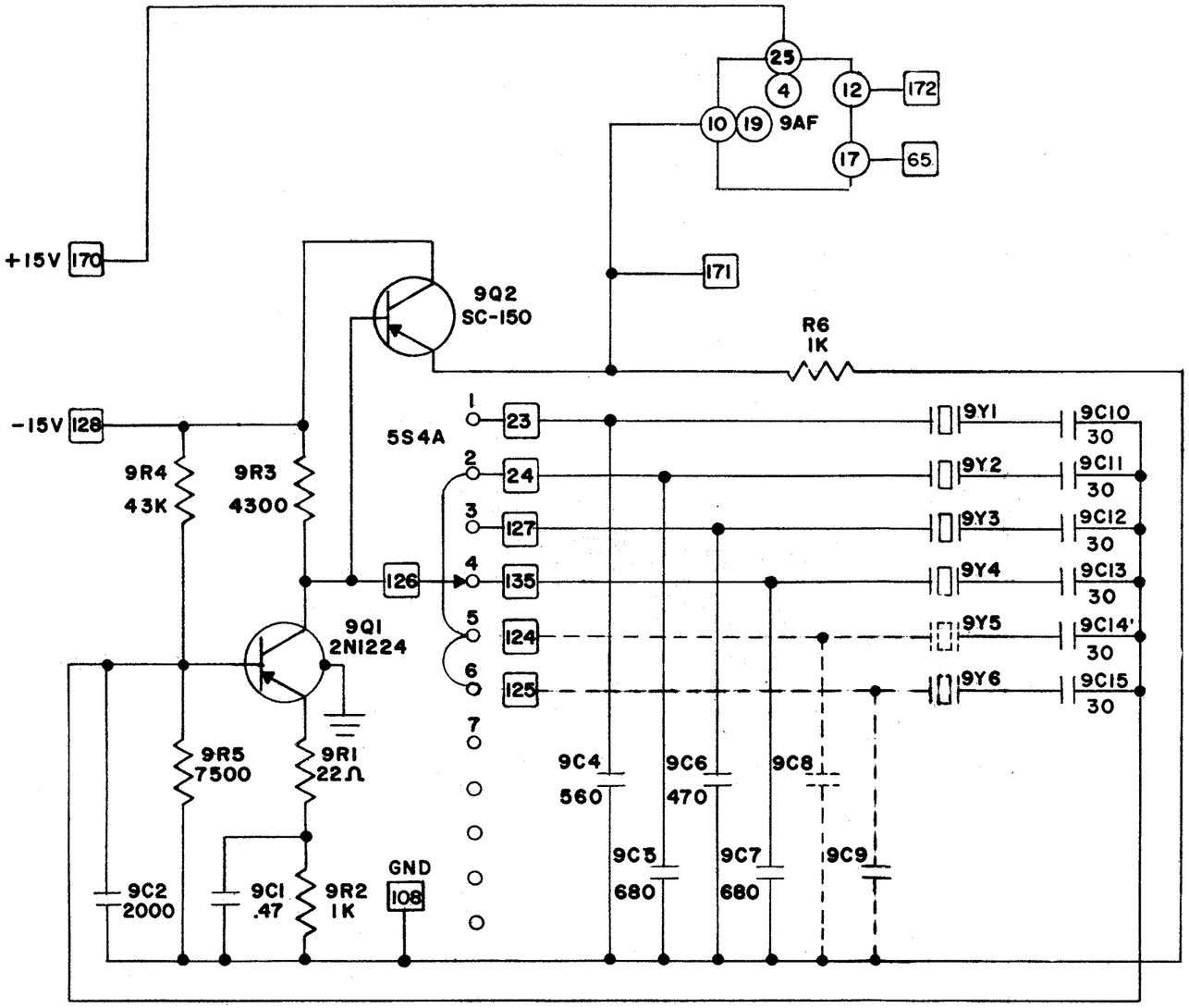


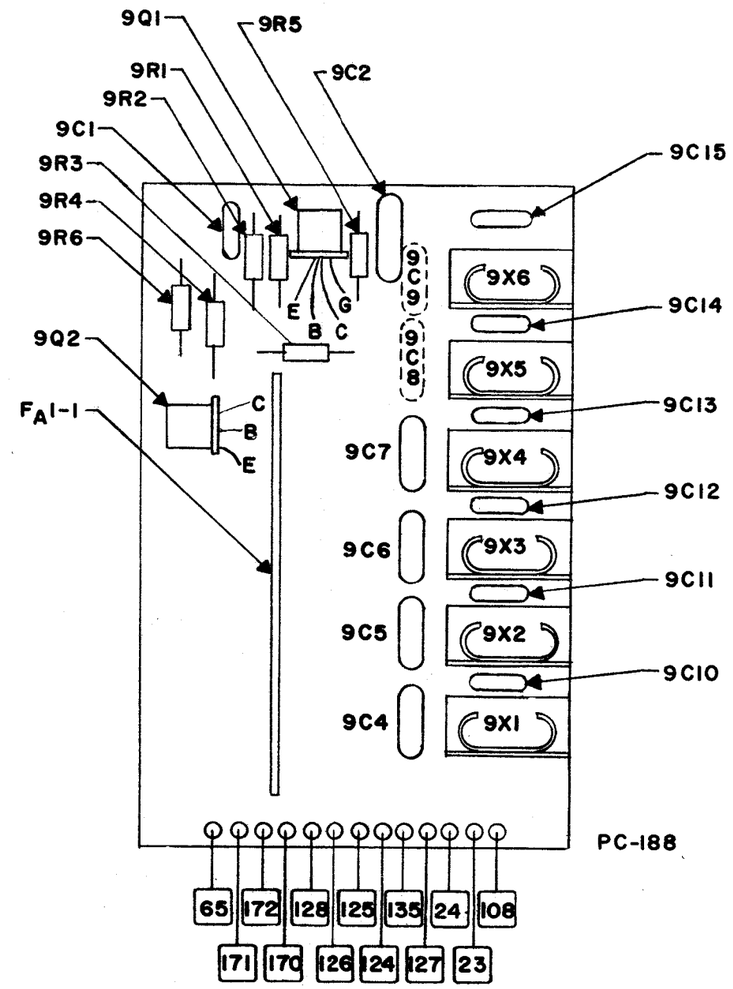
WAVEFORMS, ASSEMBLY N° 8

ILLUSTRATED FOR 5 LEVEL START-STOP OPERATION

B1930

FIGURE 9B





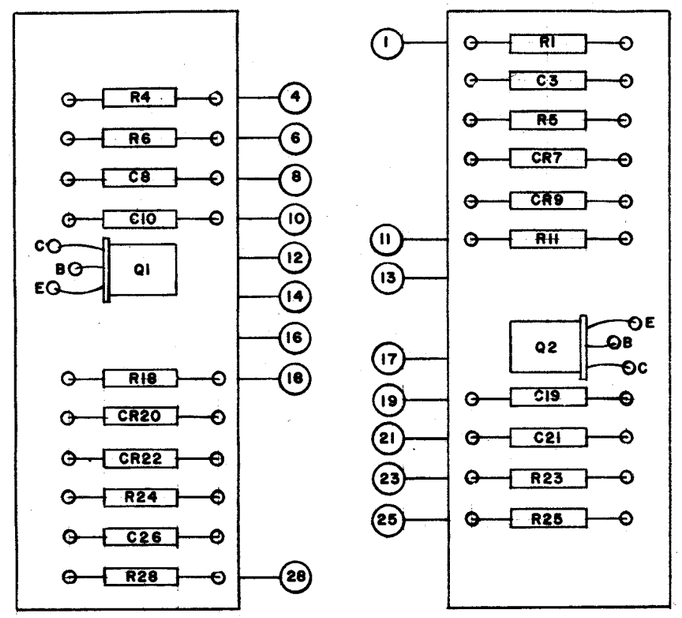
NOTE

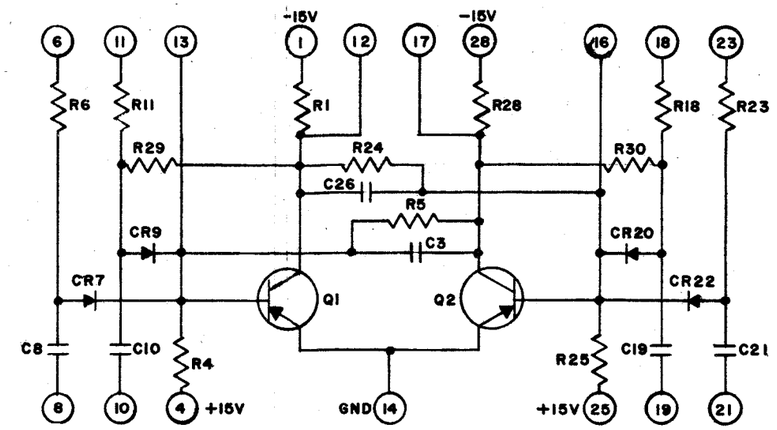
1- THE SUBMODULE DESIGNATION 9AF INDICATES A FLIP-FLOP CIRCUIT, IN POSITION A ON ASSY 9.
2- A TYPICAL COMPONENT DESIGNATION 9R3 INDICATES RESISTOR Nº 3 LOCATED ON ASSY 9.
3- DOTTED LINE COMPONENTS INDICATE PROVISIONS FOR TWO ADDITIONAL CRYSTALS.

POSITION	SPEED-BAUDS	CRYSTAL VALUE	CRYSTAL DESIGNATION
1	45.5	145.622	9Y1
2	50	120.000	9Y2
3	61.1	195.652	9Y3
4	74.2	118.720	9Y4
5	75	120.000	9Y2
6	150	120.000	9Y2

ASSEMBLY Nº 9 DIAGRAM, DT-603-3

B1932
FIGURE 9C





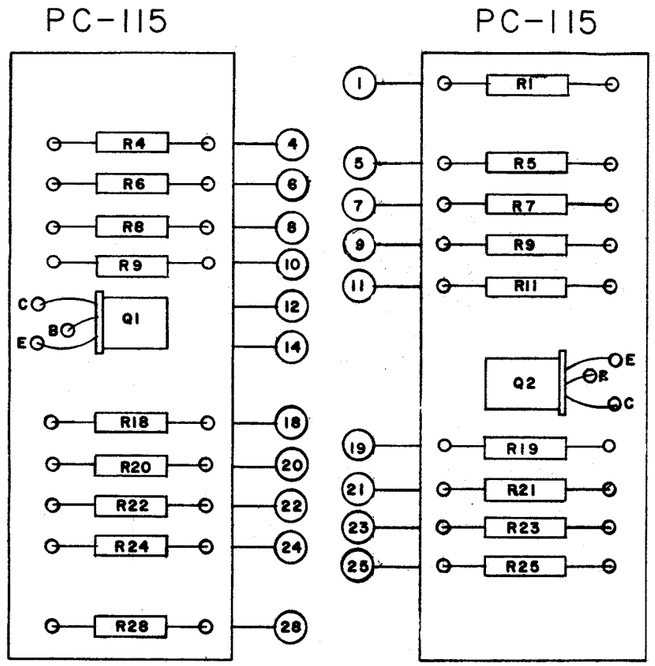
NOTES:
1 – FOR EXPLANATION OF SUBMODULE DESIGNATIONS SEE PARTS BREAKDOWN.
2 – RESISTORS R29 AND R30 ARE NOT NORMALLY USED. SEE CHART OF SUBMODULES OR PARTS LIST FOR LISTING OF SUBMODULES WHICH MAY USE THESE RESISTORS.

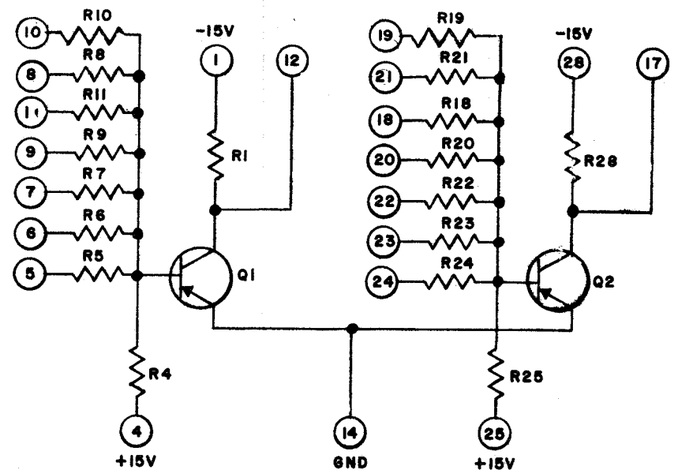
* 1K RESISTORS ARE 1/2 W ± 5%

DESIGN VALUES		Fa				Fc	Fd	Fe	Fg
Nº	DESCRIPTION	1-1	1-2	2-1	2-2	2-2	2-2	2-2	2-2
R1	RESISTOR, CARBON, 1/4W, 5%	3900	3900	3900	3900	1K *	1K *	1K *	3900
R4	RESISTOR, CARBON, 1/4W, 5%	160K	160K	160K	160K	120K	120K	120K	160K
R5	RESISTOR, CARBON, 1/4W, 5%	30K	30K	30K	30K	10K	10K	10K	30K
R6	RESISTOR, CARBON, 1/4W, 5%	—	—	30K	30K	3900	3900	30K	3900
R11	RESISTOR, CARBON, 1/2W, 5%	30K	30K	30K	30K	3900	3900	30K	3900
R18	RESISTOR, CARBON, 1/2W, 5%	30K	30K	30K	30K	3900	3900	30K	3900
R23	RESISTOR, CARBON, 1/4W, 5%	—	30K	—	30K	3900	3900	30K	3900
R24	RESISTOR, CARBON, 1/4W, 5%	30K	30K	30K	30K	10K	10K	10K	30K
R25	RESISTOR, CARBON, 1/4W, 5%	160K	160K	160K	160K	120K	120K	120K	160K
R28	RESISTOR, CARBON, 1/4W, 5%	3900	3900	3900	3900	1K *	1K *	1K *	3900
R29	RESISTOR, CARBON, 1/4W, 5%	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
R30	RESISTOR, CARBON, 1/4W, 5%	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
C3	CAPACITOR, MOLDED, MICA	82MMF	82MMF	82MMF	82MMF	33MMF	82 MMF	82 MMF	82MMF
C8	CAPACITOR, MICA	—	—	82MMF	82MMF	56 MMF	150 MMF	150 MMF	82MMF
C10	CAPACITOR, MICA	82MMF	82MMF	82MMF	82MMF	56MMF	150MMF	150MMF	82MMF
C19	CAPACITOR, MICA	82MMF	82MMF	82MMF	82MMF	56MMF	150 MMF	150MMF	82MMF
C21	CAPACITOR, DIPPED, MICA	—	82MMF	—	82MMF	56 MMF	150 MMF	150MMF	82MMF
C26	CAPACITOR, MOLDED, MICA	82MMF	82MMF	82MMF	82MMF	33MMF	82 MMF	82 MMF	82 MMF
CR7	DIODE	—	—	IN270	IN270	IN270	IN270	IN270	IN270
CR9	DIODE	IN270	IN270	IN270	IN270	IN270	IN270	IN270	IN270
CR20	DIODE	IN270	IN270	IN270	IN270	IN270	IN270	IN270	IN270
CR22	DIODE	—	IN270	—	IN270	IN270	IN270	IN270	IN270
Q1	TRANSISTOR	2N404	2N404	2N404	2N404	2N1683	2N404	2N404	2N404
Q2	TRANSISTOR	2N404	2N404	2N404	2N404	2N1683	2N404	2N404	2N404

SUBMODULE TYPE F
(FLIP-FLOP)
(C1568)

FIGURE 10





NOTE:

1. WHEN LESS THAN 7 INPUTS ARE PROVIDED, THE RESISTORS ARE PICKED ACCORDING TO THE FOLLOWING TABLE.

NUMBER OF INPUTS	Q1	Q2
1	R11	R18
2	R11,R9	R18,R20
3	R11,R9,R7	R18,R20,R22
4	R11,R9,R7,R6	R18,R20,R22,R23
5	R11,R9,R7,R6,R5	R18,R20,R22,R23,R24
6	R11,R9,R8,R7,R6,R5	R18,R20,R21,R22,R23,R24
7	R11,R10,R9,R8,R7,R6,R5	R18,R19,R20,R21,R22,R23,R24

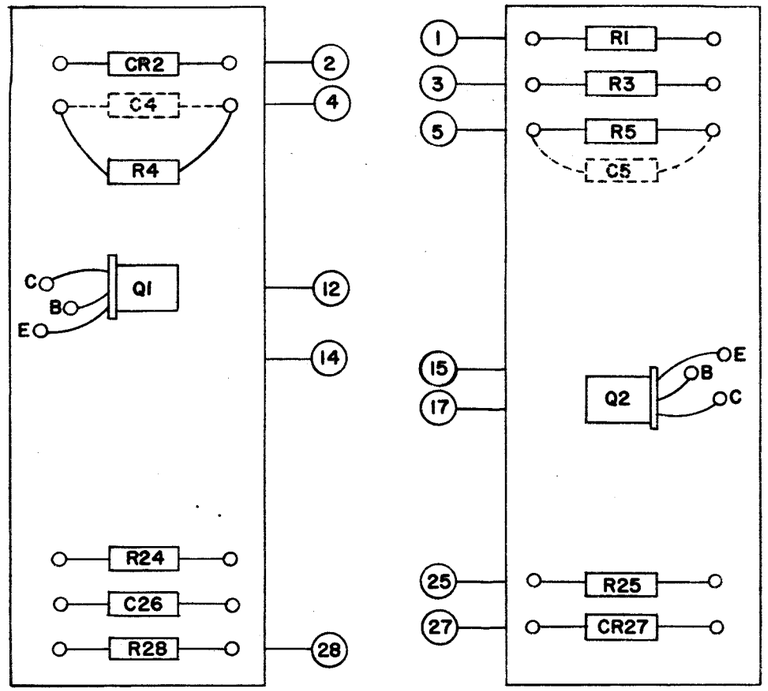
DESIGN VALUES		"a"	"b"	"h"	"k"	"u"	"m"	"L"	"n"	"f"
Nº	DESCRIPTION	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R1	RESISTOR, CARBON, 1/4W, 5%	3900	15 *	16K	16K	1K *	820 *	16 K	16K	7500
R4		160K	120K	160K	160K	43K	120K	160K	160K	160K
R5		30K	10K	—	62K	10K	16 K			43 K
R6		30K	10K	30K	62K	10K	16 K	62 K	62 K	43 K
R7		30K	10K	62K	10K	10K	16 K	62 K	62K	43 K
R8		30K	10K	62K	62K	10K	16K			43 K
R9		30K	10K	62K	62K	10K	16K	62K	62K	43 K
R10		30K	10K	62K	62K	10K	16K			43 K
R11		30K	10K	62K	62K	10K	16K	10K	10K	43 K
R18		30K	10K	62K	62K	10K	16 K	62 K	30K	43 K
R19		30K	10K	62K	62K	10K	16 K			43 K
R20		30K	10K	62K	62K	10K	16K	62K	30K	43 K
R21		30K	10K	62K	62K	10K	16K			43 K
R22		30K	10K	62K	62K	10K	16 K	62K	30K	43 K
R23		30K	10K	30K	10K	10K	16 K	10K	30K	43 K
R24		30K	10K	—	62K	10K	16K			43 K
R25		160 K	120 K	160K	160K	43K	120K	160K	160K	160 K
R28	RESISTOR, CARBON, 1/4W, 5 %	3900	1 K *	16K	16K	1K *	820 *	16 K	3900	7500
Q1	TRANSISTOR	2N404	2N404	2N404	2N404	2N1683	2N404	2N404	2N404	2N404
Q2	TRANSISTOR	2N404	2N404	2N404	2N404	2N1683	2N404	2N404	2N404	2N404

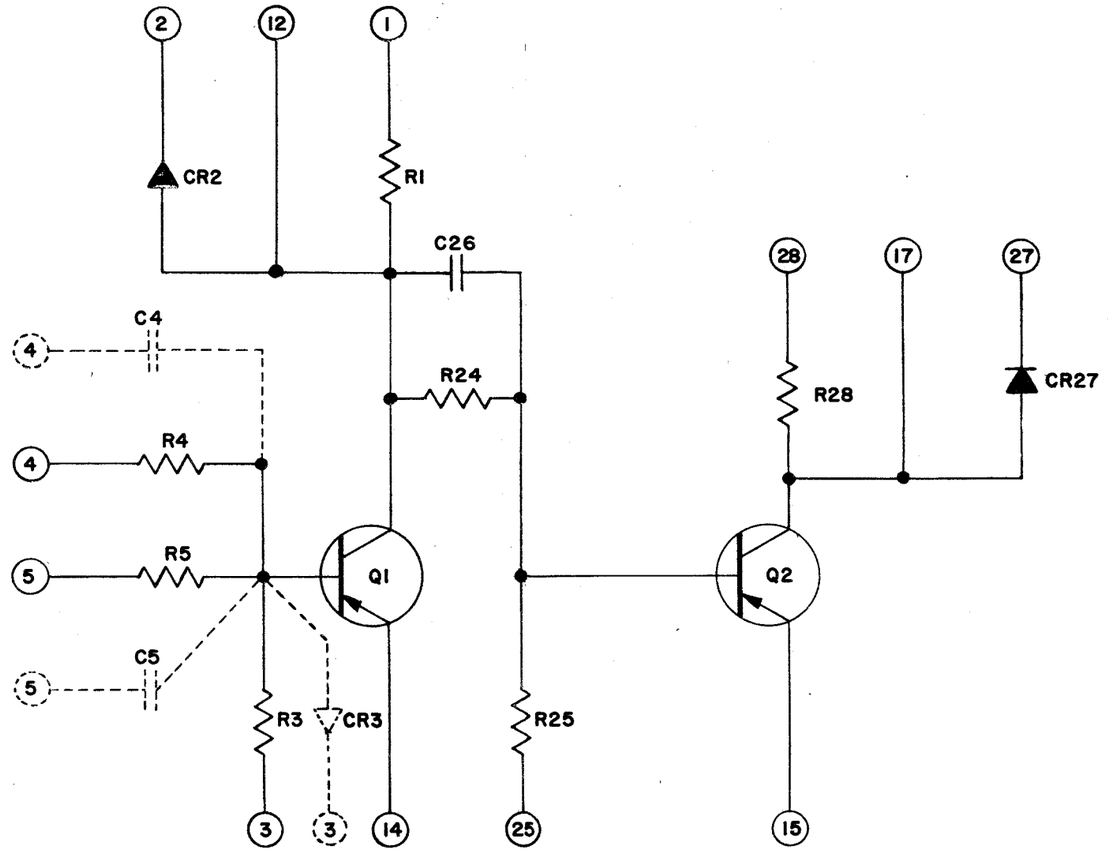
* 1K RESISTORS ARE 1/2W ± 5%

SUBMODULE, TYPE G (GATE)

(C1571)

FIGURE 11



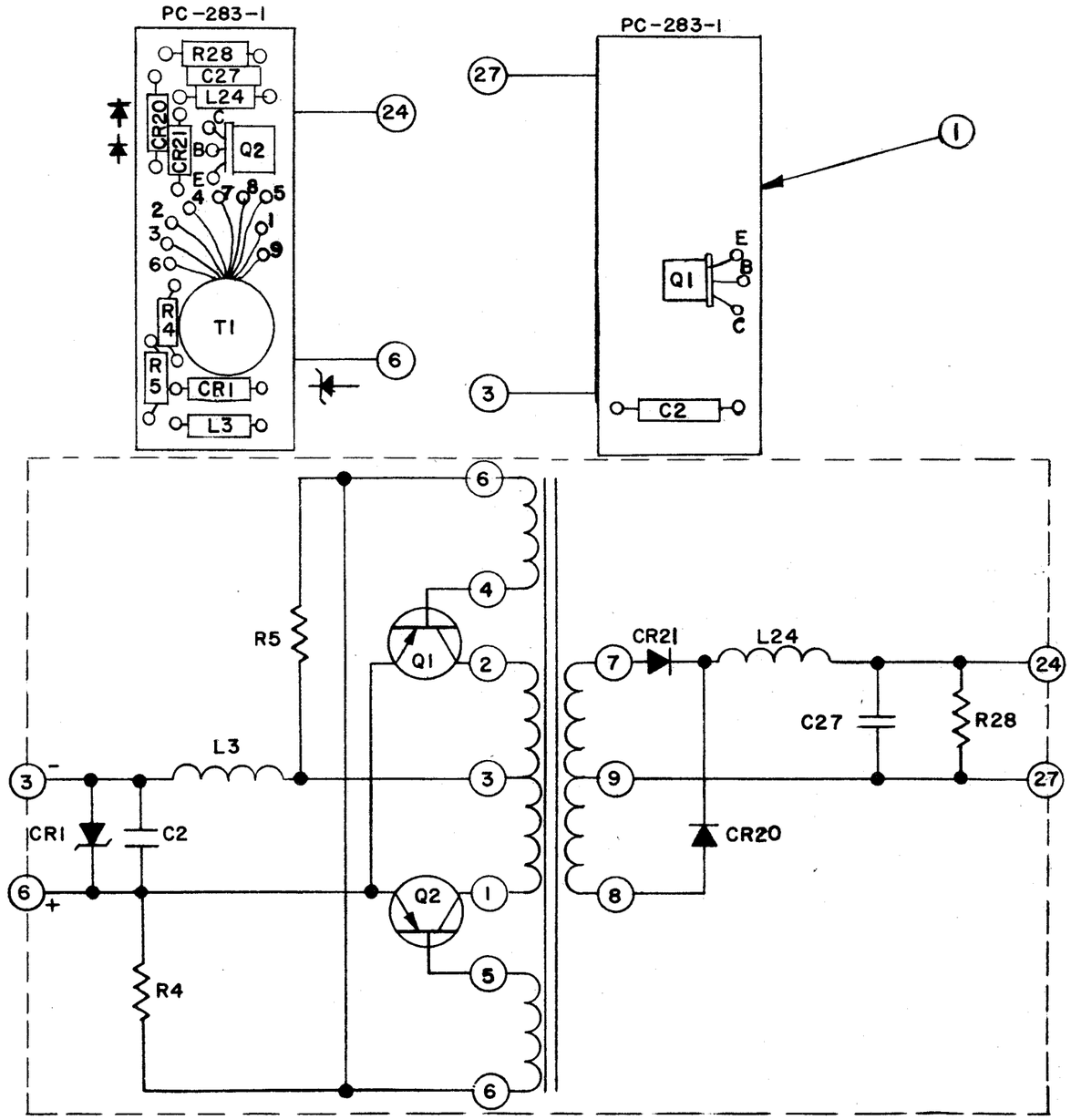


DESIGN VALUES		"A"	"B"	"C"	"D"
Nº	DESCRIPTION	VALUE	VALUE	VALUE	VALUE
R1	RESISTOR, CARBON, 1/2W, 5%	3900	7500	3900	7500
R3	1/4W	———	120K	30K	———
R4	1/4W	160K	———	———	———
R5	1/2W	30K	33K	———	100Ω
R24	1/4W	30K	43K	30K	43K
R25	1/4W,	160K	160K	160K	160K
R28	RESISTOR, CARBON, 1/2W, 5%	3900	7500	3900	7500
C4	CAPACITOR, MICA	———	82MM	———	22MMF
C5	CAPACITOR, MICA	———	———	.005	———
C26	CAPACITOR, MICA	82MM	82MM	82MM	150MM
CR2	DIODE	———	IN270	IN270	———
CR27	DIODE	———	IN270	———	———
Q1	TRANSISTOR	2N404	2N404	2N404	2N404
Q2	TRANSISTOR	2N404	2N404	2N404	2N404
CR3	DIODE	———	———	———	IN270

NOTE:
C5 LEADS TO BE SLEEVED

SUBMODULE TYPE "T" TRIGGER (C1618)

FIGURE 12



DESIGN VALUES				
NO.	DESCRIPTION	MIL	COMM.	VALUE
R4	RESISTOR, COMPOSITION, 1/2 W, ± 5%	RC20GF-163J	EB 1635	16K
R5	RESISTOR, COMPOSITION, 1/2W, ± 5%	RC20GF-303J	EB 3035	30K
R28	RESISTOR, COMPOSITION, 1/2W, ± 5%	RC20GF-331J	EB 3345	330
CR1	ZENER DIODE		IN965	IN965
CR20	DIODE		IN270	IN270
CR21	DIODE		IN270	IN270
L3	CHOKE	2500-12	*2500-12	470µh
L24	CHOKE	2500-12	*2500-12	470µh
C2	CAPACITOR, DISC	CK63AW103M	TGS-10*	.01µf
C27	CAPACITOR, DISC	CK62AW502M	CK-502*	.005µf
T1	TRANSFORMER	B 1629	B1074	
Q1	TRANSISTOR		2N1300	2N1300
Q2	TRANSISTOR		2N1300	2N1300

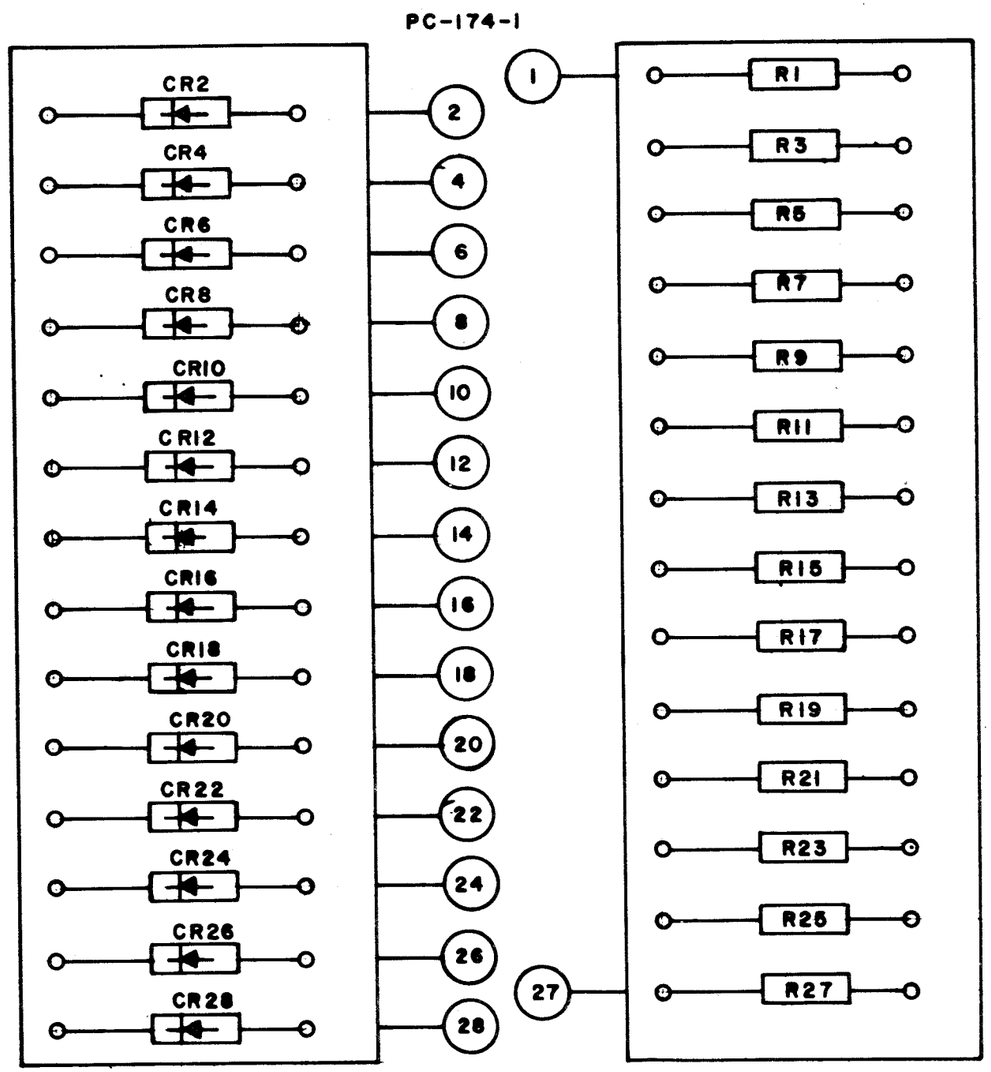
* L3 & L24 ARE DELEVAN
C2 IS SPRAGUE
C27 IS CENTRALAB

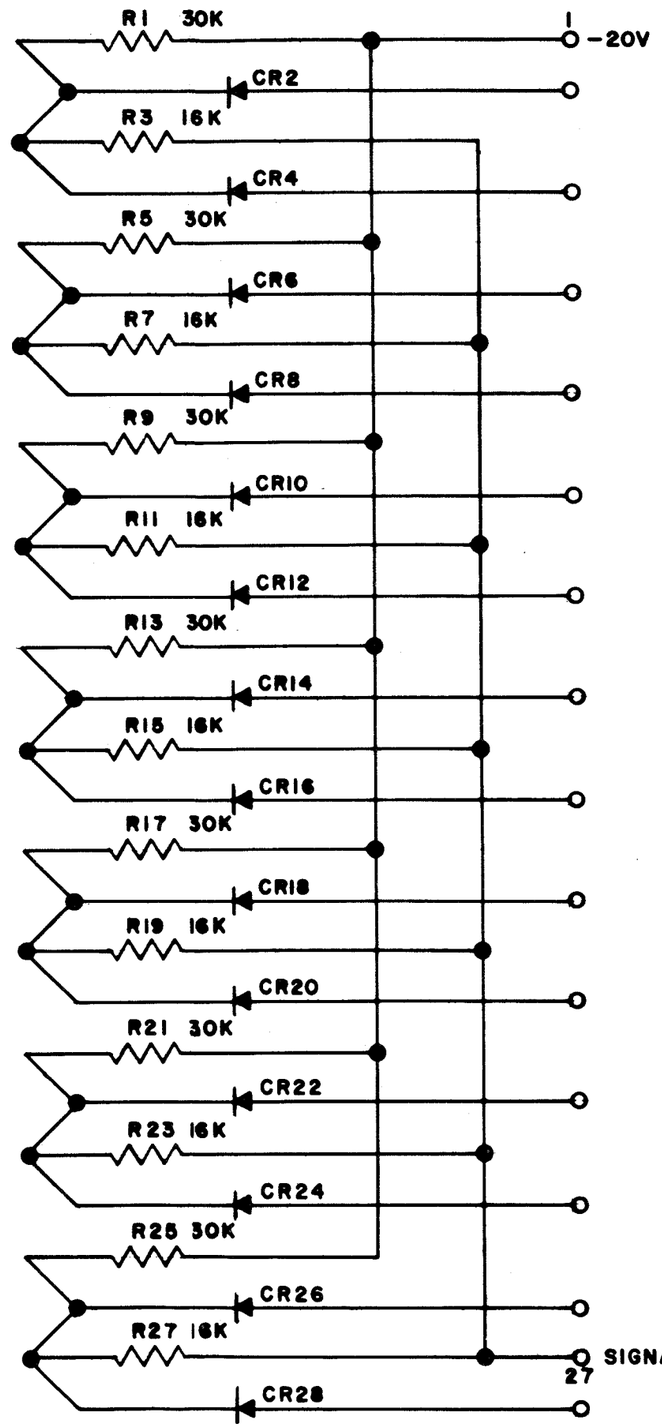
SUBMODULE TYPE "I_b", ISOLATOR

FIGURE 13

NOTE:
1 – ALL RESISTORS ARE CARBON COMPOSITION, $\frac{1}{4}$ WATT, $\pm$ 5%.

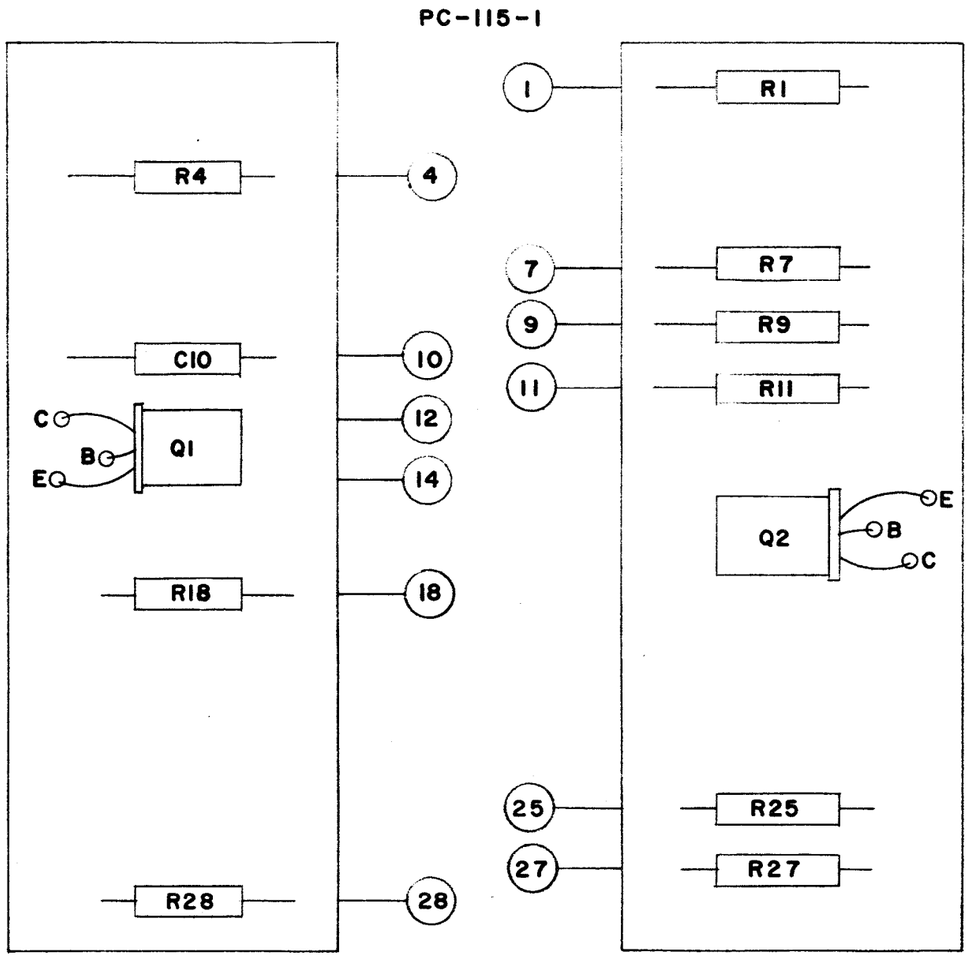
2 – ALL DIODES ARE IN270, GERMANIUM

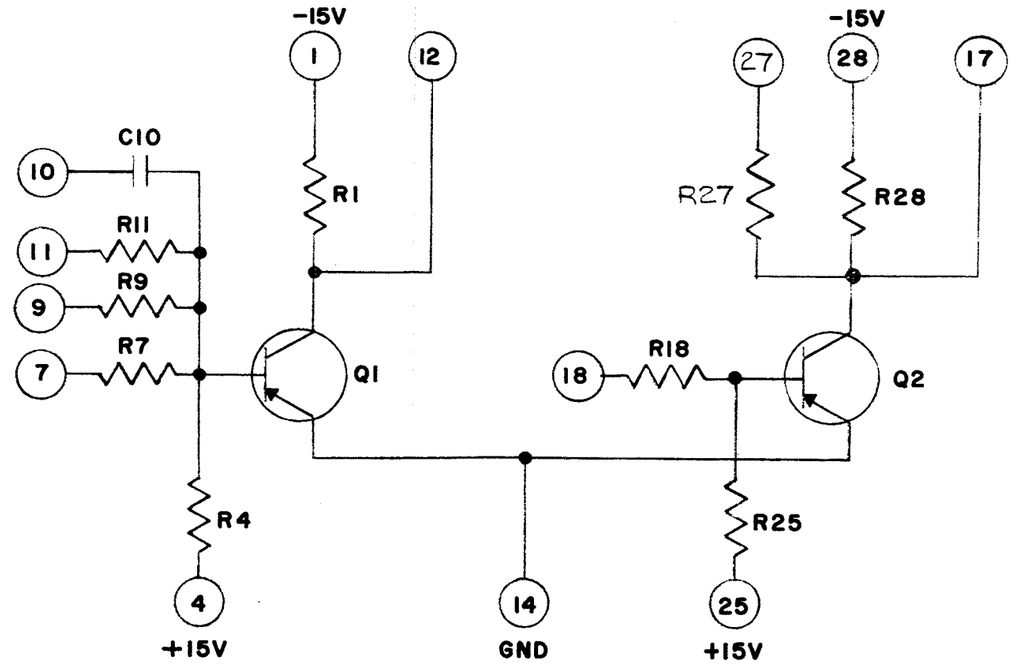




SUBMODULE, TYPE 603-S1, SPECIAL

FIGURE 14

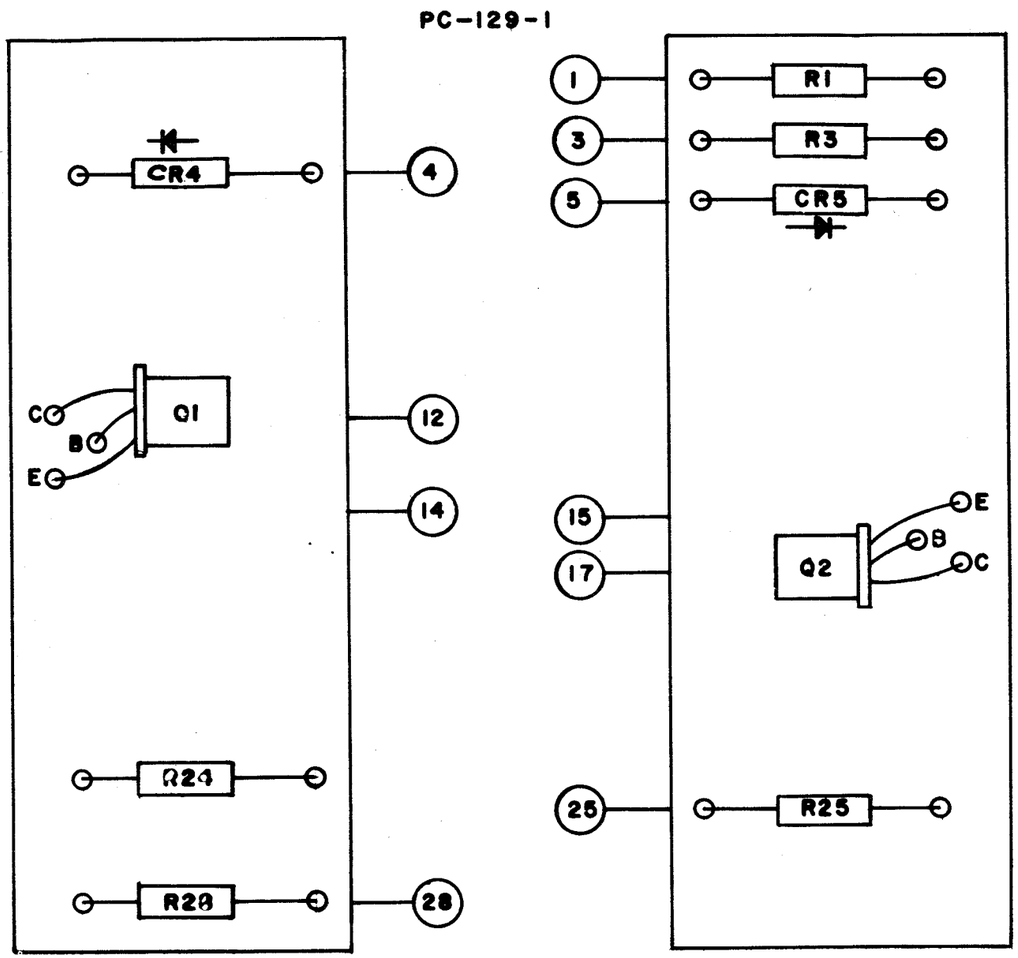


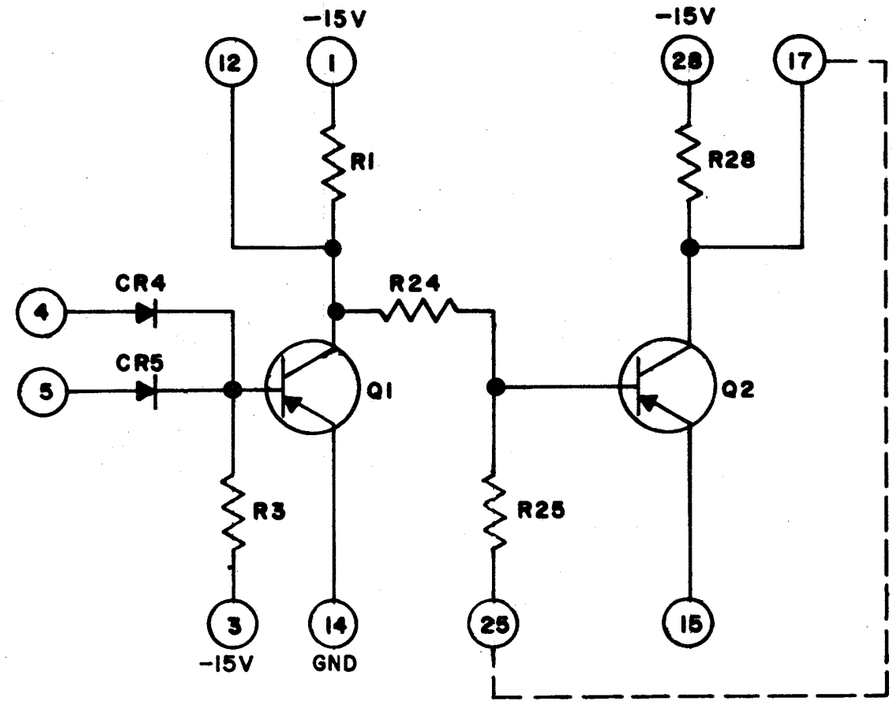


DESIGN VALUES		
PART Nº	DESCRIPTION	VALUE
R1	RESISTOR, CARBON, 1/2W, 5%	1K
R4	1/4W, 5%	120K
R7		10K
R9		10K
R11		10K
R18		47K
R25		470K
R27		10K
R28	RESISTOR, CARBON, 1/4W, 5%	16K
C10	CAPACITOR, DIPPED MICA	22MMF
Q1	TRANSISTOR	2N1300
Q2	TRANSISTOR	2N404

SUBMODULE, TYPE 603-S9 SPECIAL

FIGURE 16

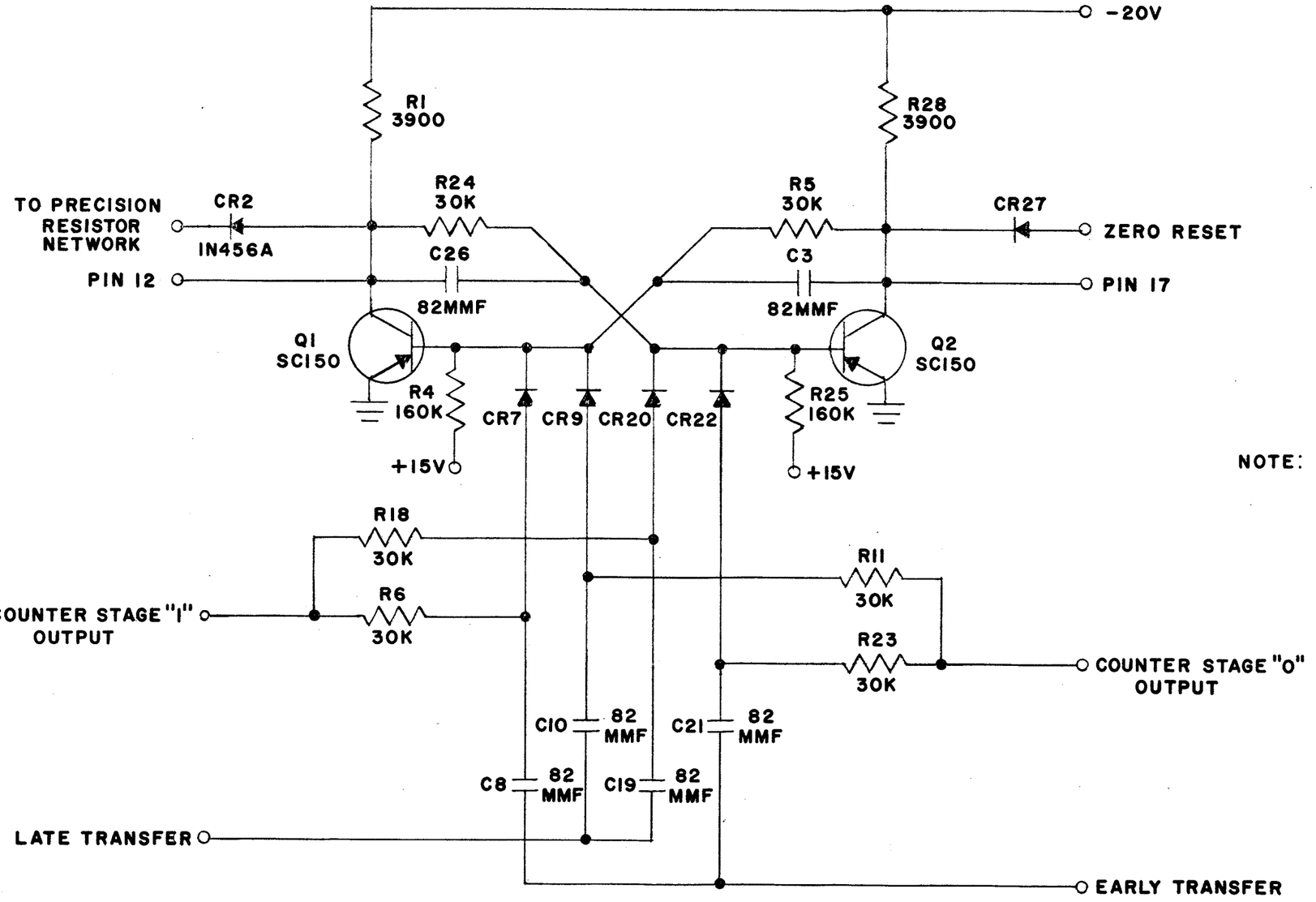




DESIGN VALUES		
Nº	DESCRIPTION	VALUE
R1	RESISTOR, CARBON, 1/4W, 5%	7500
R3	↕	43K
R24	↕	43K
R25	↕	160K
R28	RESISTOR, CARBON, 1/4W, 5%	7500
CR4	DIODE	IN270
CR5	DIODE	IN270
Q1	TRANSISTOR	2N404
Q2	TRANSISTOR	2N404

SUBMODULE, TYPE 603-S4, SPECIAL

FIGURE 17



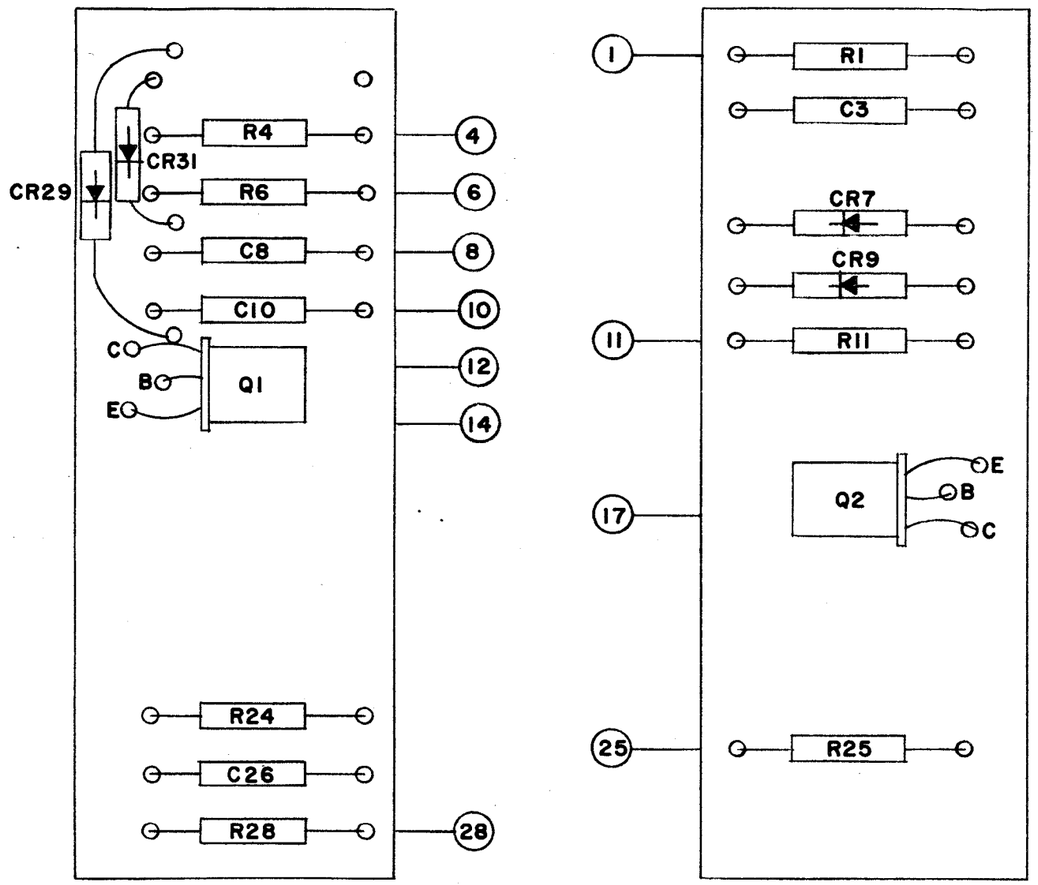
NOTE: UNLESS OTHERWISE SPECIFIED ALL DIODES ARE IN270.

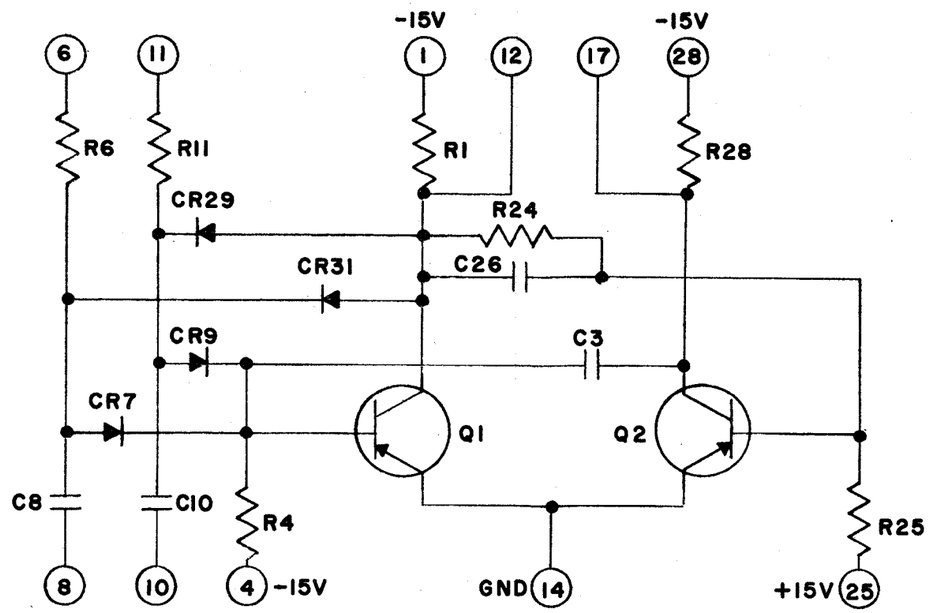
REGISTER STAGE, SCHEMATIC DIAGRAM

B1933

FIGURE 18

PC-116-1





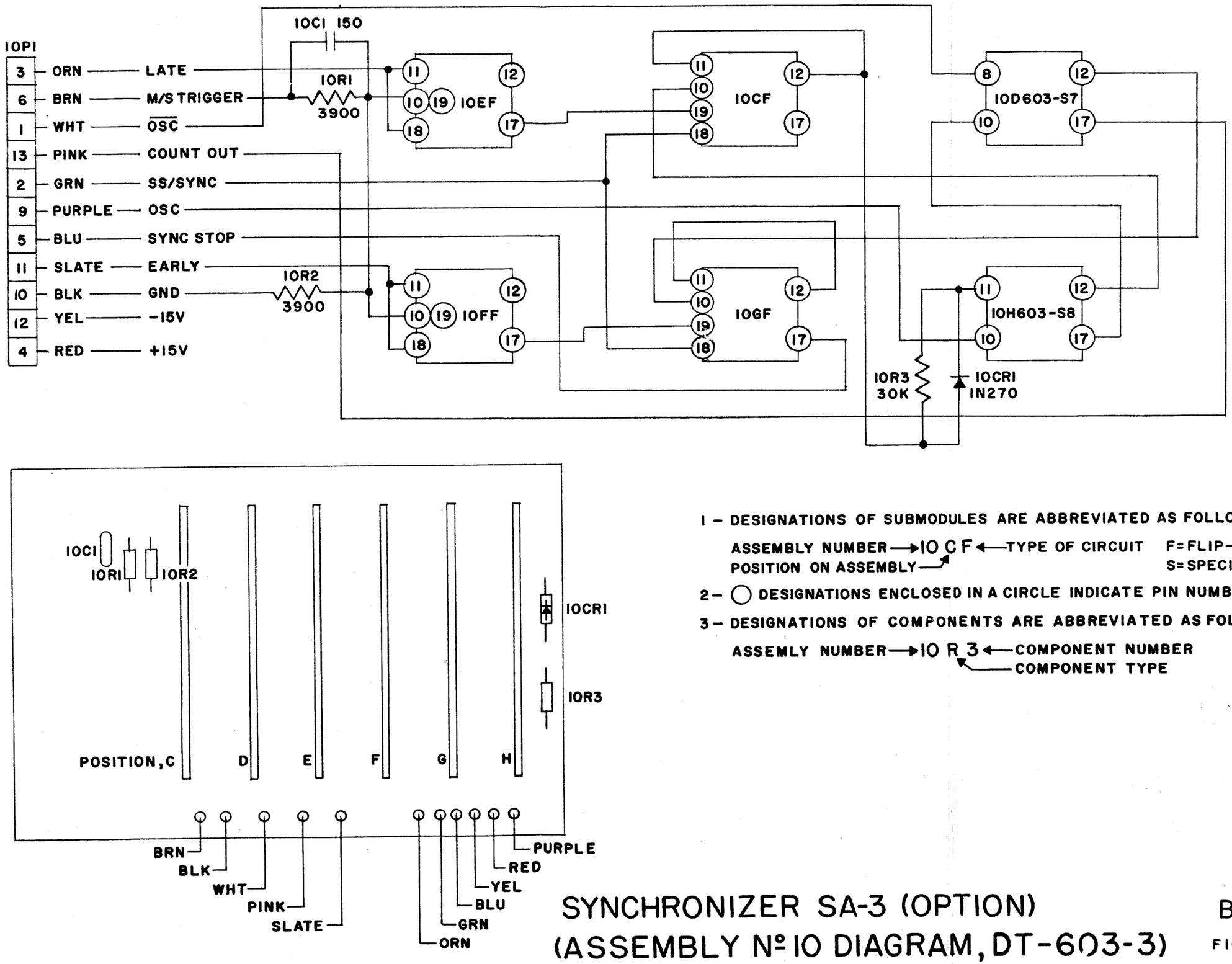
DESIGN VALUES				
Nº	DESCRIPTION		603-S7	603-S8
R1	RESISTOR, CARBON, 1/2 W, 5%		1K	1K
R4	↑ 1/4 W ↑		10K	10K
R6	↕ 1/4 W ↕		30K	OMIT
R11	↕ 1/4 W ↕		30K	NOTE 1
R24	↕ 1/4 W ↕		10K	10K
R25	↓ 1/2 W ↓		120K	120K
R28	RESISTOR, CARBON, 1/2 W, 5%		1K	1K
C3	CAPACITOR, MICA	CM15820J	82MMF	82MMF
C8	↑	CM15151J	150MMF	OMIT
C10	↓	CM15151J	150MMF	150MMF
C26	CAPACITOR, MICA	CM15820J	82MMF	82MMF
CR7	DIODE		1N270	OMIT
CR9	DIODE		1N270	1N270
CR29	DIODE		1N270	OMIT
CR31	DIODE		1N270	OMIT
Q1	TRANSISTOR		2N404	2N404
Q2	TRANSISTOR		2N404	2N404

NOTES:

1 – ON SUBMODULE 603-S8 A PIECE OF INSULATED BUSS IS SUBSTITUTED FOR RESISTOR Nº 11.

SUBMODULES, TYPE 603-S7 & 603-S8 SPECIALS

FIGURE 19



1 – DESIGNATIONS OF SUBMODULES ARE ABBREVIATED AS FOLLOWS,

ASSEMBLY NUMBER → 10 C F ← TYPE OF CIRCUIT (F = FLIP-FLOP, S = SPECIAL)
POSITION ON ASSEMBLY

2 – ◯ DESIGNATIONS ENCLOSED IN A CIRCLE INDICATE PIN NUMBERS.

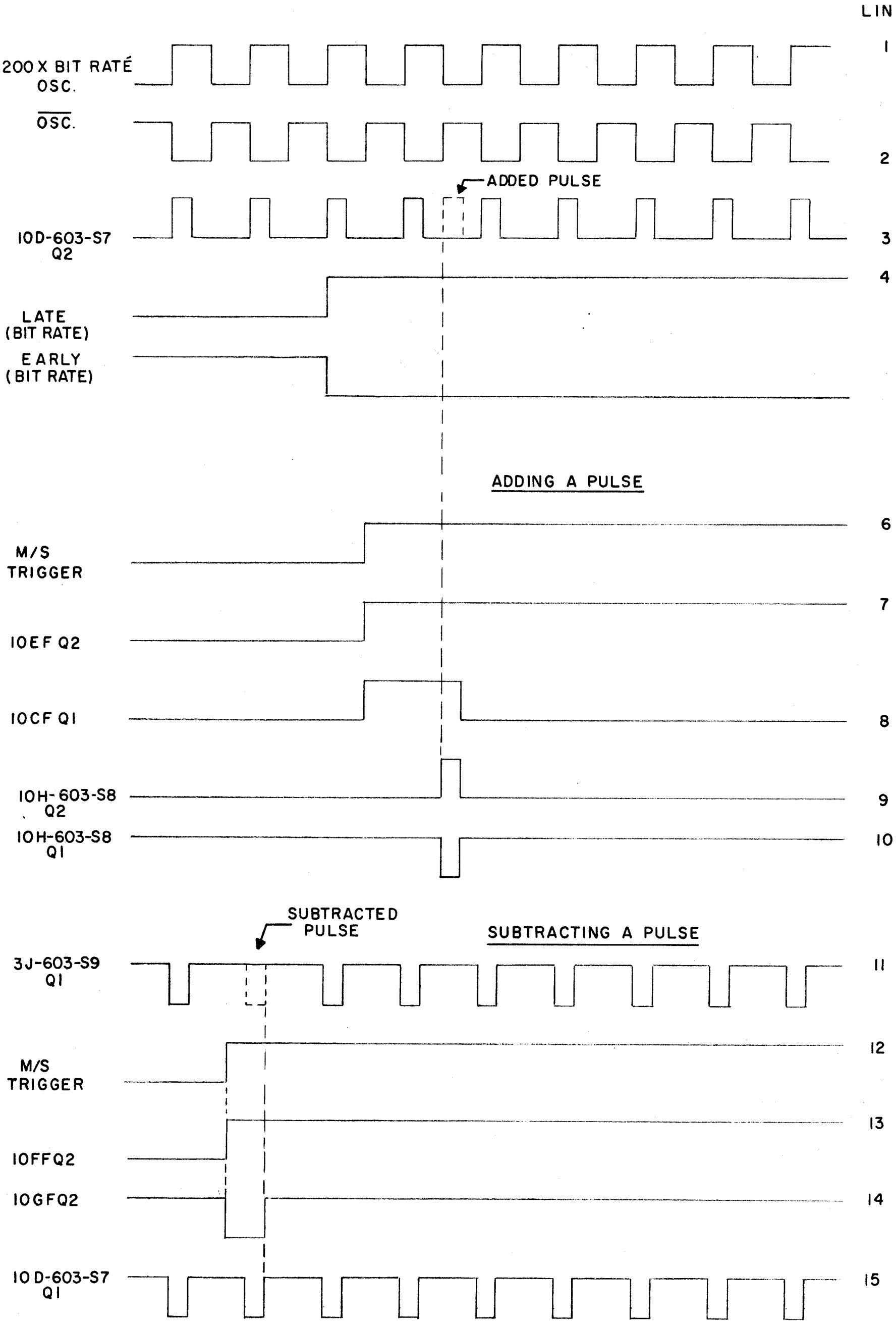
3 – DESIGNATIONS OF COMPONENTS ARE ABBREVIATED AS FOLLOWS,

ASSEMLY NUMBER → 10 R 3 ← COMPONENT NUMBER
COMPONENT TYPE

SYNCHRONIZER SA-3 (OPTION)
(ASSEMBLY Nº 10 DIAGRAM, DT-603-3)

B1931

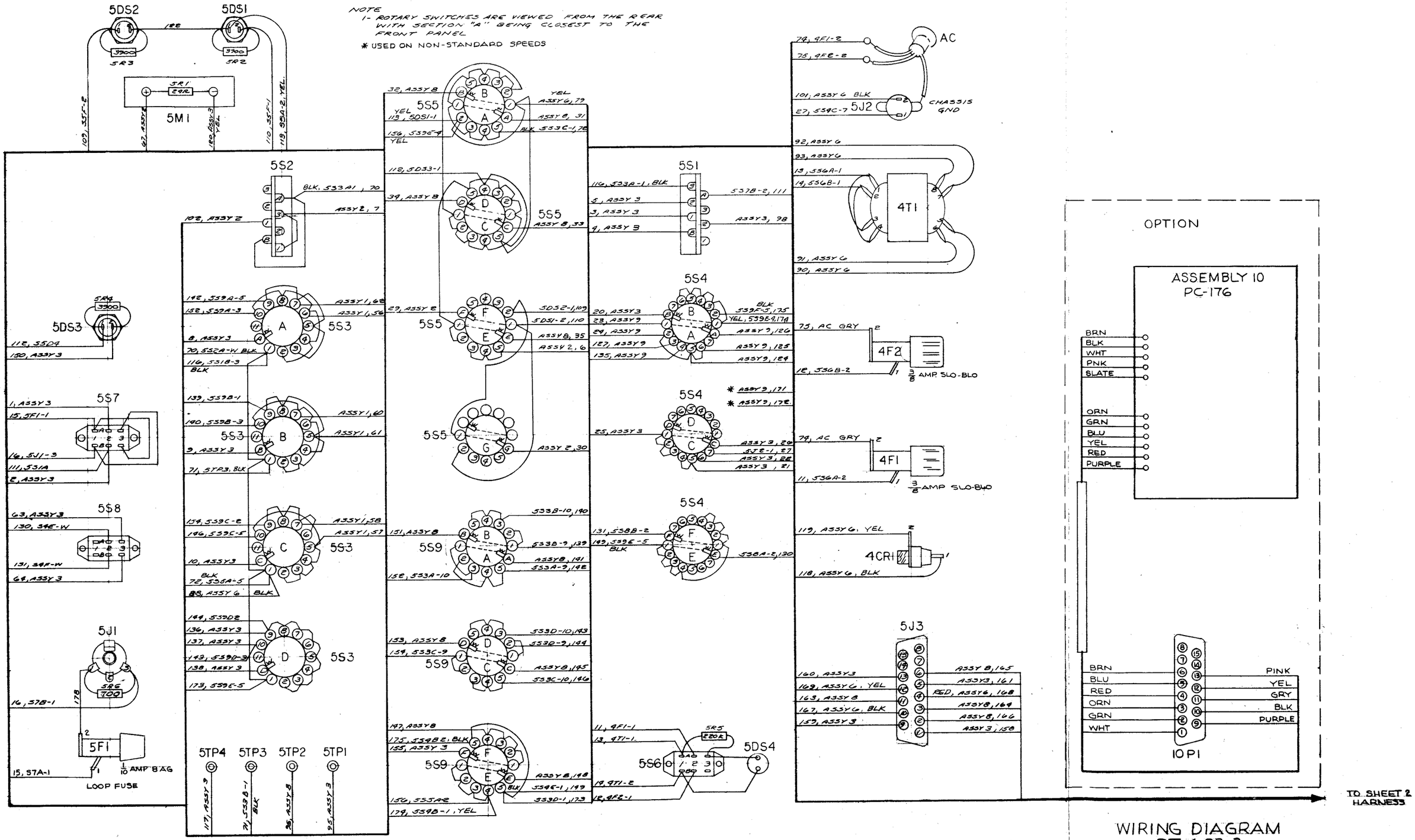
FIGURE 20



WAVEFORMS SYNCHRONIZER
ASS'Y 10

B1927

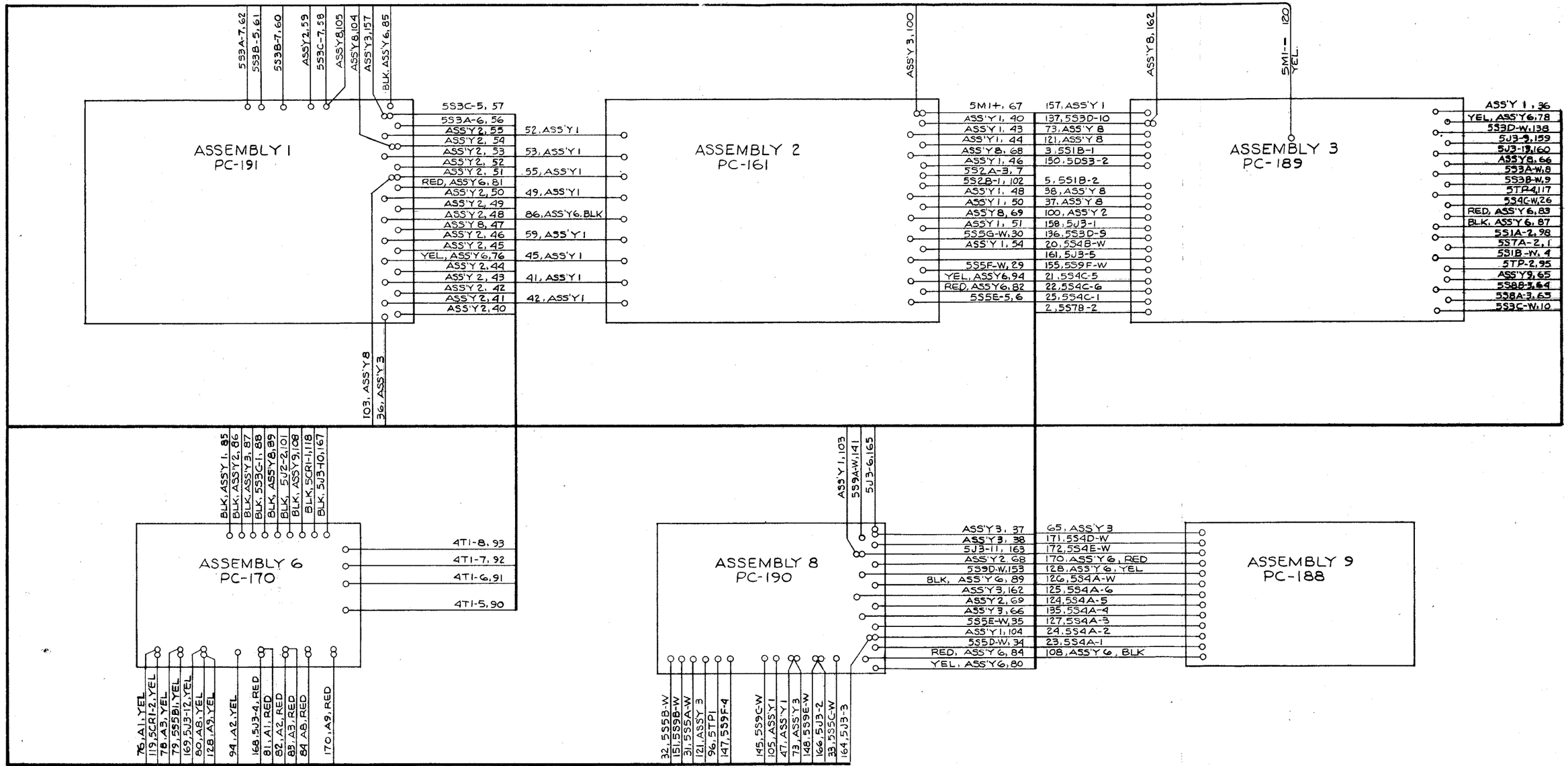
FIGURE 20B



WIRING DIAGRAM
DT-603-3
SHEET 1 OF 2

FIGURE 21

E-1913



WIRING DIAGRAM
DT-603-3
SHEET 2 OF 2

FIGURE 21

☆ U. S. GOVERNMENT PRINTING OFFICE: 1971-714-004/2541