TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS WITH PARTS LIST

ORGANIZATIONAL AND DEPOT

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RADIO TRANSMITTER T-827H/URT
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Chapter 3

STEWART-WARNER ELECTRONICS
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Functional Description

Chapter 6

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CHAPTER 3

FUNCTIONAL DESCRIPTION

3-1. INTRODUCTION

3-2. This chapter describes the major functions and principles of operation of the T-827H/URT in three levels of detail. The first is an overall description of the transmitter to the level of detail shown on the overall functional block diagram. The second level is a more detailed description of each of the functions, based on signal flow diagrams and concentrating on the functional operation of the principal assemblies and subassemblies involved in each function. Power distribution and control functions are also described with reference to the appropriate power distribution and control diagrams. The third level, based on schematic diagrams, is a description of detailed circuit operation of all electronic circuits which differ substantially from those described in NAVSHIPS 0967-LP-000-0120.

3-3. OVERALL FUNCTIONAL DESCRIPTION.

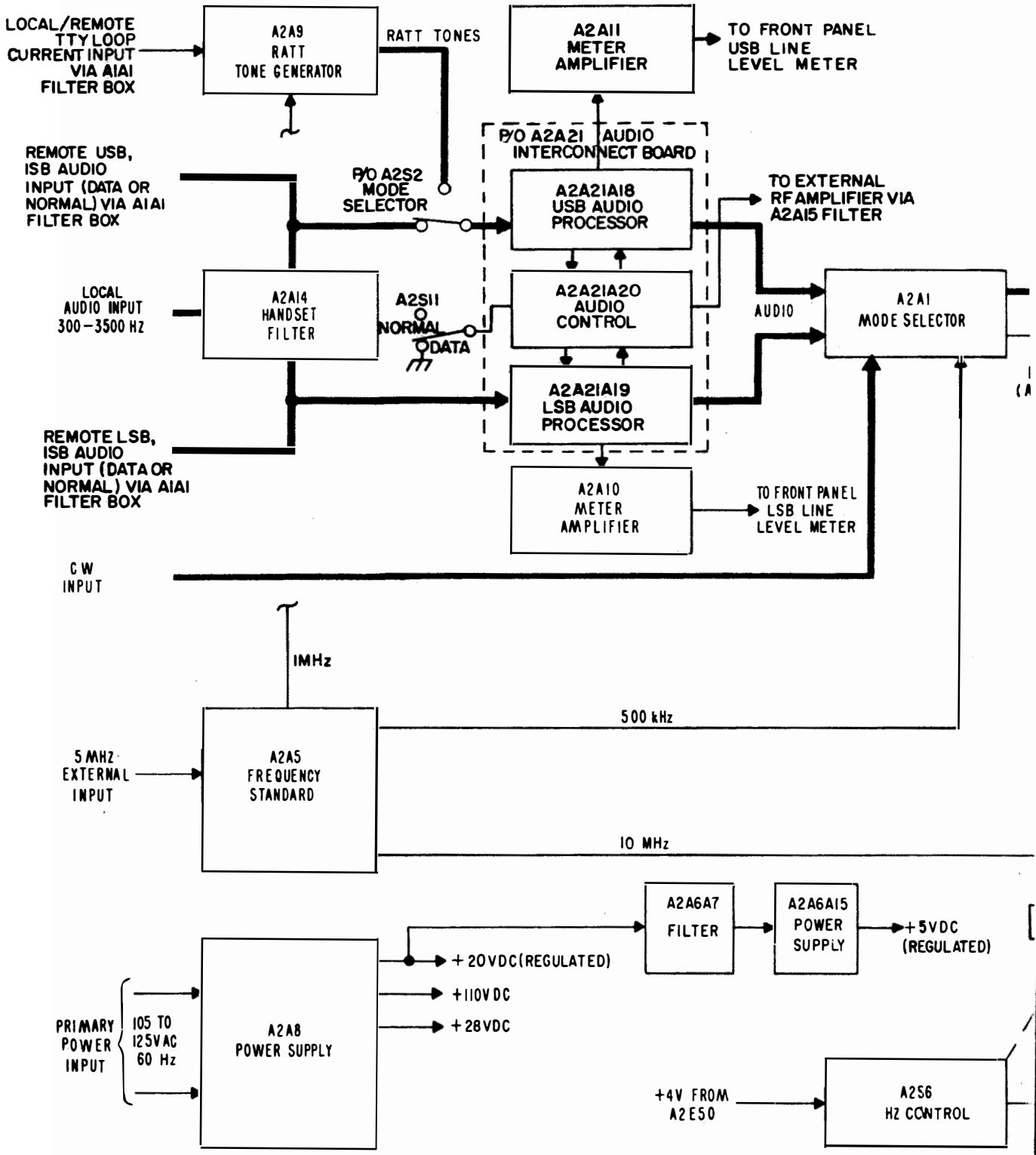
3-4. GENERAL. Figure 3-1 is an overall functional block diagram of the T-827H/URT. The arrangement of figure 3-1 and the text paragraphs follow the main signal flow through the T-827H/URT, for NORMAL and DATA transmissions. NORMAL refers to those control positions and circuits having to do with the transmission of voice, CW, and RATT. DATA refers to those control positions and circuits involved with Link-11 TADIL A transmission.

3-5. INPUT SIGNAL ROUTING. In the USB, AM, or ISB modes of operation, audio signals from external equipment are fed to Audio Processor A2A21A18 (audio inputs from a local microphone pass through Handset Filter Assembly A2A14). In the LSB or ISB modes, the audio signals are routed to Audio Processor A2A21A19 (again via A2A14 for local audio inputs). The input from teletypewriter equipment during RATT modes is sent to RATT Tone Generator Assembly A2A9, which converts the TTY loop current signals into audio frequencies representing a mark or space. One of two audio frequency pairs is selected by the front panel RATT SHIFT SELECT switch (item 11, figure 2-1). The RATT Tone Generator outputs are supplied to the Audio Processor A2A21A18 (USB channel). The USB and LSB audio processors process the input signals to provide a controlled-amplitude signal to Mode Selector Assembly A2A1. In the data mode the audio processors A2A21A18 and A2A21A19, together with the audio control A2A21A20, change the peak-to-average ratio of the data audio to optimize the transmitted signal at the antenna. After leaving the audio processors, data signals follow the same path as normal signals.

3-6. LINE LEVEL METERS. The input signal for Audio Processor A2A21A18 is also routed to Meter Amplifier Assembly A2A11, which drives the USB LINE LEVEL meter on the T-827H/URT front panel. Similarly, the front panel LSB LINE LEVEL meter is driven by the audio output signal from Meter Amplifier Assembly A2A10 which, in turn, is driven by the input signal for LSB Audio Processor A2A21A19.

3-7. MODE SELECTOR. Both audio input signals to the mode selector modulate a 500 kHz intermediate frequency (IF) carrier, which results in two double-sideband signals (with suppressed carriers). The double-sideband signals are separately filtered to remove the undesired sidebands. Mode gating, to select the USB and/or LSB output from the appropriate filter(s), is controlled by the front panel mode selector switch. During CW mode the local or remote CW key line ground is fed directly to a gated stage in the ode selector assembly A2A1, which passes the keyed 500 kHz to the IF Amplifier A2-A12. Compatible AM signals are generated in the AM mode by gating on a carrier signal which is injected into the IF amplifier A2A12 and added to the upper sideband signal.

3-8. IF AMPLIFIER. The modulated signal from Mode Selector Assembly A2A1 is amplified in IF Amplifier Assembly A2A12. Peak-


LOCAL/REMOTE TTY LOOP CURRENT INPUT VIA A1A1 FILTER BOX
A2A9 RATT TONE GENERATOR
RATT TONES
A2A11 METER AMPLIFIER
TO FRONT PANEL USB LINE LEVEL METER
P/O A2A21 AUDIO INTERCONNECT BOARD
REMOTE USB, ISB AUDIO INPUT (DATA OR NORMAL) VIA A1A1 FILTER BOX
P/O A2S2 MODE SELECTOR
A2A21A18 USB AUDIO PROCESSOR
TO EXTERNAL RF AMPLIFIER VIA A2A15 FILTER
LOCAL AUDIO INPUT 300-3500 HZ
A2A14 HANDSET FILTER
A2S11
NORMAL
DATA
A2A21A20 AUDIO CONTROL
AUDIO
A2A1 MODE SELECTOR
A2A21A19 LSB AUDIO PROCESSOR
REMOTE LSB, ISB AUDIO INPUT (DATA OR NORMAL) VIA A1A1 FILTER BOX
A2A10 METER AMPLIFIER
TO FRONT PANEL LSB LINE LEVEL METER
CW INPUT
1MHz
500 kHz
5 MHZ EXTERNAL INPUT
A2A5 FREQUENCY STANDARD
10 MHz
A2A6A7 FILTER
A2A6A15 POWER SUPPLY
+5VDC (REGULATED)
+20VDC(REGULATED)
+110VDC
+28VDC
PRIMARY POWER INPUT
105 TO 125VAC 60 Hz
A2A8 POWER SUPPLY
+4V FROM A2E50
A2S6 HZ CONTROL

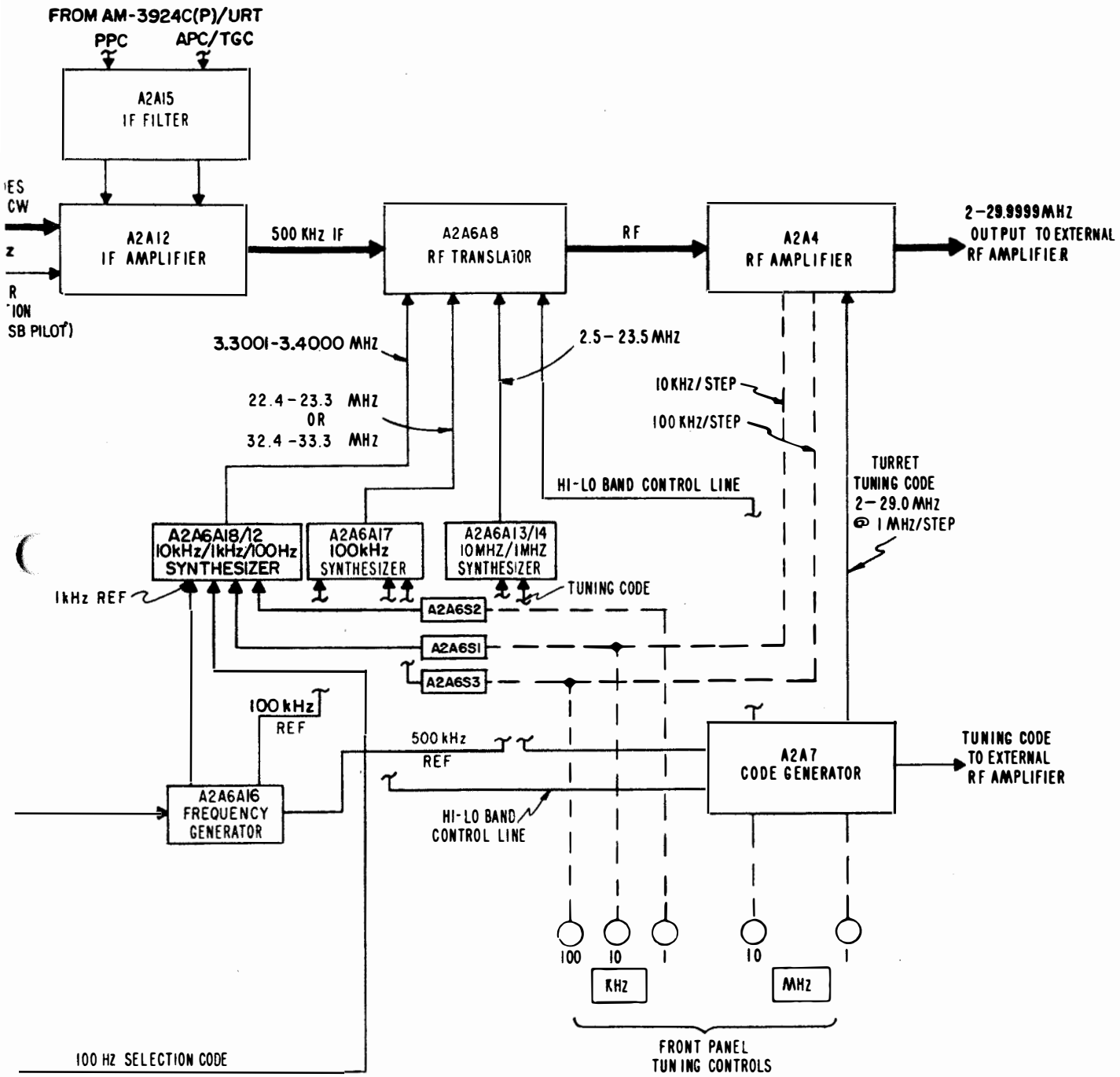


Figure 3-1. Radio Transmitter T-827H/URT, Overall Functional Block Diagram

power-control (PPC) and average-power-control (APC) voltages from the AM-3924C(P)/URT are used to control the stage gain. This prevents the T-827H/URT from overdriving the AM-3924C(P)/URT. The carrier signal for CW or AM modes is injected into the output of the first IF amplifier stage.

3-9. RF TRANSLATOR. Frequency conversion of the 500 kHz IF signal to the final rf output frequency is performed in three mixing operations in RF Translator Subassembly A2A6A8, which is a part of Translator/Synthesizer Assembly A2A6. Selection of the three specific mixing frequencies required for the conversion is accomplished by setting the front panel tuning controls. The injection frequency to the first mixer from 10 kHz/1 kHz/100 Hz synthesizer subassembly A2A6A12 ranges between 3.3001 and 3.4000 MHz. This results in a second IF of 2.8001 to 2.9000 MHz. The second IF is mixed with a 22.4 to 23.3000 MHz (lo-band) or 32.4 to 33.3 MHz (hi-band) injection frequency from the 100 kHz Synthesizer Subassembly A2A6A17. This produces a third IF which will range between 19.5 to 20.4999 MHz (lo-band) and 29.5 to 30.4999 MHz (hi-band). The third mixer receives a 2.5 to 23.5 MHz injection signal from 10 MHz/1 MHz Synthesizer Subassembly A2A6A13 and A2-A6A14. This produces a T-827H/URT rf output frequency in the range of 2.0 to 29.9999 MHz.

3-10. RF AMPLIFIER. The rf output from the third mixer stage is applied to RF Amplifier Assembly A2A4. Here the signal is amplified to produce the rf excitation to the AM-3924C(P)/URT. Selection of circuit components in the rf amplifier stages is accomplished via mechanical inputs from the 10 MHz and 1 MHz front panel controls. These generate a five-wire tuning code consisting of opens and grounds from Code Generator Assembly A2A7 and mechanical inputs from the 100 kHz and 10 kHz front panel controls.

3-11. FREQUENCY STANDARD. An external, stable, 5 MHz signal from the ship's frequency standard distribution system is normally supplied to Frequency Standard Assembly A2A5. This external 5 MHz is used as a reference for generation of the 1 MHz, 10 MHz and 500 kHz outputs. A 5 MHz, oven-mounted, crystal oscillator, within Frequency Standard Assembly A2A5, also provides a frequency standard to which all frequencies used in the T-827H/URT may be referenced. The external or internal 5 MHz frequency is converted to 10 MHz for use by Translator/Synthesizer Assembly A2A6, and to 500 kHz for use as the carrier intermediate frequency in the T-827H/URT. A 1 MHz output to the RATT Tone Generator provides for accurate reduction to audio tones. The 1 MHz output is also applied to the Translator Synthesizer connector to be used as a reference on earlier versions of Translator Synthesizers A2A6. The Frequency Standard may be operated in one of three modes: (1) INT/COMP - internal standard operation; flashing lamp indicates frequency error from external standard signal; (2) EXT NORMAL - operates on external standard with oven and internal oscillator off. The Frequency Standard will automatically switch to internal operation if external standard fails: (3) EXT STBY - operates on external standard with internal oscillator and oven on. The Frequency Standard A2A5 digital circuitry will automatically switch to internal operation if external standard fails.

3-12. FREQUENCY GENERATOR. The stable 10 MHz output from Frequency Standard Assembly A2A5 is applied to Frequency Generator Subassembly A2A6A16. Here, dividers provide the reference frequencies used in the three synthesizer circuits of Translator/Synthesizer Assembly A2A6.

3-13. FREQUENCY SYNTHESIZER. The frequency synthesizers employ phase-locked loops which compare the output frequencies with the reference frequency inputs. This ensures that the injection frequencies from the synthesizer subassemblies are accurate. The injection signals from the synthesizer subassemblies and the intermediate frequency output from IF Amplifier Assembly A2A12 are combined in RF Translator Subassembly A2A6A8. There, three mixing stages provide conversion of the 500 kHz IF signal to the desired rf output frequency. See paragraph 3-81.

3-14. Power Supply. Power Supply Subassembly A2A6A15 converts +20 Vdc from

Power Supply Assembly A2A8 (see pararaph 3-19) to the +5 Vdc used in the subassemblies of Translator/Synthesizer Assembly A2A6.

3-15. First Injection Frequency Generation. The injection frequencies used in the first frequency conversion in the mixer circuits are generated in 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12. The injection frequency is produced by a voltage controlled oscillator (VCO) in A2A6A12. The VCO is phase-locked to the 1 kHz reference signal from Frequency Generator A2A6A16. Programmable counters and frequency dividers in the A2A6A18 synthesizer subassembly establish the VCO frequency in response to the settings of the front panel 10 kHz, 1 kHz and 100 Hz controls. Any one of 1000 possible injection frequencies, spaced at 100 Hz intervals between 3.3001 and 3.4000 MHz, is then applied to the first mixer in RF Translator Subassembly A2A6A8.

3-16. Second Injection Frequency Generation. The injection frequencies used in the second frequency conversion are generated in 100 kHz Synthesizer Subassembly A2A6A17. The frequency at the output of A2A6A17 is between 22.4 and 23.3 MHz for lo-band operation, or between 32.4 and 33.3 MHz in hi-band. The front panel 100 kHz control establishes the output frequency of the VCO, which is phase-locked to the 100 kHz reference signal from Frequency Generator A2-A6A16.

3-17. Third Injection Frequency Generation. The 10 MHz/1 MHz Synthesizer Subassembly A2A6A13 generates the injection frequencies used in the third frequency conversion. One of seventeen injection frequencies between 2.5 and 23.5 MHz is produced in response to the setting of the front panel MHz controls. The injection frequency is applied to the third mixer in RF Translator Assembly A2A6A8.

3-18. CODE GENERATOR ASSEMBLY. Code Generator Assembly A2A7 produces three sets of five-wire tuning codes (opens and grounds) as determined by the settings of the front panel MHz controls. Separate tuning codes provide frequency band selection in the motor-driven turrets of the AM-3924C(P)/URT rf power amplifier and RF Amplifier Assembly A2A4. The third tuning code is applied to 10 MHz/1 MHz Synthesizer Subassembly A2A6A13. Here the injection signal required for final frequency conversion is selected by the action of the code in programming the divider network. Code Generator Assembly A2A7 also supplies a hi-lo band control signal to the A2A6A8 and A2-A6A17 subassemblies of Translator/Synthesizer A2A6.

3-19. POWER SUPPLY ASSEMBLY. Power Supply Assembly A2A8 produces three dc outputs. Two are unregulated (28 Vdc and 100 Vdc). The third is a regulated +20 Vdc. The +28 Vdc is applied to the front panel kHz and MHz indicator lamps when the mode selector switch is set to STDBY (or any operating mode). The +28 Vdc is also reduced and regulated to provide the +20 Vdc supply.

3-20. MAJOR FUNCTIONAL DESCRIPTION.

3-21. GENERAL. The T-827H/URT performs the following eleven major functions:

1. Audio amplification and modulation in normal operation (voice modes).
2. Audio amplification and processing in data operation.
3. Tone generation and modulation (RATT modes).
4. Carrier reinsertion (CW, AM and SSB pilot carrier modes).
5. IF amplification and level control.
6. IF-to-rf translation.
7. Rf amplification.
8. Frequency synthesis.
9. Standard frequency generation and distribution.
10. Power distribution.
11. Control.

The first nine of these functions are discussed in functional descriptions of the various assemblies and subassemblies involved in the generation of each function. These descriptions are based on the signal flow diagrams in Chapter 5. As far as practicable, circuits in the main signal-flow path are described first (in signal-flow order). This is followed by descriptions of the assemblies involved with frequency synthesis and standard frequency generation. Power distribution is described

with reference to the power distribution diagrams in Chapter 5 for the primary ac power and for the dc voltages in the T-827H/URT. The Control Function is described with reference to the tuning control diagram and some of the schematic diagrams in Chapter 5.

3-22. NORMAL AUDIO PROCESSING - VOICE MODES (Figure 5-1, Sheet 1). In voice modes of operation, audio in the frequency range of 300 to 3500 Hz is applied to the T-827H/URT to modulate a 500 kHz intermediate carrier frequency. The assemblies involved in this portion of the signal flow are: Filter Box Assembly A1A1 for remote audio inputs or Handset Filter Assembly A2A14 for local audio inputs; Audio Interconnect Board A2A21; Audio Processor A2A21A19 for LSB modes or Audio Processor A2A21A18 for USB modes; and Mode Selector Assembly A2A1. The 500 kHz IF output signal from the A2A1 assembly is fed to IF Amplifier Assembly A2A12. The audio signal inputs are monitored by front panel LSB Line Level and USB Line Level meters. These receive the signals from the A2A21A19 and A2A21A18 assemblies via meter Amplifier Assemblies A2A10 and A2A11 respectively.

3-23. The normal audio amplification signal flow path for LSB and USB modes appears in Figure 5-1, Sheet 1. The LSB modes include LSB, the LSB portion of ISB, and the LSB portion of ISB/RATT. The USB modes include USB, the USB portion of ISB/RATT, AM, and RATT.

3-24. NORMAL LSB MODES. When front panel LOCAL/REMOTE switch A2S1 is at REMOTE, the remote or auxiliary 600 ohm voice input signals are applied through capacitors A1A1C8 and A1A1C11, A2S1-A-R contacts 12 to 2, and A2S1-A-F contacts 7 to 9, normally closed contacts of A2A21K1 to LSB input transformer A2A21T1 primary. A2A21T1 couples the input to LSB Audio Processor A2A21A19. If A2S1 is at LOCAL, the microphone audio from front panel HANDSET connector A2J1 is supplied to A2A21A19 through Handset Filter Box A2A14, A2S1-B-F contacts 1 to 10, Mode Selector Switch A2S2-A-R contacts 8 to 9, and secondary terminal 5 of A2A21T1 when A2S2 is at LSB or ISB/RATT. The path from A2S1-B-F contact 10 to A2A21T1-5 is completed through A2S1-B-R contacts 12 to 9 and LOCAL ISB HANDSET switch A2S9 contacts 5 and 6 when A2S2 is at ISB and A2S9 is at LSB.

3-25. During NORMAL operation relay A2A21A19K1 is not energized. Therefore, the audio input signals are coupled through A2A21T1 to A2A21A19U2, where they are amplified. In addition, the A2A21A19 processor circuitry provides for amplitude control so that the maximum audio output level is limited before being sent to the Mode Selector Assembly A2A1 to modulate the 500 kHz IF. If the input signal level exceeds the standard audio reference by more than 20 dB, the A2A21A19 circuitry provides for clipping the excessive peaks. This function is performed by the network comprising DC amplifier A2A21A19Q2, threshold detector A2A21A19CR1 and compressor A2A21A19Q1. OUTPUT LEVEL potentiometer A2A21A19R8, THRESHOLD potentiometer A2A21A19R4, ATTACK time potentiometer A2A21A19R11, and DECAY time potentiometer A2A21A19R14 form a gain control circuit which acts to limit the peak excursions of the voice wave. Compressor A2A21A19Q1 and A2A21A19R5 form a variable voltage divider to control signal level to constant gain amplifier A2A21A19U2. Also, an output from A2A21A19-S goes to LSB Meter Amplifier Assembly A2A10, which drives the front panel LSB LINE LEVEL meter. The meter switch enables selection of a +10 dB range for suitable scaling.

3-26. NORMAL USB MODES. The audio from the remote or auxiliary 600-ohm input for the USB, AM, or USB portion of the ISB inputs to the T-827H/URT appears at capacitors A1A1C10 and A1A1C34. From here it goes through LOCAL/REMOTE switch A2S1-A-R contacts 8 to 10 and 4 to 6, Mode Selector Switch A2S2-D-F and A2S2-C-R, and the primary of USB input Transformer A2A21T2, where it is coupled to the USB Audio Processor A2A21A18.

NOTE

Switch connections for the various positions of mode selector switch A2S2 are shown in note H of figure 5-1.

3-27. The local microphone audio output to the USB audio processor is fed to Handset Filter Box A2A14. From there, it goes to LOCAL/REMOTE Switch A2S1-B-F, Mode Selector Switch A2S2-B-R, and LOCAL ISB HANDSET Switch A2S9 (ISB mode only). The remainder of the signal flow for USB-Normal operation parallels that for LSB-Normal operation, previously described. Signal action in the USB Audio Processor A2A21A18, Meter Amplifier Assembly A2A11 and USB LINE LEVEL Meter A2M2 is identical to that of the LSB components on the diagram.

3-28. DATA AUDIO PROCESSING (Figure 5-1, Sheet 2). One major difference between NORMAL and DATA operation is the source of the modulating audio and the type of intelligence carried. In the DATA mode of operation differential phase shifted audio tones from external equipments are applied to the T-827H/URT. After amplification and processing, these tones modulate a 500 kHz intermediate frequency carrier. The data audio tones represent multiplexed digital data from a peripheral computer which stores telemetry inputs. The assemblies involved in the signal flow of the tones are Filter Box Assembly A1A1; Audio Interconnect Board A2A21; Audio Processor A2A21A19 (LSB Modes) or Audio Processor A2A21A18 (USB Modes); and Mode Selector Assembly A2A1. After being received in the Audio Processor Assembly A2A21A19 or A2A21-A18, the data LSB or USB audio signals undergo various processing, including amplification. The processed data audio signals are fed to Mode Selector Assembly A2A1. From this point, the signal flow through the T-827H/URT in DATA is uniform for both DATA and NORMAL operation. The data audio also passes to Meter Amplifier Assembly A2A10 (LSB) or A2A11 (ISB) for monitoring by front panel LSB or USB LINE LEVEL meters A2M1 or A2M2. In data operation, only USB, LSB and ISB settings of mode selector switch A2S2 are valid. Other settings of this switch will cause failure of communications (though the radio equipment will not be damaged through such error).

3-29. DATA TONE INPUTS. Data tone inputs can be accepted via Remote/Auxiliary connectors A1A1J4, A1A1J5, A1A1J6, or via Data Audio connector A1A1J8. The first of these arrangements requires that terminals A2A21E43 through A2A21E50 be jumpered as indicated by the dotted lines connecting these terminals in figure 5-1, sheet 2. The second arrangement requires that these jumpers be removed. LSB data tones are passed to A2A21XA19 pin F/6 and pin H; USB data tones are passed to A2A21XA18 pin F/6 and pin H. Since USB and LSB audio processing are identical, except for reference designations of components involved, only LSB signal flow is described.

3-30. LSB audio processor A2A21A19 amplifies the LSB data audio tones received on pins A2A21XA19-F/6 and A2A21XA19-H in variable gain stage A2A21A19U1B to a standard level for clipping stage A2A21-A19U1A. This clipping stage removes the amplitude peaks of the data audio to maintain proper transmitted peak to average power output. The voltage divider consisting of A2A21A19R29 through A2A21A19R32 is connected to normally open contacts of A2-A21A19K1. In SSB operation, the voltage divider sets the proper level to the input of the common audio amplifier A2A21A19U2 shared by normal audio. In the ISB mode, the voltage divider reduces the audio level an additional amount in order to achieve proper output power levels. In DATA operation, the setting of DATA/NORMAL switch A2S11 to DATA position energizes relay A2A21A19K1, connecting relay terminals A2A21A19K1-2 and 3. The result is that the output of the data audio processor, comprising the audio control amplifier A2A21A19U1B and the amplitude control circuitry of A2A21A19-U1A, A2A21A19Q3, and A2A21A19Q4 and associated components, is fed to the meter circuits and to audio amplifier A2A21A19U2. Amplification and control takes place at A2A21A19U2 as described in paragraph 3-25. USB data tones are processed in exactly the same manner by A2A21-A18.

3-31. AUDIO CONTROL A2A21A20 (Figure 5-1, Sheet 3). The Audio Control Assembly A2A21A20 provides system supply and control functions for data operation. These functions are: (1) keying of the T-827H/URT and AM-3924C(P)/URT; (2) transmitter gain control (TGC) enable, TGC capacitor control, and TGC reset; (3) ISB ground, and (4) +15 Vdc and +5 Vdc supplies.

3-32. Keying. Data keying of the T-827H/URT and AM-3924C(P)/URT is accomplished by application of +6 Vdc to any of diodes A2A21A20CR14, A2A21A20CR15, A2A21A20CR16, and A2A21A20CR20. The resultant logic low at the collector of A2-A21A20Q10 is then applied, via contacts 7 and 8 of energized relay A2A21A20K2, to pin 4 of connector A2A21A20P1 to key the AM-3924C(P)/URT. Relays A2A21A20K1 and A2A21A20K2 are controlled by DATA/NORMAL switch A2S11 on the T-827H/URT front panel. In the NORMAL position of A2S11, A2A21A20K1 and A2A21A20K2 remain unenergized, allowing the CW/RATT keyline to pass through from A2A21A20P1-5 to A2A21-A20P1-E, and the ground keyline to pass through from A2A21A20P1-D to A2A21A20-P1-4. When A2S11 is switched to the DATA position, A2A21A20K2 provides a ground keyline to the AM-3924C(P)/URT, as previously described. A2A21A20K2 also grounds A2A21A20P1-D, which keeps the T-827H/URT keyed constantly. Energized relay A2A21A20K1 allows keying of the system via A2A21A20CR20 by a +6 Vdc data key signal fed through the CW/RATT keyline at the transmitter switchboard connector 1A2A1J2-S of the power amplifier.

3-33. TGC Functions. TGC enable and TGC capacitor control are initiated through output signals on pins L and 17 of A2A21A20P1 when the output of wired "NAND" A2A21-A20U2 is a logic high. This condition occurs when input pins 5, 9, 11, and 13 of A2A21-A20U2 are all logic low. As described earlier, input pin 9 is low as a result of switch A2A21A20Q10. Pins 5 and 13 are low due to a ground from the DATA/NORMAL switch when in the DATA position. Pin 11 is held low by the action of switch A2A21A20Q12 on the +20V input at A2A21A20P1-12 during the antenna coupler tune cycle. Also, during data transmission, the TADIL A audio signal at A2A21A20P1-M is rectified and amplified by A2A21A20U3 and A2A21A20Q11. Its presence keeps retriggerable A2A21A20U6 in the on state, and thus A2A21A20U6 low. When pins 9, 11, and 13 of A2A21A20U2 are all low, the output of A2A21A20U2 goes high for TGC enable (A2A21A20P1-L), and -15 Vdc is applied to A2A21A20P1-17 for TGC capacitor control. The output high of A2-A21A20U2 may be inhibited by an interlock function. If +20 Vdc or +28 Vdc is not present at A2A21A20P1-11 and A2A21A20P1-13, respectively, switch circuit A2A21A20Q9 and A2A21A20Q13 grounds the output of A2A21A20U2, and thereby prevents TGC enabling.

3-34. TGC reset occurs at system turn-on, or when the DATA/NORMAL switch is turned to DATA, or when any frequency control on the T-827H/URT is changed. At system turn-on, the base of A2A21A20Q5 senses the arrival of +5 Vdc and, through A2A21-A20Q6, causes reset of the power control system. When the data mode is selected at DATA/NORMAL switch A2S11, a ground is applied to A2A21A20P1-10, which, in turn, applies a pulse through the inverter of A2-A21A20U2 (pin 5 to pin 6). This logic high is coupled through A2A21A20C6, and inverted by A2A21A20Q6 to appear as a logic low at A2A21A20P1-15. Switching of any frequency control on the T-827H/URT provides a ground pulse at A2A21A20P1-T. This causes switches A2A21A20Q1 and A2A21A20Q2 to generate a power amplifier ground pulse at A2A21A20P1-16 for use by the antenna coupler. Additionally, switch A2A21A20Q6 generates a logic low at A2A21A20P1-15 to cause the power control system to reset itself at the new frequency.

3-35. ISB Ground. Since the average rf power output in ISB operation (USB and LSB both operating) must be reduced from 200 watts to 100 watts to limit rf peak power, the following occurs: Selection of ISB by Mode Selector Switch A2S2 causes a ground to appear at A2A21A20P1-U. Relay A2A21-A20K3 is energized, and transmits ISB grounds to Audio Processor A2A21A20A18 and A2A21A20A19 to reduce the audio drive to the modulators. The ISB ground is applied to voltage dividers R29 through R32 on the A2A21A18 and A2A21A19 boards. The voltage divider on each board forms a 6 dB voltage attenuator.

3-36. Power Supply. Regulated +15 Vdc and +5 Vdc are provided for use on assemblies A2A21A18, A2A21A19, and A2A21A20 by means of the voltage regulator A2A21A20-Q14 - A2A21A20CR23 (for +15 Vdc), and by voltage regulator A2A21A20U7 (for +5 Vdc).

3-37. AUDIO MODE GATING AND MODULATION (Figure 5-1, sheet 1). Due to the symmetrical designs of circuitry immediately succeeding the audio processor assemblies A2A21A19 and A2A21A18, only the LSB flow out of LSB audio processor A2A21A19 will be described. These paragraphs are common to DATA and NORMAL operation.

3-38. The LSB or ISB output audio from Audio Processor A2A21A19 appears at E2 of LSB balanced modulator A2A1A2. The 500 kHz standard frequency is also supplied to balanced modulator A2A1A2 through gated amplifier A2A1A4Q2. Amplifier A2A1A4Q2 is enabled by +20 Vdc during LSB operation. The 500 kHz standard frequency is gated into A2A1A4Q2 by diode A2A1A4CR1. This gating diode is enabled by +20 Vdc from the mode selector switch and the +20 Vdc (during transmit) from the transmit-receive relay A2K3. The enabling voltages are applied to A2A1A4CR1 through individual voltage dividers so that the diode is forward biased during all modes of operation except CW. In the CW mode, A2A1A4CR1 is disabled to prevent the 500 kHz frequency standard input from entering gated amplifier A2A1A4Q2.

3-39. The 500 kHz output from A2A1A4Q2 drives tuned transformer A2A1A4T2. The output of A2A1A4T2 appears at E4 of LSB balanced modulator A2A1A2. A2A1A2 is a conventional, balanced-bridge modulator which modulates the input audio onto the 500 kHz carrier IF signal to produce double sideband modulated signals. The 500 kHz carrier is suppressed by adjustable balance controls in the circuitry. The output from A2A1A2, applied to isolation transformer A2A1T1, consists of the upper and lower sideband signals produced when the 500 kHz carrier mixes with the LSB audio. The 500 kHz carrier and the audio are suppressed in the balanced modulator.

3-40. The output from isolation transformer A2A1T1 is applied to isolation amplifier A2A1A3Q1. A2A1A3Q1 is enabled by +20 Vdc from the mode selector switch in the LSB and ISB modes of operation. Isolation amplifier A2A1A3Q1 drives LSB filter A2A1FL1. The narrow passband of A2A1FL1 removes the undesired upper sideband from the double-sideband output, and further suppresses the 500 kHz carrier. The output of A2A1FL1 is applied to A2A1A5 which buffers the upper and lower sideband filters. The output of A2A1A5 at E6 is the modulated LSB signal which is passed to IF Amplifier Assembly A2A12.

3-41. LSB CARRIER BAL potentiometer A2A1A2R3 and the LSB CARRIER BAL capacitor A2A1A2C4 are used to balance the resistance and reactance in the LSB balanced modulator. The resistive and reactive balance must be proper to maintain a high degree of carrier suppression. Components A2A1A1R3 and A2A1A1C4 accomplish the same adjustment for the USB balanced modulator.

3-42. The 500 kHz carrier from Frequency Standard Assembly A2A5 is gated through A2A1A4CR1, amplifier A2A1A4Q1, transformer A2A1A4T1, and into the USB balanced modulator A2A1A1. Isolation transformer A2A1T2 drives isolation amplifier A2A1A3Q2, which drives the USB filter A2A1FL2. Isolation amplifier A2A1A3Q2 is enabled by +20 Vdc from mode selector switch A2S2 in the USB, AM, ISB, and RATT modes of operation. The narrow passband of A2A1FL2 removes the undesired LSB modulation product, and further suppresses the 500 kHz carrier. The output of A2A1FL2 is applied to A2A1A5, which buffers the upper and lower sideband filters. The output of A2A1A5 at E6 is passed to IF Amplifier Assembly A2A12.

3-43. TONE GENERATION AND MODULATION (RATT MODES). (Figure 5-2). In the RATT and ISB/RATT modes of operation a local or remote teletypewriter loop current input is applied to the T-827H/URT and is converted to an audio tone. Two of four possible audio tones, representing mark and space inputs, are generated in response to the loop current input and the position of the front panel RATT SHIFT SELECT switch. The audio tones are then amplified and processed in the same manner as the voice signals in the USB mode of operation. The assemblies involved in the signal flow for RATT tone generation and modulation are: Filter Box A1A1; RATT Tone Generator A2A9; Audio Processor A2A2A18; and mode Selector A2A1.

3-44. In the RATT mode, the teletypewriter loop current signal is applied through local input capacitors A1A1C48, A1A1C49 or remote input capacitors A1A1C22 and A1A1-C38 to the front section of LOCAL/REMOTE switch A2S1, contacts 1 and 5. Here it is directed to RATT Tone Generator Assembly A2A9 through A2R8. The input signal is then applied through polarity protection diode A2A9A1CR1 and optoelectronic coupler A2-A9A1U1.

3-45. A mark signal input (5 to 75 mA) provides the turn-on bias for optoelectronic coupler A2A9A1U1. A2A9A1U1 provides line isolation between the teletypewriter loop current lines and the tone generation circuits. Zener diode A2A9A1CR3 shunts optoelectronic coupler A2A9A1U1 so as to limit A2A9A1U1 current to 20 mA. A space signal input (no current flow) provides no bias current and therefore A2A9A1U1 stays off. Resistor A2R4, on the T-827H/URT main frame, must be connected in shunt across the teletypewriter input terminals for input loop currents in excess of 75mA in LOCAL operation. This is done by connecting A2E7 to A2E4.

3-46. Optoelectronic coupler A2A9A1U1 biases buffer amplifier A2A9A1U6A on or off in response to the teletypewriter mark and space signal inputs. The output of buffer amplifier A2A9A1U6A is applied to gates A2A9A1U6B, A2A9A1U6D and divider A2-A9A1U2.

3-47. A2A9A1Q1 and A2A9A1Q2 amplify the 1 MHz input from Frequency Standard A2A5 via A2A9P1 pin 7 to proper logic levels for divider A2A9A1U2. Dividers A1A9A1U1-U3 divide the 1 MHz to provide precise output frequencies as a function of mark/space inputs and the SHIFT SELECT switch position.

3-48. When the RATT SHIFT SELECT switch is in the 850 Hz position dividers A2-A9A1U2, -U3, -U4 are set to divide the 1 MHz input by 317 for a mark condition and by 206 for a space condition. The proper preset inputs to the dividers are set by A2-A9A1U6A, A2A9A1U6B, A2A9A1U6D and A2A9A1U5B. When the RATT SHIFT SELECT switch is in the 170 Hz position, the dividers A2A9A1U2, -U3, -U4 are set to divide by 261 for a mark condition and by 240 for a space condition. A2A9A1U5A serves to divide outputs from A2A9A1U2, -U3, -U4 by two and to generate a symmetrical square-wave for amplifiers A2A9A1Q3 and A2A9-A1Q4. Transformer A2A9A1T1 couples the RATT tones to the MODE SELECTOR switch through A2A9P1-2, -8 for distribution to Audio Transformer A2A21T2 and then to USB Audio Procesor A2A21A18.

3-49. In the RATT mode, Audio Processor Assembly A2A21A18 functions in a similar manner to normal USB modes (refer to paragraph 3-26) except that the compressor A2-A21A18Q1 is turned off by the presence of a CW/RATT ground on pin 3 of A2A21A18P1. The controlled amplitude audio output signal from A2A21A18P1-17 is fed to Mode Selector Assembly A2A1, where it is combined with the 500 kHz intermediate frequency carrier and thereafter processed in the same manner as other USB IF signals.

3-50. In the ISB/RATT mode, the audio RATT tone signal is developed as described for the RATT mode. However, the audio tone output from A2A9P1-2, -8 is fed through different contacts of mode selector switch A2S2-D-F and A2S2-C-R, to Audio Amplifier Assembly A2A21A18. As a result, the RATT tone signals modulate the upper sideband output in both the RATT and the ISB/RATT modes.

3-51. CW/AM/SSB CARRIER REINSERTION (Figure 5-3). Carrier reinsertion gating takes place in Mode Selector Assembly A2A1. Carrier reinsertion outputs are fed to IF Amplifier Assembly A2A12.

3-52. The 500 kHz carrier reinsertion signal is present during the CW, AM, and SSB pilot carrier modes of operation. The carrier reinsertion signal gating circuits are controlled by the CW keyline and the mode selector switch circuits. Operation of these circuits is described in the following paragraphs.

3-53. In the CW mode, the 500 kHz carrier reinsertion signal is enabled by the CW handkey. The local CW handkey, inserted at the front panel CW key jack A2J2, grounds terminal A2J2-3 to A2J2-1 when it is depres-

sed. This ground then appears, through LOCAL/REMOTE switch A2S1B-R and mode selector switch A2S2-E-R, at terminal A2-A1A4E11 of the 500 kHz Gates Subassembly A2A1A4, when the LOCAL/REMOTE switch is in the LOCAL position.

3-54. The ground at A2A1A4E11 forward-biases isolation diode A2A1A4CR7. This enables (forward-biases) carrier reinsertion diode A2A1A4CR6 and disables (reverse-biases) carrier shorting diode A2A1A4CR8. Under these conditions, the 500 kHz signal from Frequency Standard A2A5 (received at A2A1P2-A3) is allowed to pass to IF Amplifier A2A12 via diode A2A1A4CR6, transformer A2A1A4T3, and connector A2A1P2-A1. When the CW key is open, diodes A2A1-A4CR6 and A2A1A4CR7 are reverse-biased, and diode A2A1A4CR8 is forward-biased. This action grounds the 500 kHz signal path through capacitor A2A1A4C22; hence, the 500 kHz signal cannot appear at connector A2A1P2-A1. The foregoing biasing actions control the 500 kHz reinsertion signal in response to the opening and closing of the local CW key. This controlled output is fed to IF Amplifier Assembly A2A12. Here the 500 kHz cw signal is amplified prior to frequency conversion to the required output frequency.

3-55. Note that grounding the CW key also provides a ground return for the CW hold relay A2K5. Operation of A2K5 is included as part of the CW, RATT, and PTT keying circuits description contained in paragrph 3-112. A2A1A4E11 is not grounded in any mode except CW. Diodes A2A1A4CR6 and A2A1A4CR8 then block passage of the 500 kHz signal.

3-56. AM Carier Reinsertion. In the AM mode, operating voltage (+20 Vdc) is applied through pin 4 of connector A2A1P2 to the AM carrier reinsertion gate A2A1A4CR9 and A2A1A4CR10. The 500 kHz input signal at A2A1P2-A3 appears at % MOD ADJ potentiometer A2A1A4R39. It then passes through the AM carrier reinsertion gate A2A1A4CR9 and appears at transformer A2A1A4T3. The AM carrier reinsertion gate functions similarly to the CW carrier reinsertion gate. Diode A2A1A4CR11 is a control line isolation diode whose function is similar to that of diode A2A1A4CR7. The level of output signal from A2A1A4T3 during the AM mode may be adjusted by means of A2A1A4R39 to obtain the correct percentage of modulation. The 500 kHz signal is fed from the A2A1A4T3 output, through A2A1P2-A1, to the A2A12 assembly where it is inserted as the IF carrier.

3-57. The T-827H/URT is used with the AM-3924C(P)/URT rf power amplifier and various antenna couplers. An rf signal from T-827H/URT is sometimes required while tuning the associated antenna couplers. This rf signal is supplied whenever the AM-3924C(P)/URT provides a +20 Vdc control input at terminal T of connector A1A1J4. This +20 Vdc input gates on the AM carrier as previously described. A keyline signal is also required from the AM-3924C(P)/URT to cause the T-827H/URT to supply the AM carrier to the external equipment (see paragraph 3-112).

3-58. SSB Carrier Reinsertion. It is sometimes necessary to transmit a pilot carrier signal, along with the sideband signals, to permit receiving equipments to generate a stable carrier signal required for SSB reception. In SSB modes +20 Vdc is applied to reinsertion gate A2A1A4CR12 only when carrier reinsertion switch A2A1S1 is turned to a position other than infinity. This enables A2A1A4CR12, which then passes the 500 kHz signal from % MOD ADJ potentiometer A2-A1A4R39 to the attenuators A2A1A4R58 through A2A1A4R63. CARRIER REINSERTION switch A2A1S1 selects the desired amount of attenuation of the 500 kHz signal, and passes the signal to the primary of A2-A1A4T3. The A2A1A4T3 output is then fed through A2A1P2-A1 to IF Amplifier Assembly A2A12 where it is reinserted as the desired pilot carrier signal.

3-59. IF AMPLIFICATION AND LEVEL CONTROL (Figure 5-4). IF Amplifier Assembly A2A12 receives the 500 kHz IF input signal from Mode Selector Assembly A2A1 at A2A12A1P1A3. The A2A12 assembly amplifies the signal in three stages: A2A12A1Q2, A2A12A1Q4 and A2A12A1Q5. Average power control (APC), peak power control (PPC) and transmitter gain control (TGC) dc inputs from the AM-3924C(P)/URT rf power amplifier control the gain of these stages.

APC applies to NORMAL modes, and TGC applies to DATA modes; PPC functions in either NORMAL or DATA mode. These control voltages are capable of reducing the output of the T-827H/URT to zero from its nominal 250 mW PEP value. The amplified output of the A2A12 assembly is fed to RF Translator Subassembly A2A6A8 (part of Translator/Synthesizer Assembly A2A6). IF Amplifier Assembly A2A12 also receives a 500 kHz carrier reinsertion signal from the mode selector (A2A1). This signal appears in the CW, AM, and SSB pilot carrier modes of operation.

3-60. The audio (or data)-modulated IF input signal from Mode Selector Assembly A2A1 is coupled by A2A12A1C3 to the base of amplifier A2A12A1Q2. The base of A2A12A1Q2 is dc-biased by emitter followers A2A12A1Q1 and A2A12A1Q6. The PPC input from the AM-3924C(P)/URT rf power amplifier appears on the base of A2A12A1Q6.

3-61. The output from A2A12A1Q2 is then combined with the carrier reinsertion signal (if present) from connector A2A12A1P1-A2, and is applied to transformer A2A12A1T1. Transformer A2A12A1T1 drives gate 1 of amplifier A2A12A1Q4. The gain of A2A12-A1Q4 is adjusted by GAIN ADJ potentiometer A2A12A1R27. The output from A2-A12A1Q4 is fed to gate 1 of A2A12A1Q5, which amplifies the signal and then feeds it through transformer A2A12A1T2 to A2A12-A1P1-A1. From A2A12A1P1A1, the output is directed to the RF Translator A2A6A8.

3-62. In the CW and AM modes, and in SSB pilot carrier modes, the 500 kHz carrier signal is fed directly to amplifier A2A12A1Q4 via transformer A2A12A1T1. The signal is amplified in A2A12A1Q4 and A2A12A1Q5 and passed through transformer A2A12A1T2 to connector A2A12P1A1.

3-63. The APC (or TGC) signal from the AM-3924C(P)/URT rf power amplifier is applied through IF Filter Assembly A2A15 to amplifier A2A12A1Q3. The gain of A2A12-A1Q3 is controlled by potentiometer A2A12-A1R39. As the APC or TGC voltage increases, due to an increase of average power at the transmitter output, the amplified output of A2A12A1Q3 appears at gate 2 of amplifier A2A12A1Q5, and is used to linearly decrease gain of A2A12A1Q5 to maintain transmitter average power constant. GAIN ADJ Potentiometer A2A12A1R27 establishes a dc voltage on gate 2 of A2A12A1Q4 which sets the gain of this stage. Slope adjust potentiometer A2A12A1R39 sets the slope of the APC voltage to control the gain of A2-A12A1Q5.

3-64. The PPC signal limits the gain of amplifier A2A12A1Q2 during all modes of operation except CW. The PPC input from the AM-3924C(P)/URT rf power amplifier is applied through IF Filter Assembly A2A15 to emitter followers A2A12A1Q1 and A2A12-A1Q6. The output of A2A12A1Q1 controls the base bias of amplifier FA2A12A1Q2. The output of IF Amplifier Assembly A2A12 is limited when the peak RF amplifier power exceeds a predetermined level. The AM-3924C(P)/URT rf power amplifier is thereby protected against damage due to excessive peak-power outputs.

3-65. IF-TO-RF CONVERSION (Figure 5-5). Conversion of the intermediate frequency to the transmitted radio frequency takes place within RF Translator Subassembly A2-A6A8. This unit is part of Translator/Synthesizer Assembly A2A6. RF Translator Subassembly A2A6A8 receives the 500 kHz IF input from IF Amplifier Assembly A2A12 at A2A6P2-A2. In A2A6A8 it is converted in three mixer stages to the rf signal ranging from 2.0 to 29.9999 MHz. The output of A2-A6A8 is applied to RF Amplifier Assembly A2A4.

3-66. The mixing (injection) frequencies applied to the mixer stages are automatically selected. This is accomplished when the front panel tuning controls are set to the desired output frequency. Generation of the injection frequencies is accomplished by three frequency synthesizers (see paragraph 3-81).

3-67. Low Frequency Mixer. The 500 kHz amplitude controlled IF signal from IF Amplifier Assembly A2A12 is applied through low-pass filter A2A6A8L15 and A2A6A8-C66. It is then coupled by A2A6A8C14 to transmit-receive (TR) gating diode A2A6A8-CR2. Gating diode A2A6A8CR2 is forward

biased when grounded by TR relay A2K3. The signal then proceeds through transformer A2A6A8T2 to pins 1 and 10 of low frequency mixer A2A6A8U1. The first mixer injection frequency (3.3001 to 3.4000 MHz) from the output of 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12 is applied to pin 2 of low frequency mixer A2A6A8U1. The specific first mixer injection frequency is determined by the setting of the front panel 10 kHz, 1 kHz and 100 Hz controls. (See Table 3-1).

3-68. Low frequency mixer A2A6A8U1 combines the intermediate and injection frequencies by a subtractive mixing operation. This action causes the difference frequency (2.8001 to 2.9000 MHz) to emerge as the strongest in the output of transformer A2-A6A8T3. From A2A6A8T3, the output is coupled to L-C filter 2A6A3FL3 through forward biased TR gating diode A2A6A8CR5 and capacitor A2A6A8C18. A2A6A8FL3 has a bandpass of 2.80 to 2.90 MHz. This narrow bandpass rejects all outputs from the first mixer circuit except the desired difference frequency.

3-69. Mid-Frequency Mixer. The output of bandpass filter A2A6A8FL3 is coupled through capacitor A2A6A8C24, gating diode A2A6A8CR7, and transformer A2A6A8T5 to pins 1 and 10 of mid-frequency mixer A2A6-A8U2. TR gating diode A2A6A8CR7 is forward biased by the application of +20 Vdc from TR relay A2K3. The second input to mid-frequency mixer A2A6A8U2 is the injection signal from 100 kHz Synthesizer Subassembly A2A6A17 appearing at pin 2. The injection frequency subtractively mixes in A2-A6A8U2 with the 2.8001 to 2.9000 MHz signal from the low frequency mixer.

3-70. In lo-band, the 22.4 to 23.3 MHz injection frequency produces a 19.5000 to 20.4999 MHz output of the mid-frequency mixer. (See Table 3-1). This is coupled through transformer A2A6A8T4, gating diode A2A6A8CR8, capacitor A2A6A8C38, gating diode A2A6A8CR10, and capacitor A2A6A8-C41 to the 20 MHz L-C bandpass filter A2-A6A8FL1. Lo-band gating diodes A2A6A8-CR10, A2A6A8CR12 are forward biased by application of +20 Vdc from the hi-lo filter relay A2K2 in the main frame.

3-71. In hi-band the injection frequency from the 100 kHz synthesizers is 32.40 to 33.30 MHz. The hi-band injection frequency is mixed with the 2.8001 to 2.9000 MHz signal from the low frequency mixer to produce a 29.5000 to 30.4999 MHz output. The hi-band signal is coupled through transformer A2A6A8T4, forward biased gating diode A2A6A8CR8, capacitor A2A6A8C38 gating diode A2A6A8CR11, and capacitor A2A6-A8C40, to the 30 MHz L-C bandpass filter A2A6A8FL2. During the hi-band operation, hi-lo filter relay A2K2 applies a ground to gating diodes A2A6A8CR11 through A2A68-CR13. This reverse biases the lo-band gating diodes (A2A6A8CR10, A2A6A8CR12) and forward biases the hi-band gating diodes (A2A6A8CR11, A2A6A8CR13).

3-72. High Frquency Mixer. The signal from lo-band filter A2A6A8FL1 or hi-band filter A2A6A8FL2 is applied to pins 1 and 10 of high frequency mixer A2A6A8U3 through capacitors A2A6A8C48, A2A6A8C51, forward biased TR gating diode A2A6A8CR16, and transformer A2A6A8T7. A 2.5 to 23.5 MHz injection signal (see Table 3-1) from 10 MHz/1 MHz Synthesizeer Subassembly A2-A6A13 (via 10 MHz/1 MHz Filter Subassembly A2A6A14) is applied to A2A6A8U3 pin 2. The output signal, which ranges from 2.0 to 29.9999 MHz, is coupled through transformer A2A6A8T6, gating diode A2A6A8-CR17, and capacitors A2A6A8C56 through A2A6A8C58, A2A6A8CR14, A2A6A8L14, A2A6A8C59 to connector A2A6P3-A2 where it is coupled to RF amplifier A2A4. TR gating diode A2A6A8CR17 is forward biased by application of +20 VDc from the TR relay A2K3.

3-73. Variable Inductor A2A6A8L14 and capacitor A2A6A8C59 form a 19.5 MHz trap. This corresponds to the lo-band intermediate frequency input to the third mixer A2A6A8U3 when the output frequency is approximately 7.1 MHz. The value of A2A6-A8L14 is adjusted for maximum attenuation of the third IF signal in the output at A2A6-A8E12. The IF trap is bypassed in hi-band operation by gating diode A2A6A8CR14. This occurs when A2A6A8CR14 cathode is grounded by hi-lo filter relay A2K2.

3-74. RF AMPLIFICATION (Figure 5-6). The 2.0 to 29.9999 MHz rf signal from Trans-

Table 3-1. Comprehensive Frequency Translation Chart

MHz CONTROL SETTINGS	HIGH FREQUENCY MIXER INJECTION SIGNAL (MHz)		100 KHz CONTROL SETTING	MID-FREQUENCY MIXER INJECTION SIGNAL (MHz) IN 100 kHz STEPS		10 kHz CONTROL SETTING	LOW FREQUENCY MIXER INJECTION SIGNAL (MHz) IN 100 Hz STEPS
	LO-BAND	HI-BAND		LO-BAND	HI-BAND		
2	17.5		0	22.40	32.40	0	3.4000 to 3.3901
3	16.5		1	22.50	32.50	1	3.3900 to 3.3801
4	15.5		2	22.60	32.60	2	3.3800 to 3.3701
5	14.5		3	22.70	32.70	3	3.3700 to 3.3601
6		23.5	4	22.80	32.80	4	3.3600 to 3.3501
7	12.5		5	22.90	32.90	5	3.3500 to 3.3401
8	11.5		6	23.00	33.00	6	3.3400 to 3.3301
9		20.5	7	23.10	33.10	7	3.3300 to 3.3201
10		19.5	8	23.20	33.20	8	3.3200 to 3.3101
11	8.5		9	23.30	33.30	9	3.3100 to 3.3001
12	7.5						
13		16.5					
14	5.5						
15	4.5						
16	3.5						
17		12.5					
18		11.5					
19		10.5					
20		9.5					
21		8.5					
22	2.5						
23	3.5						
24		5.5					
25		4.5					
26		3.5					
27	7.5						
28	8.5						
29	9.5						

lator/Synthesizer A2A6 is received by RF Amplifier Assembly A2A4 at A2A4P2-A5. A2A4 amplifies the rf signal in three transistor stages and two vacuum-tube stages. The resulting rf output level is suitable for driving the Radio Frequency Amplifier AM-3924C(P)/URT. Interstage tuning networks for the frequency in use are selected by setting the front panel frequency controls.

3-75. The rf input from RF Translator Subassembly A2A6A8 is applied from connector A2A4P2-A5 to rf mixer amplifier subassembly A2A4A38. Here it is amplified by common-emitter rf amplifier A2A4A38Q1 through A2A4A38Q3. The overall gain of rf mixer amplifier A2A4A38 is controlled by adjusting the setting of rf gain potentiometer A2A4A38R6.

3-76. The rf signal from rf amplifier A2A4-A38Q3 is applied through contacts A1 and A2 of TR relay A2A4A38K1 to contact E1, located on a fixed stator strip. Here it is applied to one of 28 interstage coupling assemblies, A2A4A2-A29, mounted on a turret. Each interstage coupling assembly is tuned to the center frequency of its 1 MHz bandpass. The 28 assemblies provide coverage of the entire 2.0 to 29.9999 MHz rf frequency range. Capacitors are mounted on a rotor within the turret. These are connected in parallel with transformers in the 1 MHz bandpass coupling assemblies. This allows tuning of the assemblies to specific frequencies within the MHz bandpass.

3-77. Each of subassemblies A2A4A2-A29 has a tansformer T1 and capacitor C2. These are connected in series with capacitors in rotor assemblies A2A4A30 and A2A4A31. This constitutes the first tuned rf circuit. The second tuned circuit consists of transformer T2 and capacitor C3 within subassemblies A2A4A2-A29. These are connected in series with capacitors in rotor assemblies A2A4A32 and A2A4A33. Capacitor A2A4C1 couples the rf signal to the grid of A2A4V1. A tuned circuit in the output of A2A4V1 consists of transformer T3 and capacitor C4 of subassemblies A2A4A2-A29, in series with capacitors in rotor assemblies A2A4A34 and A2A4-A35.

3-78. The amplified rf signal at the output of A2A4V1 is coupled by A2A4C5 to the input of rf amplifier A2A4V2 via A2A4FL2. The tuned output circuit of A2A4V2 consists of transformer T4 and capacitor C5 of subassemblies A2A4A2-A29, in series with capacitors in rotor assemblies A2A4A36 and A2A4-A37. The amplified rf signal at the secondary of T4 appears at output connector A2A4-P2-A1. Here it is connected to the AM-3924C(P)/URT rf power amplifier.

3-79. A shaper pulse from power supply A2-A8 is applied to the grids of rf amplifiers A2-A4V1 and A2A4V2 from A2XA4P2-9 at the instant the T-827H/URT is keyed. This pulse appears as a large negative bias voltage to the grids of A2A4V1 and A2A4V2, momentarily holding the rf output from RF Amplifier Assembly A2A4 at zero. This key-on shaper pulse suppresses large amplitude rf signals in the output at the first instant of signal transmission. This allows the output level control circuits of the AM-3924C(P)/URT rf power amplifier to take control. The grid bias returns to normal at a rate controlled by R-C network located in Power Supply Assembly A2A8, and the T-827H/URT rf output increases to normal as control grid bias falls.

3-80. The turret-tuning assemblies of RF Amplifier Assembly A2A4 are selected in response to tuning-code signals received from Code Generator Assembly A2A7. Setting the front panel 10 MHz and 1 MHz controls to a desired frequency causes Code Generator Assembly A2A7 to provide a specific five-wire tuning code (combination of open and grounded lines) to turret decoder switch A2A4S1. Turret drive relay A2A4K1 then energizes and activates motor A2A4B1. A2A4B1 rotates the turret and decoder switch wafers until the decoder reaches a position where its contacts reflect the complement of the code generator input. When this occurs, A2A4S1 is at a position that interrupts all ground paths to A2-A4K1. Turret drive relay A2A4K1 then deenergizes, stopping motor A2A4B1. The turret is now positioned as required for the selected 10 MHz and 1 MHz control settings. The 100 kHz and 10 kHz rotor assemblies are selected by the 100 kHz and 10 kHz front panel controls through mechanical linkage.

3-81. FREQUENCY SYNTHESIS (Figure 3-2). Injection frequencies for the three frequency mixers of RF Translator Subassembly

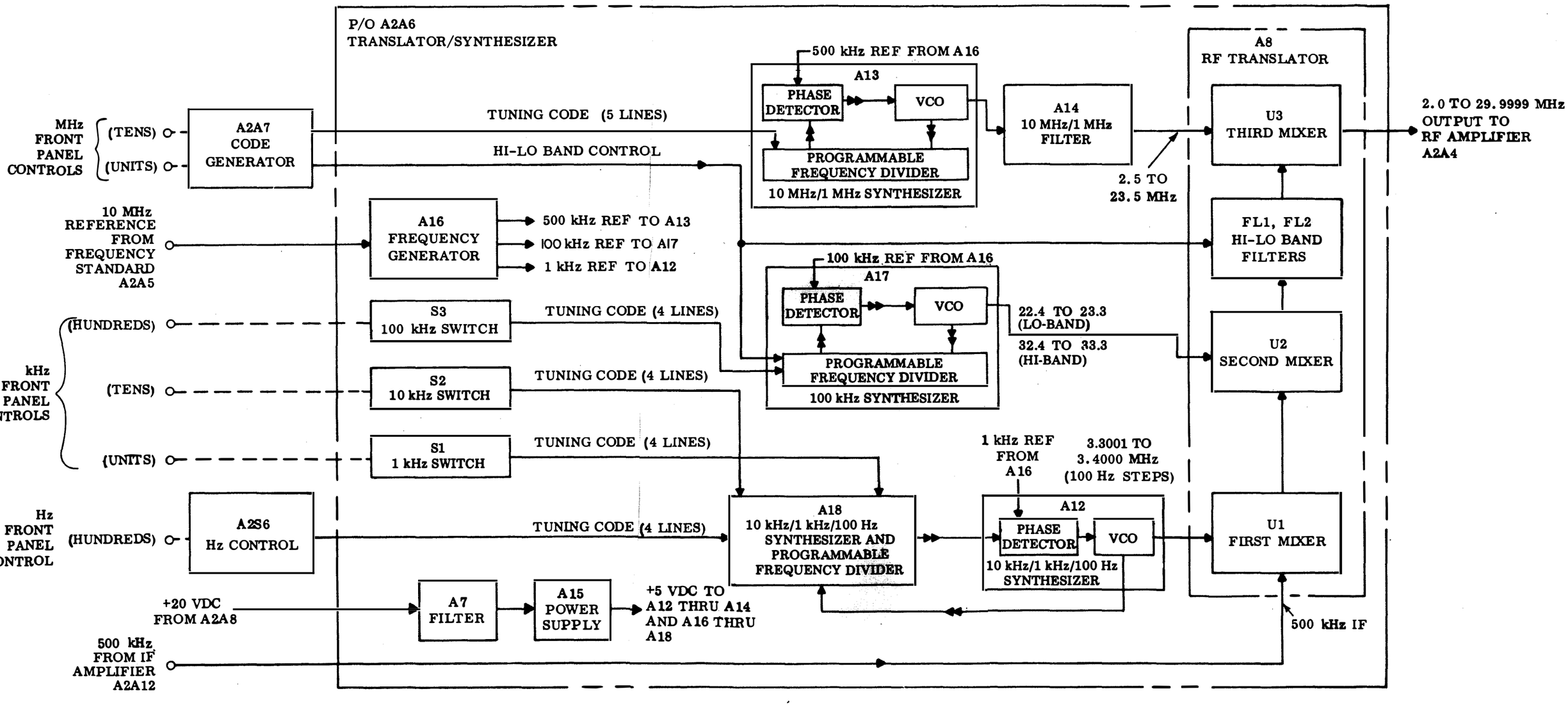


Figure 3-2. Frequency Synthesis and Translation, Functional Block Diagram

A2A6A8 are generated within the following subassemblies of Translator/Synthesizer Assembly A2A6:

1. 100 kHz Synthesizer A2A6A17
2. 10 kHz/1 kHz/100 Hz Synthesizers A2A6A12 and A2A6A18
3. 10 MHz/1 MHz Synthesizers A2A6A13 and A2A6A14

The injection frequencies are developed using reference frequencies from Frequency Generator Subassembly A2A6A16. The reference frequencies are locked to the 10 MHz output of Frequency Standard Assembly A2A5.

3-82. Frequency control is provided for the 10 MHz/1 MHz synthesizer by controls on the front panel which position Code Generator Assembly A2A7. The 100 kHz, 10 kHz and 1 kHz front panel controls use chain-drives to position coding switches A2A6S1 through A2A6S3. The 100 Hz steps are set by front panel Hz switch A2S6.

3-83. Each of the three synthesizers employs a phase-locked loop circuit to ensure that the output injection frequencies are correct. In the case of the 10 kHz/1 kHz/100 Hz unit, the output from the voltage controlled oscillator (VCO) on the A2A6A12 subassembly is applied to a programmable frequency divider. The divider, located on subassembly A2A6A18, provides one input to a phase detector. A second phase detector input, a stable 1 kHz reference, is provided by Frequency Generator A2A6A16. The output frequency of the programmable frequency divider is determined by codes set in Hz switch A2S6, 1 kHz switch A2A6S1 and 10 kHz switch A2A6S2. If the two inputs to the phase detector are not exactly the same frequency, a correction voltage is developed in the phase detector. This correction voltage is applied through a loop filter to the VCO. The VCO output frequency then changes to re-establish a 1 kHz input to the phase detector. The VCO is therefore locked to the 1 kHz standard frequency from A2A6A16. The VCO output frequency of A2A6A12 is divided by ten and applied through a filter network as the injection signal to low frequency mixer A2A6A8U1.

3-84. Synthesizer circuits A2A6A17 and A2A6A13 differ slightly from the preceeding example. All circuitry for the 100 kHz Synthesizer Subassembly A2A6A17 is located on one printed wiring board. The VCO output frequency is not divided prior to use in mid-frequency mixer A2A5A8U2. A hi-lo band control voltage, from Code Generator Assembly A2A7, is applied to the frequency divider in A2A6A17 to determine the output injection signal frequency range.

3-85. The 10 MHz/1 MHz synthesizer circuit A2A6A13 differs only in that the frequency divider is programmed by the five-line code output of Code Generator Assembly A2A7. The VCO output is filtered in the separate subassembly A2A6A14.

3-86. STANDARD FREQUENCY GENERATION AND DISTRIBUTION (Figure 5-7). Frequency Standard Assembly A2A5 provides accurate reference frequencies for use in Radio Transmitter T-827H/URT. The frequencies are produced either from a 5 MHz external input provided by a frequency standard at the installation site, or from an internal oven-controlled 5 MHz oscillator circuit. The internal 5 MHz oscillator circuit is comprised of crystal-controlled oscillator A2A5A1Q1 and associated circuitry. Precise adjustment of the oscillator output frequency is provided by A2A5A1C2 and A2A5A1C3. The 5 MHz reference frequency is divided and multiplied in Divider/Amplifier Subassembly A2A5A2 to produce the highly stable output frequencies referenced in paragraph 3-11.

3-87. Reference Control. The 5 MHz Reference Control Subassembly contains logic circuits which evaluate the incoming external 5 MHz reference signal. If the amplitude is too low, the logic circuits select the internally generated 5 MHz signal. Specifically, when the external reference falls below approximately 0.25 volts, the output from detector A2A5A4CR6 falls low enough to turn off emitter follower A2A5A4Q2. This results in logic lows at A2A5A4U1A-1 and A2A5A4-U1B-6; and logic highs at A2A5A4U1A-3 and A2A5A4U2B-5. A2A5A4U1A-2, A2A5A4-U2B-5, and A2A5A4U2D-13 are wired high in the EXT/NORM and EXT/(OVEN STBY) position of A2A5A2S1. The result is that the internal reference from A2A5A1Q3 is routed, via A2A5A4U2A through A2A5A4U2B and

A2A5A4U2C, to the Divider/Amplifier Assembly A2A5A2 for use in the equipment. The external reference line is blocked at A2A5A4U1C.

3-88. Reference Source Selection. A three position 5 MHz OSC SOURCE switch A2A5A2S1 is used to select one of two modes of the external 5 MHz source, or the internal 5 MHz source. When the 5 MHz OSC SOURCE switch is in EXT NORM position, the external standard provides the 5 MHz reference signal. At this time the Oven Subassembly A2A5A3 is off. When the 5 MHz OSC SOURCE switch is in EXT (OVEN STBY) position the external source supplies the reference signal, and the oven heater is enabled and maintains a constant temperature. When the 5 MHz OSC SOURCE switch is in INT/COMP position, the oven-stabilized crystal oscillator in A2A5A1 provides the reference signal.

3-89. When the 5 MHz OSC SOURCE switch is in EXT NORM position, pull-up resistor A2A5A4R10 provides a logic high to A2A5A4U1A-2, and NAND gate A2A5A4U1A outputs the amplified external 5 MHz frequency standard signal at A2A5A4U1A-3 and an inverted version of this signal at A2A5A4U1B-6. Thus, the inverted 5 MHz signal appears simultaneously on both inputs of A2A5A4U1C. A2A5A4U1C operates as an inverter, and the reinverted 5 MHz signal appears as the amplified 5 MHz standard frequency at A2A5A4U2C-9. Since NAND gate A2A5A4U2D-13 is at a steady logic high, A2A5A4U2D inverts the amplified external 5 MHz, which appears at A2A5A4U2B-5. A2A5A4U2B functions as an inverter; hence, A2A5A4U2C-10 sees the same signal as A2A5A4U2C-9. This causes A2A5A4U2C to function as an inverter, and the amplified 5 MHz external frequency standard is fed via A2A5A4U2C-8 to the divider/amplifier assembly A2A5A2.

3-90. When the 5 MHz OSC SOURCE switch is in EXT (OVEN STBY) position the external source supplies the reference signal with all gate logic the same as for EXT/NORM. The oven heater is enabled and maintains a constant oven temperature. When the 5 MHz OSC SOURCE switch is in INT/COMP position, the crystal oscillator in A2A5A1 provides the reference signal, and the oven maintains its constant temperature. Amplifiers A2A5A1Q1, crystal A2A5A1Y1, and associated components form a modified Pierce oscillator which provides the internal 5 MHz frequency standard. This signal is amplified by A2A5A1Q2, A2A5A1Q3 and coupled to inverter A2A5A4U2A where it is inverted and fed to NAND gate input A2A5A4U2B-4. In position 3 (INT/COMP) of 5 MHZ oscillator source switch A2A5A2S1, NAND gate terminal A2A5A4U2D-13 is held low, as is NAND gate A2A5A4U1A-2. Thus, NAND gate A2A5A4U1A-3 output stays high, blocking the external 5 MHz reference and causing A2A5A4U1B-6 and A2A5A4U2D-12 to stay low. Hence, A2A5A4U2D-11 output is high, enabling A2A5A4U2B to pass the inverted, internally generated, 5 MHz reference received from A2A5A4U2A-3. Since now A2A5A4U1C-9 is steady logic low, A2A5A4U2C-9 is high and A2A5A4U2C passes the internal 5 MHz frequency standard, again reinverted.

3-91. Oven Temperature Control Sensor. Changes in oven temperature are sensed by A2A5A3R2 and applied as an input to the differential amplifier consisting of A2A5A1Q4 and A2A5A1Q5. When oven temperature tends to increase, the resistance of A2A5A3R2 also tends to increase changing the balance of sensor bridge A2A5A1R13 through A2A5A1R16 and the corresponding input to the differential amplifier circuit. A2A5A1Q6 then provides less base current to A2A5A1Q7, decreasing conduction in A2A5A4Q5 and, the current through the heater A2A5A3R1, resulting in a tendency to oppose an increase in the crystal oven operating temperature. The reverse effect stabilizes the oven against a tendency to decrease in temperature.

3-92. Frequency Divider. Divider/Amplifier Subassembly A2A5A2 contains divider circuits and multiplier circuits. The 5 MHz input at A2A5A2E9 is amplified by A2A5A2Q1 and A2A5A2Q6. The output from A2A5A2Q1 is coupled to divide-by-five oscillator A2A5A2Q2, which is tuned to 1 MHz. The A2A5A2Q2 output is coupled to divide-by-two oscillator A2A5A2Q4 and 1 MHz amplifier A2A5A2Q3. The 1 MHz output of A2A5A2Q3 is coupled to A2A5P1A3 via the parallel reso-

nant circuit combination of A2A5A2C13 and A2A5A2T1. The output of A2A5A2Q4 is amplified in 500 kHz amplifier A2A5A2Q5. It is coupled to A2A5P1-A1 and A2A5P1-A2 via the parallel resonant circuit formed by A2A5A2C22 and A2A5A2T2.

3-93. Frequency Multiplier. The 5 MHz output of A2A5A2Q6 is coupled to 10 MHz amplifier A2A5A2Q7. A2A5A2Q7 is tuned to the second harmonic of the input 5 MHz by capacitor A2A5A2C31. The 10 MHz input to amplifier A2A5A2Q8 is further amplified and appears at the primary of transformer A2-A5A2T3, which is part of a parallel resonant circuit tuned by trimmer A2A5A2C33. The 10 MHz output from A2A5A2T3 appears at A2A5P1-A5. The output from A2A5A2Q6 is also applied to 5 MHz amplifier A2A5A2Q9. Capacitor A2A5A2C38 is adjusted to provide the proper 5 MHz output at A2A5P1-A6.

3-94. Comparator Circuit. Setting oscillator source switch A2A5A2S1 in the INT/COMP position grounds one input to each of NAND gates A2A5A4U1A and A2-A5A4U2D. This action results in a visual comparison of the internally generated 5 MHz reference and the external 5 MHz input. NAND gates A2A5A4U1A and A2A5-A4U2D cause the internal 5 MHz to be present at NOR gate A2A5A4U2C and the external input to be blocked. Both the internal and external signals are present at the input of phase detector A2A5A4U1D. The output of A2A5A4U1D is a series of pulses with a repetition rate equal to the frequency difference between reference oscillators. Amplifier A2A5A2Q10 and lamp driver A2A5A2-Q11 raise the power level of the pulses to drive the lamp. (In some units, Amplifier A2A5A2Q10 and Lamp Driver A2A5A2Q11, with associated components, are replaced by a simplified LED circuit performing the same function.) The flash rate of the lamp equals the difference in frequency between the internal and external reference oscillators and permits an accurate adjustment of the internal oscillator A2A5A1Q1 with tuning capacitors A2A5A1C2 and A2A5A1C3.

3-95. FREQUENCY GENERATOR (Figure 5-8). The 10 MHz output from Frequency Standard Assembly A2A5 appears at connector A2A6A16P1A1. It is applied to a two-stage amplifier consisting of A2A6A16Q1, A2A6A16Q2 and associated components. The amplified 10 MHz signal is shifted to the proper logic level by level shifter A2A6A16-U1A. Buffer stages A2A6A16U1B and A2-A6A16U1C isolate the output of A2A6A16-U1A from the succeeding divider circuit. The 10 MHz logic level signal then appears at the input of decade divider A2A6A16U2. Divider A2A6A16U2 applies a 1 MHz signal output to binary/decade divider A2A6A16U3. The binary division output from pin 12 of A2A6A16U3 is used as the 500 kHz reference signal in 10 MHz/1 MHz Synthesizer Subassembly A2A6A13. The decade division output from pin 11 of A2A6A16U3 is used as the 100 kHz reference signal by the 100 kHz Synthesizer Subassembly A2A6A17. It is also applied to decade dividers A2A6-A16U4 and A2A6A16U5. The 1 kHz output of A2A6A16U5 appears at connector A2A6-A16P1A3 for use in 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12 when +4.3 Vdc is present at input connector A2A6A16-P1-9. This +4.3 Vdc causes transistor switch A2A6A16Q3 to conduct and A2A6A16Q4 to cut off. The resulting positive voltage at the collector of A2A6A16Q4 is applied to NAND gate A2A6A16U6B. This opens the gate and passes the 1 kHz reference signal through NOR gate A2A6A16U6D to connector A2A6-A16P1-A3. The positive collector voltage from A2A6A16Q4 is also applied to inverter A2A6A15U6A, which causes NAND gate A2-A6A16U6C to close and isolate the vernier 1 kHz reference from NOR gate A2A6A16U6D.

3-96. 10 kHz/1 kHz/100 Hz Synthesizer (Figure 5-9). The 10 kHz/1 kHz/100 Hz Synthesizer Subassemblies A2A6A18 and A2A6-A12 produce the 3.3001 to 3.4000 MHz injection signals used in the low-frequency mixing circuits of RF Translator Subassembly A2-A6A8. An electronic, closed loop servo system compares the output signal with a 1 kHz input reference signal from Frequency Generator Subassembly A2A6A16. Any error detected is converted into a dc control voltage which corrects the output frequency. When the phase difference between the output signal and the reference signal is constant, the loop is locked.

3-97. The injection signal is generated by a voltage controlled oscillator (VCO) assembly

A2A6A12A1. The VCO is comprised of LC oscillator A2A6A12A1U1 and its associated components. A2A6A12A1L1, A2A6A12A1C2 through A2A6A12A1C3, and the varactor diode A2A6A12A1CR1 form the tank circuit which determines the oscillator output frequency. A2A6A12A1CR1 presents capacitance in the tank, whose value is determined by the amount of applied voltage. The VCO output frequency ranges from 33.001 to 34.000 MHz. The output of the VCO is applied to emitter follower A2A6A12A1Q1, which isolates LC oscillator A2A6A12A1U1 from the output circuitry loads. The output is then applied to inverters A2A6A12U2A through A2A6A12U2C, which provide the correct logic level input to pin 8 of decade divider A2A6A12U3. The 3.3001 to 3,4000 MHz output signal from pin 2 of A2A6A12U3 is inverted by A2A6A12U2D and applied to bandpass filter A2A6A12L6-L10 and A2A6-A12C10-C12. The level of injection signal output is adjustable by means of variable resistor A2A6A12R16. The output from LC oscillator A2A6A12A1U1 is also applied to the divider network subassembly A2A6A18.

3-98. The divider network Subassembly A2-A6A18 divides the 34.000 MHz input by the factor necessary to produce a 1 kHz output. Prescaler A2A6A18U1 divides the 33.001 to 34.000 MHz VCO output by 11 when a logic low (0 to +0.4 Vdc) from pin 7 of counter control logic A2A6A18U2 is applied to pins 9 and 10 of A2A6A18U1. Prescaler A2A6A18-U1 continues to divide by eleven until divider A2A6A18U3 has counted down from a preset number to zero. At this time, counter control logic A2A6A18U2 applies a logic high (+2.4 to +5.0 Vdc) to pins 9 and 10 of A2A6-A18U1. Prescaler A2A6A18U1 now divides by a factor of ten until cascade dividers A2-A6A18U4 - A2A6A18U7 reach the all-zero state. The counting cycle is now complete and the dividers are reset in preparation for the next cycle.

3-99. The purpose of cascaded dividers A2-A6A18U4 through A2A6A18U7 is to form the required division to synthesize the indicated mixing frequency from the approximately 3.3989 MHz output of prescaler A2A6A18U1. BCD converters A2A6A18U9 and A2A6A18U10 form the required codes to program dividers A2A6A18U4 through A2-A6A18U7 to correct divisors. These divisors are determined by the settings of coding switches A2A6S1 and A2A6S2 on the chassis of A2A6, as read in on A2A6A18P1-3 through A2A6A18P1-6 and A2A6A18P1-12 through A2A6A18P1-15. The 100 Hz inputs on A2-A6A18P1-8 through A2A6A18P1-11, from 100 Hz switch A2S6, determine the programming of preset divider A2A6A18U3. Resistors A2A6A18R22 - A2A6A18R25 and A2A6A18R18 - A2A6A18R21 are pull-up resistors for integrated circuit inputs A2A6-A18U10-10, 11, 12, 13 and A2A6A18U9-10, 11, 12, 13. Counter control logic A2A6A18-U2 totals the individual counts to dividers A2A6A18U4 through A2A6A18U7, and generates a reset pulse to begin the next count cycle.

3-100. The output of the divider network is applied to pin 3 of phase detector A2A6A12-U1. A2A6A12U1 develops an output in proportion to the magnitude and direction of the phase difference between the divider network output and the 1 kHz reference input from Frequency Generator Subassembly A2-A6A16. The phase detector output enables transistor A2A6A12Q2 of the charge pump circuit through resistor A2A6A12R19, or it enables transistor A2A6A12Q3 through resistor A2A6A12R4. The output of the charge pump is applied to loop filter A2A6A12C2, A2A6A12R7 and A2A6A12R9, which filters the pulses providing the dc control voltage to be applied to the variable capacitance diode A2A6A12A1CR1. The dc control voltage will decrease or increase the bias on A2A6A12-A1CR1, changing the capacitance of A2A6-A12A1CR1, as required, to establish the proper output frequency from the VCO.

3-101. 100 kHz Synthesizer (Figure 5-10). The 100 kHz Synthesizer Subassembly A2A6-A17 produces the injection frequency of 22.40 to 23.30 MHz (lo-band) or 32.40 to 33.30 MHz (hi-band) used in the mid-frequency mixer circuits of RF Translator Subassembly A2A6A8. A comparison of figure 5-10 with figure 5-9 shows that, except for component values, most circuits are identical to the corresponding circuits of the 10 kHz/1 kHz/100 Hz synthesizer.

3-102. The frequency divider network divides the VCO output frequency by a number

in the range of 224 to 233 or 324 to 333 as determined by the setting of the 100 kHz coding switch A2A6S3 and the state of the hi-lo band control line at pin 7 of A2A6A17-P1. The divider network output is applied to phase detector A2A6A17U1. The phase detector compares the output signal with the 100 kHz reference signal from Frequency Generator Subassembly A2A6A16. Any error detected causes the VCO frequency to be corrected in the same manner described for the 10 kHz/1 kHz/100 Hz Synthesizer.

3-103. Programmable divider network A2-A6A17U4 through A2A6A17U8 functions similarly to the 10 kHz/1 kHz/100 Hz synthesizer divider network except there are no complement converters, and division control is preset to either 2 or 3 in response to the state of the hi-lo band control input at A2-A6A17P1-7. Transistor A2A6A17Q3 converts the +20 Vdc/ground control input into logic low/logic high levels for application to data pin 5 of A2A6A17U8. Thus, A2A6A17U8 is preset to divide-by-2 for a +20 Vdc control input (lo-band) and to divide-by-3 for a ground control input (hi-band).

3-104. The VCO output is applied to amplifier A2A6A17Q1. The setting of variable resistor A2A6A17R10 establishes the output signal level. The signal is applied from the collector of A2A6A17Q1 to a bandpass filter consisting of A2A6A17L4 - A2A6A17L7, A2-A6A17C15, A2A6A17C17 and A2A6A17C18. Amplifier A2A6A17Q2 provides isolation and a low impedance output to the mid-frequency mixing circuits of RF Translator Assembly A2A6A8.

3-105. 10 MHz/1 MHz Synthesizer (Figure 5-11). The 10 MHz/1 MHz Synthesizer Subassembly A2A6A13 and 10 MHz/1 MHz Filter Subassembly A2A6A14 provide one of 17 injection frequencies, in the range of 2.5 to 23.5 MHz, to the high frequency mixer circuit of RF Translator Subassembly A2A6A8. A 20 to 50 MHz VCO output signal is applied through a programmable frequency divider network to establish one input to phase detector A2A6A13U1. Phase detector A2A6-A13U1 then compares this signal with a 500 kHz reference signal supplied by Frequency Generator Subassembly A2A6A16, and generates a dc correction voltage (via loop filter A2A6A13U2, A2A6A13C3, A2A6A13R8) to lock the VCO frequency.

3-106. The VCO output signal is applied to level shifters A2A6A13U4A and A2A6A13-U4B, which provide logic level conversion to divider A2A6A13U5. A2A6A13U5 provides divisions by 2, 4, or 8, at pins 5 and 6, 9 and 2, respectively.

3-107. The gating circuitry selects the outputs from divider A2A6A13U5 and the appropriate filter in 10 MHz/1 MHz Filter Subassembly A2A6A14. If pins 1 and 2 of A2-A6A13U11 are at logic high and logic low levels, respectively, NAND gates A2A6A13-U4C - A2A6A13U4D will open and pass the divided-by-8 output of A2A6A13U5 to the divider network via NOR gate A2A6A13U7A - A2A6A13U7C and enable 4 MHz filter switch A2A6A14Q1. In a similar manner, NAND gates A2A6A13U6A - A2A6A13U6B enables the divided-by-4 output of A2A6A13U5 when output pin 1 of A2A6A13U11 is at a logic low. NAND gate A2A6A13U6C-U6D selects the divided-by-2 output from A2A6A13U5. Diodes A2A6A13CR5-A2A6A13CR6 monitor the lines from pins 2 and 1 of A2A6A13U11 and cut off A2A6A13Q2 if either is low. This action closes the divide-by-2 gates. When both lines are at logic high A2A6A13Q2 turns on, opening gates A2A6A13U6C-U6D and enabling switch A2A6A14Q7.

3-108. Decade dividers A2A6A13U9 and A2A6A13U10 are preset via the data inputs to pins 2, 11 and 14. A five-wire tuning code consisting of open circuits and grounds from Code Generator Assembly A2A7 is applied through filter assembly A2A6A13A1 to input pins 10 through 14 of A2A6A13U11. The five binary bits from code generator A2A7 represent any of 28 combinations of settings of the front-panel 10 MHz and 1 MHz dials. These input codes are converted to natural BCD format in eight bit-positions at the output of A2A6A13U11. The code is then applied to data pins 5, 11 and 14 of A2A6A13-U10 and pins 2, 11, and 14 of A2A6A13U9.

3-109. Counter Control Logic A2A6A13U8 monitors the count in dividers A2A6A13U9 and A2A6A13U10, accepts the output of NOR gates A2A6A13U7A-A2A6A13U7C at A2A6A13U8-1, and passes the divided 500 kHz output to phase detector input A2A6-

A13U1-3. NOR gates A2A6A13U7A-A2A6-A13U7C will select only one of the divided frequencies from NAND gates A2A6A13U4C-A2A6A13U4D and A2A6A13U6A-A2A6A13-U6D. These NAND gates are enabled, along with MHz Filter Switches A2A6A14Q1, A2-A6A14Q4, and A2A6A14Q7, by the BCD outputs of A2A6A13U11-1 and A2A6A13U11-2 and the outputs of NAND gate A2A6A13Q2. Inductors A2A6A14L6, A2A6A14L12, and A2A6A14L18 function as rf suppressor chokes to the V_{cc} power supply for the filter amplifiers.

3-110. The three filter networks within 10 MHz/1 MHz Filter Subassembly A2A6A14 operate in the same manner. The injection signal is supplied to a conventional, untuned RF amplifier. A variable resistor in the emitter circuit of the RF amplifier adjusts the output level applied to the bandpass filter. This filter rejects all frequencies except the desired injection signal. Buffers A2A6-A14Q3, A2A6A14Q6, and A2A6A14Q7 provide a low impedance injection signal source for RF Translator Subassembly A2A6A8.

3-111. CW, RATT, DATA, and PTT KEYING CONTROL (Figure 5-12). In local CW operation, the cw handkey grounds CW Hold Relay A2K5 to initiate keying of the T-827H/URT. In remote CW/RATT operation, keying is initiated by a ground supplied from the associated CW/RATT equipment at connector A1A1J4-c. In either case, the ground path is directed to A2K5 via switch elements A2S1-B-R and A2S2-E-R. A2K5 is thereby energized, and completes a ground path via A2K5B1 and A2K5B2, switch element A2S2-E-F, contacts A2 and A3 of unenergized PTT Relay A2K4, to pin X2 of T/R Relay A2K3. A2K3 becomes energized, and applies the transmit mode operating voltages to the T-827H/URT circuits. Capacitors A2A8C10 and A2A8C11 discharge through the CW HOLD relay coil, causing A2K5 to remain energized for approximately one second after the cw handkey is released. Thus, the T-827H/URT remains in a ready-to-transmit condition during the intervals between cw code pulses. No relay contacts actually switch at the cw keying rate. Local RATT keying is accomplished via the RATT key input at connector A1A1J7-A. This energizes A2K3 via a ground path through contacts 3 and 5 of switch section A2S1-B-R, contacts 4 and 6 of switch section A2S2-E-F, and contacts A2, A3 of unenergized PTT RELAY A2K4.

3-112. With DATA/NORMAL switch A2S11 set at DATA, relays A2A21A20K1 and A2-A21A20K2 on Audio Control Assembly A2-A21A20 energize and place the T-827H/URT into DATA mode in LSB, USB, or ISB, depending on the setting of the Mode Selector Switch A2S2. The ground to relay A2K3 is held through the contacts of relay A2A21-A20K2. The +6 Vdc applied to DATA Keyline Input A2A1J8-E is connected to A2A21XA20-7 on the Audio Control Assembly, causing A2A21A20Q10 to conduct. This provides a ground keyline connection to A1A1J4-K through contacts of relay A2A21A20K1, and allows various relays in the AM-3924C(P)/URT amplifier to operate.

3-113. The PTT relay A2K4 is energized by +12 Vdc from the local handset (at HANDSET Connector A2J1) during local operation. In remote operation, it is energized by the remote 12 Vdc and return (at rear case connector A1A1J4-K and H). When energized, A2K4 connects a keyline ground through the de-energized tune relay A2K1 to contact X2 of TR relay A2K3. The keyline ground causes A2K3 to energize and apply the transmit operating voltages to the T-827H/URT circuits.

3-114. Tune relay A2K1 energizes during tuning operations. This is accomplished by the ground path provided by Code Generator Assembly A2A7 or by RF Amplifier Assembly A2A4. Contact X2 of A2K1 is grounded whenever turret relay A2A4K1 is energized. The energized tune relay A2K1 removes +28 Vdc from the +20 Vdc regulator A2Q1 to disable transmit voltages during the tuning cycle. Tune relay A2K1 is also energized by a ground path from Code Generator Assembly A2A7 whenever the front panel MHz controls are set to the 00 or 01 position.

3-115. POWER DISTRIBUTION. (Figures 5-13 thru 5-15).

3-116. AC Power Distribution (Figure 5-13). A 105 to 125 Vac, 48 to 420 Hz, single phase, power source is required by transmit-

ter T-827H/URT. It is connected at pins R and S of connector A1A1J4 or pins A and C of connector A1A1J3. The input at A1A1J4 is used when the T-827H/URT is part of Radio Transmitting Set AN/URT-23C(V)1. A1A1J3 is used when the T-827H/URT is operated independently of Radio Transmitting Set AN/URT-23C(V)1. AUX/NORM switch A1S2 (figure 2-2) selects the A1A1J3 or A1-A1J4 input. Power is then routed to interlock switch A1S2. Interlock switch sections A1S2A and A1S2B open both sides of the line when the main frame chassis is extended from the case. Power from A1S2 is connected to mode selector switch sections A2-S2-B-F and A2S2-A-F through case-to-mainframe connectors A1P1 and A2J21. Contact is made between pins 11 and 12 of A2S2-B-F and pins 6 and 7 of A2S2-A-F in all mode selector positions except OFF. Power from A2S2 is connected to pins 1 and 6 of power transformer A2T1 through fuses A2F2 and A2F1. In all mode selector switch A2S2 positions except OFF and STBDY, switching LOCAL/REMOTE switch A2S1 to REMOTE results in power available at A1A1J4-U through A2J21-45. Power at A2T1-1 and 6 energizes a secondary winding that produces 6.3 Vac at pins 13 and 14, 131 Vac at pins 7 and 8, and 35 Vac at pins 9 and 10. The 6.3 Vac at pins 13 and 14 is directed to RF Amplifier A2A4 through connector A2XA4P2 pins 7 and 8. Here it provides filament voltage for A2A4-V1 and A2A4V2. The 131 Vac and 35 Vac are inputs to power supply A2A8. The full wave bridge rectifiers shown in A2A8 are responsible for outputs of 110 Vdc and 28 Vdc.

3-117. +28 Vdc Distribution (Figure 5-14). Bridge rectifier A2A8CR5-A2A8CR8 of Power Supply assembly A2A8 provides an unfiltered dc output to A2A8E6. Inductor A2-L2, located on the main frame, and capacitors A2A8C1 and A2A8C2 filter this output to provide +28 Vdc at A2E22. A2E22 supplies the filtered +28 Vdc to five locations: A2-A8E5, A2E45, A2S2-C-F pins 1, 4, 7, and 9, A2J21-24 and A2K6X1. A2A8E5 supplies +28 Vdc to voltage dropping resistor A2A8R1 in series with dial lamps A2DS3 and A2DS4. The +28 Vdc at A2E45 is connected to A2A5-P1-3 in Frequency Standard A2A5 to supply the crystal oscillator oven heater circuitry. A2S2-C-F supplies +28 Vdc to A2E23 in all voice modes of operation. This switch section also provides the 28 Vdc to A2E20 in all positions except OFF and STDBY. A2R3, connected to A2E23 from A2E11, is part of a voltage regulator. This resistor, in conjunction with regulator diode A2CR8, maintains +12 Vdc to A2J1-D through Handset Filter Box A2A14. The +28 Vdc at A2E20 branches in four directions: to tune relay A2K1, to A2A4 via A2XA4P1-7, to CW Hold Relay A2K5, and to E9 of A2A8. From tune relay A2K1, +28 Vdc is applied to X1 of Hi-Lo Filter Relay A2K2 and the collector of series regulator A2Q1.

3-118. +20 Vdc and +5 Vdc Distribution (Figure 5-15). The +28 Vdc on the collector of A2Q1 is reduced to +20 Vdc and regulated by circuitry contained in power supply A2A8. The +20 Vdc output at A2A8E20 appears at distribution terminals A2E24 and A2E46. From here it is directed to Audio Processors A2A21A18, A2A21A19 and Audio Control A2A21A20 via Interconnect Board Terminals A2A21E16 and A2A21E26, Frequency Standard Assembly A2A5, Translator/Synthesizer Assembly A2A6, Meter Amplifier Assemblies A2A10 and A2A11, Mode Selector Assembly A2A1, IF Amplifier Assembly A2A12 through inductor A2A15L1, and to the AM-3924C(P)/URT power amplifier. When the T-827H/URT is keyed, the +20 Vdc is also switched through TR relay A2K3 to RF Amplifier Assembly A2A4, Translator/Synthesizer Assembly A2A6, Mode Selector Assembly A2A1, hi-lo filter relay A2K2, and the front and rear wafers of mode selector switch A2-S2-A. The mode selector switch distributes the +20 Vdc to RATT Tone Generator Assembly A2A9 and Mode Selector Assembly A2A1. The switched +20 Vdc from TR relay A2K3 enables gating circuits, in RF Translator Subassembly A2A6A8, in the transmit mode. The +20 Vdc, or ground, from contact B2 of hi-lo filter relay A2K2 is applied to the Translator/Synthesizer A2A6 to select the 20 MHz or 30 MHz IF used for final frequency up-conversion. The +20 Vdc for Translator/Synthesizer Assembly A2A6 is applied through Filter Subassembly A2A6A7 to Power Supply Subassembly A2A6A15. Power Supply Subassembly A2A6A15 produces the +5 Vdc required by circuits within the A2A6 subassemblies and zener diode A2CR10 in the T-827H/URT main frame. The +4.3 Vdc resulting from A2CR10 is used in the front

panel Hz switch and in control circuitry within Frequency Generator Subassembly A2A6A16.

3-119. +110 Vdc Distribution (Figure 5-15). The +110 Vdc power is rectified in Power Supply Assembly A2A8 and routed through filter inductor A2L1 to terminal A2-E9. A2E9 is connected to contact A2 of TR relay A2K3. When the T-827H/URT is keyed, TR relay A2K3 applies +110 Vdc through contact A1 to RF Amplifier Assembly A2A4. The +110 Vdc is the plate and screen voltage supply for the tubes in RF Amplifier Assembly A2A4.

3-120. TUNING (Figure 3-3). Tuning of the T-827H/URT is accomplished by setting the front panel MHz, kHz, and Hz controls to indicate the desired transmit signal frequency. This frequency is digitally displayed in the windows above the MHz and kHz controls and on the skirt of the Hz Knob. Positioning the front panel frequency controls tunes the T-827H/URT by electrical and mechanical means.

3-121. When the front panel MHz contols are positioned, Code Generator Assembly A2A7 produces a five-line tuning code (combinations of open and grounded lines). These are applied to RF Amplifier Assembly A2A4 and the BCD converter of 10 MHz/1 MHz Synthesizer Subassembly A2A6A13. A motor in RF Amplifier Assembly A2A4 positions a coding ring consisting of A2A4S1-A and A2-A4S1-B. The coding ring contains segments corresponding to the complements (or images) of the five-line tuning code received from Code Generator Assembly A2A7. When the MHz frequency controls are repositioned, the motor will energize through one or more of the five input lines from Code Generator Assembly A2A7 and coding ring A2A4S1. Contact 6 of A2A4S1-A establishes a ground path to X2 of turret drive relay A2A4K1. A2A4K1 energizes and applies +28 Vdc to turret drive motor A2A4B1. The energized motor then rotates the turret and the code ring. This action continues until all five code lines are open-circulated, at which time the ground path to turret drive relay A2A4K1 is broken. The turret is then positioned as required by the front panel MHz control settings. Band pass filters are contained in the motor-driven turret. The proper bandpass filters corresponding to the front panel frequency setting are selected as the turret assembly is mechanically positioned.

3-122. The five-line code applied to A2-A6A13 is converted to a four-line code (binary coded decimal) by BCD converter A2-A6A13U11. This four-line code establishes the injection frequency output from 10 MHz/1 MHz Synthesizer Subassembly A2A6-A13. Table 3-2 lists the five-line tuning code outputs generated by Code Generator Assembly A2A7 for both RF Amplifier Assembly A2A4 and 10 MHz/1 MHz Synthesizer Subassembly A2A6A13. Also listed in table 3-2 are five-line code outputs used for frequency band selection within the AM-3924C(P)/URT rf power amplifier.

3-123. Code Generator Assembly A2A7 also produces a single-line output applied to contact X1 of hi-lo band relay A2K2. The hi-lo band control output is an open or ground as listed in table 3-2. This causes A2K2 to apply +20 Vdc for all low band frequencies or ground for all high band frequencies through contact B2, to the RF Translator A2A6A8 and 100 kHz Synthesizer A2A6A17 subassemblies.

3-124. Mechanical selection of bandpass filter networks within RF Amplifier Assembly A2A4 occurs when the front panel 100 kHz and 10 kHz controls are positioned. Gears and chain drives couple the controls to 100 kHz and 10 kHz rotor assemblies in RF Amplifier Assembly A2A4. Chain-drive mechanisms are also used to couple the front panel 100 kHz, and 1 kHz controls to coding switches in Translator/Synthesizer Assembly A2A6. The coding switches convert the position of the kHz controls to individual four-line tuning codes for use in various subassemblies of Translator/Synthesizer Assembly A2A6.

3-125. The 100 Hz incremental tuning is accomplished by the front panel Hz control. It selects a four-line tuning code, consisting of grounds and +4.3 Vdc lines. These are applied to 1 kHz/10 kHz/100 Hz Synthesizer Subassembly A2A6A18. Tuning of the 1 kHz/10 kHz/100 Hz Synthesizer Subassembly A2A6A18 is described in paragraphs 3-80 and 3-81.

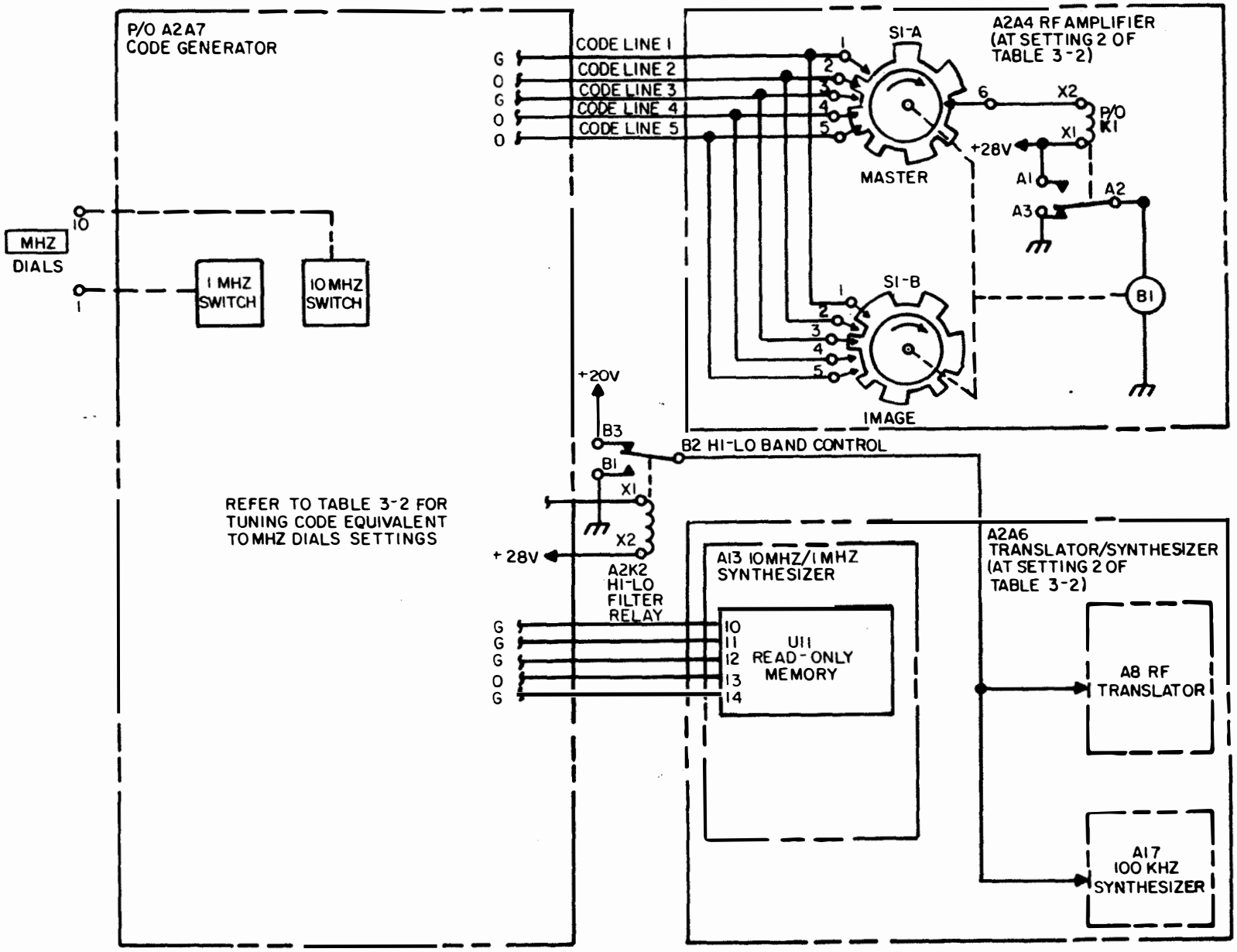


Figure 3-3. Radio Transmitter T-827H/URT, Tuning, Simplified Schematic Diagram

Table 3-2. Tuning Code Chart

MHz and 100 kHz CONTROL SETTING	A2A4 CODE LINES 1	2	3	4	5	A2K2 CONTROL LINE	A2A6A13 CODE LINES 1	2	3	4	5	ASSOCIATED EXTERNAL RF POWER AMPLIFIER (SUCH AS AM-3007B/URT) PASSBAND MHz	CODE LINES 1	2	3	4	5
2	G	O	G	O	O[1]	O	G	G	G	O	G	2.0 - 2.4999	O	O	O	O	G
2.5												2.5 - 2.9999	O	O	O	G	G
3.	O	G	O	O	O	O	G	O	G	G	G	3.0 - 3.4999	O	O	G	G	G
3.5												3.5 - 3.9999	O	G	G	G	G
4	G	O	O	O	G	O	G	G	O	G	G	4.0 - 4.9999	G	G	G	G	O
5	O	O	O	G	G	O	O	G	G	O	G	5.0 - 5.9999	G	G	G	O	G
6	O	O	G	G	O	G	O	G	O	O	O	6.0 - 6.9999	G	G	O	G	G
7	O	G	G	O	G	O	G	O	O	G	G	7.0 - 7.9999	G	O	G	G	G
8	G	G	O	G	G	O	G	G	O	O	G	8.0 - 9.9999	O	G	G	G	O
9	G	O	G	G	O	G	G	O	G	O	O						
10	O	G	G	O	O	G	G	G	O	G	O	10.0 - 11.9999	G	G	G	O	O
11	G	G	O	O	O	O	O	O	G	G	G						
12	G	O	O	O	O	O	O	O	O	G	G	12.0 - 13.9999	G	G	O	O	G
13	O	O	O	O	G	G	G	O	G	G	G						
14	O	O	O	G	O	O	O	G	G	G	O	14.0 - 15.9999	G	O	O	G	O
15	O	O	G	O	G	O	O	O	G	G	O						
16	O	G	O	G	G	O	G	G	G	G	O	16.0 - 17.9999	O	O	G	O	O
17	G	O	G	G	G	G	G	O	O	G	G						
18	O	G	G	G	G	G	G	G	O	O	G	18.0 - 19.9999	O	G	O	O	G
19	G	G	G	G	O	G	G	G	G	O	O						
20	G	G	G	O	O	G	O	G	G	G	G	20.0 - 21.9999	G	O	O	G	G
21	G	G	O	O	G	G	O	O	G	G	G						
22	G	O	O	G	O	O	O	O	O	O	G	22.0 - 23.9999	O	O	G	G	O
23	O	O	G	O	O	O	G	G	G	G	O						
24	O	G	O	O	G	G	O	G	G	G	O	24.0 - 25.9999	O	G	G	O	O
25	G	O	O	G	G	G	O	O	G	G	O						
26	O	O	G	G	G	G	G	G	G	G	O	26.0 - 27.9999	G	G	O	O	O
27	O	G	G	G	O	O	O	O	O	G	G						
28	G	G	G	O	G	O	O	O	G	G	G	28.0 - 29.9999	G	O	O	O	O
29	G	G	O	G	O	O	O	G	G	G	G						

[1] "O" indicates open; "G" indicates ground.

3-126. CIRCUIT LEVEL DESCRIPTIONS.

3-127. GENERAL. The following paragraphs describe the circuits contained in the maintenance schematic diagrams of individual assemblies and subassemblies of the T-827H/URT. The descriptions are in assembly and subassembly alphanumeric order. Descriptions are brief where circuits are conventional and circuit theory is covered in NAVSHIPS 0967-LP-000-0120. Full descriptions are provided for unconventional circuits and peculiar applications of conventional circuits. Figures 3-4 through 3-32 are simplified schematics or functional block diagrams of integrated circuits (ICs) used in the T-827H/URT. In those cases where an IC contains multiple identical circuits, such as M38510/00104 in figure 3-4, the typical circuit will be shown once and a circuit matrix chart will indicate the pertinent pin differences. For example, circuit 1 of figure 3-4 has pins 1 and 2 as inputs A and B, respectively, with pin 3 being output C. For circuit 2, pins 4 and 5 are the inputs, and pin 6 is the output, etc.

3-128. TRANSMITTER CASE A1 (Figure 5-28). The Transmitter Case A1 houses Transmitter Main Frame A2, Filter Box Assembly A1A1, and miscellaneous electronic components.

3-129. FILTER BOX ASSEMBLY A1A1 (Figure 5-28). Filter Box Assembly A1A1 is mounted at the rear of the T-827H/URT Case A1. A1A1 houses feed-through capacitors used to filter incoming and outgoing signals. It also contains six connectors which function as follows:

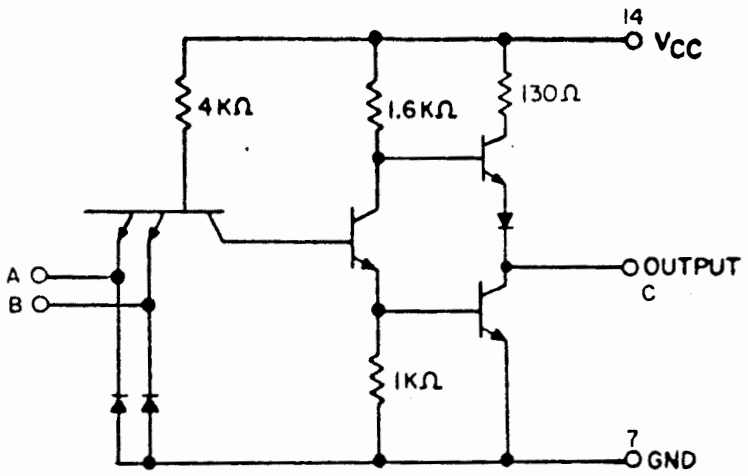
J3	115 Vac Auxiliary Supply Input
J4	APC, TGC, and PPC inputs Carrier +20V input Remote Modulation inputs, (voice modes) Remote TTY inputs Remote +12 Vdc inputs CW/RATT Ground CW/RATT Keyline input
J5	Auxiliary USB/AM/ISB Input
J6	Auxiliary LSB/ISB input
J7	Local TTY inputs (+ and -) Local RATT keyline input
J8	Data Audio input Data Keyline input

3-130. TRANSMITTER MAIN FRAME A2. Main frame A2 includes the front panel, the chassis on which the plug-in assemblies are mounted, and other electronic components. Schematic diagram Figure 5-28 shows the wiring of control and hard-wired assemblies in Main Frame A2 and Case A1. The hard-wired assemblies include Power Supply Assembly A2A8, Meter Amplifier Assemblies A2A10 and A2A11, Handset Filter Assembly A2A14, IF Filter Assembly A2A15, and Audio Interconnect Assembly A2A21. The case and main frame schematic diagram also shows the Filter Box Assembly A1A1, AUX/NORM switch A1S1, interlock switch A1S2, and all jacks and connectors mounted on the rear of Case A1.

3-131. Information on the primary and secondary signal flow between assemblies of the main frame is provided by the T-827H/URT overall functional block diagram (Figure 3-1), the signal flow diagrams (Figures 5-1 through 5-11), and the control and power distribution diagrams (Figures 5-12 through 5-15). Figure 5-18 provides connection and wiring information on the main frame interconnections, and may be used when following a signal path through the T-827H/URT.

3-132. LOCAL/REMOTE switch A2S1 and MODE SELECTOR switch A2S2 sections are shown in the Figure 5-28 schematic diagram at locations near the point where the section is connected. Complete views of A2S1 and A2S2 switch sections are included on sheet 1 of Figure 5-28. Circuits for individual controls and relays on the main frame are described in paragraphs pertaining to the circuits they control. The circuits involving the hard-wired assemblies are described on the following pages.

3-133. Input and Output Filtering. Sheets 1 and 3 of Figure 5-28 show the entry and exit connectors and feed-through capacitors in Filter Box Assembly A1A1. Filtering is applied to signal inputs and outputs to prevent unwanted mixing of radio and



TRUTH TABLE

INPUT		OUTPUT
A	B	C
L	L	H
H	L	H
L	H	H
H	H	L

Positive logic $Y = \overline{AB}$
H = HIGH LEVEL
L = LOW LEVEL

CKT	A	B	C
1	1	2	3
2	4	5	6
3	9	10	8
4	12	13	11

QUAD DEVICE.
ONE CKT SHOWN.
TABLE INDICATES
PIN CONNECTIONS FOR
ALL FOUR CIRCUITS.

Figure 3-4. Integrated Circuit, Quadruple, 2-Input Positive NAND Gate, M38510/00104 (5400), Simplified Schematic Diagram

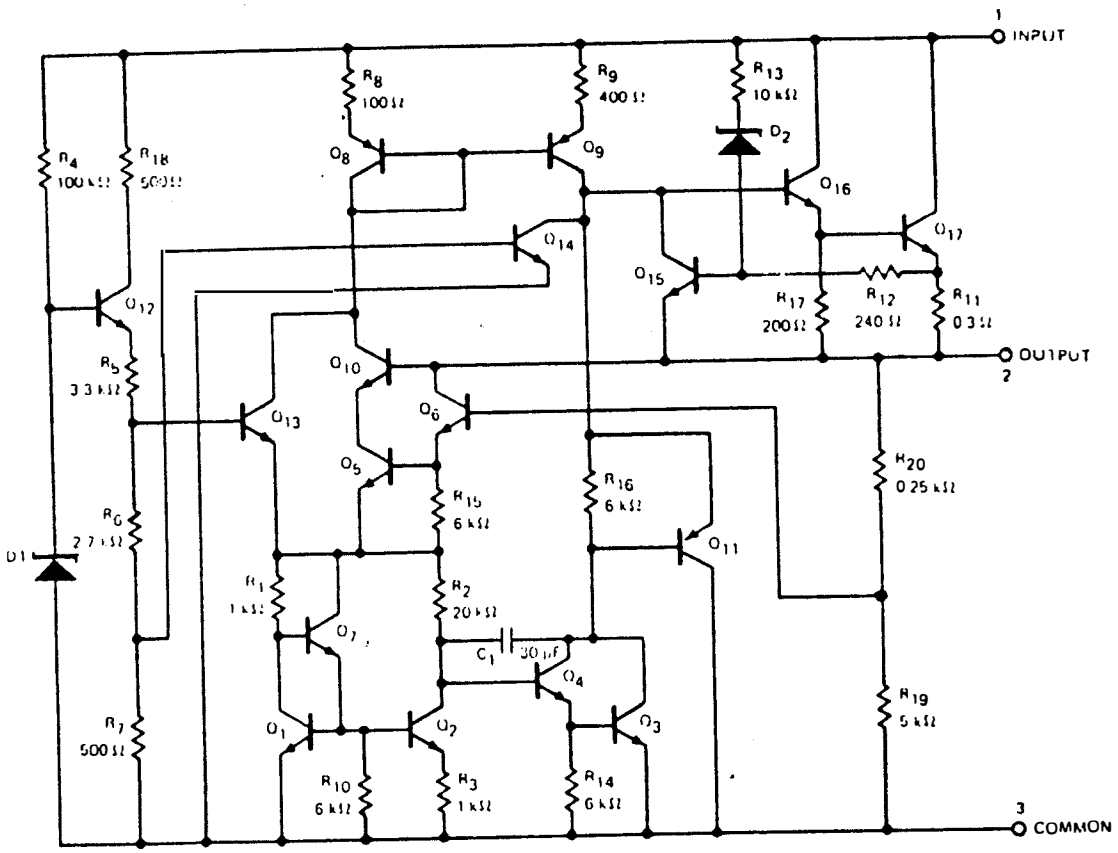
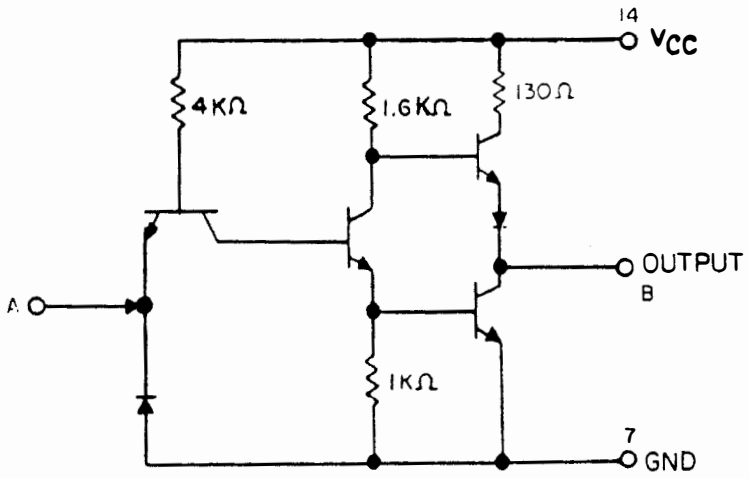


Figure 3-5. Integrated Circuits, Voltage Regulators, 78M05HMQB (48P226600-01), 78M20HMQB (48P226600-02), SG7815T/883B (48P226600-03), Simplified Schematic Diagram



CKT	A	B
1	1	2
2	3	4
3	5	6
4	9	8
5	11	10
6	13	12

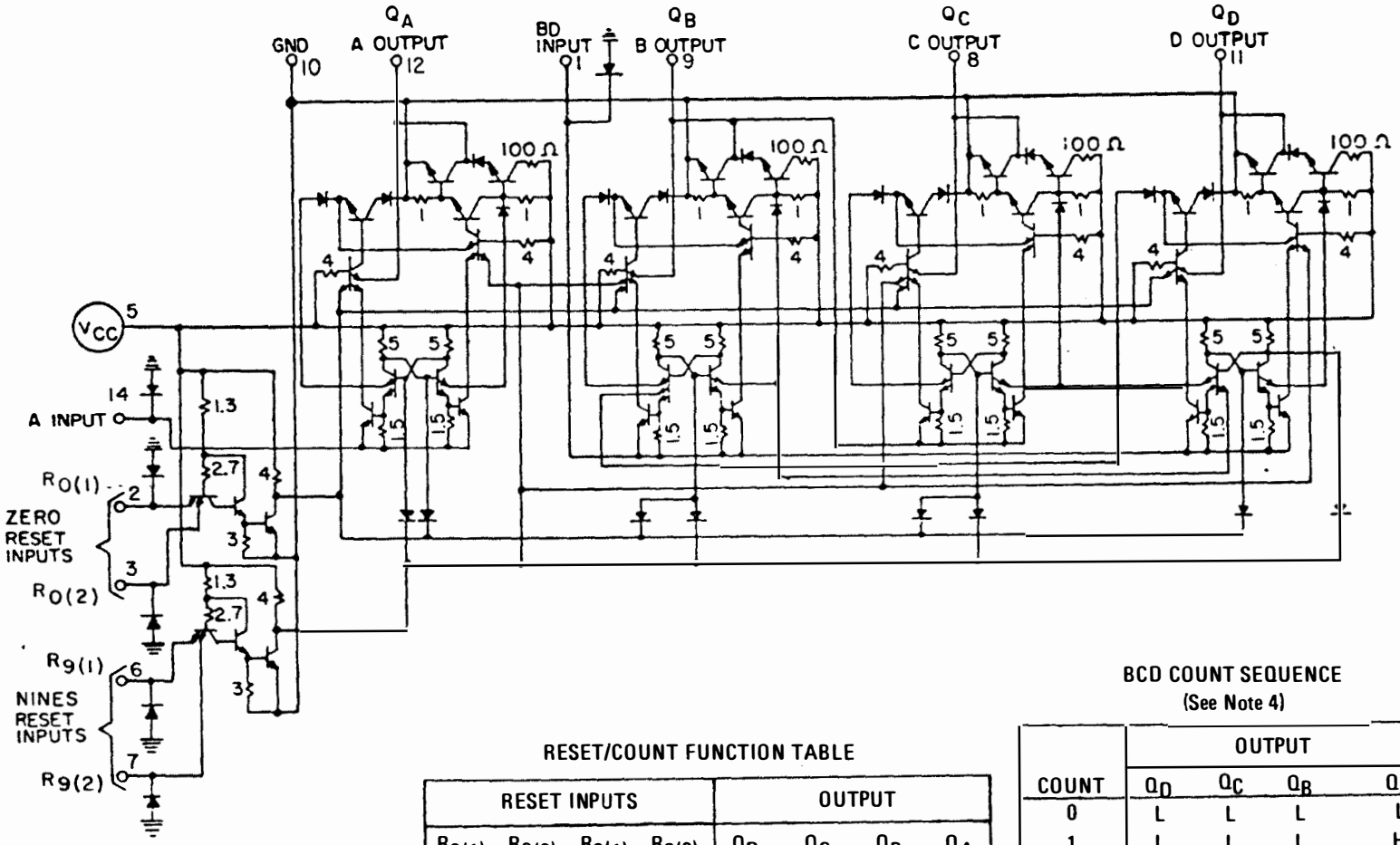
HEX DEVICE.
ONE CIRCUIT SHOWN.
TABLE INDICATES
PIN CONNECTIONS FOR
ALL SIX CIRCUITS.

TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

Postive logic $Y = \overline{A}$
H = HIGH LEVEL
L = LOW LEVEL

Figure 3-6. Integrated Circuit, Hex, 1-Input Inverter Gate, M38510/00105 (5404), Simplified Schematic Diagram



NOTES:

1. Unless otherwise specified, resistor values are in kilohms.
2. Component values shown are nominal.
3. Pins 4 and 13 not connected.
4. Output Q_A is connected to input B for BDC count.
5. H = HIGH LEVEL; L = LOW LEVEL.

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{O(1)}$	$R_{O(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

BCD COUNT SEQUENCE
(See Note 4)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Figure 3-7. Integrated Circuit, High Speed Decade Counter, M38510/01307 (5490), Simplified Schematic Diagram

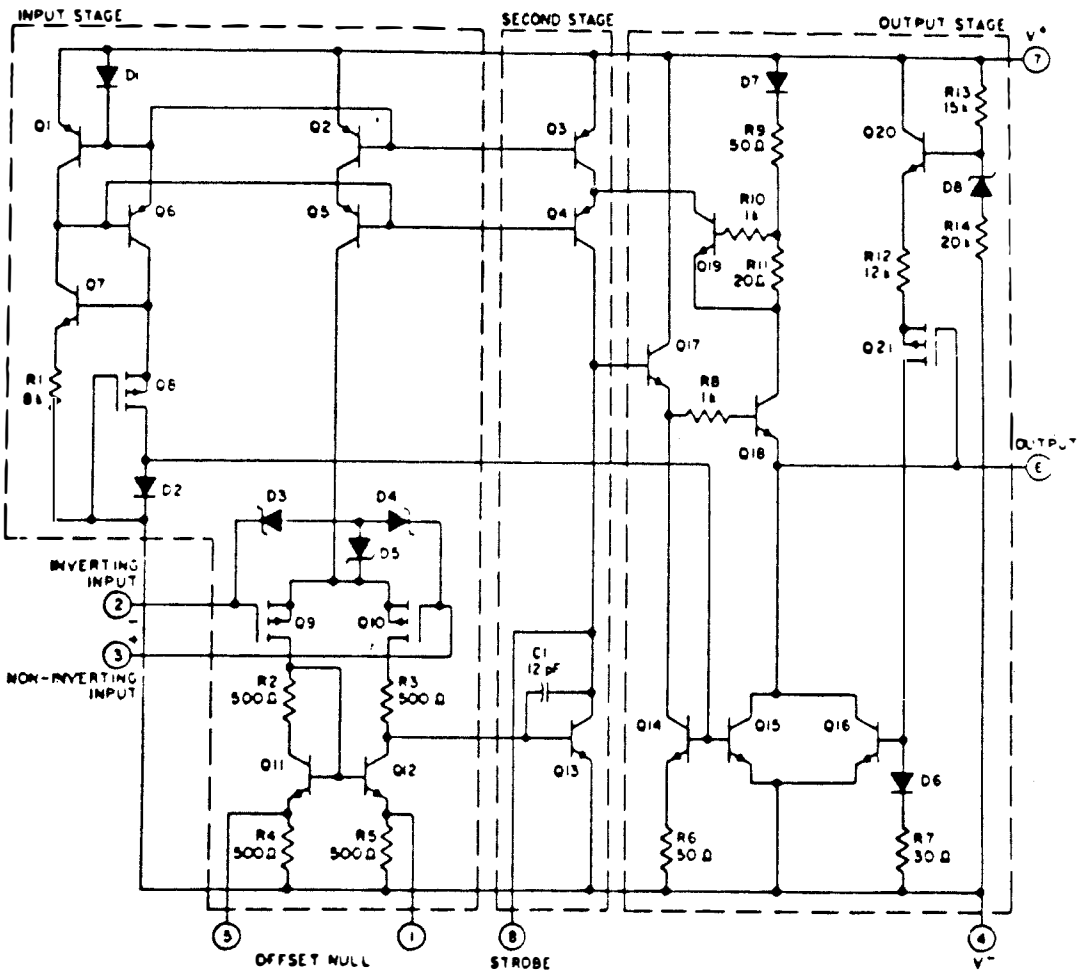


Figure 3-8. Integrated Circuit, Operational Amplifier, CA3140S/3 (48P226682-01), Simplified Schematic Diagram

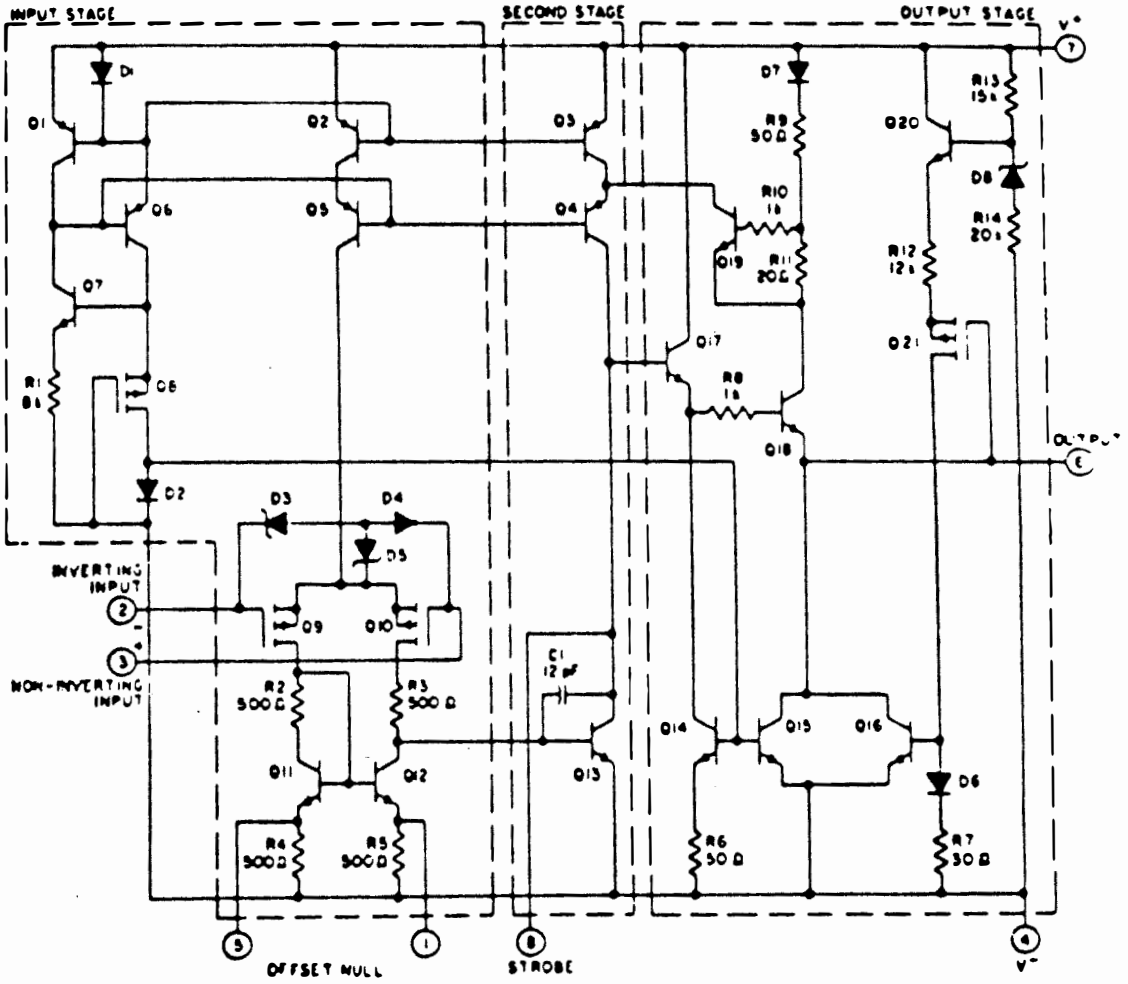
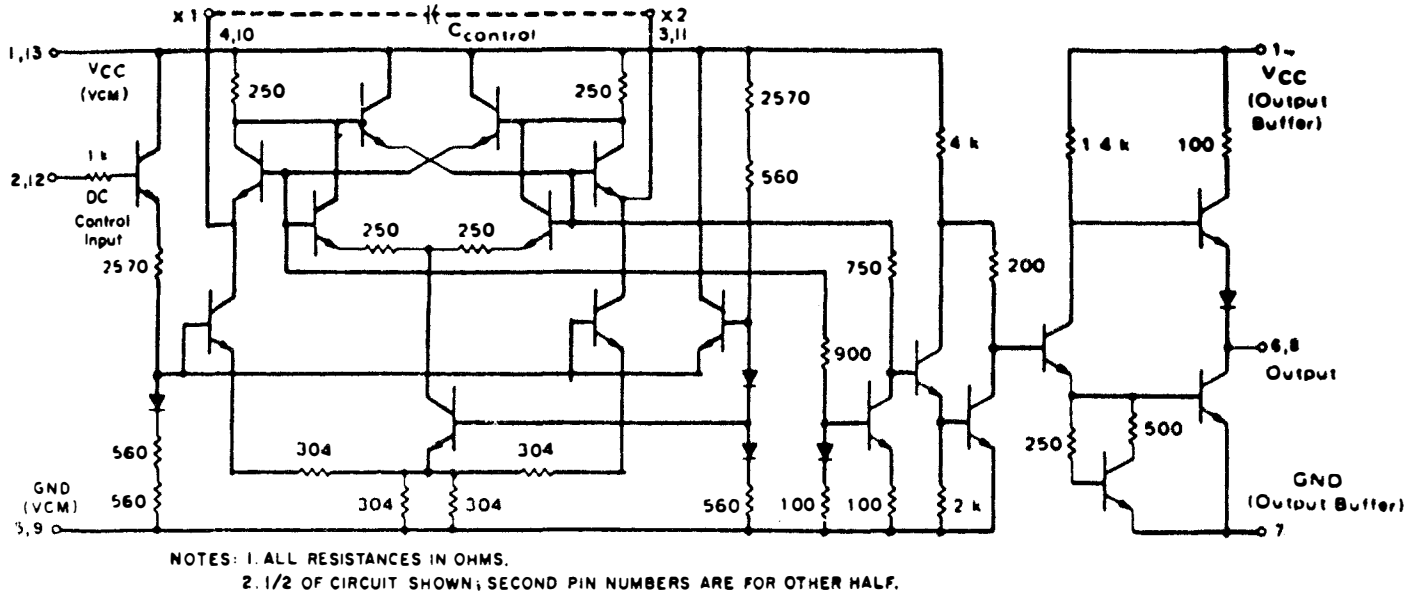
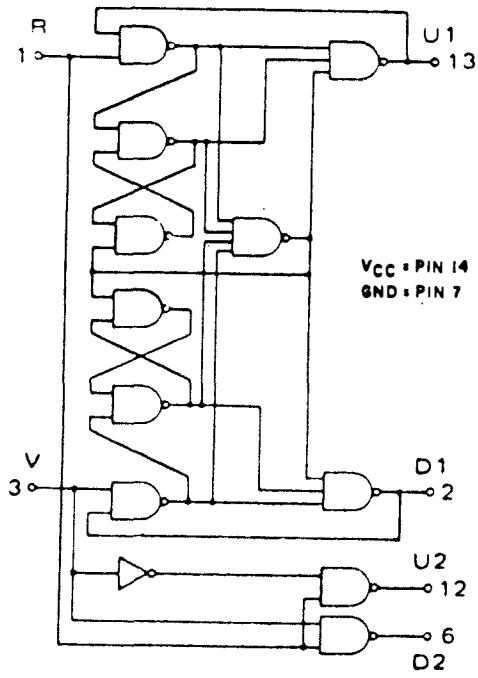


Figure 3-8. Integrated Circuit, Operational Amplifier, CA3140S/3 (98738/48P226682-01) Alt. (50097/C31312-001), Simplified Schematic Diagram



NOTES: 1. ALL RESISTANCES IN OHMS.
2. 1/2 OF CIRCUIT SHOWN; SECOND PIN NUMBERS ARE FOR OTHER HALF.

Figure 3-9. Integrated Circuit, Dual Voltage-Controlled Multivibrator, MC4324BCBJS (50097/C31357-001), Simplified Schematic Diagram

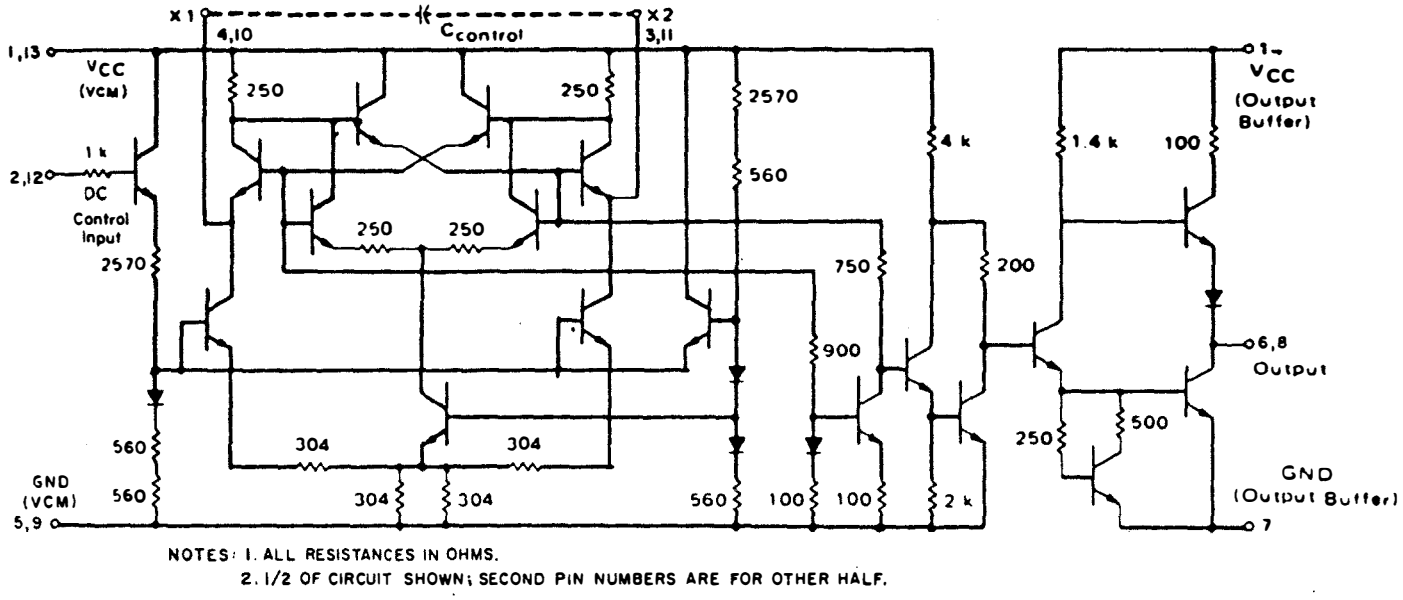


INPUT STATE	INPUT		OUTPUT			
	R	V	U1	D1	U2	D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

U1 and D1 outputs are sequential; i.e., they must be sequenced in the order shown.

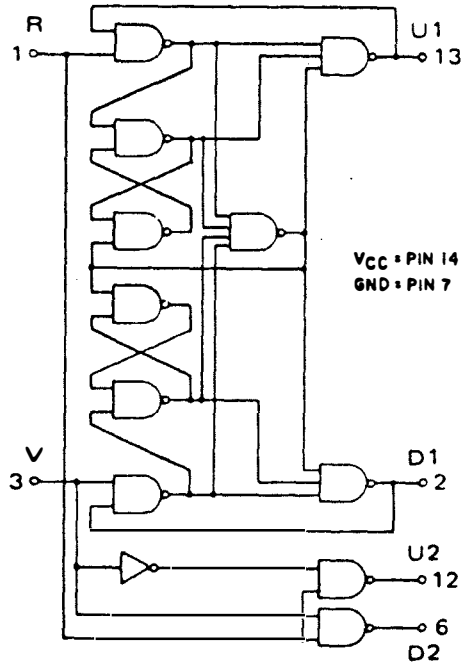
U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.
X = Irrelevant

Figure 3-10. Integrated Circuit, Phase Detector, MC4344DCBS (98738/48P226446-01) Alt. MC4344BCBJS (50097/C31351-001), Logic Diagram



NOTES: 1. ALL RESISTANCES IN OHMS.
2. 1/2 OF CIRCUIT SHOWN; SECOND PIN NUMBERS ARE FOR OTHER HALF.

Figure 3-9. Integrated Circuit, Dual Voltage-Controlled Multivibrator, MC4324DCBS (48P226457-01), Simplified Schematic Diagram

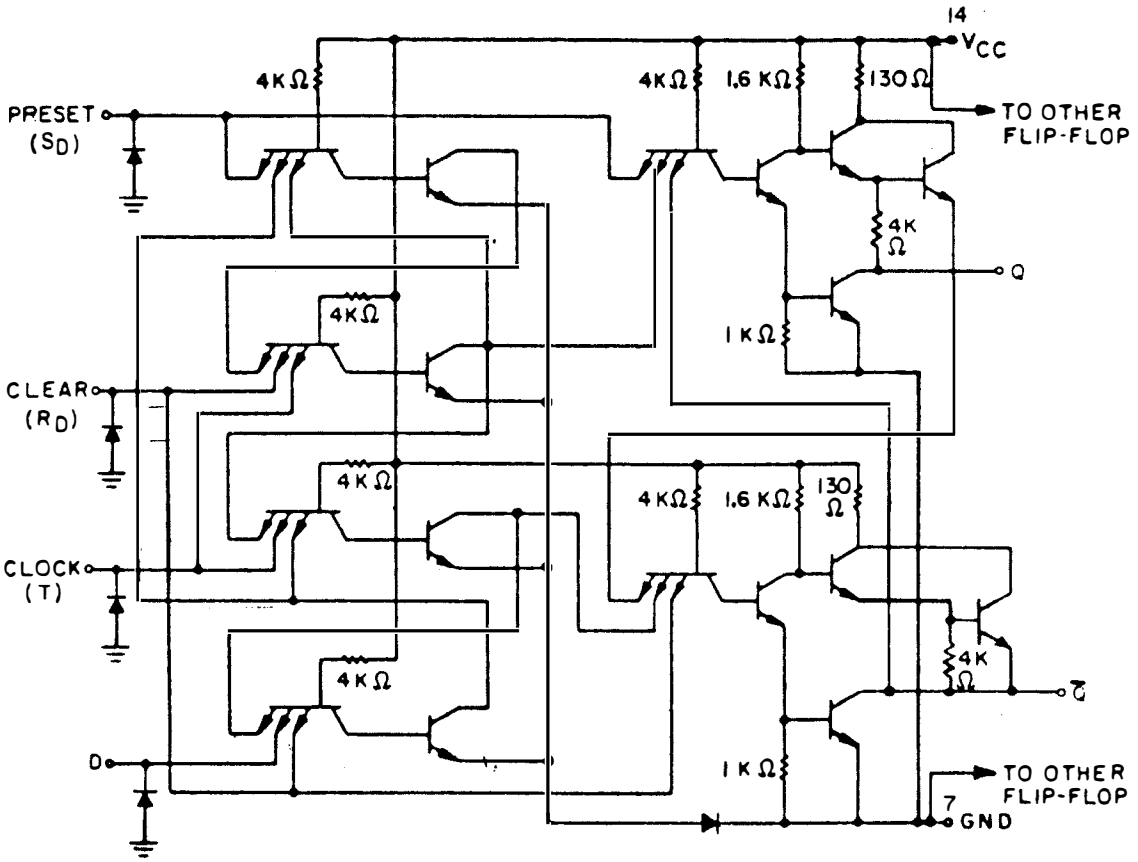


INPUT STATE	INPUT R	INPUT V	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

U1 and D1 outputs are sequential; i.e., they must be sequenced in the order shown.

U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.
X = Irrelevant

Figure 3-10. Integrated Circuit, Phase Detector, MC4344DCBS (48P226446-01), Logic Diagram



TRUTH TABLE

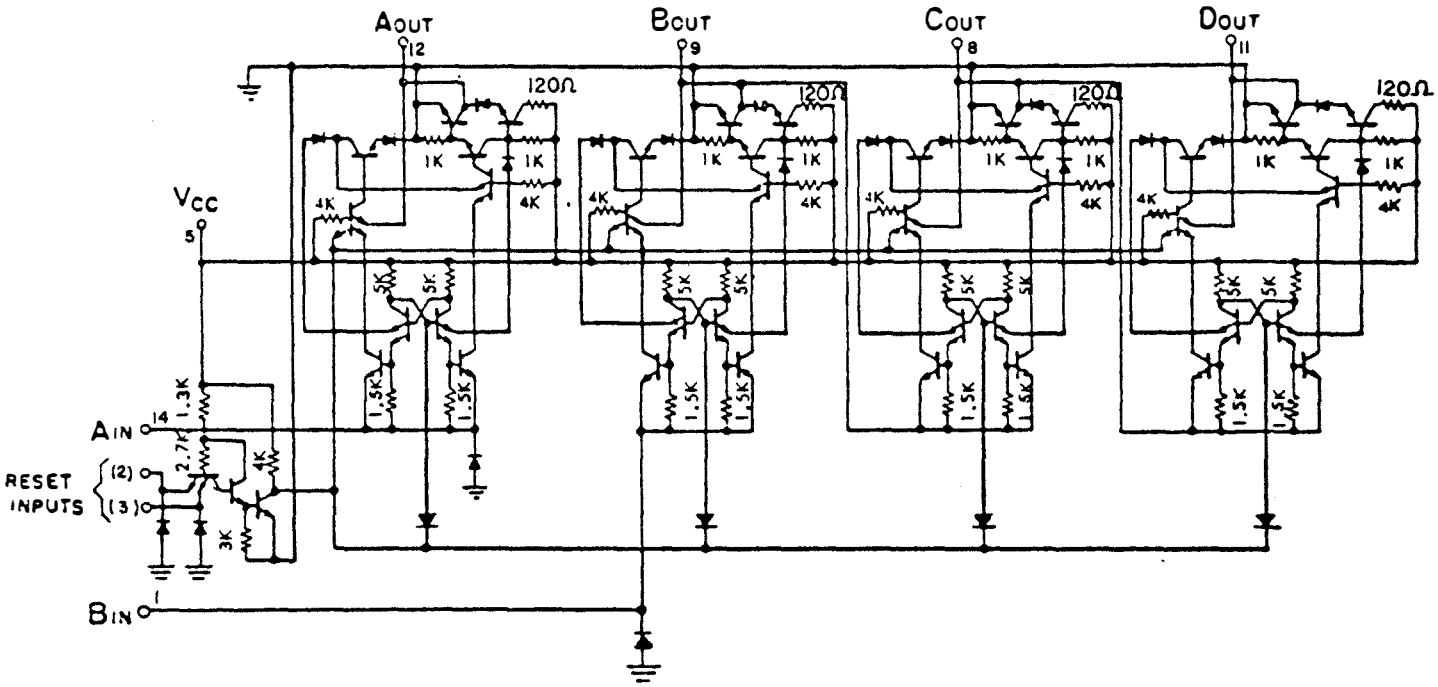
INPUT	OUTPUTS	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH LEVEL;
L = LOW LEVEL

CKT	D	T	R_D	S_D	Q	$\overline{Q}$
1	2	3	1	4	5	6
2	12	11	13	10	9	8

DUAL DEVICE.
ONE CIRCUIT SHOWN.
TABLE INDICATES
PIN CONNECTIONS
FOR BOTH CIRCUITS.

Figure 3-11. Integrated Circuit, Dual D-Type Edge-Triggered Flip-Flop, M38510/00205 (5474), Simplified Schematic Diagram



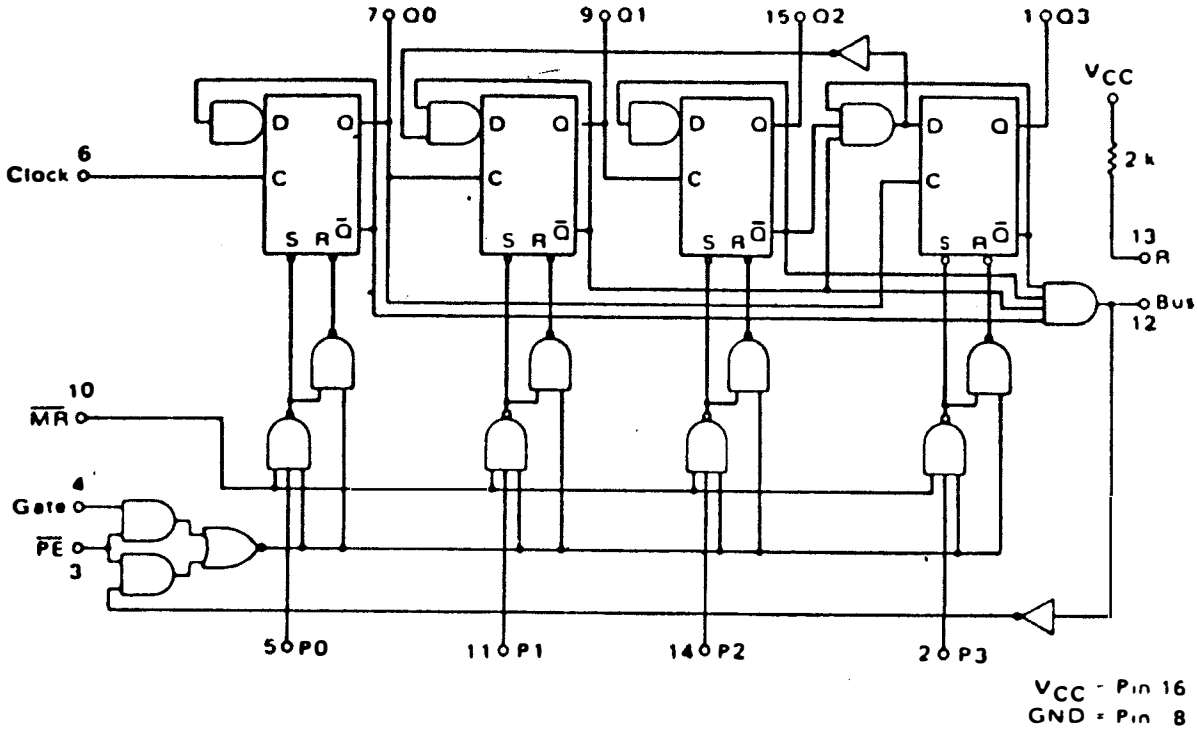
FUNCTION TABLE

COUNT	OUTPUT D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES:

1. Output A connected to input B.
2. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
3. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.
4. H = HIGH LEVEL; L = LOW LEVEL
5. Component values shown are typical.
6. GNO = Pin 10

Figure 3-12. Integrated Circuit, 4-Bit Binary Counter, M38510/01302 (5493), Simplified Schematic Diagram

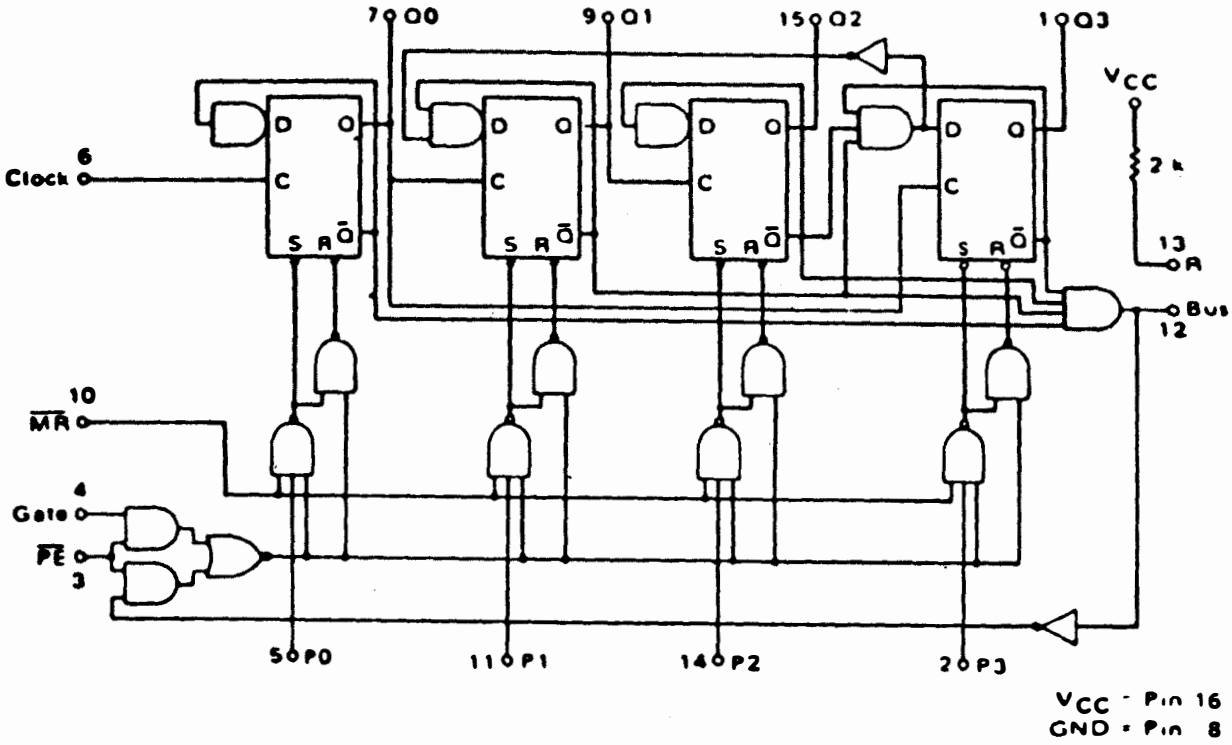


FUNCTION TABLE

	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

1 = OPEN CIRCUIT; 0 = GROUND
COUNTER PROGRAMMED FOR
÷8 OPERATION

Figure 3-13. Integrated Circuit, Programmable Modulus N Decade Counter, MC544416DEBS (48P226460-01) Functional Block Diagram

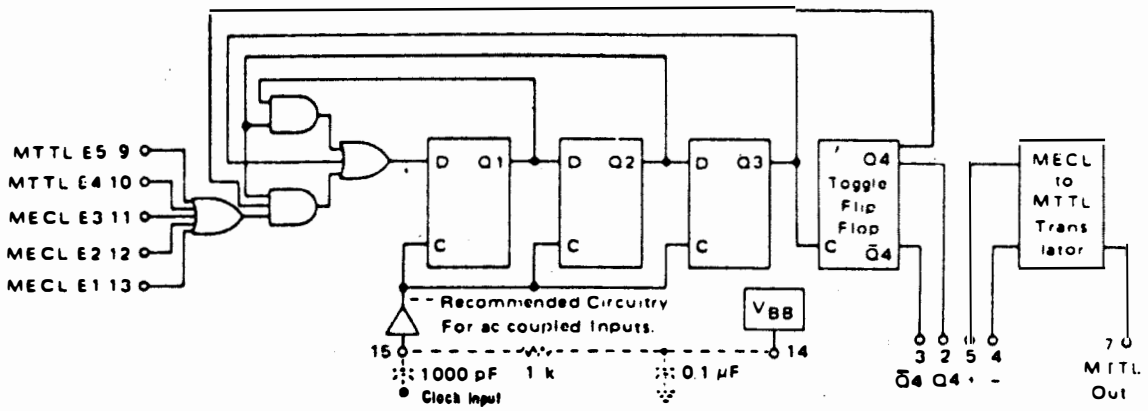


FUNCTION TABLE

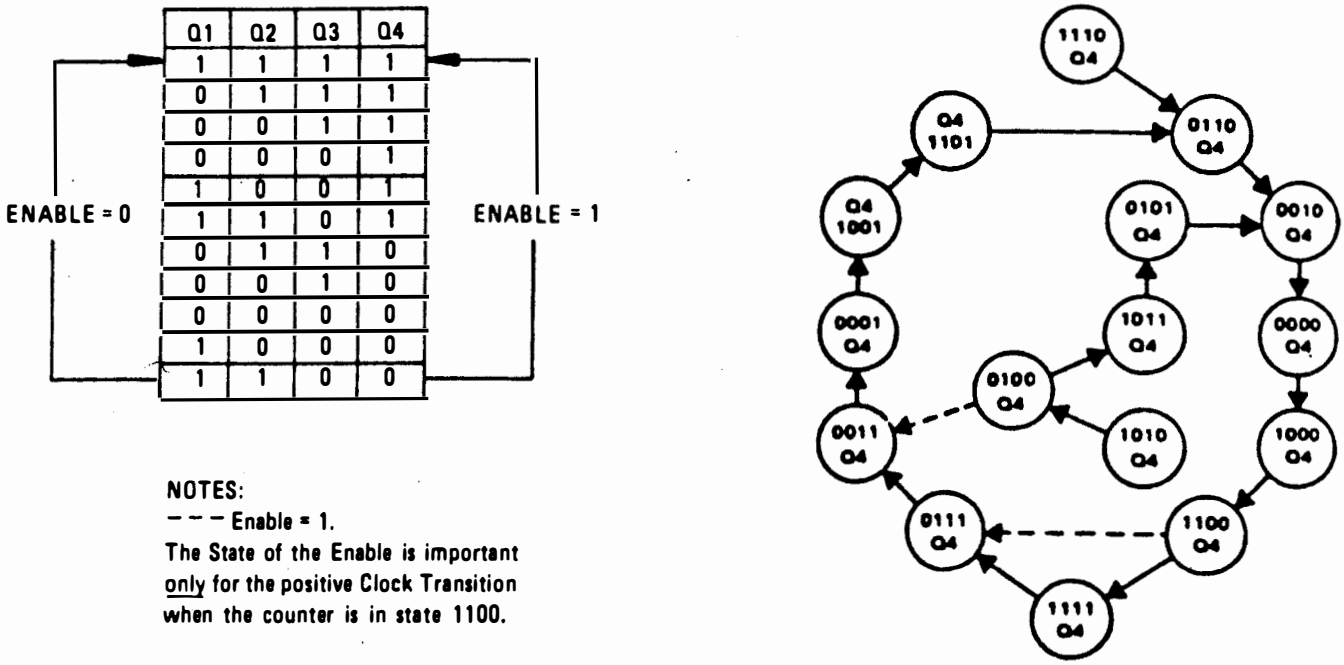
COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

1 = OPEN CIRCUIT; 0 = GROUND
COUNTER PROGRAMMED FOR
÷8 OPERATION

Figure 3-13. Integrated Circuit, Programmable Modulus N Decade Counter, MC4316DEBS (98738/48P226460-01) Alt. MC4316BEBJS (50097/C31355-001), Functional Block Diagram

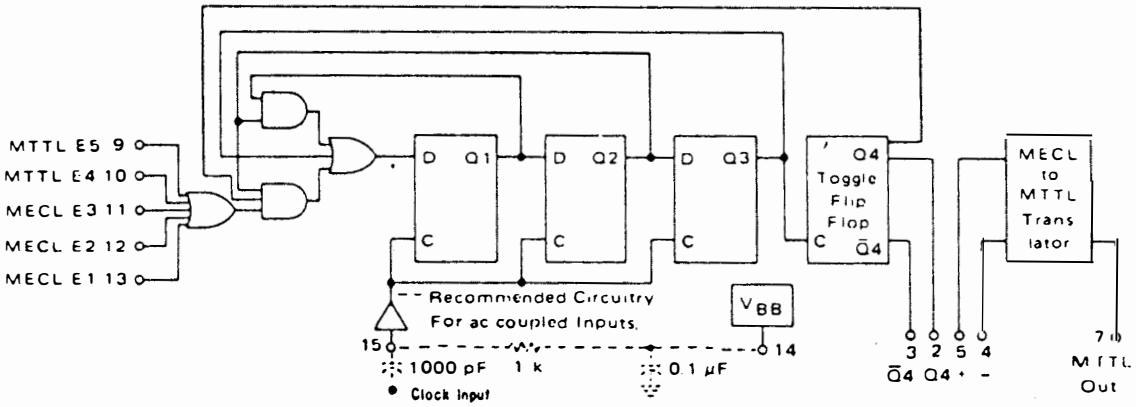


STATE DIAGRAM



NOTES:
– – – Enable = 1.
The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

Figure 3-14. Integrated Circuit, MC12513DEBS (98738/48P226458-01) Alt. MC12513BEBJS (50097/C31358-001), Logic Diagram

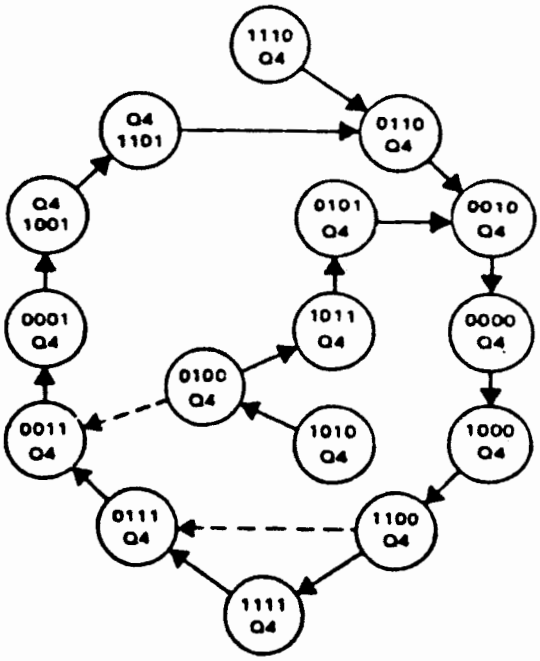


STATE DIAGRAM

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

ENABLE = 0

ENABLE = 1



NOTES:
– – – Enable = 1.
The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

Figure 3-14. Integrated Circuit MC12513DEBS (48P226458-01), Logic Diagram

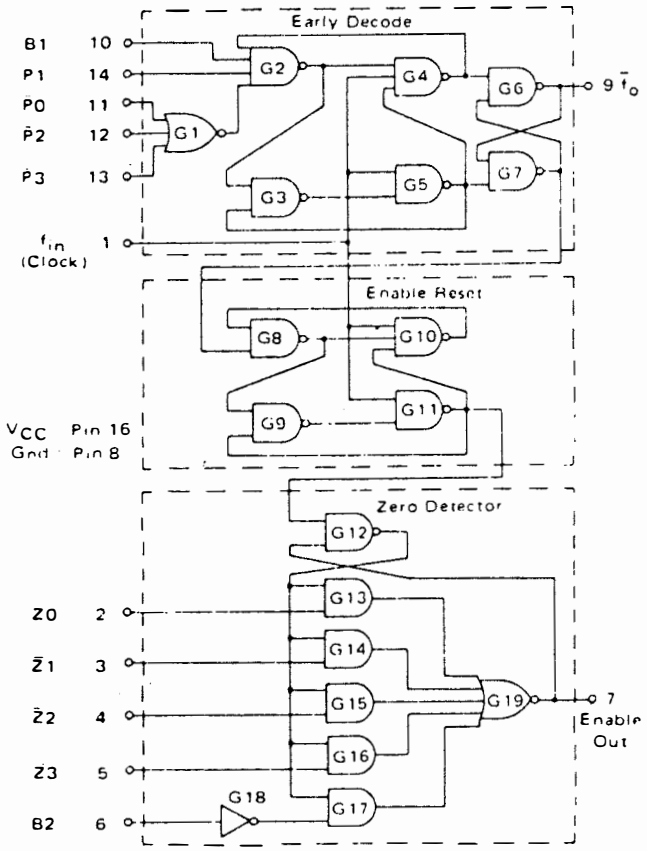


Figure 3-15. Integrated Circuit MC12514DEBS (48P226459-01), Logic Diagram

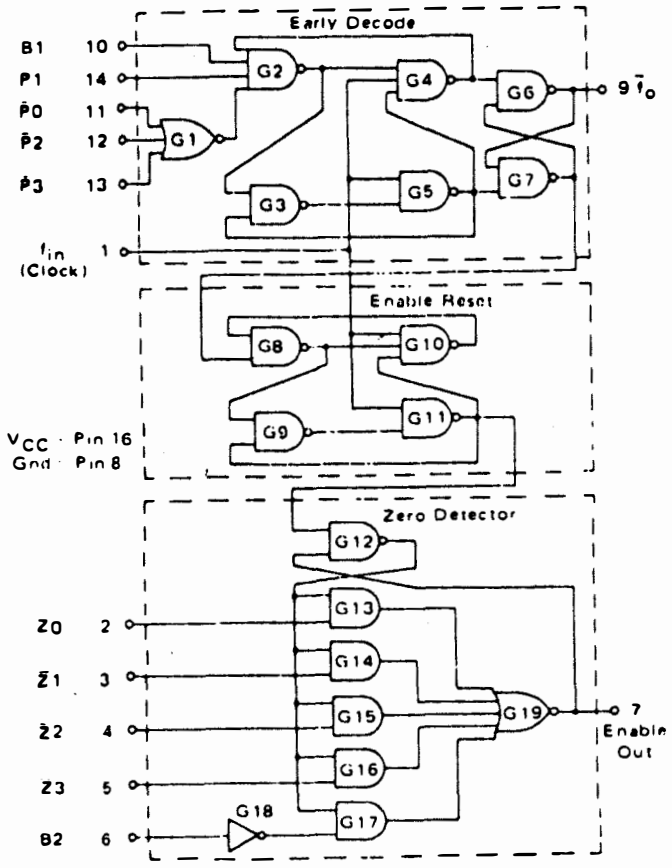
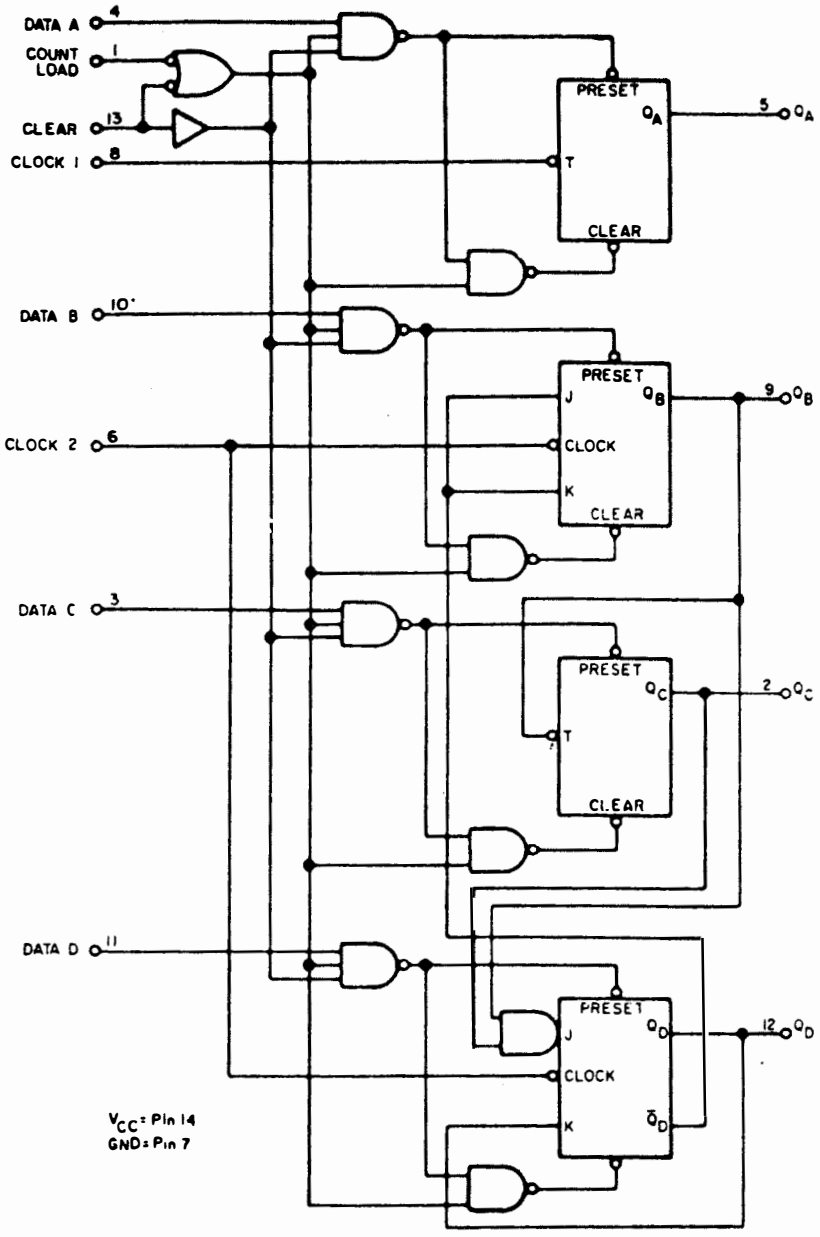


Figure 3-15. Integrated Circuit, MC12514DEBS (98738/48P226459-01), Alt. MC12514BEBJS (50097/C31354-001), Logic Diagram

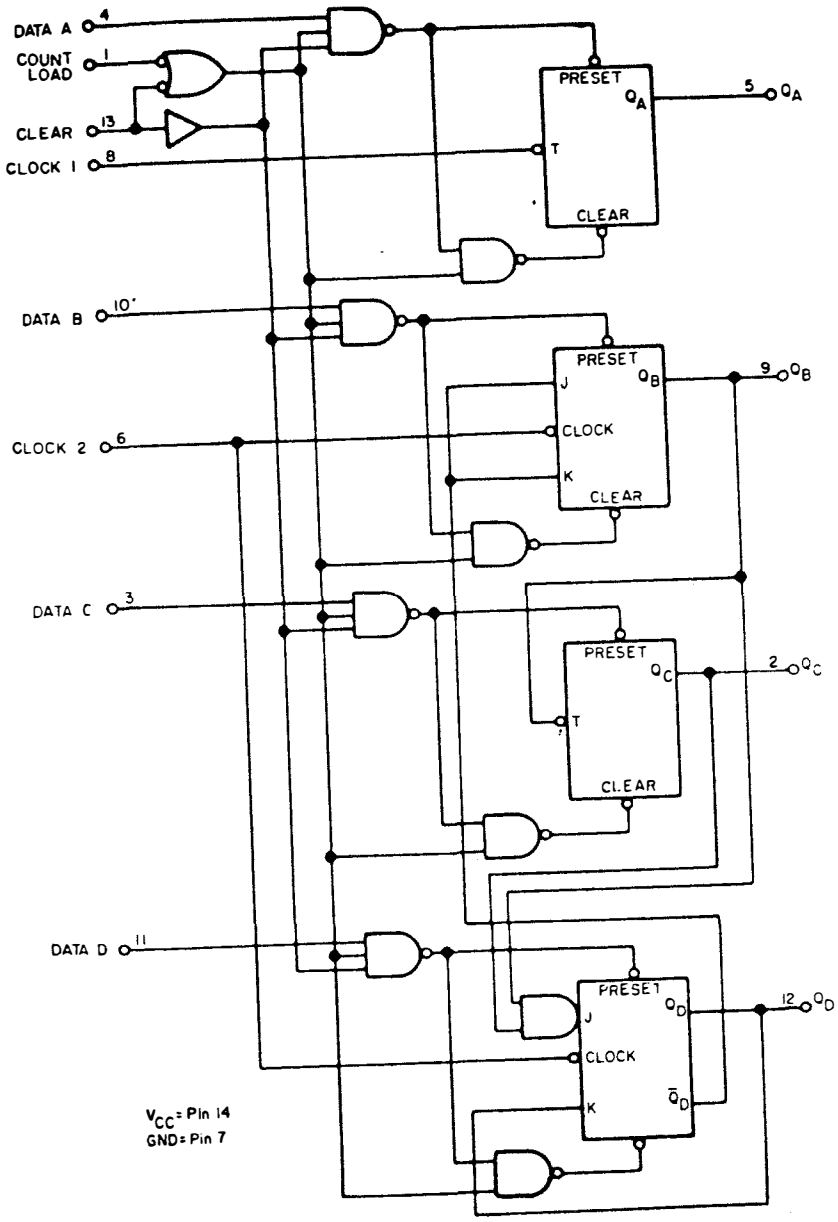


FUNCTION TABLE
DECADE (BCD)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = HIGH LEVEL;
L = LOW LEVEL
Output Q_A connected to clock - 2 input.

Figure 3-16. Integrated Circuit, Programmable Decade (BCD) Counter, SNC54196J (98738/48P226449-01) Alt. SNJ54196J (50097/C31311-002), Functional Block Diagram

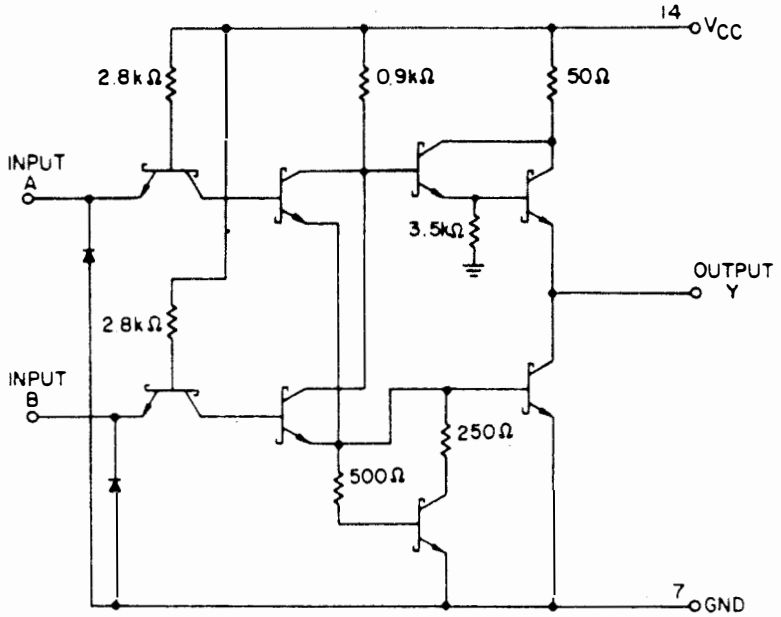


FUNCTION TABLE
DECADE (BCD)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = HIGH LEVEL;
L = LOW LEVEL
Output Q_A connected to clock - 2 input.

Figure 3-16. Integrated Circuit, Programmable Decade (BCD) Counter, SNC54196J (48P226449-01), Functional Block Diagram



CKT	A	B	Y
1	2	3	1
2	5	6	4
3	8	9	10
4	11	12	13

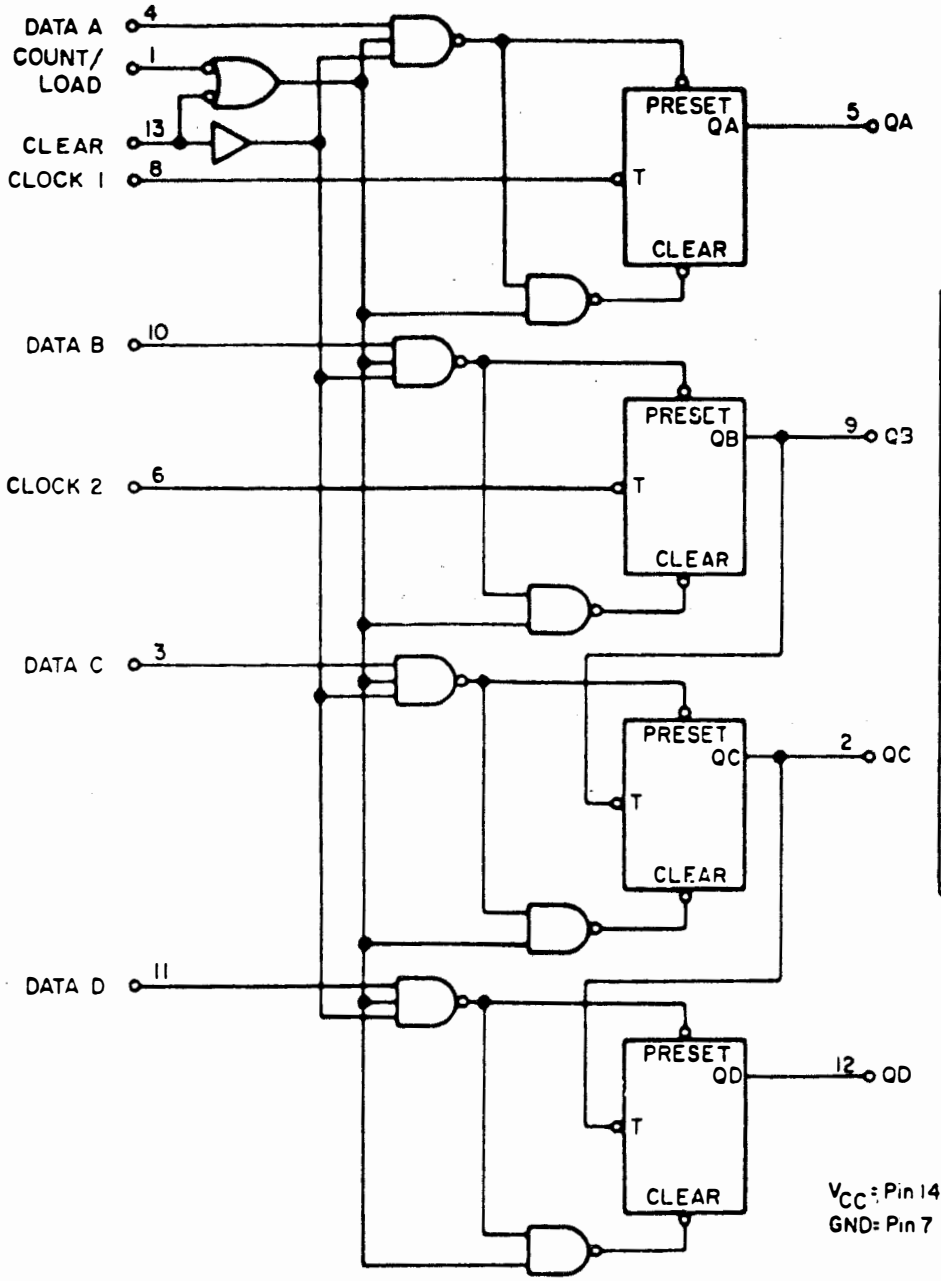
QUAD DEVICE.
ONE CIRCUIT SHOWN.
TABLE INDICATES
PIN CONNECTIONS FOR
ALL FOUR CIRCUITS.

TRUTH TABLE

A	B	Y
H	L	L
L	H	L
H	H	L
L	L	H

H = HIGH LEVEL;
L = LOW LEVEL

Figure 3-17. Integrated Circuit, Quad 2-Input NOR Gate, SNC54S02J (48P226451-01), Simplified Schematic Diagram

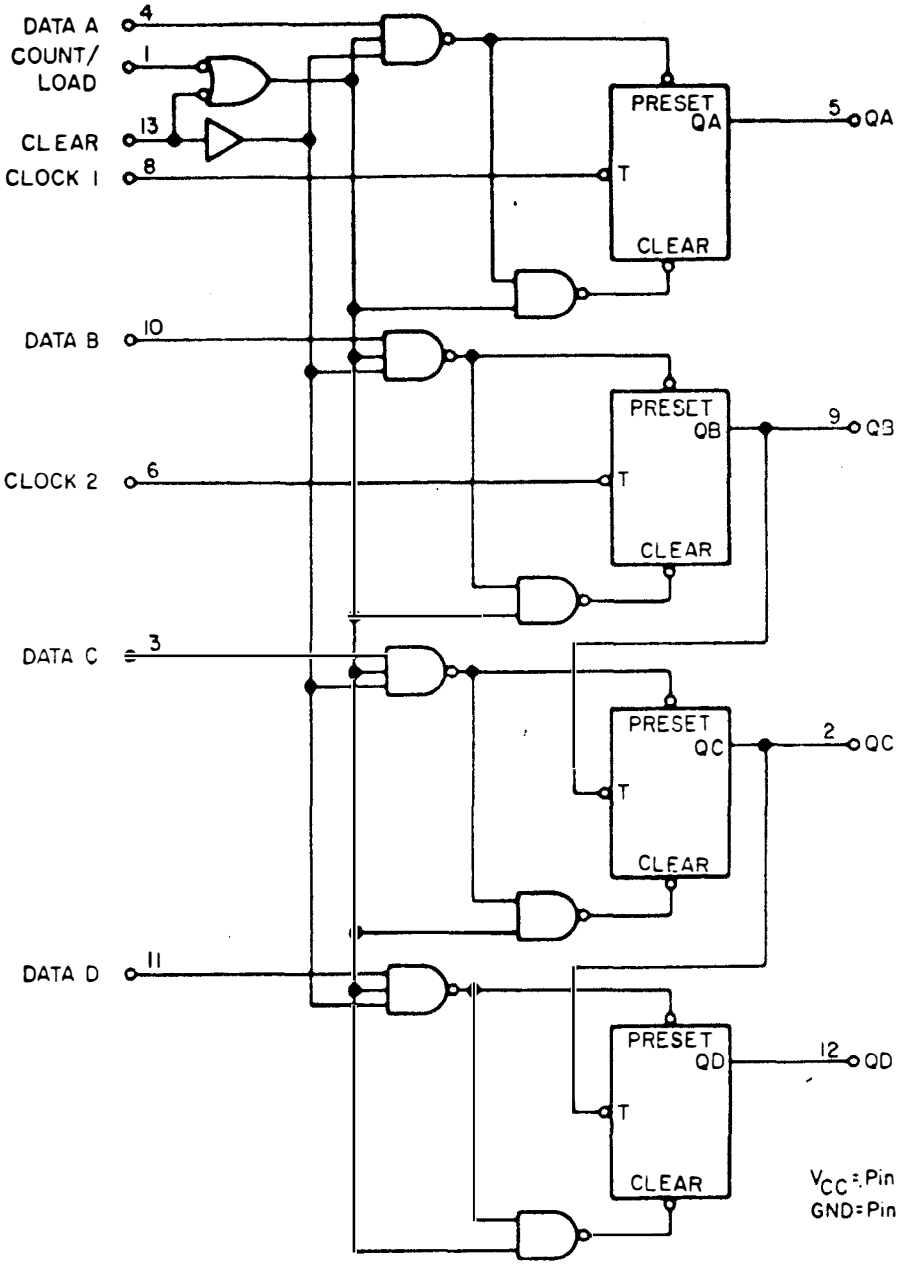


FUNCTION TABLE

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH LEVEL;
L = LOW LEVEL
Output Q_A connected to clock - 2 input.

Figure 3-18. Integrated Circuit, Programmable Binary Counter, SNC54197J (98738/48P226455-01) Alt. SNJ54197J (50097/C31353-001), Functional Block Diagram

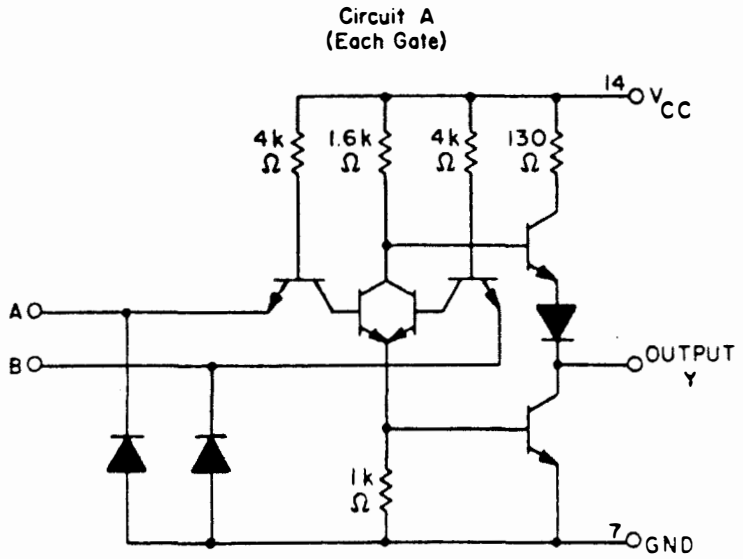


FUNCTION TABLE

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH LEVEL;
L = LOW LEVEL
Output Q_A connected to clock · 2 input.

Figure 3-18. Integrated Circuit, Programmable Binary Counter, SNC54197J (48P226455-01), Functional Block Diagram



TRUTH TABLE

A	B	Y
H	L	L
L	H	L
H	H	L
L	L	H

H = HIGH LEVEL;
L = LOW LEVEL

QUAD DEVICE.
ONE CIRCUIT SHOWN.
TABLE INDICATES PIN CONNECTIONS FOR ALL FOUR CIRCUITS.

CIRCUITS A AND B INDICATE DIFFERENT INTERNAL VALUES FOR DIFFERENT VENDORS.

CKT	A	B	Y
1	2	3	1
2	5	6	4
3	8	9	10
4	11	12	13

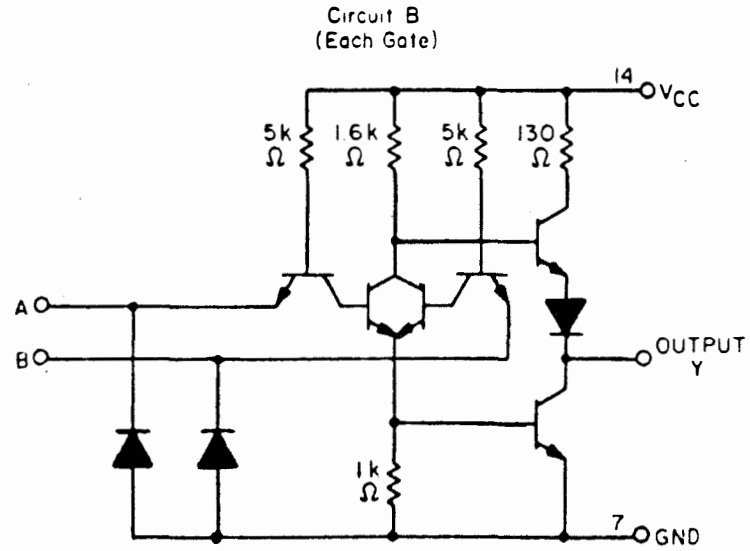


Figure 3-19. Integrated Circuit, Quadruple 2-Input Positive NOR Gate, M38510/00401 (5402), Simplified Schematic Diagram

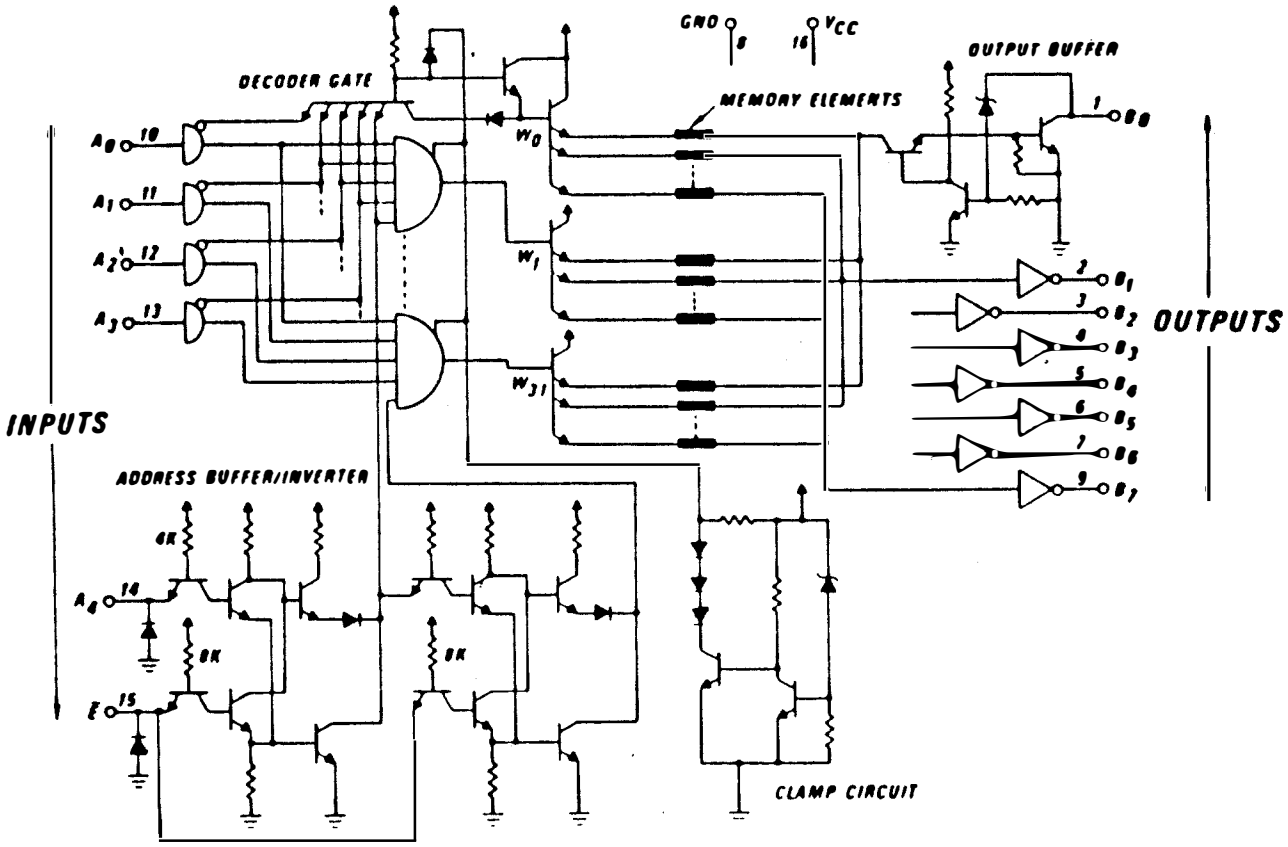


Figure 3-20. Integrated Circuit, Programmed Read-Only Memory, CC4335F (48P226463-01), Simplified Schematic Diagram

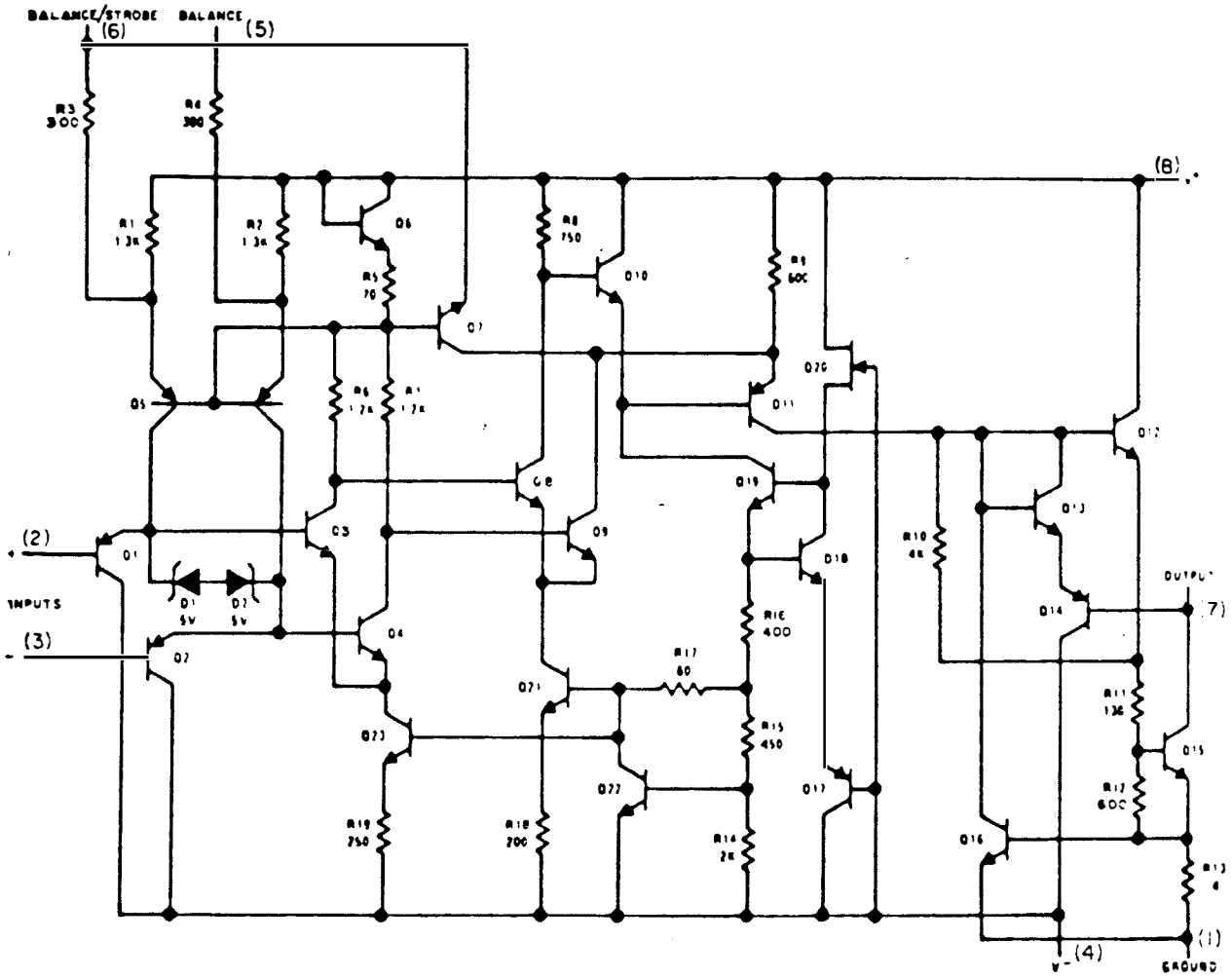


Figure 3-21. Integrated Circuit, Precision Voltage Comparator/Buffer, M38510/10304 (LM111), Simplified Schematic Diagram

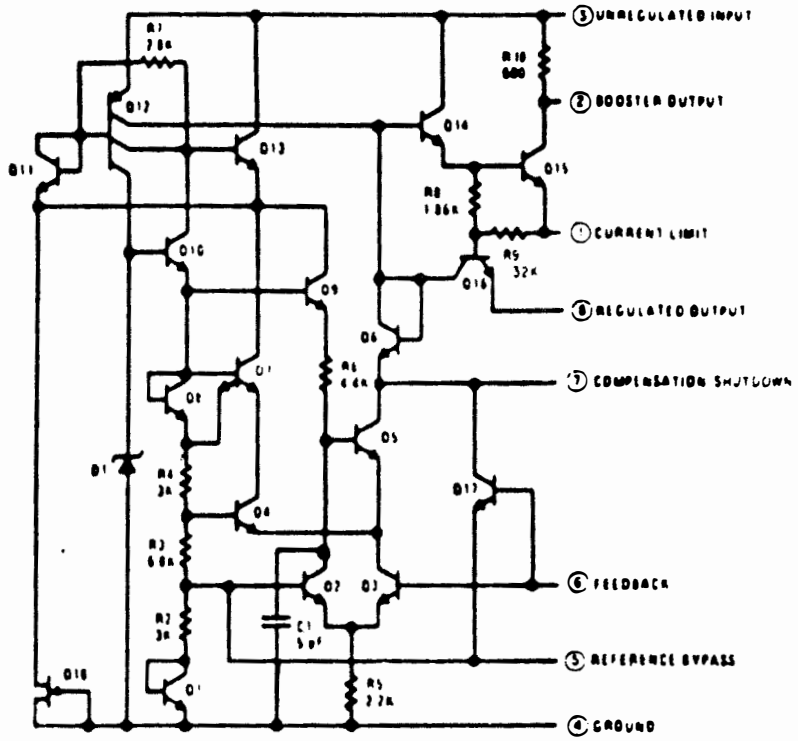


Figure 3-22. Integrated Circuit, Voltage Regulator, LM105H883 (98738/48P226461-01) Alt. LM105H/883B (50097/C31356-001), Simplified Schematic Diagram

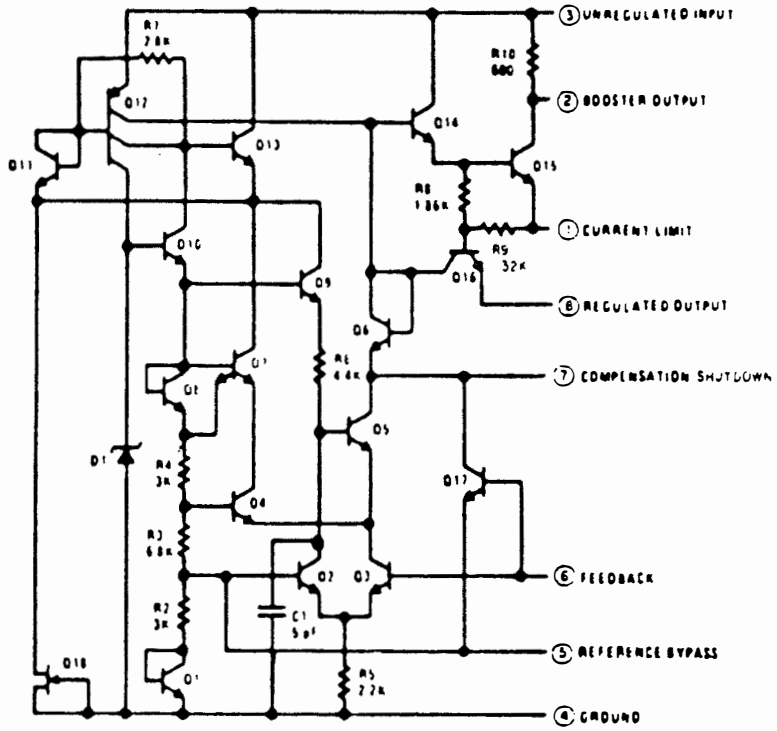
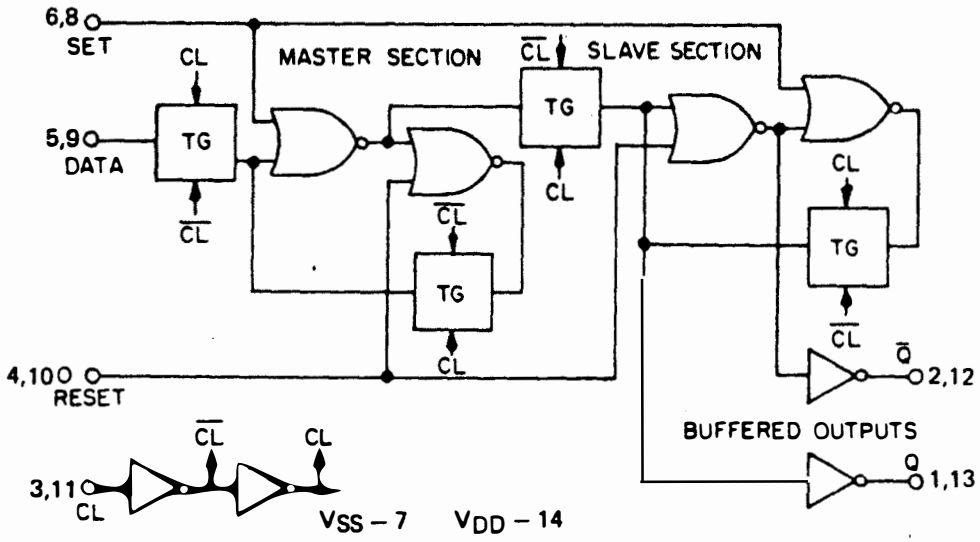


Figure 3-22. Integrated Circuit, Voltage Regulator, LM105H/883 (48P226461-01), Simplified Schematic Diagram

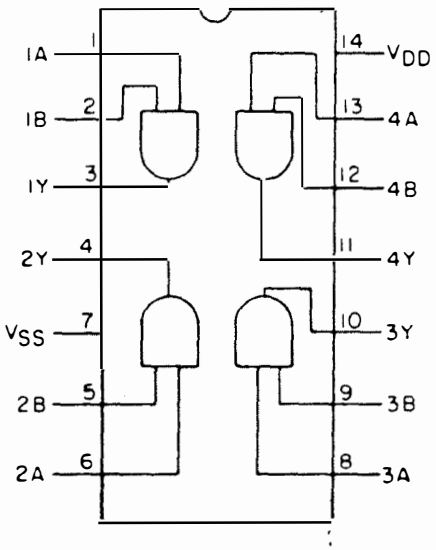


TRUTH TABLE

INPUTS				OUTPUTS		
CL Δ	D	R	S	Q	$\overline{Q}$	
⌐	L	L	L	L	H	
⌐	H	L	L	H	L	
⌙	X	L	L	Q	$\overline{Q}$	NO CHANGE
X	X	H	L	L	H	
X	X	L	H	H	L	
X	X	H	H	*	*	

Positive logic
H = HIGH LEVEL;
L = LOW LEVEL
* = Invalid condition
Δ = Level change
X = Irrelevant

Figure 3-23. Integrated Circuit, Dual D-Type Edge-Triggered Flip-Flop, M38510/05101BCB (4013A), Logic Diagram



TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

POSITIVE LOGIC $Y = A \cdot B$
H = HIGH LEVEL;
L = LOW LEVEL

Figure 3-24. Integrated Circuit, Quadruple 2-Input AND Gate, M38510/17001BCB (4081B), Logic Diagram

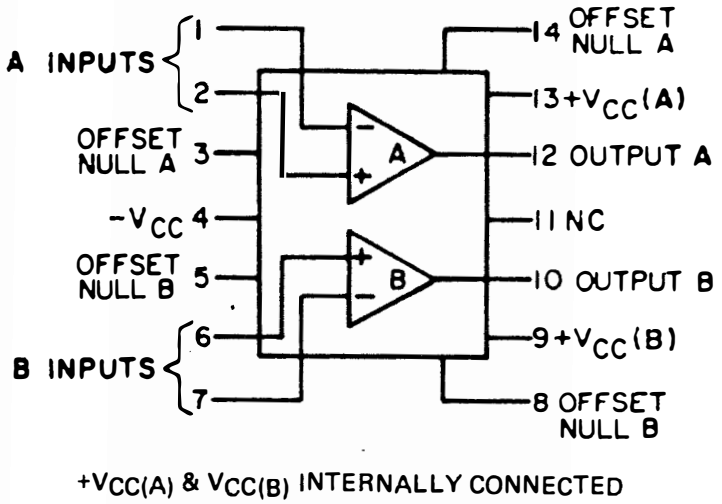


Figure 3-25. Integrated Circuit M38510/10102BCB (747A), Logic Diagram

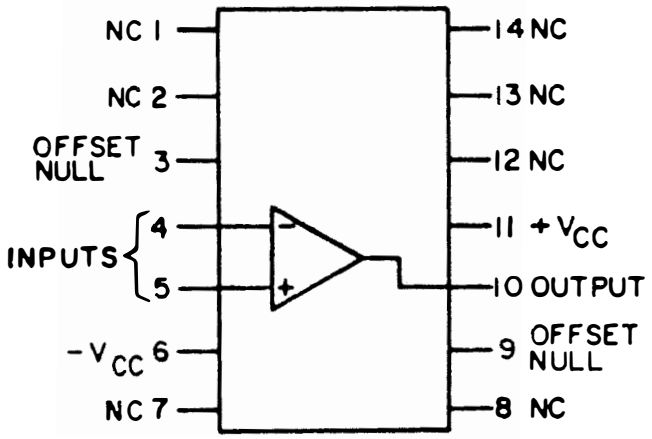
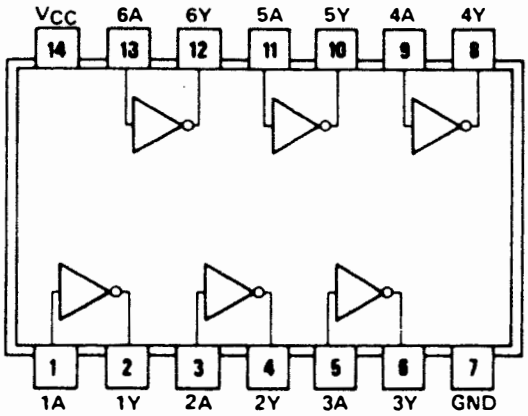


Figure 3-26. Integrated Circuit M38510/10101BCB (741A), Logic Diagram

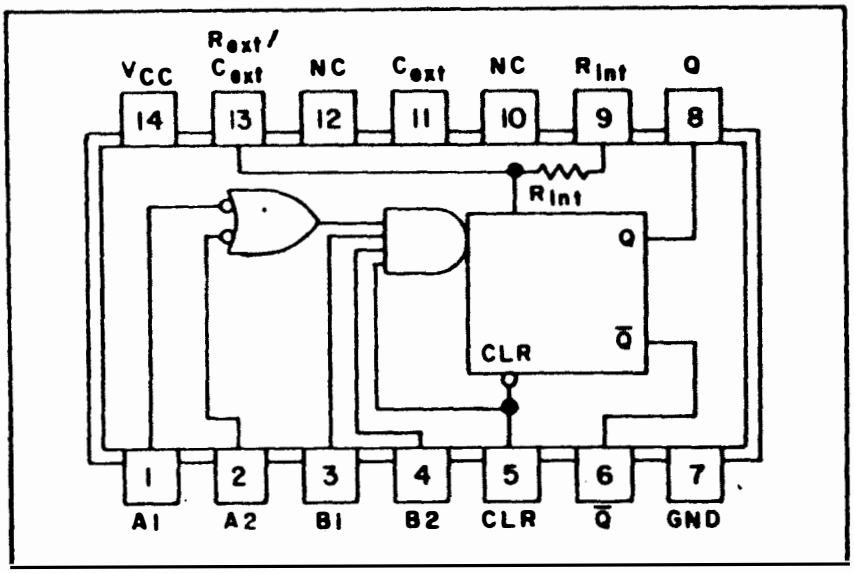


TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

POSITIVE LOGIC $Y = \overline{A}$
H = HIGH LEVEL
L = LOW LEVEL

Figure 3-27. Integrated Circuit, Hex 1-Input Inverter Gate, M38510/00108BCB (SNC54S04J), Logic Diagram

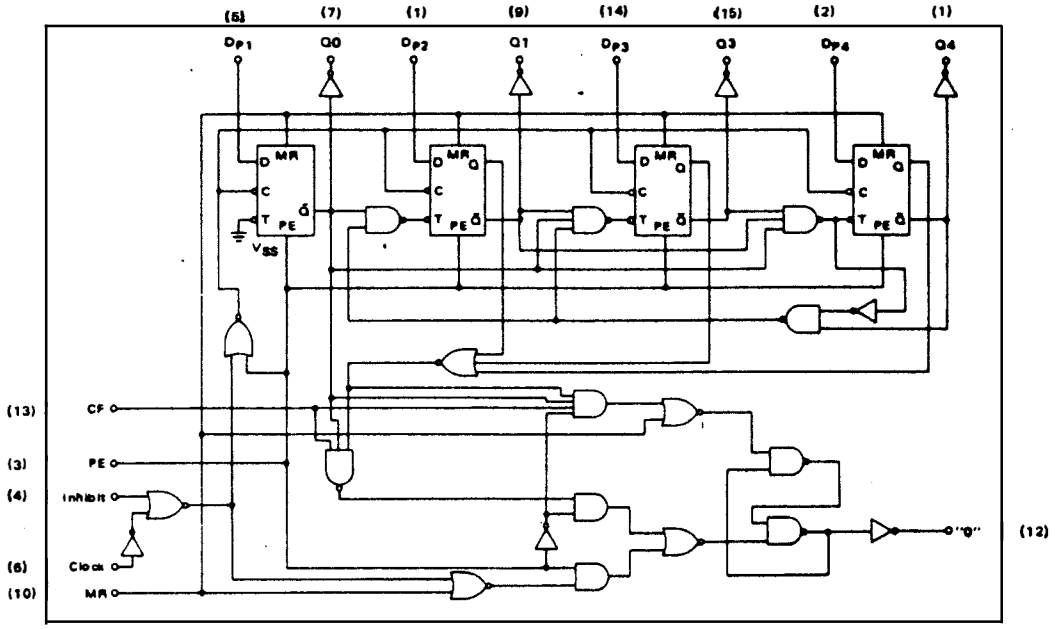


TRUTH TABLE
AND
FUNCTIONAL DESCRIPTION

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

H = HIGH LEVEL (steady state),
L = LOW LEVEL (steady state),
↑ = transition from low to high level,
↓ = transition from high to low level,
⎍ = one high level pulse,
⎎ = one low level pulse,
X = irrelevant

Figure 3-28. Integrated Circuit, Single Monostable Multivibrator, M38510/31403BCB (54LS122), Logic Diagram



VDD – PIN (16)
VSS – PIN (8)

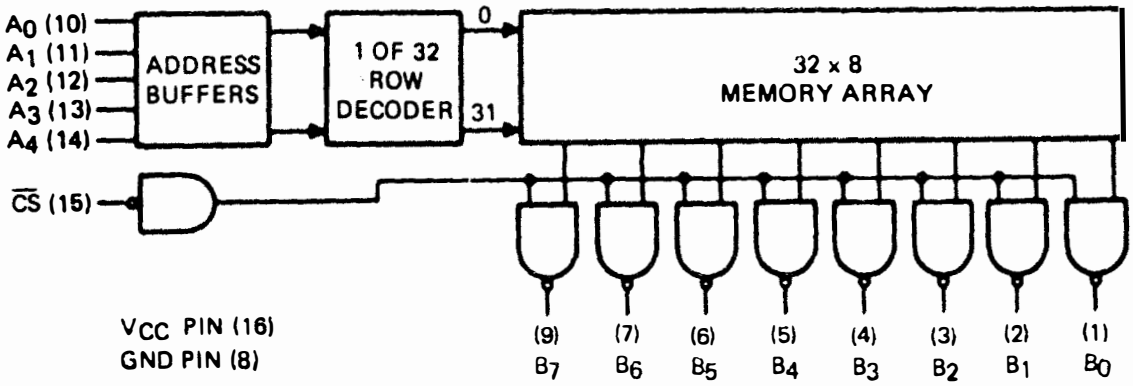
TRUTH TABLES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
⌒	0	0	0	Count - 1
X	1	0	0	No Count
1	⌒	0	0	Count - 1
X	X	1	0	Preset
X	X	X	1	Reset

1 = OPEN CIRCUIT;
0 = GROUND;
X = IRRELEVANT

	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Figure 3-29. Integrated Circuit, Programmable Divide-by-N 4-Bit Counter, BCL4522 (48P228316-01), Logic Diagram

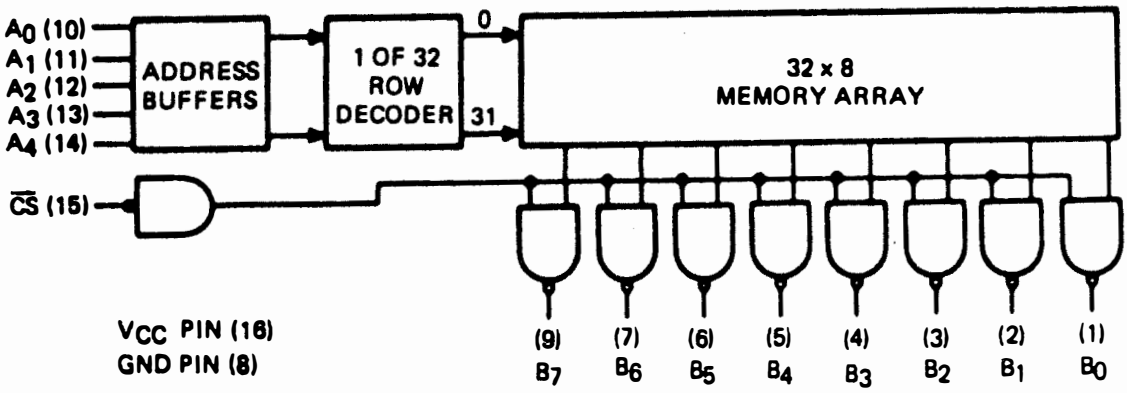


FUNCTION TABLE

INPUTS					OUTPUTS							
A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	1	0	0	0	1	1	0	0	1
0	0	0	1	0	0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0	1	0	1	1	1
0	0	1	0	0	0	0	0	1	0	1	1	0
0	0	1	0	1	0	0	0	1	0	1	0	1
0	0	1	1	0	0	0	0	1	0	1	0	0
0	0	1	1	1	0	0	0	1	0	0	1	1
0	1	0	0	0	0	0	0	1	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	0	0	0	0	1	1	0	0	1
1	0	0	0	1	0	0	0	1	1	0	0	0
1	0	0	1	0	0	0	0	1	0	1	1	1
1	0	0	1	1	0	0	0	1	0	1	1	0
1	0	1	0	0	0	0	0	1	0	1	0	1
1	0	1	0	1	0	0	0	1	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	1	1
1	0	1	1	1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	0	0	1	0	0	0	1
1	1	0	0	1	0	0	0	1	0	0	0	0

1 = OPEN CIRCUIT; 0 = GROUND
Addresses not shown are unprogrammed.

Figure 3-30. Integrated Circuit, 32 x 8 Prom, HMI-7603-8 (98738/48P228344-01) Alt. (50097/M31310-003), Block Diagram



FUNCTION TABLE

INPUTS					OUTPUTS							
A_0	A_1	A_2	A_3	A_4	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
1	1	1	1	0	0	1	0	1	0	0	0	0
0	0	0	0	1	0	1	1	1	0	0	0	0
1	1	0	0	1	0	1	0	0	1	0	0	0
1	0	0	0	1	0	1	0	0	0	1	0	0
1	1	1	0	0	1	0	0	1	0	1	0	0
1	1	0	0	0	1	0	1	1	0	1	0	0
1	0	0	0	0	1	0	0	0	1	1	0	0
0	0	0	1	1	1	0	0	0	0	0	1	0
0	0	1	1	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	1	0	0	1	0
1	0	0	1	0	1	1	0	0	1	0	1	0
0	0	1	0	0	1	1	0	0	0	1	1	0
0	1	0	0	0	1	1	1	0	0	1	1	0
0	0	0	1	0	1	1	0	1	0	1	1	0
0	0	1	0	1	1	1	0	0	1	1	1	0
0	1	0	1	1	1	1	0	0	0	0	0	1
1	0	1	1	1	1	1	1	1	0	0	0	1

1 = OPEN CIRCUIT; 0 = GROUND.
Addresses not shown are unprogrammed.

Figure 3-31. Integrated Circuit, 32 x 8 Prom, CC4335F, (98738/48P226463-01), Alt. HMI-7602-8 (50097/M31310-002), Block Diagram

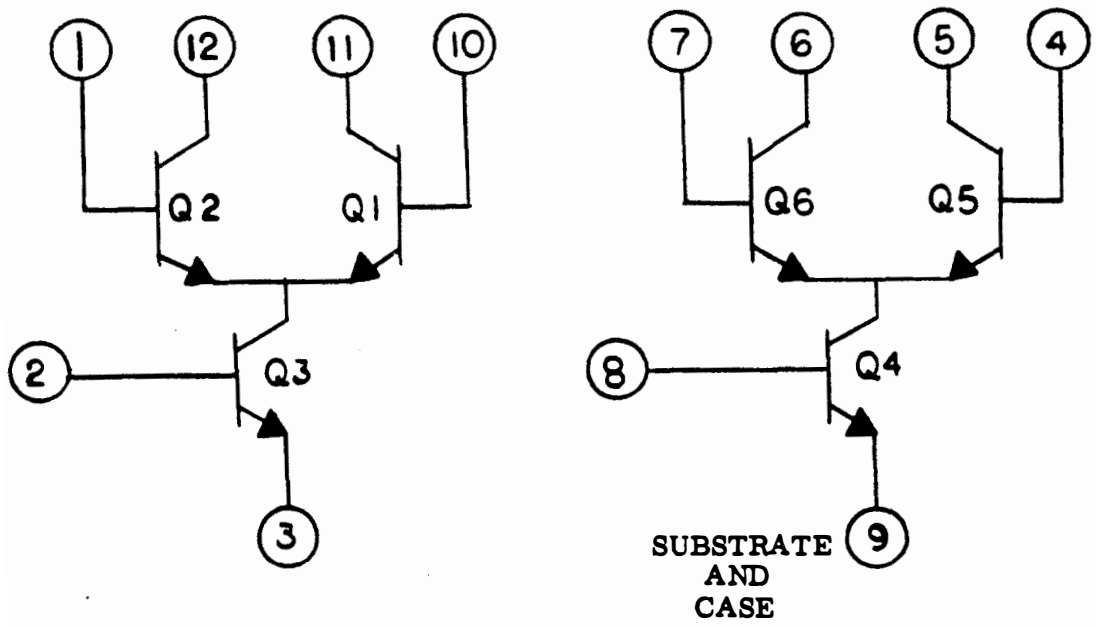


Figure 3-32. Integrated Circuit, Dual High-Frequency Differential Amplifier, CA3049T/3 (48P228318-02), Schematic Diagram

intermediate frequency signals with the T-827H/URT entry and exit signals.

3-134. Power Control and Distribution (Figure 5-28, Sheet 3). Power Supply Assembly A2A8 contains two full-wave bridge rectifier circuits and a +20 Vdc regulator circuit. The rectifier bridge comprised of A2A8CR1 through A2A8CR4 produces an output which is filtered by inductor A2L1 and capacitor A2C1. This 110 Vdc output is used to power the plate and screen circuits of the vacuum tubes in RF Amplifier Assembly A2A4. The rectifier bridge comprised of A2A8CR5 through A2A8CR8 is responsible for the +28 Vdc output which is distributed as described in paragraph 3-117.

3-135. The +28 Vdc is applied to the collector of A2Q1. The output from the emitter of series regulator A2Q1 appears across the voltage divider consisting of A2A8R9, A2A8R10, and A2A8R11. The wiper arm of variable resistor A2A8R10 provides one input to differential amplifier A2A8U1. The second input to A2A8U1 is a constant +4.7 Vdc supplied by voltage reference diode A2A8CR13 and the voltage divider consisting of A2A8R4, A2A8R5, A2A8R17. Any change in the emitter voltage of series regulator A2Q1 causes a change at the input of A2A8U1. A change in the voltage output of A2A8U1 is amplified by A2A8Q1, A2A8Q2 and applied as a change in base bias of A2Q1. This changes the conduction of A2Q1, resulting in correction of the +20 Vdc output. The actual value is determined by the setting of potentiometer A2A8R10. In summary, any variation in the +20 Vdc output is detected by A2A8U1. The conduction of A2Q1 is changed to return the output voltage to +20 Vdc. Output filtering of the +20 Vdc is provided by capacitor A2A8C6. Refer to paragraph 3-118 for a description of the +20 Vdc distribution.

3-136. Meter Amplifiers (Figure 5-28, Sheet 1). Meter Amplifier Assemblies A2A10 and A2A11 amplify audio signals to LSB LINE LEVEL meter A2M1 and USB LINE LEVEL meter A2M2. The two meter amplifier assemblies are identical. Each receives an audio signal input from its associated Audio Processor Board assembly A2A21A18 and A2A21A19. The signal is connected through LSB LINE LEVEL meter switch A2S8, to A2A10 and USB LINE LEVEL meter switch A2S7, to A2A11. The position of switch A2S8 or A2S7 determines the amplitude of the audio input signal to A2A10 or A2A11.

3-137. When switch A2S8 or A2S7 is set in the -10 dB position, a negative 10 dB must be added to the meter indication on the scale to determine the actual audio line level. When switch A2S8 or A2S7 is set in the +10 dB position, the audio signals are attenuated by resistors A2A10R1-R3 or A2A11R1-R3. Thus, a positive 10 dB must be added to the meter scale to determine the true audio line level.

3-138. Panel Illumination (Figure 5-28, Sheet 3). When the mode selector switch is set to any position other than OFF, lamps A2DS3 and A2DS4 illuminate the numerical readouts associated with the front panel MHz and kHz tuning controls. The +28 Vdc panel lamp voltage is applied through voltage dropping resistor A2A8R1.

3-139. Handset Filtering (Figure 5-28, Sheets 1 and 3). Handset Filter Assembly A2A14 filters intermediate and radio frequency signals from the local handset line. The circuit consisting of A2A14L1, A2A14C2, and A2A14C4 filters the audio line of HANDSET connector A2J1. The circuit consisting of A2A14C1 and A2A14CX3 filters the +12 Vdc handset PTT line.

3-140. IF Filtering (Figure 5-28, Sheet 1). IF Filter Assembly A2A15 filters the APC and PPC voltage inputs from the rf power amplifier and the +20 Vdc input to IF Amplifier Assembly A2A12. These filters prevent rf signals from appearing on the APC and PPC lines or on the +20 Vdc bus. A2A15CR1 isolates the T-827H/URT +20 Vdc bus from the AM-3924C/URT tone carrier +20 Vdc.

3-141. AUDIO INTERCONNECT ASSEMBLY A2A21 (Figure 5-28, Sheet 1). The Audio Interconnect Assembly A2A21 contains the normal audio input transformers A2A21T1 (LSB) and A2A21T2 (USB) and wiring for plug-in socket jacks A2A21XA18, A2A21XA19, and A2A21XA20. These sockets are permanently mounted on the assembly, and provide receptacles for the following plug-in

printed wiring assemblies: LSB Audio processor A2A21A19; USB Audio processor A2A21A18; and Audio control A2A21A20. The A2A21 assembly is permanently hard-wired to the T-827H/URT chassis. Also mounted on the assembly are relays A2A21K1 and A2A21K2. Terminals A2A21K1-9 and A2A21K2-9 are connected to A2A21E13, which receives either an open or +27 Vdc from DATA/NORMAL switch A2S11.

3-142. During NORMAL operation, an open is received and relays A2A21K1 and A2A21K2 are unenergized. In this condition, the LSB/ISB 600 ohm inputs from A2J4-f, g are connected to the primary of A2A21T1 via relay terminals A2A21K1-2, -4 and A2A21K1-6, -8. Also in NORMAL operation, the USB/AM/ISB input lines from A2J4-r, q are connected to the primary of A2A21T2 via relay terminals A2A21K2-2, -4 and A2A21K2-6, -8. Transformer secondary terminals A2A21T1-4 and A2A21T2-4 are connected to an AC ground via A2A21E41 on the interconnect assembly and A2A8E13 on the low voltage power supply assembly. Audio transformers A2A21T1 and A2A21T2 provide an impedance match to the 600 ohm LSB and USB NORMAL audio input lines, and the proper signal level at terminals A2A21T1-6 and A2A21T2-6 to drive the audio processor assemblies A2A21A18 and A2A21A19. Center tap terminal A2A21T1-5 is connected via A2A21E23 to LOCAL ISB HANDSET switch A2S9-6, and A2A21T2-5 to A2S9-4 via A2A21E24. With voice input via the handset, the LSB or USB audio channel, selected for ISB, is then applied directly to the secondary through A2S9 to the appropriate tap on A2A21T1-5 or A2A21T2-5. Under these conditions, the direct input, without additional impedance matching provided by the audio transformer, is satisfactory.

3-143. When DATA/NORMAL switch A2S11 is in the DATA position, +27 Vdc from A2A21E13 to A2A21K1-9 and A2A21K2-9 energizes these relays. Data audio on the LSB/ISB inputs A1A1J4-f, g and A1A1J6-A, B bypasses transformer A2A21T1 via terminal pairs 2, 3 and 7, 8 of energized relay A2A21K1, and is directed to LSB Audio Processor A2A21A19 via the jumper pairs E43, E44 and E45, E46 on Audio Interconnect Assembly A2A21. Likewise, data audio on the USB/AM/ISB inputs A1A1J4-r, q and A1A1J5-A, B bypasses transformer A2A21T2 via terminal pairs 2, 3 and 7, 8 of energized relay A2A21K2, and is directed to USB Audio Processor A2A21A18 via the jumper pairs E47, E48 and E49, E50 on Audio Interconnect Assembly A2A21. Data audio on connectors A2J8-A through A2J8-D is channeled to the proper audio processor via terminals E19, E31, E32, and E34 of Audio Interconnect Assembly A2A21.

3-144. AUDIO PROCESSORS A2A21-A18/19 (Figure 5-44). Two Processors, A2-A21A18 and A2A21A19, are incorporated in the T-827H/URT. Audio Processor A2A21-A18 handles USB, AM, and RATT modes of operation; A2A21A19 handles the LSB mode; both processors handle the ISB mode. The audio processors function to provide constant amplitude audio signals as partial input to the modulating circuits. Jumper wires on terminals A2A21E43 through A2A21E50 allow the installing agency the ability to connect data audio to the normal remote USB and LSB audio inputs. With jumpers connected as indicated in Key 25 of Table 2-1, and figure 5-28, sheet 1, data audio can be fed in from either the normal remote and auxiliary USB and LSB inputs or from the Data Audio input connector A1J8. With jumpers removed, data audio can be fed in only from the A1J8 connector. Since the physical design of the two audio processors is identical, only A2A21A18 will be described in the succeeding paragraphs.

3-145. For normal audio operation, relay A2A21A18K1 is unenergized, and the normal audio input at A2A21A18P1-U is directed, via contacts 2, 4 of relay A2A21A18K1, to the audio amplifier consisting of fixed gain amplifier A2A21A18U2 and a speech compression circuit A2A21A18Q1. The incoming normal audio is also fed to Line Level Meter A2M2 via connector A2A21A18P1-S. Prior to entering the amplifier and speech compression circuits, the normal audio is applied to THRESHOLD level control A2A21A18R4. A2A21A18R4 is set to the minimum input signal level which will maintain a constant output signal amplitude. The audio signal is applied across A2A21A18R4 and A2A21A18-Q1, and couples through A2A21A18R6 to pin 4 of A2A21A18U2. Audio amplifier A2A21-

A18U2 provides a fixed voltage gain of approximately 20. A2A21A18C24 and A2A21A18C3 are decoupling capacitors. The amplified signal is applied to the base of dc amplifier A2A21A18Q2 by way of A2A21A18R9 and A2A21A18C8. Threshold detector A2A21A18CR1 is forward biased by the positive half cycles of the audio signal. In the negative half cycles, A2A21A18CR1 is reversed biased and A2A21A18Q2 conducts. Capacitor A2A21A18C10 discharges and the voltage is applied to the gate of the compressor A2A21A18Q1. The gate voltage controls the input signal level at A2A21A18U2-4 and maintains a constant output level at A2A21A18U2-10. In the RATT mode a ground at P1-3 forward biases Q5 and disables Q1, allowing U2 to provide the full gain of 20. To provide temperature compensation, thermistor A2A21A18RT1 shunts resistor A2A21A18R7. As temperature increases, the thermistor resistance decreases, permitting a greater percentage of the audio signal to be present at the output A2A21A18P1-17. Resistor A2A21A18R8 is variable for adjustment of the signal level presented to the balanced modulator circuits in the Mode Selector Assembly A2A1.

3-146. For data audio operation, the data audio input at A2A21A18P1-F, 6 and A2A21A18P1-H is applied at A2A21A18T1 and fed to linear amplifier A2A21A18U1B-1. The gain of A2A21A18U1B is set by potentiometer A2A21A18R33. When the output amplitude of A2A21A18U1A exceeds a preset level, adjusted by clip level potentiometer A2A21A18R26, A2A21A18Q3 or A2A21A18Q4 reduces the gain of A2A21A18U1A by its feedback through A2A21A18R24. Voltage divider A2A21A18R31-A2A21A18R32 reduces the signal to a level below the transmitter audio automatic control threshold. The processed data audio is directed, via contacts 2, 3 of energized relay A2A21A18K1, to the audio amplifier and speech compression circuits for additional processing identical to that described for normal audio in the preceding paragraph. The data audio at relay terminals A2A21A18K1-2, 3 is also directed to Line Level meter A2M2 via connector A2A21A18P1-S.

3-147. Audio Control A2A21A20 (Figure 5-45). The Audio Control Assembly A2A21A20 performs the following functions associated with data operation: (1) voltage interlocks; (2) T-827H/URT and AM-3924C(P)/URT keying; (3) TGC enable, reset and capacitor control; (4) data ISB grounds; and (5) +15 Vdc and +5 Vdc supplies.

3-148. Voltage Interlocks. The interlock function prevents data operation if +20 Vdc or +24 Vdc are not present at pins 11 and 13, respectively, of connector A2A21A20P1. If both voltages are present, A2A21A20CR8 and A2A21A20CR9 are off and so A2A21A20Q9 and A2A21A10Q13 are both off. If either voltage is absent, one of the diodes A2A21A20CR8 or A2A21A20CR9 is on through A2A21A20R21 or A2A21A20R22. If A2A21A20Q9 and A2A21A20Q13 are on, the collector of A2A21A20Q13 is at a logic low (0.0 to 0.4 Vdc); hence, TGC enable at A2A21A20P1-L is at a logic low, TGC action is inhibited, and data operation is effectively prohibited.

3-149. T-827H/URT and AM-3924C(P)/URT Keying. The T-827H/URT is always keyed in the data mode of operation, and the AM-3924C(P)/URT is keyed only when data audio tones are present. This keying is accomplished by energizing relays A2A21A20K1 and A2A21A20K2. In the unenergized condition, relays A2A21A20K1 and A2A21A20K2 allow the CW/RATT keyline and the ground keyline to pass through the audio control assembly without alteration.

3-150. In the normal mode of operation, the ground keyline at A2A21A20P1-D is fed through contacts 2, 4 of unenergized relay A2A21A20K2, and outputted at A2A21A20P1-4. In the data mode, A2A21A20P1-D is grounded through contacts 2, 3 of energized relay A2A21A20K2, which keeps the T-827H/URT keyed constantly. In the normal mode of operation, the CW/RATT keyline at A2A21A20P1-5 is passed through contacts 2, 4 of unenergized relay A2A21A20K1, and outputted at A2A21A20P1-E. In the data mode, energized relay A2A21A20K1 allows keying of the system through contacts 2, 3 and via A2A21A20CR20 by a +6 Vdc data key signal fed through the CW/RATT keyline at A2A21A20P1-5. Keying of the system in data mode can also be accomplished by a +6 Vdc data key signal on pins H, J, or 7 of A2-

A21A20P1. The data key turns on A2A21-A20Q10 so that the logic low necessary to key RF Amplifier AM-3924C(P)/URT will be present at A2A21A20P1-4 through contacts 7, 8 of energized relay A2A21A20K2.

3-151. TGC Enable and TGC Capacitor Control. The TGC functions of enable and capacitor control are provided as follows. The audio sample for TGC is received at A2-A21A20P1-M. Dual operational amplifier A2A21A20U3, transistor A2A21A20Q11 and one-shot multivibrator A2A21A20U6 form an audio signal detector. A2A21A20U3, A2-A21A20CR11 and A2A21A20CR12 function as a full-wave bridge rectifier with gain for the USB and/or LSB signal input. The resulting signal at the base of A2A21A20Q11 is a series of positive spikes for each audio zero voltage crossing. The resulting negative spikes on the collector of A2A21A20Q11 maintain A2A21A20U6 pin 6 at a low logic state as long as data audio is present. This logic low is sent to pin 11 of wired "AND" A2A21A20U2. A2A21A20U2 pin 13 sees a logic low if the DATA/NORMAL switch is in the DATA position. A2A21A20U2 pin 9 will be a logic low if A2A21A20Q10 is on. A2-A21A20U2 pin 3 is permanently wired to ground (a logic low). Thus, if pins 3, 9, 11 and 13 of A2A21A20U2 are at logic lows, pins 4, 8, 10, and 12 will be at logic highs (+2.4 Vdc to +5.0 Vdc). Additionally, A2-A21A20U2 pin 1 will be at a logic high if +20 Vdc and +28 Vdc are present at pins 11 and 13, respectively, of A2A21A20P1. The "anded" logic highs at the output of A2A21-A20U2 represent the required TGC enable at A2A21A20P1-L for the TGC counter in the AM-3924C(P)/URT.

3-152. A2A21A20Q11 shifts the analog levels from A2A21A20U3 to TTL-compatible levels for multivibrator A2A21A20U6. A2-A21A20Q11 turns on with each half cycle of audio greater than -6 dBm, causing A2A21-A20U6 to be triggered. The output at A2-A21A20U6-6 goes low and remains in that state until approximately 1.5 milliseconds after all audio is removed. This logic low is sent to pin 11 of A2A21A20U2. This same condition is established by the presence of a +20 Vdc carrier insertion signal at A2A21-A20P1-12. This signal turns on A2A21A20-Q12, which grounds the output of A2A21-A20U6-6, and provides a logic low to pin 11 of A2A21A20U2. When the DATA/NORMAL switch is in the DATA position, the resulting ground (logic low) at A2A21A20P1-10 appears on pin 13 of A2A21A20U2. The presence of a data key signal (+6 Vdc) from the audio processors A2A21A18/A2A21A19 or from an external key at pins H, J, or 7 of A2A21A20P1 causes A2A21A20Q10 to turn on and its collector to go low, thereby providing a logic low to pin 9 of A2A21A20U2. The logic lows at pins 3, 9, 11, 13 of A2A21-A20U2 appear as logic highs at pins 4, 8, 10, 12, respectively. These constitute the TGC enable logic high at A2A21A20P1-L, provided that +28 Vdc interlock voltage from the AM-3924C(P)/URT is present at A2A21A20P1-11. These voltages hold A2A21A20Q9 and A2A21A20Q13 off, which results in a logic high at pin 1 of A2A21A20U2. This completes the required "anding" of A2A21A20U2 outputs, and subsequent enabling of the TGC counter via the resultant logic high at A2-A21A20P1-L. The logic high at A2A21A20U2 pin 1 is inverted to a logic low at pin 2. The logic level of A2A21A20U2-2 is level-shifted in A2A21A20Q7-A2A21A20Q8 to provide -15 Vdc to A2A21A20P1-17 for TGC capacitor control to the AM-3924C(P)/URT.

3-153. TGC Reset. Reset functions set the TGC counter to maximum count, i.e. full attenuation at the transmitter. TGC reset is logic low when: (1) the system is turned on; (2) the DATA/NORMAL switch is turned to DATA; or (3) a ground pulse occurs by changing any of the MHz or kHz frequency knobs.

3-154. As the +5 Vdc builds up at system turn-on, A2A21A20Q6 is turned on through A2A21A20R12 and A2A21A20CR5. The resultant logic low at the collector of A2A21-A20Q6 initiates TGC reset at A2A21A20P1-15. When the +5 Vdc supply builds up to greater than +4.2 Vdc (determined by A2-A21A20CR4), A2A21A20CR4 begins to conduct through A2A21A20R13 to turn on A2-A21A20Q5. With A2A21A20Q5 on, the voltage at its collector is too low to maintain A2A21A20Q6 on, and the TGC reset function is effectively completed.

3-155. When the DATA/NORMAL switch A2S11 is changed from NORMAL to DATA, the ground at A2A21A20P1-10 is inverted by

A2A21A20U2, and appears as a logic high at A2A21A20U2-6. This is coupled through A2-A21A20C6 to turn on A2A21A20Q6, thereby providing a logic low at A2A21A20P1-15. The on period is determined by the time constant set by A2A21A20C6 and A2A21A20-R14. A ground pulse (as a result of turning any MHz or kHz tuning control) is present on A2A21A20P1-T. This pulse is inverted by A2A21A20Q1 and sent through A2A21A20-CR3 to turn on A2A21A20Q6. The resulting logic low at the collector of A2A21A20Q6 provides the required TGC reset at A2A21-A20P1-15. A2A21A20Q2 inverts the signal on the collector of A2A21A20Q1 to create the PA ground pulse on A2A21A20P1-16 for use by the AM-3924C(P)/URT.

3-156. Data ISB Grounds. A ground is required for the LSB and USB Audio Processors A2A21A18 and A2A21A19 for ISB data mode operation. In this mode of operation, the audio processors reduce the audio drive to the modulators to limit rf peak power output. When Mode Selector switch A2S2 is placed in the ISB position, a ground appears at A2A21A20P1-U. Relay A2A21A20K3 is energized by the appearance of this ground on A2A21A20K3-9. The required ISB ground for USB and LSB then appears at pins P and 14 of A2A21A20P1 via contact pairs 2, 3 and 6, 7 of relay A2A21A20K3.

3-157. +15 Vdc and +5 Vdc Power Supplies. Audio assemblies A2A21A18, A2-A21A19, and A2A21A20 require +15 Vdc. This voltage is developed by A2A21A20Q14. The +20 Vdc from A2A21A20P1-S is dropped by A2A21A20R41 and applied to +16 Vdc Zener diode A2A21A20CR23. This zener sets the base voltage for emitter follower A2-A21A20Q14. The emitter output provides the required +15 Vdc output. The A2A21A20 assembly requires +5 Vdc which is provided by voltage regulator A2A21A20U7. The input to A2A21A20U7 is the +15 Vdc from the emitter of A2A21A20Q14.

3-158. MODE SELECTOR ASSEMBLY A2-A1 (Figure 5-29). Mode Selector Assembly A2A1 contains the Balanced Modulator Subassemblies A2A1A1 and A2A1A2 employed for USB and LSB modulation; Isolation Amplifier Subassembly A2A1A3; and single-sideband filters A2A1FL1 and A2A1FL2. The Mode Selector also contains 500 kHz Gates Subassembly A2A1A4. A2A1A4 contains gating circuits which control the distribution of the 500 kHz modulator input signal, and the CW and AM carrier reinsertion signals. The mode selector also contains Buffer Amplifier A2A1A5, which buffers the two sideband filters.

3-159. The two balanced modulators (A2-A1A1 and A2A1A2) are identical in circuitry, but receive audio from different sources. Subassembly A2A1A1 receives audio to be transmitted on USB from Audio Processor A2A21A18. Subassembly A2A1A2 receives audio to be transmitted on LSB from Audio Processor A2A21A19. A2A1A1 and A2A1A2 are conventional, balanced-bridge modulators. Here, the input audio signals are mixed with the 500 kHz intermediate frequency carrier signal. The output of the balanced modulator consists of the sum and difference frequencies (upper and lower sidebands). The 500 kHz carrier and audio are suppressed. Carrier suppression is achieved by balancing, using MOD BAL ADJ controls A2A1A1R3, A2A1A1C4, A2A1A2R3, and A2A1A2C4.

3-160. The outputs of the balanced modulators are applied to the isolation amplifiers in subassembly A2A1A3. Isolation amplifiers A2A1A3Q1 and A2A1A3Q2 apply this signal to an associated LSB or USB filter (A2A1FL1 or A2A1FL2). The output from filter A2A1-FL1 is lower sideband only; the output from filter A2A1FL2 is upper sideband only. The filter outputs are connected to amplifiers A2A1A5Q1 and A2A1A5Q2 which buffer the signals and also provide for balancing the outputs by the adjustment of A2A1A5R6. The outputs of the buffer amplifiers are connected to a common output at A2A1A5E4. A2A1P1-A1 connects the sideband signals to IF Amplifier Assembly A2A12. Either of the two balanced modulators may operate singly, or both may operate simultaneously. This depends on the selected mode of operation.

3-161. Gated amplifiers A2A1A4Q1 and A2A1A4Q2 function as switches between the balanced modulators and the 500 kHz input line. Gated amplifiers A2A1A4Q1 and A2-A1A4Q2 receive the 500 kHz signal through gating diode A2A1A4CR1. Diode A2A1A4-CR1 is biased on by application of the +20

Vdc transmit voltages from A2A1P2-7. A2-A1A4Q1 is enabled when +20 Vdc is applied to its emitter from A2A1P2-8. This occurs when the mode selector switch A2S2 is set in any mode except CW. Enabling A2A1A4Q1 gates the input 500 kHz into the primary of A2A1A4T1. The output of A2A1A4T1 is connected by coaxial cable to A2A1A1E4 of USB Balanced Modulator A2A1A1. A2A1A4Q2 functions identically when the mode selector switch is set in modes requiring LSB operation.

3-162. The cw keyline ground input at A2-A1P2-5 causes cw key gate A2A1A4CR7 to conduct. This biases cw carrier reinsertion gate A2A1A4CR6 on and A2A1A4CR8 off. The 500 kHz input at A2A1P2-A3 is then supplied as a carrier reinsertion signal to output transformer A2A1A4T3. A2A1A4CR8 conducts at all times when the cw keyline ground input is not present at A2A1A4CR7. Conduction of A2A1A4CR8 grounds the output of A2A1A4CR6 through A2A1A4C22. This prevents leakage of the 500 kHz signal.

3-163. In SSB modes, +20 Vdc from A2A1-P2-7 is applied to reinsertion gate A2A1A4-CR12 via Carrier Reinsertion switch A2A1-S1. This enables A2A1A4CR12, which then passes the 500 kHz signal from % MOD ADJ potentiometer A2A1A4R39 to Carrier Reinsertion switch A2A1S1. Changing settings of switch A2A1S1 attenuates the 500 kHz signal by a preselected amount from transformer A2A1A4T3. The A2A1A4T3 output is then fed through A2A1P2-A1 to IF Amplifier Assembly A2A12, where it is reinserted as the desired pilot carrier signal.

3-164. When the mode selector switch is set in the AM mode, AM carrier reinsertion gates A2A1A4CR9 and A2A1A4CR11 are biased on by application of +20 Vdc from A2-A1P2-4. Conduction through A2A1A4CR11 reverse biases AM carrier reinsertion gate A2A1A4CR10. This action allows the 500 kHz carrier reinsertion signal to pass through A2A1A4CR9 to output transformer A2A1A4-T3. A2A1A4CR11 is biased off in all other modes, and A2A1A4CR10 conducts. Undesired 500 kHz leakage signal from A2A1A4-CR9 is then grounded by capacitor A2A1A4-C26.

3-165. RF AMPLIFIER ASSEMBLY A2A4 (Figure 5-30). The rf amplifiers A2A4V1 and A2A4V2 of RF Amplifier Assembly A2A4 are conventional tuned circuits, capable of tuning over the range from 2.0 to 29.9999 MHz. The RF Amplifier Assembly tuning turret contains twenty-eight MHz bandpass filter coupling networks (subassemblies A2-A4A2 through A2A4A29 depicted in Figures 7-20 through 7-47). As indicated in notes 3 and 7 of figure 5-30, portions of three of the 28 turret subassemblies are used to tune a 1 MHz band (e.g., for 2-MHz tuning, subassemblies A2A4A20, A2A4A25, and A2A4A2 are involved). Selection of the appropriate portions of each of these turret subassemblies is accomplished by rotation of the MHz controls on the front panel.

3-166. In order to tune to the desired frequency within any 1-MHz band, the 100 kHz and 10 kHz controls are used to mechanically select grid and plate tank-capacitor subassemblies, as shown in notes 1, 2, 5 and 6 of figure 5-30. For example, in tuning to 550 kHz within any MHz band, capacitor C6 and C15 of subassembly A2A4A30, A2A4A33, A2A4A34 and A2A4A37 tune the 100-kHz increment (0.5 MHz), and capacitor C6 of subassemblies A2A4A31, A2A4A32, A2A4A35 and A2A4A36 tunes the 10-kHz increment (0.05 MHz).

3-167. The selection of the desired 1-MHz band is accomplished by rotating the front panel MHz controls to the desired frequency. These controls are not mechanically connected to the turret; instead, the controls rotate switch wipers in Code Generator Assembly A2A7. This results in an output from the code generator of a five-line code consisting of circuit grounds and opens (see table 3-2).

3-168. A five-line combination for each frequency band is applied through contacts 1 through 5 of A2A4P1, and from there to the turret decoder A2A4S1. Wafer A2A4S1A is the decoder, and connects the ground(s) from the code generator to relay A2A4K1, which energizes and applies +28 Vdc to motor A2-A4B1 (via relay contacts A2A4K1-A1 and A2A4K1-2). As the motor drives the turret and the turret decoder, relay A2A4K1 remains energized until decoder A2A4S1A

reaches a position where no ground is provided to the motor relay. For instance, if the code generator output is GOOOO where "G" is ground and "O" a circuit open, then decoder A2A4S1A will rotate until its contacts reflect an open-closed-closed-closed-closed configuration on contacts A2A4S1A-1, 2, 3, 4, 5. Since the ground for relay A2A4K1 is supplied by any grounded line from the code generator, the decoder switch A2A4S1A is rotated until its contacts all see open circuits. Wafer A2A4S1B is complementary to A2A4S1A and receives its inputs in parallel with A2A4S1A on code lines 1 through 5 from the Code Generator Assembly A2A7. Thus, when the input code lines are GOOOO, contacts A2A4S1B-1 through A2A4S1B-5 will be open-closed-closed-closed-closed as the complement of the A2A4S1A-1 through A2-A4S1A-5 terminal connections.

3-169. The purpose of switch wafer A2A4-S1B is to provide re-entrant ground paths for A2A4S1A via Code Generator Assembly A2-A7. Code Generator Assembly A2A7 functions in such a way that all of the open-circuit lines present at A2XA4P1-1 through A2XA4P1-5 corresponding to a given setting of the front-panel frequency controls are tied together. For example, if code line 1 assumes a circuit open for a new code — say, OOGOO — then the ground present on A2S1-A-3 will connect to A2S1B-3, to A2S1B-1 to A2S1A-2 (because A2S1A-2 connects through the code generator A2A7 to A2S1A-1, both being open) and since A2S1A-2 is closed contact to ground now, relay A2A4K1 will energize. Once turret rotation ceases, the turret assemblies A2A4A1 through A2A4A29 are positioned as required to connect the tuning elements that will tune the rf amplifier stages to the selected frequency band.

3-170. FREQUENCY STANDARD ASSEMBLY A2A5 (Figure 5-31). Frequency Standard Assembly A2A5 contains four subassemblies: Oscillator and Oven Control A2A5A1, Divider/Amplifier A2A5A2, Oven Body A2-A5A3, and 5 MHz Reference Control A2A5-A4. The A2A5A1 subassembly uses a temperature-controlled crystal oscillator to provide a stable 5 MHz reference frequency. Subassembly A2A5A4 monitors the 5 MHz signal from the A2A5A1 oscillator and the 5 MHz input from an external frequency standard. The A2A5A4 control circuitry automatically switches to the internal 5 MHz source if the external standard signal falls below a minimum level. The 5 MHz source selected by A2A5A4 is applied to Divider/Amplifier Subassembly A2A5A2 which provides the 10 MHz, 5 MHz, 1 MHz and 500 kHz outputs of A2A5. A visual comparator circuit in A2A5-A2 allows comparison of the internal crystal oscillator frequency to the input from an external standard.

3-171. Input Circuit Operation (EXT NORM Mode). The external 5 MHz reference signal is applied to 5 MHz Reference Control Subassembly A2A5A4 via A2A5J3-1, terminated by A2A5A4R1, and coupled through A2A5A4C1 and current limiting resistor A2-A5A4R2 to the base of amplifier A2A5A4Q1. Operating bias for A2A5A4Q1 is established by resistors A2A5A4R3, A2A5-A4R5, A2A5A4R6, and temperature compensation diodes A2A5A4CR1 through A2A5A4-CR4.

3-172. When the external 5 MHz reference signal input at A2A5J3-1 is approximately 400 mVrms or greater, the amplified positive voltage swings developed by A2A5A4Q1 charge capacitor A2A5A4C2 through diode A2A5A4CR6. The time constant of A2A5-A4C2 and A2A5A4Q2 base is such that A2-A5A4C2 retains a positive charge sufficient to turn on A2A5A4Q2, and thus maintains A2A5A4U1A-1 at a logic high. Pull-up resistor A2A5A4R10 also places a logic high at A2A5A4U1A-2. This causes output pin 3 of A2A5A4U1A to be at a logic low, and places A2A5A4U2D-12 at a logic high through the action of inverter A2A5A4U1B. Because it is reverse biased, isolation diode A2A5A4CR5 in the path with A2A5A4R7 prevents sink current to A2A5A4U1A-3. Since A2A5A4-U2D-13 is also high, a logic low appears at A2A5A4U2D-11 and A2A5A4U2B-5. Under this condition, the output of gate A2A5A4-U2B-6 is always high, and therefore gate A2A5A4U2C-10 remains at a logic high. Since A2A5A4U1C-9 is also at a logic high, the output of NAND gate A2A5A4U1C-8 will be an inversion of the amplified 5 MHz standard frequency at A2A5A4Q1 collector. NAND gate A2A5A4U2C-8 under this condition will output the external 5 MHz standard to Divider/Amplifier Subassembly A2A5A2.

3-173. When the external 5 MHz reference signal at A2A5J3-1 drops below approximately 250 mVrms, as determined by the value of A2A5A4R3, the output level at the collector of A2A5AQ1 is no longer sufficient to forward bias detector diode A2A5A4CR6. Capacitor A2A5A4C2 then discharges to ground through emitter follower A2A5A4Q2 until the voltage at the base of A2A5A4Q3 is insufficient for conduction and A2A5A4Q2 is cut off. Input pin 1 of A2A5A4U1A is then at a logic low level through emitter resistor A2A5A4R9. Output A2A5A4U1A-3 is high, A2A5A4U18-6 is low, A2A5A4U2B-5 is high, so that the internal 5 MHz frequency standard from oscillator and oven control subassembly A2A5A1P5 appears at the output of gate A2A5A4U2B-6. Since A2A5A4U1C-9 is now low, A2A5A4U1C-8 output is held high, which allows NAND gate A2A5A4U2C to pass the internal 4 MHz frequency standard inverted through gate A2A5A4U2C-8 and on to Divider/Amplifier Subassembly A2A5A2-E9 via A2A5J3-4.

3-174. The output level of inverter A2A5-A4U1B changes from logic high to logic low when A2A5A4Q2 is cut off, which switches A2A5A4Q4 from saturation to cut-off. The voltage at A2A5A4Q4 collector then forward biases the base of emitter follower A2A5A4-Q3, and +28 Vdc is supplied by A2A5A4Q3 emitter to input pin 1 of +20 Vdc regulator A2A5A4U3. Zener diode A2A5A4CR7 prevents the base-emitter voltage on A2A5A4Q3 from exceeding 30 Vdc during transients. The +15 Vdc output from pin 2 of A2A5A4U3 is routed through A2A5A4E5 and A2A5A3J1-A4 to Oscillator and Oven Control Subassembly A2A5A1, and the internal 5 MHz oscillator and oven control circuits are energized.

3-175. The internal 5 MHz oscillator output is applied through A2A5A3J1-A5, A2A5-A4E1, and inverter A2A5A4U2A to input pin 4 of A2A5A4U2B. Since logic high levels are now applied to A2A5A4U2B-5 and A2A5A4-U2C-9, the internal 5 MHz signal is gated through A2A5A4U2B and A2A5A4U2C to Divider/Amplifier Subassembly A2A5A2.

3-176. A2A5A4U1A-3 is at a logic low when A2A5A4Q2 is cut off by a low external signal level input. This logic high initiates a current flow through A2A5A4R7 and A2A5-A4CR3 through A2A5A4CR5, which raises the bias level of A2A5A4Q1 base. This bias increase produces a hysteresis effect whereby an increase of the external signal level input to 400 mVrms is now required to switch back to external operator as described in paragraph 3-172.

3-177. Input Circuit Operation (EXT OVEN STBY Mode). When 5 MHz OSC SOURCE switch A2A5A2S1 is set to EXT (OVEN STBY), circuit operation is the same as previously described, with the following exceptions. The emitter of A2A5A4Q4 is no longer grounded through contact 2 of A2A5A2S1. A2A5A4Q4 is off, turning A2A5A4Q3 on. Plus 28 Vdc is applied to input pin 1 of +15 Vdc regulator A2A5A4U3. The oscillator and oven control circuits are energized continuously, so the internal 5 MHz reference signal is immediately available if the external 5 MHz frequency standard fails.

3-178. Input Circuit Operation (INT/COMP Mode). Setting switch A2A5A2-S1 in the INT/COMP position applies +28 Vdc power to regulator A2A5A4U3 in the same manner as described for the EXT (OVEN STBY) mode. +20 Vdc power is applied to the comparator circuit through A2A5A2S1-9. A2A5A2S1-3 is grounded by A2A5A2S1-4, which grounds pin 2 of A2A5A4U1A and pin 13 of A2A5A4U2D. This condition sets the outputs of A2A5A4U1A and A2A5A4U2D at logic high. The logic high from A2A5A4U2D-11 is applied to A2A5A4U2B-5. This gates the internal 5 MHz oscillator signal from inverter A2A5A4U2A through A2A5A4U2B. The logic high at A2A5A4U1A-3 is inverted by A2A5A4U1B and applied to A2A5A4U1C-9. This prevents the external 5 MHz signal from reaching NAND gate A2A5A4U2C. The internal 5 MHz signal is gated by A2A5A4-U2B-6 through A2A5A4U2C to the A2A5A2 subassembly. The signal at A2A5A4U2B-6 also appears at phase detector A2A5A4U1D-12 for use in the comparator circuit.

3-179. Oven Control Circuit Operation. The +10 Vdc operating voltage for the oven control and oscillator circuits is derived from the +15 Vdc output of A2A5A4U3 by a voltage regulator comprised of dropping resistor A2A5A1R9, zener diode A2A5A1CR1, and capacitor A2A5A1C7. The +10 Vdc is applied

to the resistance bridge consisting of A2A5A1R13 through A2A5A1R16 and A2A5A3R2. +10 Vdc is also applied to A2A5A1Q4, A2A5A1Q5 and A2A5A1Q6 through load resistors A2A5A1R17, A2A5A1R18 and A2A5A1R22. Amplifier A2A5A1Q4 is biased by the reference voltage at the junction of A2A5A1R14. A2A5A1R16 and the feedback through A2A5A1R23. A2A5A1Q4, together with emitter follower A2A5A1Q5, form a conventional differential amplifier circuit.

3-180. The base of A2A5A1Q5 is biased by the voltage at the junction of resistor A2A5A1R13 and sensor A2A5A3R2. This voltage varies as the internal temperature of oven body A2A5A3 changes due to the resistance vs temperature characteristic of A2A5A3R2, which is mounted on the oven surface. When the oven temperature rises, the base voltage of A2A5A1Q5 increases. The increased conduction of A2A5A1Q5 increases the voltage drop across emitter resistor A2A5A1R19. The increase in voltage across A2A5A1R19 results in a decrease of base-emitter bias on A2A5A1Q4. A2A5A1Q4 reduces conduction, thus increasing the voltage at A2A5A1Q4 collector. The increased collector voltage appears at the base of amplifier A2A5A1Q6 as a decrease in bias. This results in reduced conduction of A2A5A1Q6 and the voltage drop across A2A5A1R20 is thus reduced. Bias on emitter follower A2A5A1Q7 is also reduced, and the corresponding decrease in voltage on the emitter of A2A5A1Q7 is seen at the base of power amplifier A2A5A4Q5. A2A5A4Q5 conducts less, which reduces the current flow through oven heater A2A5A3R1. If the temperature of the oven decreases below the value established by the setting of potentiometer A2A5A1R15, the circuit operates to increase the current flow through A2A5A3R1, thereby increasing the oven temperature. The value of feedback resistor A2A5A1R23 is selcted to control the damping coefficient so as to prevent excessive temperature overshoot or excessive response time.

3-181. 5 MHz Osclator Circuit Operation. The internal 5 MHz oscillator circuit consists of crystal A2A5A1Y1, oscillator A2A5A1Q1, amplifiers A2A5A1Q2 and A2A5A1Q3, and associated components. It is a conventional, parallel mode, Colpitts oscillator. Oscillations are sustained by the collector to base feedback through A2A5A1Y1. Parallel capacitors A2A5A1C2 and A2A5A1C3 provide fine and coarse adjustment, respectively, of the oscillator frequency.

3-182. The values of capacitors A2A5A1C8 and A2A5A1C11 are selected to provide the proper range of adjustment for the variable capacitors. Two conventional untuned amplifiers (A2A5A1Q2, A2A5A1Q3) provide amplification of the 5 MHz signals. Load resistor A2A5A1R8 and resistor A2A5A1R12 form a voltage divider to prevent A2A5A1Q3 collector voltage from exceeding +5 Vdc. This avoids damaging inverter A2A5A4U2A. The 5 MHz signal at the base of A2A5A1Q3 is applied to a detector circuit consisting of A2A5A1CR2, A2A5A1C10 and A2A5A1R11. This circuit provides negative feedback through resistor A2A5A1R10 to the base of oscillator A2A5A1Q1. This feedback acts to maintain a constant output amplitude. The value of feedback resistor A2A5A1R10 determines the output level at the collector of A2A5A1Q3.

3-183. Comparator Circuit Operation. When connected, the external 5 MHz reference appears at the collector of A2A5A4Q1 and pin 13 of phase comparator A2A5A4U1D. When the 5 MHz OSC SOURCE switch A2A5A2S1 is set to the INT/COMP position, the internal 5 MHz oscillator signal is gated to input pin 12 of A2A5A4U1D. If the two 5 MHz signals to A2A5A4U1D differ in frequency, positive pulses appear at the output of A2A5A4U1D. These pulses vary in width and rate in proportion to the phase difference between the 5 MHz signals. The output pulses from A2A5A4U1D are coupled through capacitor A2A5A2C41 to the base of Amplifier A2A5A2Q10 and are amplified. When the 5 MHz signals are exactly the same frequency, A2A5A2DS1 may be illuminated or extinguished for extended periods of time. If only one 5 MHz signal is present at the input of A2A5A4U1D, the output will be a constant positive dc voltage. This dc voltage is blocked by A2A5A2C41. A2A5A2Q10 is cut off, and the bias to A2A5A2Q11 (through A2A5A2R53, A2A5A2R55, and A2A5A2R56) allows A2A5A2DS1 to illuminate at a constant intensity. In some units, Amplifier A2A5A2Q10 and Lamp Driv-

er A2A5A2Q11, with associated components, are replaced by a simplified LED circuit performing the same function.

3-184. Divide-by-five Oscillator Circuit. The 5 MHz signal at A2A5A4U2C-8 is coupled by A2A5A2C1 to amplifier A2A5A2Q1. Resistor A2A5A2R1 and capacitor A2A5A2-C2 act to decrease the rise and fall times of the 5 MHz logic level transitions and thereby decrease the switching time of amplifier A2A5A2Q1. A2A5A2Q1 provides synchronizing signals to 1 MHz Colpitts oscillator A2-A5A2Q2 and associated components. The value of A2A5A2C44 establishes the range of variable capacitor A2A5A2C7. A2A5A2C7 adjust the oscillator to synchronize on the incoming reference signal. The 1 MHz output from the emitter of A2A5A2Q2 is coupled through A2A5A2R10, A2A5A2R13, A2-A5A2C10 to amplifier A2A5A2Q3. A2A5-A2Q3 controls the output of transformer A2A5A2T1. Variable capacitor A2A5A2C13 allows adjustment of the waveshape at A2-A5A2T1 output. Terminal 4 of A2A5A2T1 is directly connected to output connector A2-A5P1-A3. The values of A2A5A2R17 and A2A5A2R28 are selected for the proper 1 MHz output signal amplitude at A2A5P1-A3.

3-185. Divide-by-two Oscillator Circuit. The 1 MHz signal from A2A5A2Q2 emitter is coupled through resistor A2A5A2R19 and capacitor A2A5A2C14 to the input of A2A5-A2Q4. A2A5A2Q4 and associated components comprise a conventional, 500 kHz, Colpitts oscillator. Operation of the 500 kHz oscillator and amplifier A2A5A2Q5 is similar to the 1 MHz oscillator circuit. Variable capacitors A2A5A2C16 and A2A5A2C22 perform the functions corresponding to A2A5-A2C7 and A2A5A2C13, respectively, in the 1 MHz oscillator circuit. Resistors A2A5A2-R30 and A2A5A2R31 perform the functions corresponding to A2A5A2R17 and A2A5A1-R18.

3-186. Multiply-by-two Circuit. The 5 MHz signal from A2A5A4U2C-8 is coupled through capacitor A2A5A2C25 and resistor A2A5A2R32 to the base of 5 MHz amplifier A2A5A2Q6. A2A5A2C23 and A2A5A2R32 act to decrease the rise and fall times of the 5 MHz signal. The output of A2A5A2Q6 is coupled through A2A5A2C27 to amplifier A2A5A2Q7. A2A5A2Q7 and associated circuitry are tuned to 10 MHz by variable capacitor A2A5A2C31 in the collector circuit. The 10 MHz signal is amplified by A2A5A2Q8 and appears in the primary of A2A5A2T3. A2A5A2T3 and associated components function similarly to A2A5A2T1 described above.

3-187. 5 MHz Output Circuit. The 5 MHz output from A2A5A2Q6 is coupled to amplifier A2A5A2Q9, which is tuned to 5 MHz. The output of A2A5A2Q9 is coupled through capacitor A2A5A2C39 to output connector A2A5P1-A6. Variable capacitor A2A5A2C38 is used to adjust the output waveshape. A2-A5A2R49 is selected to establish the output amplitude.

3-188. TRANSLATOR/SYNTHESIZER ASSEMBLY A2A6 (Figure 5-32). The translator/synthesizer is comprised of nine major subassemblies listed below.

1. Filter Subassembly A2A6A7, a conventional pi filter which filters the +20 Vdc input to Power Supply Subassembly A2A6-A15.
2. 100 kHz Synthesizer Subassembly A2-A6A17.
3. 10 kHz/1 kHz/100 Hz Synthesizer Subassembly (No. 1) A2A6A18.
4. 10 kHz/1 kHz/100 Hz Synthesizer Subassembly (No. 2) A2A6A12.
5. 10 MHz/1 MHz Synthesizer Subassembly A2A6A13.
6. 10 MHz/1 MHz Filter Subassembly A2A6A14.
7. RF Translator Subassembly A2A6A8.
8. Frequency Generator Subassembly A2A6A16.
9. Power Supply Subassembly A2A6A15.

NOTE

Reference designations A2A6A1 through A2A6A6 and A2A6A9 through A2A6A11 are not used in Radio Transmitter T-827H/URT in order to distinguish the Translator/Synthesizer from earlier models.

3-189. The chassis of the Translator/Synthesizer Assembly A2A6 serves as a base and an interconnection/interface mount for the nine subassemblies which perform the func-

tions of the assembly. When the Translator/Synthesizer chassis is mounted in the main frame, three couplers (A2A6MP8, MP12, MP16, figure 7-63) on the bottom are engaged by mechanically driven couplers on the main frame. Each coupler drives one of the switches A2A6S1 through S3, which provide tuning codes for the kHz synthesizers.

3-190. The front panel 100 kHz, 10 kHz and 1 kHz controls are connected by drive chains to couplers on the equipment main frame. When a front panel control is rotated, its associated chain rotates the coupler, thereby positioning the associated coding switch in Translator/Synthesizer Assembly A2A6. The 100 kHz control positions A2A6S3, the 10 kHz control positions A2A6S2, and the 1 kHz control positions A2A6S1. These switches supply a four-line tuning code consisting of opens (BINARY 1) and grounds (BINARY 0) to the synthesizer circuits. The synthesizers produce the injection frequencies used in RF Translator Subassembly A2A6A8. Refer to Table 3-1. When the front panel 100 kHz control is in zero position, the 100 kHz digit of the injection frequency, in both hi and lo bands, is 4. As shown in Figure 5-32, A2A6S3 deck C is open at this setting (contact 1) and the remaining three decks are grounded. Similarly, if the front panel control is set at 300 kHz, the 100 kHz digit of the injection frequency is 7 in both hi and lo bands. In this position the wipers of all four decks of A2A6S3 will be on contact 8, producing an open circuit for all decks except deck B. The 100 kHz digit of the injection frequency increases progressively from 4 thru 9 to 3 as the 100 kHz control is increased from 0 to 9. Switches A2A6S2 and A2A6S1 operate in a similar manner. The 10 kHz switch A2A6S2 and the 1 kHz switch A2A6S1 are natural binary coded decimal (BCD) switches, converting the decimal dial position to BCD. The injection frequency decreases progressively as either the 10 kHz or 1 kHz control is increased. Table 3-1 indicates the injections for the various control positions.

3-191. RF Translator (Figure 5-33). The RF Translator Subassembly A2A6A8 contains the circuits effecting IF-to-RF conversion. The signal flow direction required for the T-827H/URT application is established by gating diodes within the rf translator. Frequency conversion is accomplished in three mixer stages. These progressively combine the IF with injection signals from the synthesizer subassemblies A2A6A17, A2A6A12 and A2A6A14 of Translator/Synthesizer Assembly A2A6.

3-192. Biasing of the gating diodes, which determine the signal path through the rf translator, is accomplished with the dc voltage and ground present at A2A6A8J5 and A2A6A8J7 respectively. The voltage at A2A6A8J4 determines whether the 20 MHz bandpass filter or the 30 MHz bandpass filter is enabled. The input at A2A6A8J4 may be either +20 Vdc for lo band operation or ground for hi band. This is controlled by the hi-lo filter relay A2K2. When the input is +20 Vdc, diodes A2A6A8CR10 and A2A6A8CR12 are biased into conduction. This serves to direct the rf signal through 20 MHz bandpass filter A2A6A8FL1. When A2A6A8J4 is grounded, diodes A2A6A8CR11 and A2A6A8CR13 conduct, directing the rf signal through 30 MHz bandpass filter A2A6A8FL2.

3-193. A2A6A8J5 and A2A6A8J7 inputs are at ground and +20 Vdc, respectively, until the T-827H/URT is keyed. This condition forward biases diodes A2A6A8CR3, A2A6A8CR6, A2A6A8CR9, A2A6A8CR15 and A2A6A8CR18, resulting in no output supplied to the RF Amplifier Assembly A2A4. When the T-827H/URT is keyed, the A2A6A8J5 and A2A6A8J7 inputs are +20 Vdc and ground respectively. The previously described gating diodes are now reverse-biased and gating diodes A2A6A8CR2, A2A6A8CR5, A2A6A8CR7, A2A6A8CR8, A2A6A8CR16 and A2A6A8CR17 are forward-biased.

3-194. Mixer stages A2A6A8U1 through A2A6A8U3 operate in an almost identical manner. They utilize type CA3049 integrated circuits which provide both mixing and amplification. The first input to low frequency mixer is an injection frequency in the range of 3.3001 to 3.4000 MHz. It is received at A2A6A8E6 from 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12, and applied to pin 2 of A2A6A8U1. Resistors A2A6A8R56 and A2A6A8R11 provide the proper impedance termination for the output of A2A6A12 and input of A2A6A8U1. Ther-

mistor A2A6A8RT1 produces an increase in the injection signal input level applied to mixer A2A6A8U1 whenever the operating temperature increases. Resistor A2A6A8R3 controls the effect thermistor A2A6A8RT1 has on the injection signal input level.

3-195. The second input to the mixer is the 500 kHz IF signal. It is received at A2A6A8-E1 from IF Amplifier Assembly A2A12, and applied to low frequency mixer A2A6A8U1 through lowpass filter A2A6A8L15, capacitor A2A6A8C14, forward-biased gating diode A2A6A8CR2 and transformer A2A6A8T2. A2A6A8R14 is a swamping resistor, placed across the primary winding of input transformer A2A6A8T2 to provide the required bandwidth. The signal at the secondary of A2A6A8T2 is applied as the second input to pins 1 and 10 of A2A6A8U1. Resistive divider A2A6A8R59, A2A6A8R60 and A2A6A8R61 applies bias voltage through the split secondary winding of A2A6A8T2 to the internal amplifiers associated with pins 1 and 10. The sum and difference output signals exit from pins 11 and 12 of A2A6A8U1 and are applied to the primary winding of output transformer A2A6A8T3. A2A6A8R4 is a series dropping resistor in the +20 Vdc path to the amplifiers within A2A6A8U1. Capacitors A2A6A8C8, A2A6A8C15, and A2A6A8C17 provide rf bypassing for the internal biasing circuits within mixer A2A6A8U1. The output from A2-A6A8U1 is then directed through A2A6A8-CR5 to bandpass filter A2A6A8FL3. Only the 2.8001 to 2.9000 MHz element (difference frequency) is passed through A2A6A8-CR7 and A2A6A8T5 to the input of mid-frequency mixer A2A6A8U2.

3-196. In mid-frequency mixer A2A6A8U2, the signal from A2A6A8T5 is mixed with the injection signal (22.4 to 23.3 MHz lo-band or 32.4 to 33.3 MHz hi-band) from 100 kHz Synthesizer Subassembly A2A6A17 and filter A2A6FL5 at A2A6A8E8. The 19.5000 to 20.4999 MHz (lo-band) or 29,5000 to 30.4999 MHz (hi-band) output from A2A6A8U2 then passes through gating diode A2A6A8CR8 to bandpass filter A2A6A8FL1 or A2A6A8FL2 as determined by the voltage at A2A6A8J4. The filtered output is applied through A2A6-A8C48, A2A6A8C51, gating diode A2A6A8-CR16, and transformer A2A6A8T7 to the input of mixer A2A6A8U3.

3-197. A2A6A8U3 performs the high frequency conversion by mixing the input at pin 1 with the 2.5 to 23.5 MHz injection at pin 2. The frequencies developed across the secondary of A2A6A8T6 are fed through forward-biased gating diode A2A6A8CR17 and capacitor A2A6A8C58 to A2A6A8CR14, A2-A6A8L14 and A2A6A8C59 in series with A2-A6A8C57. The signal is then coupled to A2-A6A8E12 by A2A6A8C56. In lo-band operation, A2A6A8CR14 is reversed biased so that the signal must flow through A2A6A8L14 and A2A6A8C59 in parallel. A2A6A8L14 and A2A6A8C59 are resonant at 19.6 MHz to remove a spurious signal.

3-198. Frequency Generator (Figure 5-38). Frequency Generator Subassembly A2-A6A16 receives a stable 10 MHz reference from Frequency Standard Assembly A2A5. Using integrated circuit dividers, the frequency generator produces the 500, 100 and 1 kHz reference frequencies used in the frequency synthesizer circuits.

3-199. The stable, 10 MHz reference output from Frequency Standard A2A5 is applied to Frequency Generator Subassembly A2A6-A16 via connector A2A6A16P1-A1. It is terminated by resistor A2A6A16R1, and coupled through A2A6A16C5 to the input of two-stage, common emitter amplifier A2A6-A16Q1, A2A6A16Q2. Resistors A2A6A16R2, A2A6A16R3, A2A6A16R6 and A2A6A16R7 provide base bias for A2A6A16Q1 and A2A6-A16Q2. Shunt peaking inductors A2A6A16-L6, A2A6A16L7 and stray capacitance form high impedance parallel L-C networks to improve high frequency response. The emitters are partially bypassed by capacitors A2A6-A16C7 and A2A6A16C9 to improve stability.

3-200. The amplified 10 MHz signal at the collector of A2A6A16Q1 is capacitively coupled via A2A6A16C8 to the base of A2A6-A16Q2. Amplifier A2A6A16Q2 provides additional amplification and applies the 10 MHz signal through capacitor A2A6A16C10 to a level shifter consisting of inverter A2A6-A16U1A, capacitor A2A6A16C11, and resistors A2A6A16R10, R11. The sinusoidal 10 MHz signal at input 1 of A2A6A16U1A is converted into a square wave output at pin 2, which is then suitable for driving the remaining integrated circuit gates and dividers of subassembly A2A6A16.

3-201. The integrated circuit divider chain A2A6A16U2, A2A6A16U5 is isolated from the level shifter circuit components by a buffer stage consisting of inverters A2A6A16U1B and A2A6A16U1C. The 10 MHz output signal at pin 12 of inverter A2A6A16U1C is applied to input pin 14 of decade divider A2A6A16U2, which applies a 1 MHz input signal to pin 14 of binary decade divider A2A6A16U3. Output pin 12 (binary divider) of A2A6A16U3 provides a 500 kHz clock pulse to connector A2A6A16P1-A2 for use as the reference frequency input to 10 MHz/1 MHz Synthesizer Subassembly A2A6A13.

3-202. The 500 kHz clock pulse at A2A6A16U3-12 is also applied to input pin 1 of another divider within A2A6A16U3, which provides a 100 kHz output signal from pin 11. This is distributed to pin 1 of decade divider A2A6A16U4 and to connector A2A6A16P1-A4 for use by 100 kHz synthesizer assembly A2A6A17. Divider A2A6A16U4 then provides a 10 kHz clock pulse output at pin 12 to input pin 1 of decade divider A2A6A16U5. The 1 kHz output from pin 12 of A2A6A16U5 is applied to A2A6A16U6B pin 12 which is part of gating circuit A2A6A16U6A-A2A6A16U6D. This gating circuit selects either the 1 kHz output of A2A6A16U5 or the variable 1 kHz frequency output of the phase-locked loop circuit (consisting of A2A6A16U9 through A2A6A16U17 and A2A6A16Q5) as the reference frequency for 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12.

3-203. The gating circuit is enabled when level shifter A2A6A16Q3, A2A6A16Q4 responds to the +4.3 Vdc input at connector A2A6A16P1-9. The +4.3 Vdc from zener diode A2CR10, located on the T-827H/URT main frame, is applied to voltage divider A2A6A16R12, A2A6A16R13. Transistor A2A6A16Q3 is then biased on and A2A6A16Q4 is biased off. This action applies +5 Vdc through load resistor A2A6A16R15 to inverter A2A6A16U6A and NAND gate A2A6A16U6B. This logic high level input at A2A6A16U6B-13 allows the 1 kHz pulse at A2A6A16U6B-12 to appear as a logic low at input pin 1 of NAND gate A2A6A16U6D. Input pin 2 of A2A6A16U6D is maintained at a constant logic high due to the logic low applied through inverter A2A6A16U6A to input pin 4 of NAND gate A2A6A16U6C. Each negative transition of the 1 kHz pulse gates pin 3 of A2A6A16U6D, resulting in a logic high level output. The circuits comprised of A2A6A16U7 through A2A6A16U17, and associated components, are inactive for T-827H/URT application. Their operation is covered in Technical Manual EE125-AD-OMI-010/E510-R1051G for Radio Receiver R-1051G/URR.

3-204. 10 kHz/1 kHz/100 Hz Synthesizer. The 10 kHz/1 kHz/100 Hz Synthesizer Subassemblies A2A6A18 (Figure 5-40) and A2A6A12 (Figure 5-34) produce the 3.3001 to 3.4000 MHz injection signal used in the low-frequency mixer of RF Translator Subassembly A2A6A8. A phase-locked loop is used to ensure accuracy of the injection frequency. The phase-locked loop is a servo system in which the output signal is locked to the 1 kHz input reference signal from Frequency Generator Subassembly A2A6A16. The phase of the output signal is compared with the phase of the 1 kHz reference in A2A6A12, and any difference is converted into a dc error correction voltage. This error correction voltage alters the output frequency to maintain a constant phase difference between the output and the 1 kHz reference signal.

3-205. The output signal is generated by the voltage-controlled oscillator (VCO) consisting of variable capacitance diode A2A6A12A1CR1, LC oscillator A2A6A12A1U1, and associated components. The frequency at A2A6A12A1U1 is 33.001 to 34.000 MHz. This is determined by the reactance of the LC tank circuit comprised of varactor diode A2A6A12A1CR1, capacitors A2A6A12A1C2, A2A6A12A1C3, and inductor A2A6A12A1L1. A dc control voltage biases A2A6A12A1CR1 (through resistor A2A6A12A1R1) to establish the correct value of the LC tank circuit reactance, thereby determining the specific output frequency from A2A6A12A1U1. Capacitors A2A6A12A1C1 and A2A6A12A1C4 complete the signal path for the 33.001 to 34.000 MHz oscillations in the LC tank circuit.

3-206. The output signal at pin 3 of A2A6A12A1U1 is applied to a programmable frequency divider network on 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A18. The programmable frequency divider network se-

lects the injection frequency in response to the positions of the front panel 100 Hz control A2S6, the 1 kHz coding switch A2A6S1, and the 10 kHz coding switch A2A6S2 on the chassis of Translator/Synthesizer A2A6. For example, if the front panel controls are set for a frequency of 1,100 Hz, the divider network will be programmed to divide the VCO output frequency by 33,989. In the phase-locked condition, the VCO output frequency is exactly 33.989 MHz and the divider network output frequency is exactly 1 kHz. If the VCO output is slightly off frequency, the output from the divide-by-33,989 network will no longer be exactly 1 kHz.

3-207. The divider network output is applied to pin 3 of phase detector A2A6A12U1, which develops negative pulsed output in proportion to the magnitude and direction of the phase difference between the divider network output and the 1 kHz reference input from Frequency Generator Subassembly A2A6A16. The negative pulses are applied through resistor A2A6A12R4 and A2A6A12-R19 to the charge pump circuit comprised of transistors A2A6A12Q1 through A2A6A12-Q3. The charge pump amplifies the negative going pulses from A2A6A12R4, or inverts and amplifies the negative going pulses from A2-A6A12R19. The charge pump output (which consists of negative or positive going pulses, respectively) is applied to loop filter A2A6-A12C2, A2A6A12R7, and A2A6A12R9, which converts the output pulses from the charge pump into the dc frequency control voltage required by variable capacitance diode A2-A6A12A1CR1. If the phase difference between the pin 1 and pin 3 inputs to A2A6A12-U1 is not constant, the dc frequency control voltage will decrease or increase the reverse bias across A2A6A12A1CR1, and the capacitance of A2A6A12A1CR1 will change, as required, to establish the proper output frequency from the VCO.

3-208. The output signal at pin 3 of A2A6-A12A1U1 is also applied to emitter follower A2A6A12A1Q1, which isolates LC oscillator A2A6A12A1U1 from the output circuitry of 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12. From the emitter of A2-A6A12A1Q1, the VCO output is applied to amplifiers A2A6A12U2A through A2A6A12-U2C, which increase the amplitude of the 33.001 to 34.000 MHz signal and provide the correct logic level input to pin 8 of decade divider A2A6A12U3. The 3.3001 to 3.4000 MHz output signal from pin 2 of A2A6A12U3 is inverted by A2A6A12U2D and applied to the bandpass filter consisting of A2A6A12L6 through A2A6A12L10 and A2A6A12C10 through A2A6A12C12. The narrow pass-band and sharp cutoff characteristics of this filter attenuate frequencies outside the injection signal range to prevent spurious responses. The injection signal amplitude is adjusted by potentiometer A2A6A12R16 to establish the proper injection signal level to the low frequency mixing circuit of RF Translator Subassembly A2A6A8.

3-209. The A2A6A18 assembly (see Figure 5-40) performs the division of the A2A6A12-A1U1 VCO output frequency to provide the 1 kHz frequency for the A2A6A12U1 phase detector. Dual Modulus Prescaler A2A6A18U1 divides inputs on pin 15 by either 10 or 11 depending upon whether pins 9 and 10 are at a logic high or low respectively. This divided frequency output from A2A6A18U1 pin 7 is applied to counters A2A6A18U3 and A2A6-A18U4 and to counter control logic device A2A6A18U2. Once each kilohertz period, the inputs to A2A6A18U2 on pins 10 through 14 achieve the logic states necessary to produce an output at pin 9. This output is the 1 kHz frequency for the phase detector A2A6-A12U1.

3-210. Dual Modulus Prescaler A2A6A18U1 will divide by 11 if the 100 Hz control (A2S6) is in any hundred position other than 000. This division by 11 will continue until outputs from A2A6A18U3 at pins 7, 9, 15 and 1 are all logic lows. These logic lows at A2A6-A18U2 pins 2, 3, 4, and 5 force A2A6A18U2 pin 7 to a logic high for the balance of a counting cycle. This logic high is applied to A2A6A18U1 pins 9 and 10, which makes the dual modulus prescaler divide by 10 for the balance of a counting cycle. A counting cycle begins and ends with each output from A2A6A18U2 pin 9. The number of input pulses to A2A6A18U1 pin 15 will be the count set into A2A6A18U3 through A2A6-A18U7.

3-211. Cascading of dividers A2A6A18U4 through A2A6A18U7 is accomplished by sup-

plying the input to each divider from the pin 1 output of each preceding divider. Thus, the preset count in A2A6A18U7 represents the most significant digit in the programmable divider network. The preset count (pin 12) outputs of dividers A2A6A18U5 through A2-A6A18U7 are connected in parallel so that the data reset pulse is applied to pin 10 of A2A6A18U2 only when A2A6A18U5 through A2A6A18U7 have all counted down from their preset numbers to the zero state. Control logic in A2A6A18U2 also monitors the state of divider A2A6A18U4 to determine the end of the counting cycle.

3-212. Since the divider network output is taken from pin 9 of A2A6A18U2, an output pulse will be present only when A2A6A18U3 and A2A6A18U4 through A2A6A18U7 have counted down from their preset numbers to zero. As an example, assume that the front panel kHz and 100 Hz controls have been set at 2,500 Hz to select a low frequency mixer stage injection frequency of 3.3975 MHz. In this case counts of 5, 7, 9, 3 and 3 are preset in dividers A2A6A18U3 through A2A6A18U7, respectively. With A2A6A18U3 preset to divide-by-5, prescaler A2A6A18U1 divides-by-11 five times. After 55 input pulses to pin 15 of A2A6A18U1, preset divider A2A6A18U3 reaches the all zero state and counter control logic A2A6A18U2 changes the divisor of A2A6A18U1 from 11 to 10. At this time, cascade divider A2A6A18U4 through A2A6-A18U7 has also decreased by five (from the preset divisor of 3.397) and is at the 3.392 count. Since the divisor of A2A6A18U1 is now 10, cascade divider A2A6A18U1 through A2A6A18U7 decreases by one count for every ten input pulses to prescaler A2A6-A18U1, and therefore reaches the all zero state after 33.920 input pulses have been applied to pin 15 of A2A6A18U1. When this occurs, A2A6A18U3 and A2A6A18U4 through A2A6A18U7 are in the all zero state, and one output pulse is applied from pin 9 of counter control logic A2A6A18U2 to input pin 3 of phase detector A2A6A12U1.

3-213. Note that the total number of input pulses required for one output pulse is 33.920 plus 55, or 33,975. Since the phase detector input pulses must occur at a 1 kHz rate in phase-locked condition, the outut frequency of VCO assembly A2A6A12A1 is locked at 1 kHz times 33,975 or 33,975 MHz. The VCO output is then applied through decade divider A2A6A12U3 to provide a 3,3975 MHz injection signal to the low-frequency mixing circuit of RF Translator Subassembly A2A6A8 as previously described.

3-214. Programming of dividers A2A6A18-U3 through A2A6A18U6 is controlled by the setting of the front panel 10 kHz, 1 kHz, and 100 Hz controls. For example: 100 Hz control A2S6 applies one of ten binary coded decimal (BCD) words to input pins 8 through 11 of A2A6A18P1. The BCD words are formed by applying either an open circuit (logic low) or +4.3 Vdc (logic high) to each of the four code lines, with the input at A2A6-A18P1-11 corresponding to the least significant bit of the word. The code from the 100 Hz control undergoes logic level conversion in level shifters A2A6A18Q1 through A2A6-A18Q8, which change the logic low/high levels from the switches to the TTL logic low/high levels which are the required inputs to complement converter A2A6A18U8.

3-215. Each BCD word (see note 1 of Figure 5-9) applied to input pins 10 through 13 of A2A6A18U8 represents a unique setting of the front panel 100 Hz control. The outputs from pins 1 through 4 of A2A6A18U8 are then applied to the data pins of divider A2A6A18U3, with the code from A2A6A18U8 pin 1 representing the least significant bit. For example, when the front panel 100 Hz control is set to 300, the BCD word 3 (0011) is applied to A2A6A18U8, and is converted into 7 (0111) on pins 4, 3, 2, and 1 respectively, for programming of divider A2A6A18U3. (See notes 1 and 2 of figure 5-9.) Divider A2A6A18U3 is then preset to count down from the number 7.

3-216. Programming of divider A2A6A18-U4 differs from the previous paragraphs in that the preset counts depend upon whether the 100 Hz control is in the 000 position or not. (See note 3 of Figure 5-9.) If the 100 Hz control is in the 000 position, A2A6A18U8 pin 5 is at a logic zero. (See note 1 of figure 5-9.) The logic zero is applied to A2A6A18-U9 pin 14. Thus, the output of A2A6A18U9 will be the 10's complement of the input from kHz switch A2A6S1. If, however, the 100 Hz control is in other than the 000 posi-

tion, pin 5 of A2A6A18U8 will be at a logic high and A2A6A18U9 will perform the 9's complement of any input from the kHz switch. Thus, 7000 on the Hz and kHz dials will be programmed as its 10's complement into A2A6A18U9 i.e., as (0011) on pins 2, 14, 11 and 5 of A2A6A18U4, while 7100 will be programmed at its 9's complement into A2-A6A18U4 as 2 (0010) on pins 2, 14, 11 and 5.

3-217. Programming of A2A6A18U5 is accomplished in a similar manner to A2A6A18-U4. The BCD word from 10 kHz switch A2-A6S2 is applied to converter A2A6A18U10. (See note 3 of Figure 5-9.) If both the Hz and kHz controls are set at 0, A2A6A18U10 will perform the 10's complement of the input BCD word from the 10 kHz control since pin 14 of A2A6A18U10 will be at a logic zero. However, if either the Hz or kHz control is set other than at 0, A2A6A18U10 pin 14 will be set at a logic high and a 9's complement conversion of the input BCD word from the 10 kHz control will be performed by A2A6A18U10. A2A6A18U10 conversion outputs on pins 1 through 4 program A2A6A18U5 on pins 5, 11, 14 and 2. A2A6A18U6 is programmed as a 4 if the Hz, kHz and 10 kHz controls are all at 0. For this condition pin 6 of A2A6A18U10 will be at a logic high. This logic high is applied to A2A6A18U6 and programs it to a 4. If, however, any or all of the Hz, kHz or 10 kHz controls are set at other than 0, A2A6A18U10 pin 5 will be at a logic high. This logic high is applied to pins 5 and 11 of A2A6A18U6, and A2A6A18U6 is programmed as a 3. Three and four are the only programmed states for A2A6A18U6. A2A6-A18U7 is always programmed for three by applying 5 volts through A2A6A18R2 to pins 5 and 11.

3-218. 100 kHz Synthesizer A2A6A17 (Figure 5-39). The 100 kHz Synthesizer Subassembly A2A6A17 produces the injection frequency of 22.4 to 23.3 MHz (lo-band) or 32.4 to 33.3 MHz (hi-band) used in the mid-frequency mixer circuits of RF Translator Subassembly A2A6A8. This synthesizer uses phase-locked loop circuitry similar to that used in 10 kHz/1 kHz/100 Hz Synthesizer Subassembly A2A6A12/A2A6A18. The phase detector (A2A6A17U1), charge pump (A2A6-A17Q6 through A2A6A17Q8), loop filter (A2A6A17C2 - A2A6A17C3, A2A6A17R8, A2A6A17R32 - A2A6A17R33), VCO (A2A6-A17A1CR1, A2A6A17A1L1, A2A6A17A1U1) and variable divisor (A2A6A17U6 through A2A6A17U8) circuits are identical to the corresponding circuits of the 10 kHz/1 kHz/100 Hz synthesizer except for component values.

3-219. The VCO output from pin 3 of LC oscillator A2A6A17A1U1 is applied through emitter follower A2A6A17A1Q1 to a programmable frequency divider network consisting of integrated circuits A2A6A17U4 through A2A6A17U8. This network divides the VCO output frequency by a number in the range of 224 to 233 or 324 to 333 as determined by the setting of the front panel 100 kHz control and the state of the hi-lo band control line at pin 7 of A2A6A17P1. From pin 9 of A2A6A17U5, the divider network output is applied to input pin 3 of phase detector A2A6A17U1. The phase detector produces an error correction output proportional to the phase difference between the divider network output signal and the 100 kHz reference signal from Frequency Generator Subassembly A2A6A16. The VCO output is phase-locked to the 100 kHz reference signal as previously described. Since the phase-locked loop maintains the programmable frequency divider output at exactly 100 kHz, the VCO output is a discrete frequency in the range of 22.4 to 23.3 MHz (lo-band) or 32.4 to 33.3 MHz (hi-band).

3-220. Programmable divider network A2-A6A17U4 through A2A6A17U8 functions in the same manner as the 10 kHz/1 kHz/100 Hz synthesizer divider network. The front panel 100 kHz control is coupled to coding switch A2A6S3 via a mechanical chain-drive mechanism. For each position of the front panel control, the coding swich generates a unique, offset BCD word. This BCD word consists of open circuits and grounds, and is converted to standard BCD format (grounded and +5 Vdc lines) by pull-up resistors. The BCD word is then applied to the data input (pins 2, 14, 11 and 5) of divider A2A6A17U6 to establish the preset counts.

3-221. When the front panel controls are set at 400 kHz, the data input to A2A6A17U6 is a BCD 8 (1000). (See note 1 of figure 5-10.) A Divider A2A6A17U6 is preset to 8.

Divider A2A6A17U7 is preset for 2 for 100 kHz control settings of 0 through 5, and to 3 for 100 kHz settings of 6 through 9. For 100 kHz control settings of 0 through 5 the logic level at either pin 2 or 14 of A2A6A17U6 is a logic high, through pull-up resistor A2A6-A17R24 or A2A6A1R25. These levels are applied to NOR gate A2A6A17Q4 and A2A6-A17Q5. The common collector (NOR gate output) will be a logic low, and A2A6A17U7 will be preset to 2. For 100 kHz settings of 6 through 9 both inputs to the NOR gate will be at a logic low so the NOR gate output will be at a logic high and A2A6A17U7 will be preset to three.

3-222. Divider A2A6A17U8 is preset to either 2 or 3 in response to the state of the hi-lo band control input at A2A6A17P1-7. Transistor A2A6A17Q3 converts the +20 Vdc/-ground control input into logic low/logic high levels for application to data pin 5 of A2A6A17U8. Thus, A2A6A17U8 is preset to 2 for a +20 Vdc control input (lo-band) and to 3 for a ground control input (hi-band).

3-223. The VCO output is also applied to a conventional common-emitter amplifier A2-A6A17Q1, which isolates the VCO from the output stage circuitry. The gain of A2A6-A17Q1 is set by means of potentiometer A2-A6A17R10 to establish the proper output signal level. The signal is applied from the collector of A2A6A17Q1 to bandpass filter A2-A6A17L4 - A2A6A17L7, A2A6A17C15, A2-A6A17C17 and A2A6A17C18. This filter attenuates undesired signals outside the range of 22.4 to 33.3 MHz. Common emitter amplifier A2A6A17Q2 provides a low impedance output for filter assembly A2A6FL5.

3-224. 22.9/32.9 MHz Filter Assembly A2-A6FL5 (Figure 5-32). Filter assembly A2-A6FL5 serves to remove unwanted spurious signals from the output of the 100 kHz A2-A6A17 assembly. When the set is tuned to lo-band, the injection frequency is between 22.4 and 23.3 MHz, while for a high band the frequency is between 32.4 and 33.3 MHz. Filter Assembly A2A6FL5 receives hi/lo band information from A2A6P1-20 to enable the internal hi/lo band filter. Internal steering diodes direct the A2A6A17 output through either the high or low narrow band filters. The A2A6FL5 output is applied as the injection signal for use in the mid-frequency mixing circuits of RF Translator assembly A2-A6A8.

3-225. 10 MHz/1 MHz Synthesizer Subassembly A2A6A13 (Figure 5-35). The 10 MHz/1 MHz Synthesizer Subassembly A2A6-A13 accepts a 500 kHz reference signal from Frequency Generator Subassembly A2A6A16 and a five-line tuning code (consisting of opens and grounds) from Code Generator Assembly A2A7. The A2A6A13 subassembly provides one of 17 injection frequencies in the range of 2.5 to 23.5 MHz to the high frequency mixer circuit of RF Translator Subassembly A2A6A8.

3-226. The phase-locked loop operation is identical to that previously described for the 10 kHz/1 kHz/100 Hz and 100 kHz synthesizers; that is, the 20 to 50 MHz VCO output signal is applied through a programmable frequency divider network to establish one input to phase detector A2A6A13U1. Phase detector A2A6A13U1 then compares the phase of this signal with the phase of a 500 kHz reference signal supplied by Frequency Generator Subassembly A2A6A16, and generates a dc frequency correction voltage (via loop filter A2A6A13U2, A2A6A13C3, A2A6-A13R8) to lock the VCO on frequency.

3-227. Programmable dividers A2A6A13-U9, A2A6A13U10 are preset, via data inputs to pins 2, 14, 11 and 5, in the same manner as the previously described dividers (A2A6A16-U15, A2A6A16U16, A2A6A17U6, A2A6A17-U8, and A2A6A18U3 through A2A6A18U7). A five-wire tuning code (consisting of open circuits and grounds) from Code Generator Assembly A2A7 is applied through filter assembly A2A6A13A1 to input pins 10 through 14 of read-only memory A2A6A13U11. Each tuning code corresponds to a unique setting of the front panel MHz controls, and is converted to BCD format via A2A6A13U11. When the front panel controls are set to 19 MHz, the input to code lines 1 through 5 will be G, G, G, O, O (where "G" represents a ground and "O" represents an open circuit) as shown in table 3-2.

3-228. The grounded and open lines are converted to logic low and logic high levels, respectively, via pull-up resistors and the in-

put code 0, 0, 0, 1, 1 is applied to pins 10 through 14 of A2A6A13U11. Pins 6, 7 and 9 of A2A6A13U11 then apply the code 0, 1, 0 to data pins 5, 11 and 14 of A2A6A13U10, which is thereby preset to 2. In like manner, pins 3, 4, and 5 of A2A6A13U11 preset the count of A2A6A13U9 at one. Since the dividers are in a cascade configuration, the input frequency at pin 6 of A2A6A13U9 is divided by 21 and appears at output pin 9 of counter control logic A2A6A13U8 for application to the phase detector.

3-229. The VCO output signal is applied to programmable dividers A2A6A13U9, A2A6A13U10 through fixed divider A2A6A13U5. Assuming that the front panel controls are set at 19 MHz and that the VCO is phase-locked to the reference signal at pin 1 of A2A6A13U1, a 42.0 MHz signal from pin 3 of LC oscillator A2A6A13U3 is applied through emitter follower A2A6A13Q1 to pin 6 of A2A6A13U4. Both A2A6A13U4A and A2A6A13U4B provide logic level conversion and buffering for reliable operation of divider A2A6A13U5. A2A6A13U5 then provides output signals of 21, 10, 5 and 5.25 MHz at pins 5 and 6, pin 9, and pin 2, respectively. Selection of the 10.5 MHz output from pin 9 of A2A6A13U5 is accomplished by gating circuitry in response to the signals from output pins 1 and 2 of read-only memory A2A6A13U11. Since, in the example, the programmable divider network is preset to divide-by-21, the 10.5 MHz signal appears as a 500 kHz signal at input pin 3 of phase detector A2A6A13U1, as required for the phase-locked condition.

3-230. The gating circuitry selects the proper output from divider A2A6A13U5 and also selects the appropriate filter network within 10 MHz/1 MHz Filter Subassembly A2A6A14. If pins 1 and 2 of A2A6A13U11 are at logic low and logic high levels, respectively, NOR gates A2A6A13U4C and A2A6A13U4D will open and pass the 5.25 MHz output of A2A6A13U5 to the programmable frequency divider network via NOR gate A2A6A13U7A through A2A6A13U7C, and to output connector A2A6A13A1P1-A2. The logic low level at pins 9 and 12 of A2A6A13U4 is also applied to transistor switch A2A6A14Q1, which then applies operating voltage to the 2.5 to 5.5 MHz filter network. In a similar manner, NAND gates A2A6A13U6A and A2A6A13U6B select the 10.5 MHz output of A2A6A13U5 whenever output pin 2 of A2A6A13U11 is at a logic low level.

3-231. Selection of the 21 MHz output from A2A6A13U5 is accomplished by a NAND gate comprised of A2A6A13CR5, A2A6A13CR6, and A2A6A13Q2. Diodes A2A6A13CR5, A2A6A13CR6 monitor the control lines from pins 1 and 2 of A2A6A13U11 and, if either line is at a logic low level (i.e., either the 2.5 to 5.5 MHz or 7.5 to 12.5 MHz gates are open), transistor A2A6A13Q2 is cut off. In this condition, the collector of A2A6A13Q2 is at a logic high level and the 14.5 to 23.5 MHz gates are closed. When both control lines are at a logic high level, diodes A2A6A13CR5, A2A6A13CR6 cause transistor A2A6A13Q2 to turn-on, and the logic low at the collector of A2A6A13Q2 opens gates A2A6A13U6C, A2A6A13U6D. This condition applies operating voltage, via transistor switch A2A6A14Q7, to the 14.5 to 23.5 MHz filter network in 10 MHz/1 MHz Filter Subassembly A2A6A14.

3-232. 10 MHz/1 MHz Filter Subassembly A2A6A14 (Figure 5-36). The 10 MHz/1 MHz Filter Subassembly filters the outputs of 10 MHz/1 MHz Synthesizer Subassembly A2A6A13. A2A6A14 contains three separate circuits: A 4 MHz bandpass filter, a 10 MHz bandpass filter, and a 19 MHz bandpass filter. These circuits perform identically, and differ only in the electrical values of their component parts. Each circuit filters a specific portion of the 10 MHz/1 MHz Synthesizer output band. Only one circuit at a time is active, as selected by the outputs of read-only memory A2A6A13U11. Since circuit performance is identical for all three circuits, only the 4 MHz circuit will be described.

3-233. The 2.5 to 5.5 MHz injection signal from A2A6A13 at A2A6A14P1-A1 is coupled through A2A6A14C1 to the base of amplifier A2A6A14Q2. At the same time a control signal (ground) applied at A2A6A14P1-1 turns on transistor switch A2A6A14Q1, which applies operating voltage to amplifier A2A6A14Q2 and to buffer A2A6A14Q3. The conventional, untuned amplifier A2A6A14Q2 utilizes shunt peaking inductor A2A6A14L1

and a partially bypassed emitter resistance (provided by capacitor A2A6A14C4) to establish uniform gain over the 2.5 to 5.5 MHz frequency range. The voltage gain of A2A6A14Q2 is adjusted by means of potentiometer A2A6A14R7. From the collector of A2A6A14Q2, the amplified 2.5, 3.5, 4.5, or 5.5 MHz signal is coupled through A2A6A14C2 to a bandpass filter consisting of A2A6A14L2 through A2A6A14L5, A2A6A14C3, and A2A6A14C5, A2A6A14C6. The bandpass filter attenuates signals outside the 2.5 to 5.5 MHz frequency range, and applies the desired signal through A2A6A14C7 to the base of emitter follower A2A6A14Q3. The emitter of A2A6A14Q3 provides a low impedance injection signal source through capacitor A2A6A14C29, for the subassembly output at A2A6A14P1-A4. Resistors A2A6A14R9, A2A6A14R10 provide operating bias for A2A6A14Q3; A2A6A14C8 and A2A6A14L6 provide power supply decoupling. Buffers of all circuits (A2A6A14Q3, A2A6A14Q6, and A2A6A14Q9) utilize A2A6A14R31 as the same emitter resistor.

3-234. Power Supply Subassembly A2A6A15 (Figure 5-37). The power supply subassembly receives +20 Vdc from Filter Subassembly A2A6A7. Power Supply A2A6A15 generates the +5 Vdc required to operate the translator/synthesizer subassemblies. A solid state switching regulator design is used which provides high efficiency and minimizes dissipation in the regulating elements. It employs two separate current-limiting stages to protect the supply.

3-235. The +20 Vdc input is filtered by capacitors A2A6A15C2, A2A6A15C3, A2A6A15C16, and applied to oscillator A2A6A15U1. A2A6A15U1 is a free-running 30 to 35 kHz oscillator with regenerative feed-back through resistor A2A6A15R2 and capacitor A2A6A15C1. Dropping resistors A2A6A15R1, A2A6A15R3 and feedback resistor A2A6A15R4 provide a voltage reference at input pin 2 of A2A6A15U1 to maintain a constant amplitude square wave output at A2A6A15U1-7. This output is applied through low-pass filter A2A6A15R6 and A2A6A15C4 to the reference input of voltage regulator A2A6A15U2-5. A2A6A15U2 applies a regulated 5 volt square-wave from output pin 2 to switch driver A2A6A15Q1. This square-wave drives A2A6A15Q1 into conduction. The output of A2A6A15Q1 provides base bias for switch A2A6A15Q3. Switch A2A6A15Q3 is overdriven to provide fast turn-on time. When A2A6A15Q1 and A2A6A15Q3 are conducting, energy is stored in inductor A2A6A15L1 and capacitors A2A6A15C9, A2A6A15C10, and supplied to the load. When A2A6A15Q1 and A2A6A15Q3 are off, the energy stored in A2A6A15L1 and A2A6A15C9, A2A6A15C10 powers the load. Diode A2A6A15CR2 provides the return path for the current.

3-236. Regulation of the filtered +5 Vdc at A2A6A15E4 is provided by feedback voltage dividers A2A6A15R14 through A2A6A15R16. This network applies feedback to pin 6 of A2A6A15U2. The switching duty-cycle is controlled by this feedback voltage, so that if the output voltage increases, the feedback voltage to A2A6A15U2-6 also increases, causing the duty-cycle to decrease and thereby the output voltage to decrease to the required value. Resistor A2A6A15R15 is selected to provide a +5.1 to +5.2 Vdc output voltage for a 2 ampere output current level. The current through switch A2A6A15Q3 flows through series resistor A2A6A15R9. This provides bias on current limiter A2A6A15Q2. When the voltage drop across A2A6A15R9 becomes large enough to forward bias A2A6A15Q2, the current limiter transistor functions as the control element. A2A6A15Q2 applies feedback through resistor A2A6A15R13 to input pin 6 of A2A6A15U2, thus reducing the output voltage of the circuit. Resistor A2A6A15R11 limits the base current of A2A6A15Q2. Capacitor A2A6A15C5 ensures that A2A6A15Q2 does not turn on from current spikes through A2A6A15Q3, caused by recovering the stored energy through power diode A2A6A15CR2. Current limiting is provided for the booster output A2A6A15U2-2 by connecting the regulated output from A2A6A15U2-8 through resistor A2A6A15R8 to the current limiting input A2A6A15U2-1. These current limiting circuits protect the power supply against damage due to a short circuited output. The current limiters also keep the regulator operation in the switching mode to prevent excessive dissipation in switch A2A6A15Q3.

3-237. Code Generator Assembly A2A7 (Figure 5-41). The schematic diagram for

Code Generator Assembly A2A7 shows the printed wiring boards and the shorting bar switch segments of the assembly. The shorting-bar switch segments are mechanically positioned by the front panel 1 MHz and 10 MHz controls. Figure 5-41 can be used to make a graph of the switch segments in the positions corresponding to the setting of the front panel MHz controls. The ground-connecting paths can then be traced through the assembly.

3-238. POWER SUPPLY ASSEMBLY A2A8 (Figure 5-28, Sheet 3). The circuits of Power Supply Assembly A2A8 are shown in detail in sheet 3 of Figure 5-28 as part of the Transmitter Main Frame A2. These circuits are described in paragraphs 3-134 and 3-135.

3-239. RATT TONE GENERATOR ASSEMBLY A2A9 (Figure 5-42). The RATT Tone Generator Assembly A2A9 receives teletypewriter loop current inputs and generates audio tone outputs to represent the teletypewriter mark and space signals. The audio tones are displaced by ±425 or ±85 Hz from a 2000 Hz reference. Displacement is determined by the setting of the front panel RATT SHIFT SELECT switch.

3-240. The RATT tone generator consists of four parts. These are: Optoelectronic coupler A2A9A1U1 and its associated components; 1 MHz level shifter A2A9A1Q1 and A2A9A1Q2; programmable frequency dividers A2A9A1U2 through A2A9A1U4; and output divider and driver A2A9A1U5A, A2A9A1Q3, A2A9A1Q4 and A2A9A1T1. The optoelectronic coupler A2A9A1U1 and associated circuitry isolates the teletypewriter current from the T-827H/URT circuitry. The 1 MHz level shifting circuitry consisting of A2A9A1Q1 and A2A9A1Q2 receives the low level 1 MHz signal from the frequency standard and amplifies it to a level suitable for the programmable divider. Programmable divider A2A9A1U2 - A2A9A1U4 divides the 1 MHz signal in response to the mark/space input and the RATT SHIFT SELECT switch A2S10. The output divider circuitry divides the programmable divider output by two and makes a symmetrical square-wave; A2A9A1Q3 and A2A9A1Q4 standardize the square-wave amplitude; and A2A9A1T1 provides a balanced output for Audio Processor A2A21A18.

3-241. Optoelectronic coupler A2A9A1U1 consists of a light emitting diode (LED) and a photo sensitive transistor. A mark signal input (5 to 75 mA at A2A9A1P1 pin 4) passes through polarity protection diode A2A9A1CR1 to the LED in A2A9A1U1, and then through A2A9A1R6 to A2A9A1P1 pin 3. A2A9A1CR3 shunts any current in excess of 20 mA to protect the LED. When the LED is turned on by the mark current, the associated transistor A2A9A1U1 also turns on. The transistor current raises the voltage across A2A9A1R13 which creates a logic high at the output of AND gate A2A9A1U6A-3. Thus, A2A9A1U6-3 will be a logic high for a mark input and a logic low, signified by no input current, for a space condition.

3-242. 1 MHz from Frequency Standard A2A5 is applied to the RATT Tone Assembly through A2A9A1P1-7. Common emitter transistor A2A9A1Q1 amplifies the low level input. A2A9A1R7 and A2A9A1R8 provide bias voltage, while A2A9A1R9, A2A9A1R11 and A2A9A1C3 provide gain stabilization and emitter by-passing. The output at the collector of A2A9A1Q1 is applied to common emitter amplifier A2A9A1Q2 through coupling network A2A9A1C4 and A2A9A1R16. The collector signal at A2A9A1Q2 approximates a 1 MHz squarewave for programmable divider A2A9A1U2.

3-243. Programmable dividers A2A9A1U2 through A2A9A1U4 are decade down counters which are preset each time all three arrive at the zero count state. Pins 5, 11, 14 and 2 of A2A9A1U2 through A2A9A1U4 are the programming pins, and are set by AND gates A2A9A1U6A, A2A9A1U6D and flip-flop A2A9A1U5B connected as an inverter. When the RATT SHIFT SELECT switch A2S10 is in the 850 position, and for a mark input, the programming inputs to A2A9A1U2 are logic highs at pins 5, 11 and 14, and a permanent logic low is at pin 2. Therefore, A2A9A1U2 is preset to 7. In a similar manner A2A9A1U3 and A2A9A1U4 are preset to 1 and 3 respectively. This condition divides the input 1 MHz by 317 or approximately 3155 Hz. This output will be further divided by two in A2A9A1U5A for the required mark frequency. For a space condition A2A9A1U2 through A2A9A1U4 are preset to six, zero and two so as to divide the 1 MHz by 206 for

an output of approximately 4854 Hz. When the RATT SHIFT SELECT switch is in the 170 Hz position, the counters are set to divide by 261 for a mark condition and by 240 for a space condition. These divisions yield approximately 3831 and 4166 respectively.

3-244. A2A9A1U5A divides the unsymmetrical output from programmable dividers A2A9A1U2 through A2A9A1U4 by two, and provides a symmetrical squarewave for push-pull amplifier A2A9A1Q3 and A2A9A1Q4. A2A9A1Q3 and A2A9A1Q4 standardize the squarewave amplitude. An attenuator, consisting of resistors A2A9A1R21 through A2-A9A1R24, reduces the amplitude to a level which will give the required 0.8 volts p-p balanced output at A2A9A1T1 pins 4 and 7. This balanced output is sent to A2A9A1P1 pins 2 and 8. The balanced output prevents shorting of the RATT assembly output when the center tap of A2A21T2 is grounded.

3-245. METER AMPLIFIER ASSEMBLIES A2A10 and A2A11 (Figure 5-28, Sheet 1). Meter Amplifier Assemblies A2A10 and A2-A11 are mounted on the T-827H/URT front panel and described together with the Transmitter Main Frame A2. (Refer to paragraph 3-136.)

3-246. IF AMPLIFIER ASSEMBLY A2A12 (Figure 5-43). IF Amplifier Assembly A2A12 provides three gain-controlled stages for DATA, SSB, RATT and AM modes of operation, and two gain-controlled stages for CW operation. Gain is controlled by the average power control (APC or TGC) input at A2-A12P1-6 and the peak power control (PPC) input at A2A12P1-7. The APC (or TGC) and PPC inputs are dc voltages applied by the AM-3924C(P)/URT. APC applies to NORMAL operation and TGC applies to DATA operation. Both power-control feedback signals are supplied over the same line, but originate from different circuits in the AM-3924C(P)/URT. PPC will function in either DATA or NORMAL operation. The APC and PPC inputs control the gain of amplifiers A2A12A1Q2 and A2A12A1Q5. This is accomplished by varying bias in response to the output of A2A12A1Q1 and A2A12A1Q3. The PPC input exerts control via amplifier A2-A12A1Q2, at a point prior to carrier reinsertion. Thus, the PPC input gain control voltage only affects the sideband levels. PPC voltage does not change the amplitude of the carrier reinsertion signal used during AM and SSB pilot carrier modes from A2A12P1-A2. The APC input exerts control over both the carrier and sideband signals at amplifier A2-A12A1Q5. The time constant of the APC circuitry within the external associated rf power amplifier AM-3924C(P)/URT prevents the APC level from varying with modulation peaks. The gain of the IF is set by A2A12-A1R27 and the slope of gain reduction with APC is set by A2A12A1R39. A2A12A1RT1 temperature compensates the IF.

3-247. During the USB and LSB modes, the 500 kHz signal from A2A12P1-A3 is applied to amplifier A2A12A1Q4 after amplification by A2A12A1Q2. During the CW, AM and SSB pilot carrier modes, the 500 kHz signal from A2A12P1-A2 is applied directly to amplifier A2A12A1Q4. The signal is amplified in A2-A12A1Q4 and A2A12A1Q5 and passed through transformer A2A12A1T2 to connector A2A12P1-A1.

3-248. HANDSET FILTER ASSEMBLY A2-A14 (Figure 5-28, Sheets 1 and 3). Handset Filter Assembly A2A14 consists of conventional L-C and capacitive filtering circuits which are part of the Transmitter Main Frame A2. The description of its circuits is included with that of the main frame (refer to paragraph 3-139).

3-249. IF FILTER ASSEMBLY A2A15 (Figure 5-28, Sheet 1). IF Filter Assembly A2A15 consists of filter circuits which are mounted on the main frame. The circuit description is included with the main frame (refer to paragraph 3-140).