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TI 6620.2A

INSTRUCTION BOOK

RECEIVER, RADIO AN/GRR-23 and AN/GRR-24

VOLUME 2

EQUIPMENT CONTRACTOR
INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
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RECORD OF CHANGES

DIRECTIVE NO. 6620 AN/GRR-23

CHANGE TO BASIC	SUPPLEMENTS			OPTIONAL USE	CHANGE TO BASIC	SUPPLEMENTS			OPTIONAL USE
		Chg	Chap						

FAA Form 1320-5 (5-68) SUPERSEDES PREVIOUS EDITION

VOLUME 2

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LIST OF ILLUSTRATIONS (con.)

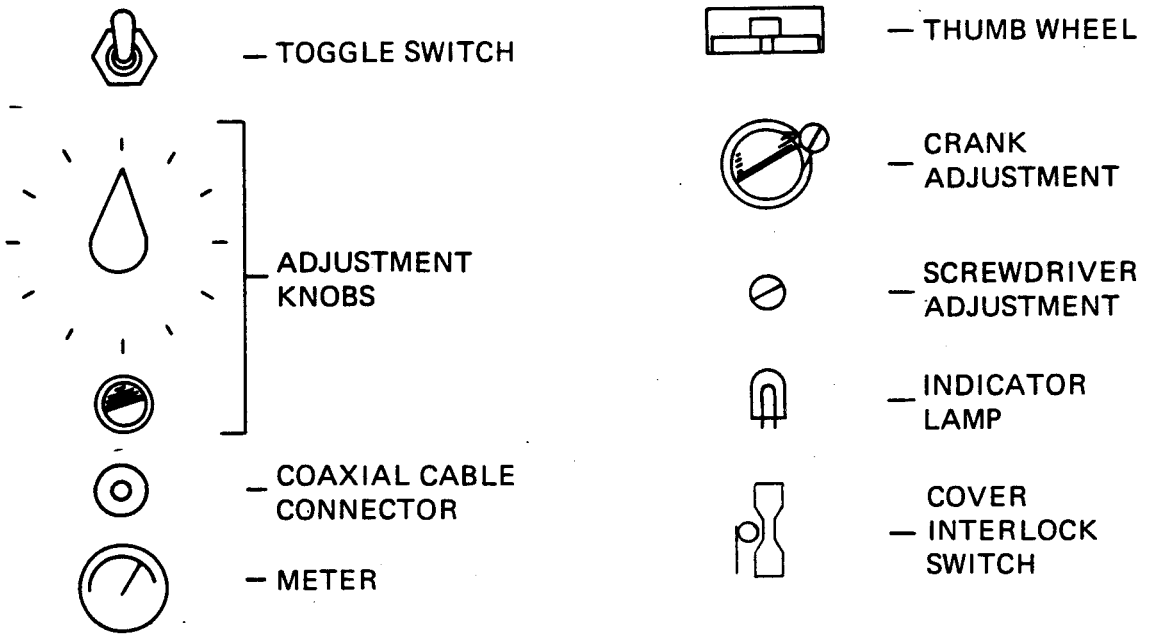
LIST OF TABLES

FUNCTIONAL INDEX

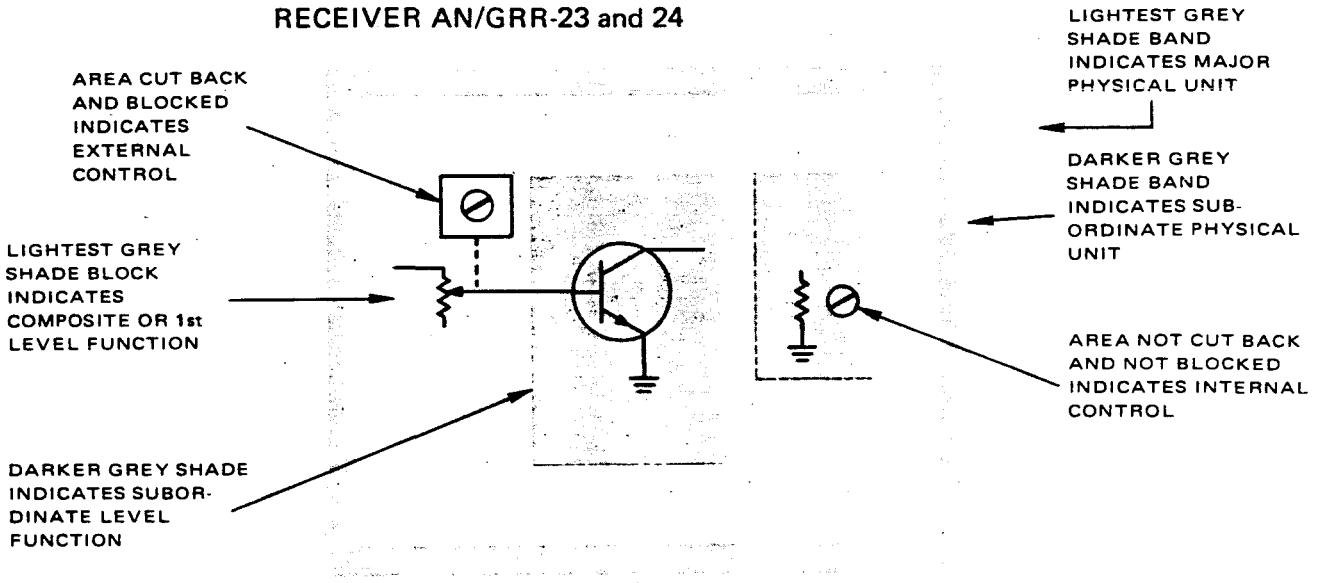
CIRCUIT IDENTIFIER CODES

CATEGORY	DEFINITION
C	Composite circuit (one which is sub-functionalized); composite functional entities containing one or more of the functional entities (N, Q, V, or X) given in this list are preceded by C.
L	Used in logic diagrams only to identify lowest level of functional grouping of logic circuits.
M	Microwave components (duplexers, attenuators, etc.).
N	Linear networks; functional entities containing several linear components (resistors, capacitors, etc.) arranged in a network or containing a single element used as network are preceded by N.
Q	Circuits containing one or more non-linear elements which may be either active or passive; functional entities containing transistors are preceded by Q.
V	Circuits containing one or more non-linear elements which may be either active or passive; functional entities containing vacuum tubes are preceded by V.
X	Circuits containing one or more non-linear elements which may be either active or passive; functional entities containing semiconductor diodes are preceded by X.

CODE	DEFINITION
AGC	Automatic gain control
ALC	Audio level control
AMP	Amplifier
ANC	Antenna coupler
AT	Attenuator
AUA	Audio amplifier
AUO	Audio oscillator
BCG	Battery charging
BUF	Buffer
CA	Control amplifier
CGT	Compression gate
CMP	Compression
CMR	Comparator
CTR	Counter
CPR	Clipper
DET	Detector
DFA	Differential amplifier
DG	Diode gate
DL	Delay line
EF	Emitter follower
FDR	Frequency doubler
FDV	Frequency divider
FL	Filter
FQD	Frequency quadrupler
GAT	Gating
HTR	Heater
LA	Lamp (indicating)
LIM	Limiter, limiting
LO	Local oscillator
LS	Level shifter
LVC	Level control circuit
MIC	Microphone
MIX	Mixer
MMV	Monostable multivibrator
MOD	Modulator
MON	Monitor
MTC	Matches
MTG	Matching
OSC	Oscillator
PS	Power supply
RCT	Rectifier
REG	Regulator
RFA	Radio frequency amplifier
RLY	Relay
SW	Switch
TB	Terminal board
TFR	Transformer
TR	Transmit-receive
VD	Voltage divider
VDR	Voltage doubler
VR	Voltage regulator



EXPLANATION OF SPECIAL SYMBOLS



EXPLANATION OF SHADED AREAS

SECTION 11

DIAGRAMS

11.1 INTRODUCTION.- This section contains the schematic diagrams for the vhf and uhf receivers and their subassemblies. The schematics of the individual integrated circuits used in the receiver are also included. Shaded blocked diagrams and texts and blocked schematic diagrams and texts complete this section. The interconnecting wiring between subassemblies and between subassemblies and external connections is listed in table 11-1.

11.2 USE OF SUBASSEMBLY SCHEMATIC DIAGRAMS.- The subassembly schematics in this section are intended chiefly as maintenance tools together with the assembly drawings and photographs in section 10. Test points (TP) and measurement points (MP) are accentuated and the d.c. voltages at these points are listed on each schematic.

11.3 SHADED BLOCKED DIAGRAMS AND TEXTS.- Figures 11-30 through 11-33 present a second-level functional description of the vhf and uhf receivers in blocked diagrams and companion blocked texts. Figures 11-34 and 11-35 present a functional block diagram and companion text for the optional oscillator-synthesizer module that may be used in either receiver unit.

11.4 SHADED BLOCKED SCHEMATIC DIAGRAMS AND TEXTS.- Figures 11-36 through 11-39 present the shaded functionally oriented blocked schematic diagrams and companion text discussions of the uhf and vhf receivers, respectively. It should be noted in these schematics that the mixer/multiplier (A2) is shown only in the G2 configuration, which is only slightly different from the G1 configuration. Figures 11-40 and 11-41 present the shaded functionally oriented blocked schematic diagram and companion text of the oscillator-multiplier and the optional oscillator-synthesizer module that may be used in either receiver unit.

Table 11-1. Receiver Wire List

Wire number	From terminal			To terminal			Type	Gauge	Color	Approx. length (inches)	Notes	Remarks
	Connector	Pin	Conn lug	Connector	Pin	Conn lug						
1	J15	16	2	E4		4	E	22	0	9		
2	J15	14	2	J3	2	DF	E	22	7	11½		
3	J15	13	2	J3	3	DF	E	22	2	11¾		
4	J15	12	2	J4	13	DF	E	22	4	13½		
5	J15	11	2	J4	8	DF	E	22	9	13¾		
6	J15	10	2	J9	8	DF	Y	22	5	15½	1	
7	J15	9	2	J6	5	DF	E	22	6	15½		
8	J15	8	2	J7	7	DF	E	22	95	13		
9	J15	6	2	J6	6	DF	E	22	1	16¼		
10	J15	4	2	J7	11	DF	E	22	96	13¾		
11	J15	3	2	J8	5	DF	E	22	93	16		
12	J15	2	2	J4	7	DF	E	22	90	16		
13	J15	1	2	J5	8	DF	E	22	8	18½		
14	J14	T	4	J5	13	DF	E	22	96	16½		
15	J14	R	4	J5	12	DF	E	22	95	16½		
16	S1	1	4	J4	15	DF	E	22	91	5		
17	S1	2	4	R1	1	2	E	22	9	4		
18	S1	3	4	J4	9	DF	E	22	3	15		
19	R1	2	4	J4	10	DF	E	22	7	14½		
20	R1	3	2	J4	11	DF	E	22	8	14½		
21	R3	1	2	R2	1	2	E	22	1	4		
22	R3	1	2	J4	5	DF	E	22	1	15		
23	R3	3	2	R2	3	2	E	20	0	4		
24	R3	3	2	E4		4	E	20	0	10¾		
25	R3	2	2	J5	7	DF	E	22	7	17		
26	R2	2	2	J5	5	DF	E	22	90	16¾		
27	J3	1	DF	E3		4	E	20	0	4¼		
28	J3	4	DF	J6	3	DF	E	22	2	9		
29	J3	6	DF	J7	3	DF	E	22	2	6½		
30	J3	8	DF	J8	3	DF	E	20	2	8½		
31	J3	9	DF	J9	3	DF	E	20	2	9		

Table 11-1. Receiver Wire List (con.)

Wire number	From terminal: Connector	Pin	Conn lug	To terminal: Connector	Pin	Conn lug	Type	Gauge	Color	Approx. length (inches)	Notes	Remarks
32	J3	10	DF	J4	3	DF	E	20	2	8½		
33	J3	11	DF	J5	3	DF	E	20	2	10		
34	J3	12	DF	J6	2	DF	E	22	7	8¾		
35	J4	1	DF	E3		4	E	20	0	4		
37	J4	6	DF	J5	15	DF	E	22	6	8¾		
38	J4	14	DF	E6		2	E	22	5	6		
39	J5	1	DF	E2		4	E	20	0	4¼		
40	J5	9	DF	C2	1	2S	E	22	4	11¼	2	
41	J5	11	DF	C3	1	2S	E	22	3	11¼	2	
42	J5	10	DF	C4	1	2S	E	22	9	11¼	2	
43	J7	1	DF	E7		4	E	20	0	7½		
44	J7	5	DF	E6		2	E	22	5	4		
45	J6	1	DF	E7		4	E	20	0	3		
46	J8	1	DF	E7		4	E	20	0	7½		
47	J9	9	DF	E6		2	E	22	5	10		
48	J9	1	DF	E5		4	E	20	0	5		
49	J9	5	DF	C5		2S	Y	22	6	10	3&2	
50	J9	7	DF	J4	12	DF	E	22	95	7¾		
53	C1	1	2S	E6		2	E	22	5	14	2	
54	C8	1	2S	XF3	1	4	E	22	6	23¾	2	
55	XF3	2	4	S2	3	4	E	22	7	9½		
56	S2	7	4	J3	7	DF	E	22	6	18		
60	J3	5	DF	J6	4	DF	E	22	92	7		
61	C6	1	2S	XF1	1	4	R	20	8	22½		
62	C7	1	2S	SF2	1	4	R	20	98			
63	XF1	2	4	S2	1	4	R	20	1	11		
64	XF2	2	4	S2	2	4	R	20	91			
* 65	Withdrawn by AF P 6500.1 CHG Chap											
66	Withdrawn by AF P 6500.1 CHG Chap											
67	S2	5	4	J3	14	DF	R	20	8	8½		
68	S2	6	4	J3	15	DF	R	20	98			

Table 11-1. Receiver Wire List (con.)

Wire number	From terminal: Connector	Pin	Conn lug	To terminal: Connector	Pin	Conn lug	Type	Gauge	Color	Approx. length (inches)	Notes	Remarks
* 69	E4		2	XDS1	1	2	E	22	0	12 1/2		
70	J15	13	2	XDS1	2	2	E	22	2	14 1/2		*

NOTES - CODE IDENTIFICATION

"Wire number" column: Numbers 36, 51, 52, 57, 58, and 59 deleted.

"Conn lug" columns:
- DF denotes 502056-402 contact, female
- S denotes sleeving, insulation
- 2 denotes 1/4" strip length
- 4 denotes 1/2" strip length

"Type" column:
- E denotes 4590 wire
- Y denotes 4596 wire, shielded and jacketed
- R denotes 517875 wire, twisted pair

"Color" column:
- 0 Black
- 1 Brown
- 2 Red
- 3 Orange
- 4 Yellow
- 5 Green
- 6 Blue
- 7 Violet
- 8 Gray
- 9 White

"Notes" column:
1. Solder shields of wire gates
2. Denotes sleeving, insulation
3. Solder shield of wire 49 at E1 and E5

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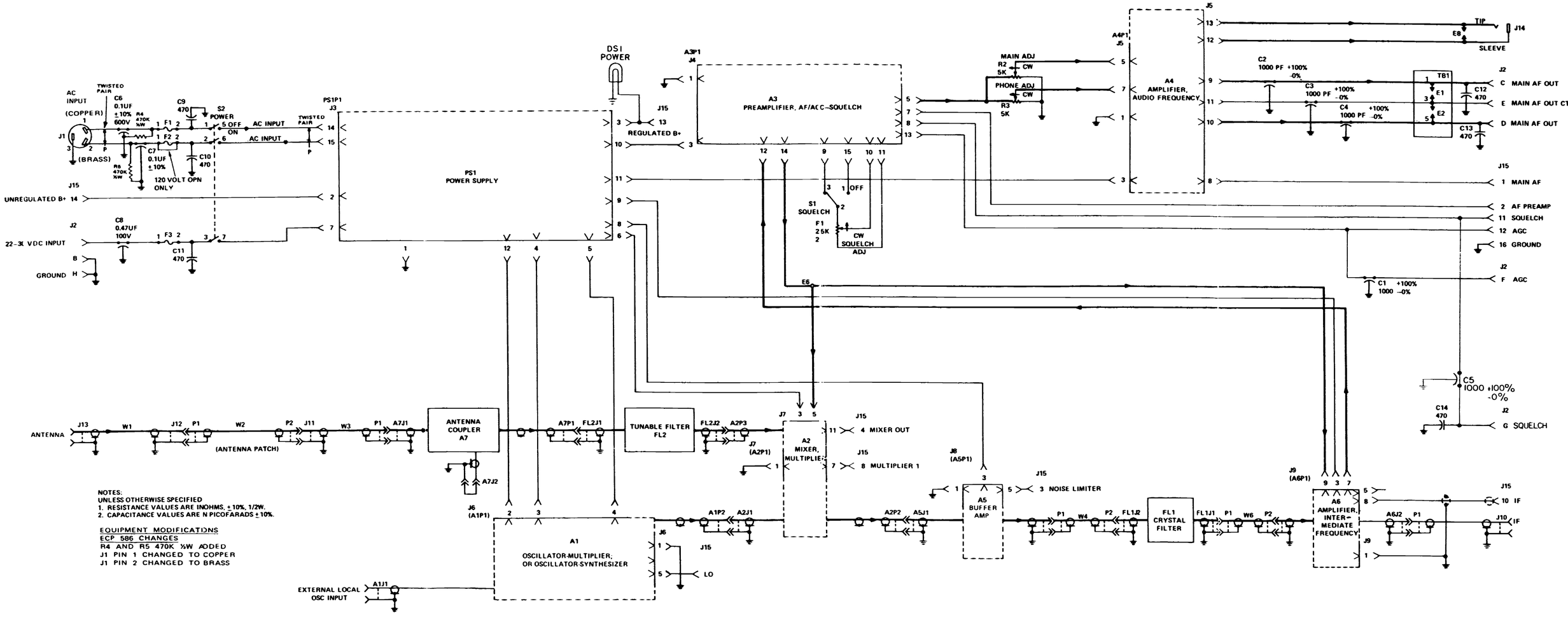
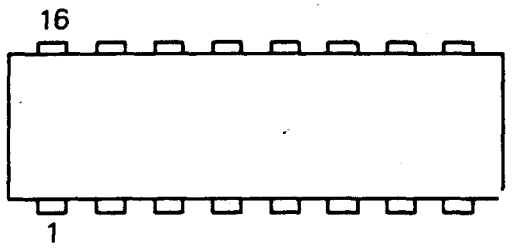


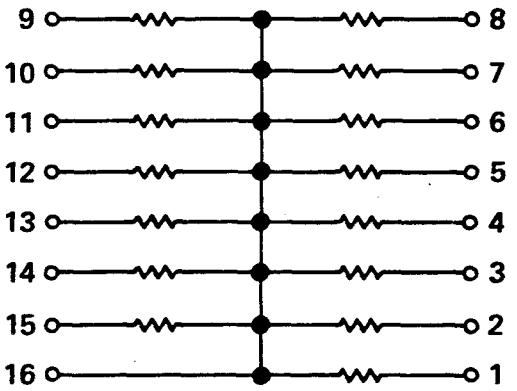
NOTES:
UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS, ±10%, 1/2W.
2. CAPACITANCE VALUES ARE N PICOFARADS ±10%.

EQUIPMENT MODIFICATIONS
ECP 586 CHANGES
R4 AND R5 470K ½W ADDED
J1 PIN 1 CHANGED TO COPPER
J1 PIN 2 CHANGED TO BRASS

Figure 11-1. VHF/UHF Receiver Schematic

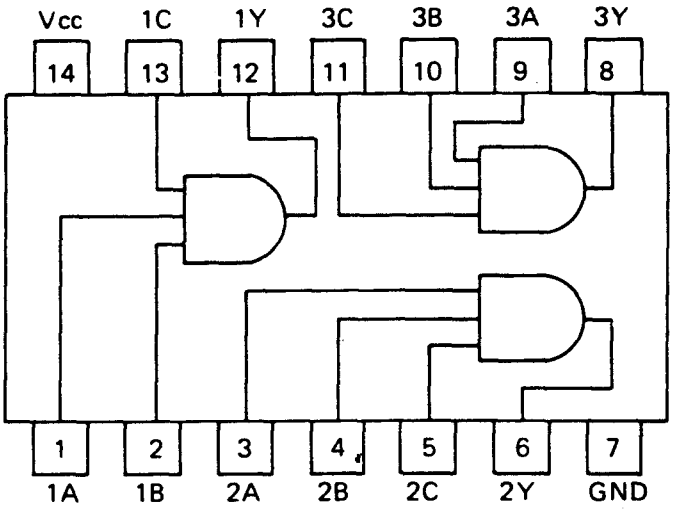


PIN ASSIGNMENT (TOP VIEW)



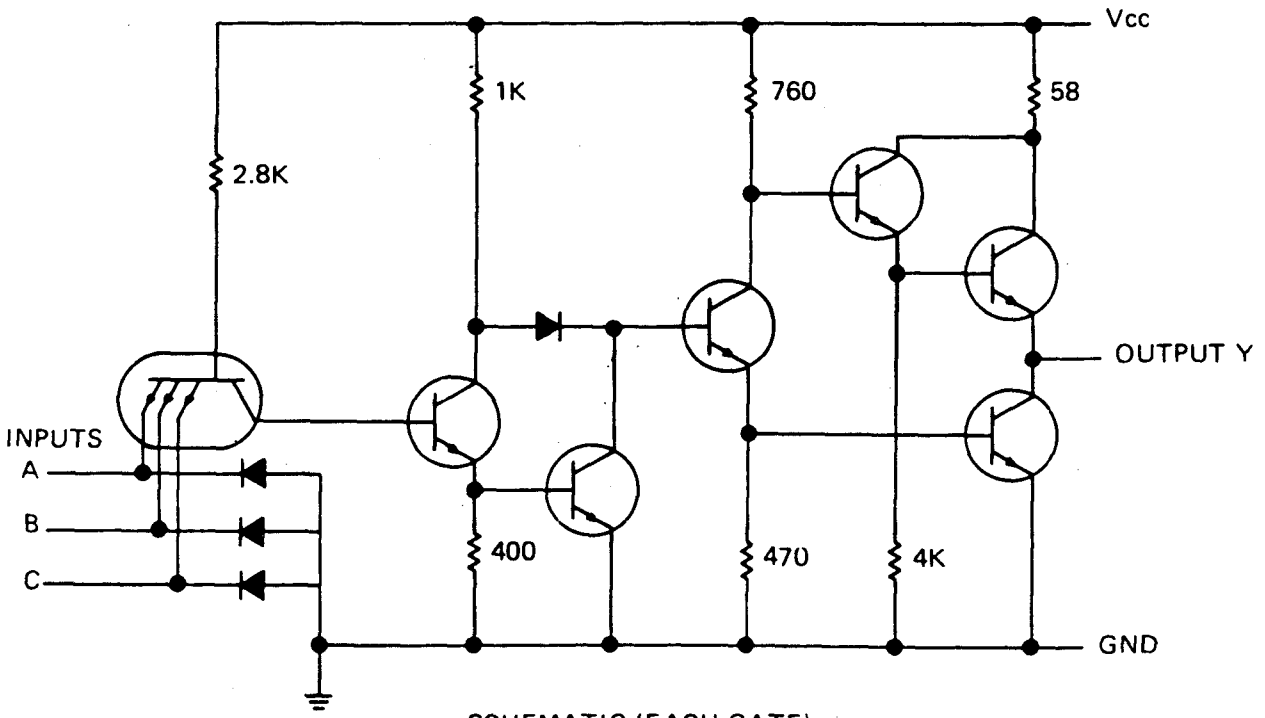
SCHEMATIC

Figure 11-2. Fixed Resistor Network Integrated Circuit (509435-1)



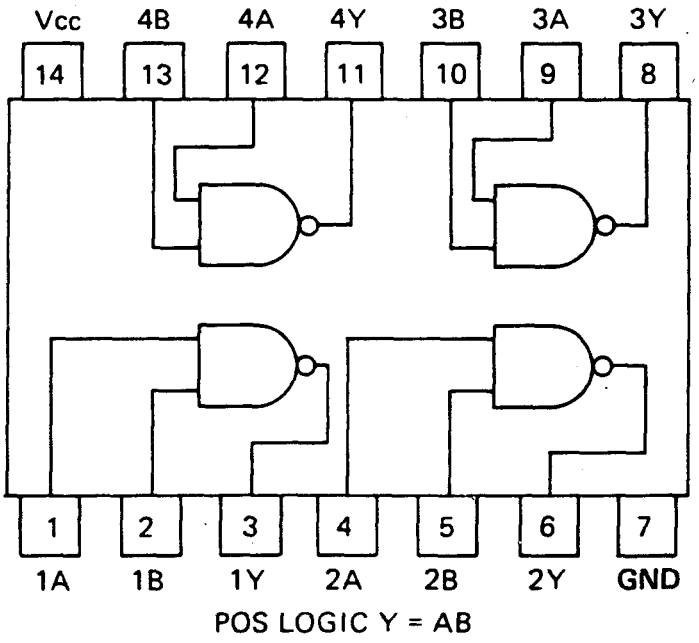
POSITIVE LOGIC: Y = ABC

PIN ASSIGNMENT (TOP VIEW)



SCHEMATIC (EACH GATE)

Figure 11-3. Triple Three-Input Positive AND Gate Integrated Circuit (SN54H11J-00)



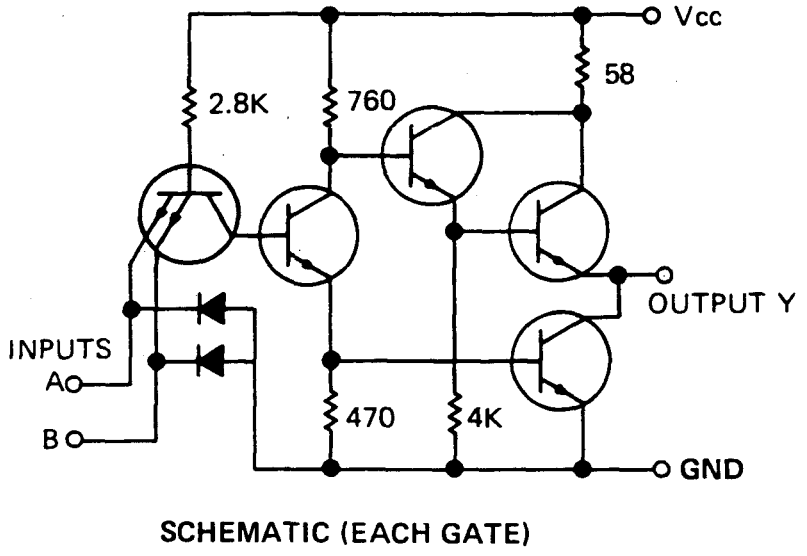
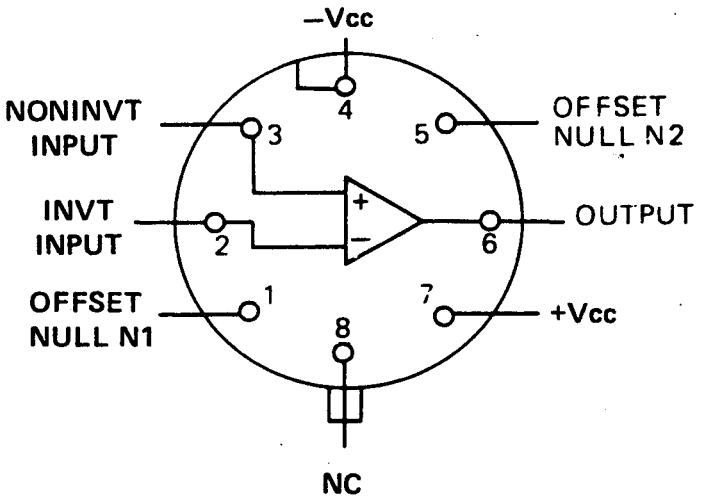
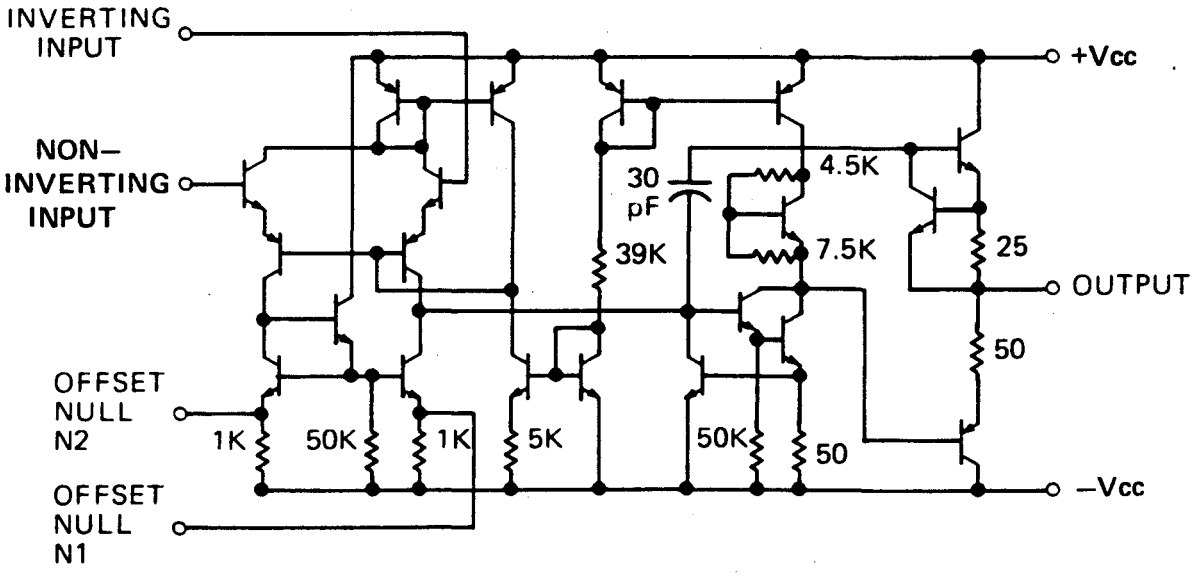


Figure 11-4. Quadruple Two-Input Positive NAND Gate Integrated Circuit (SN5400J-00)



BOTTOM VIEW SHOWN
CASE CONNECTED TO –Vcc
POWER SUPPLY AT PIN 4



SCHEMATIC

Figure 11-5. Operational Amplifier Integrated Circuit (SN52741L-00)

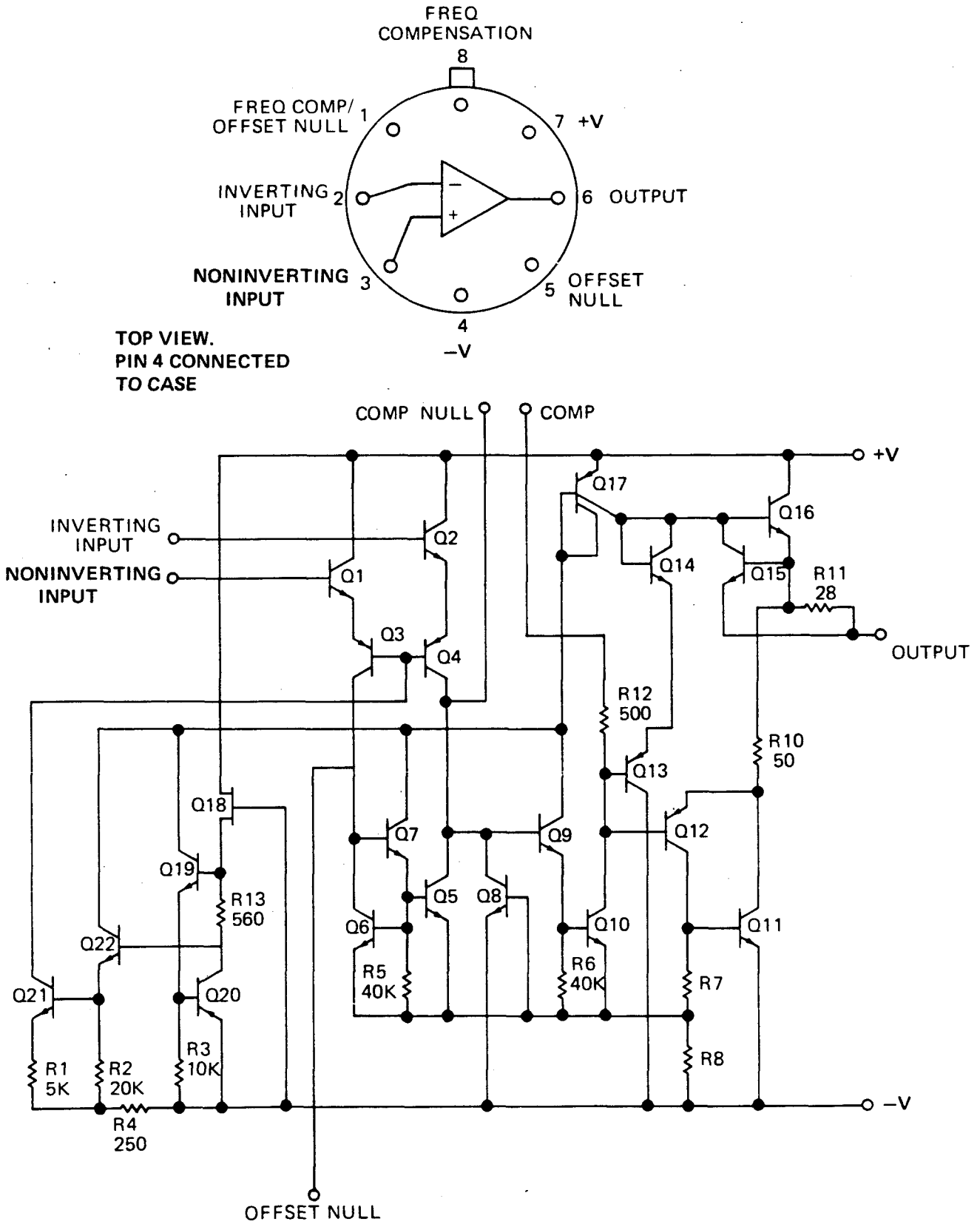
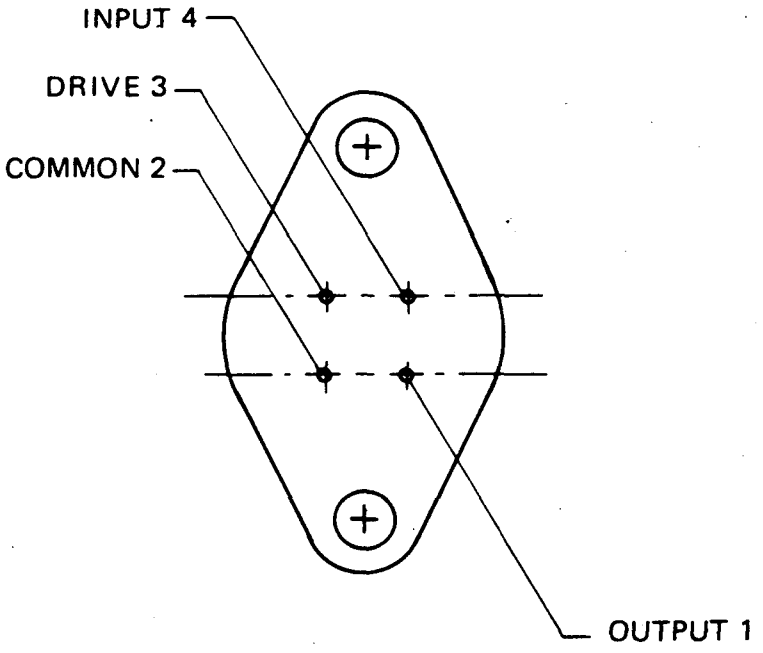
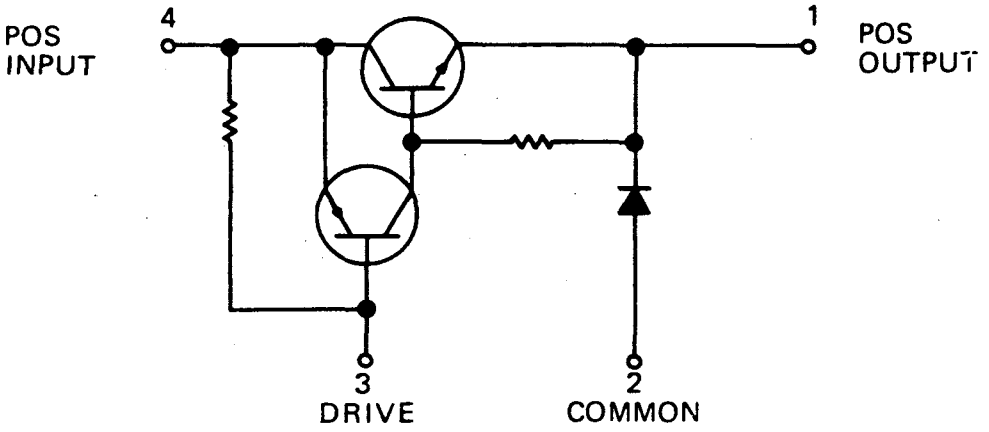


Figure 11-6. Operational Amplifier Integrated Circuit (LM101AH)

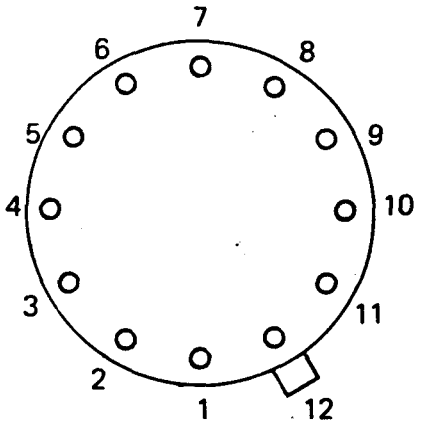


TERMINAL ARRANGEMENT (BOTTOM VIEW)

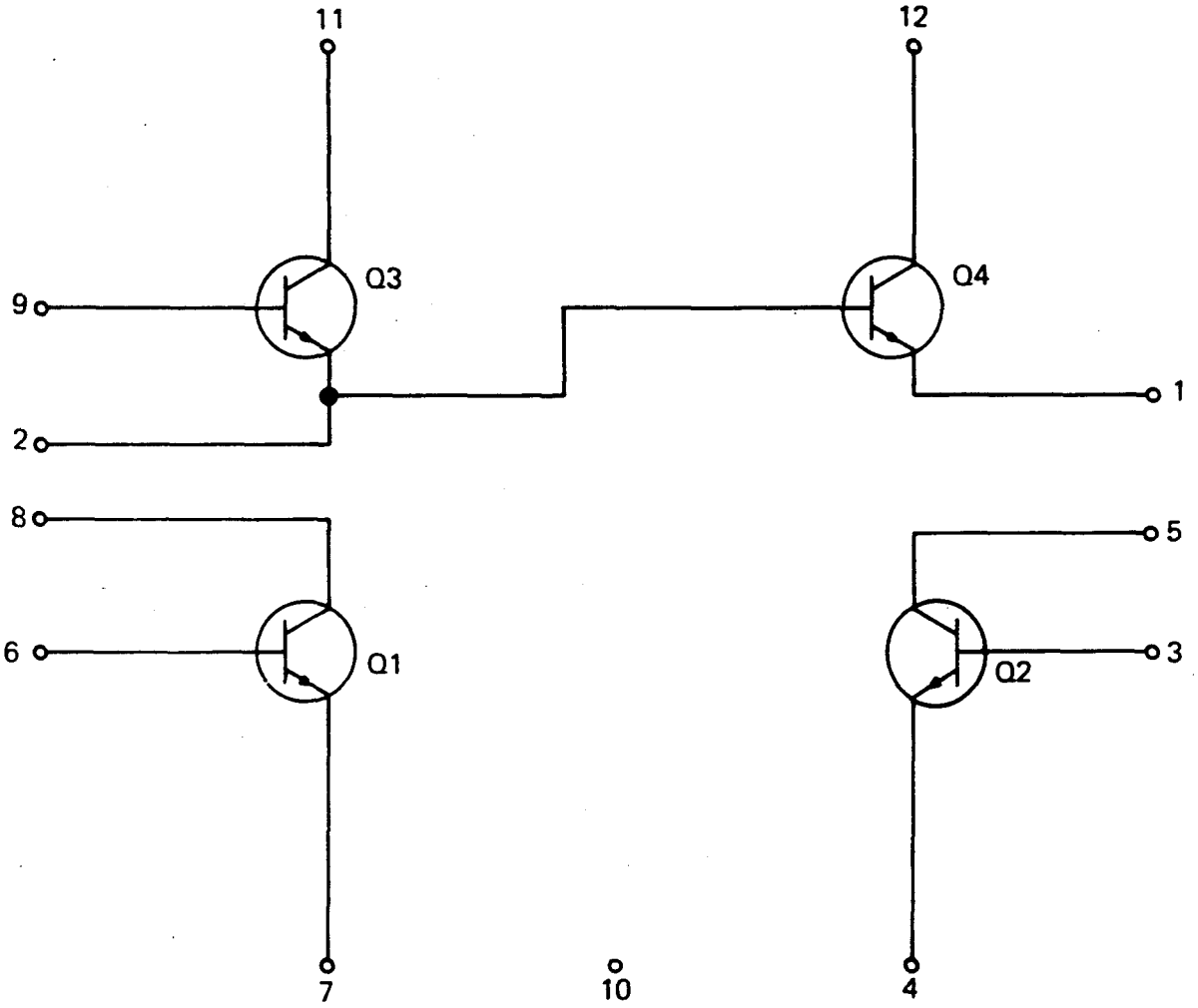


SCHEMATIC

Figure 11-7. Switching Regulator Integrated Circuit (PIC600)



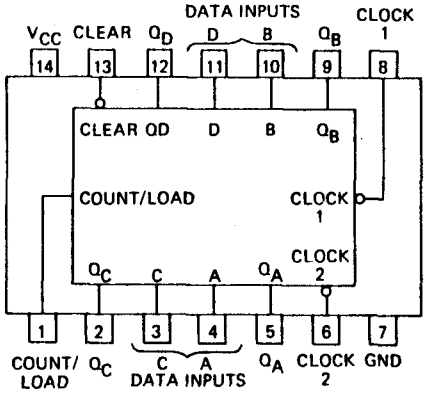
TERMINAL ARRANGEMENT (BOTTOM VIEW)



SCHEMATIC

Figure 11-8. Transistor Array Integrated Circuit (CA3118T)

TERMINAL CONFIGURATION (TOP VIEW)



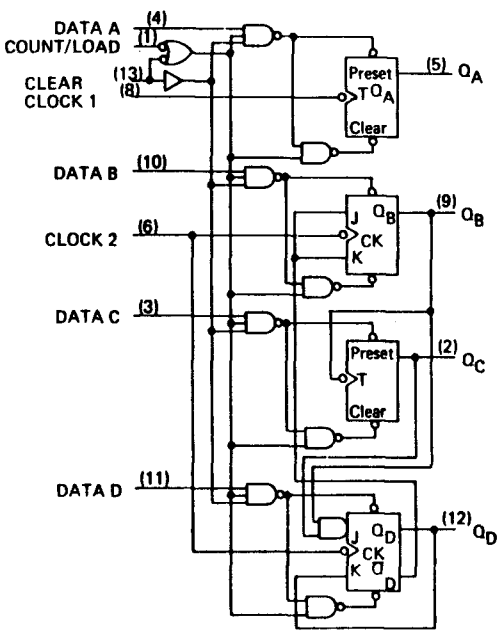
DECADE (BCD)
(SEE NOTE A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(SEE NOTE B)

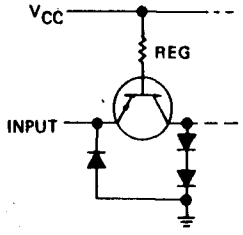
COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = HIGH LEVEL
L = LOW LEVEL
NOTES:
A. OUTPUT Q_A CONNECTED TO CLOCK-2 INPUT.
B. OUTPUT Q_D CONNECTED TO CLOCK-1 INPUT.



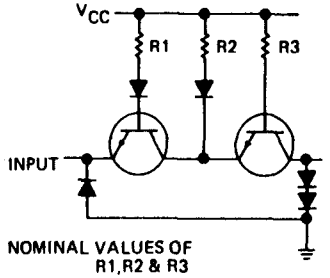
FUNCTIONAL BLOCK DIAGRAM

EQUIVALENT OF COUNT/ LOAD, CLEAR & DATA INPUTS



COUNT/LOAD
DATA: REG = 4K NOM
CLEAR: REG = 2K NOM

EQUIVALENT OF CLOCK INPUTS



NOMINAL VALUES OF R1,R2 & R3

INPUT
CLOCK 1 4K
CLOCK 2 3K

TYPICAL OF ALL OUTPUTS

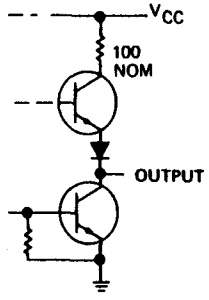


Figure 11-9. High-Speed Counter Integrated Circuit (SN54196J-00)

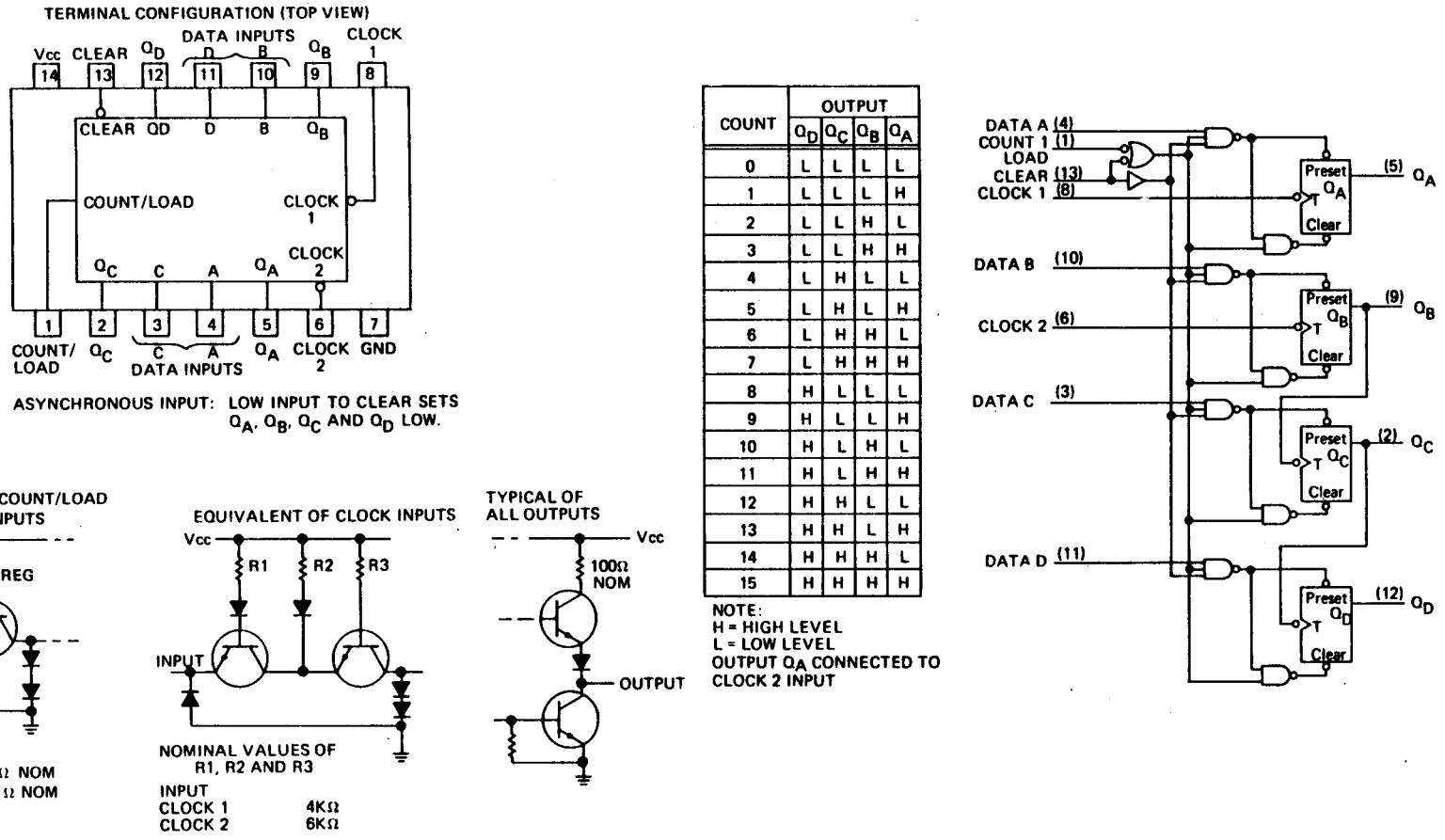
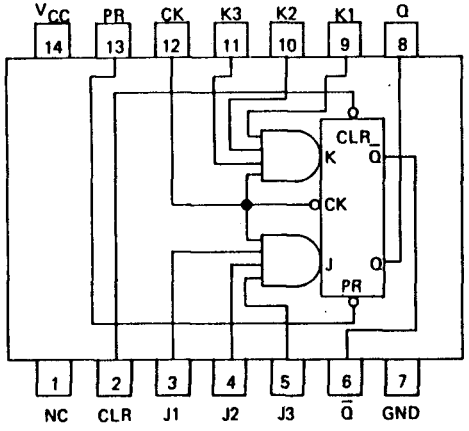
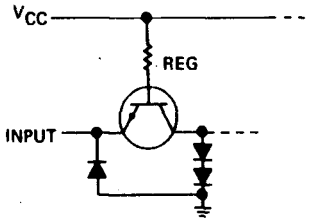


Figure 11-10. High-Speed Counter Integrated Circuit (SN54197J-00)

TERMINAL CONFIGURATION
(TOP VIEW)

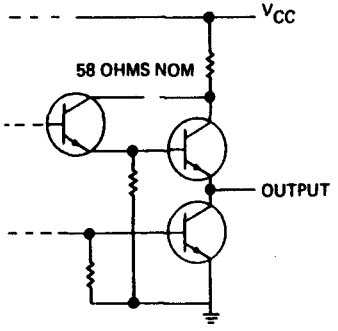


EQUIVALENT OF
EACH INPUT

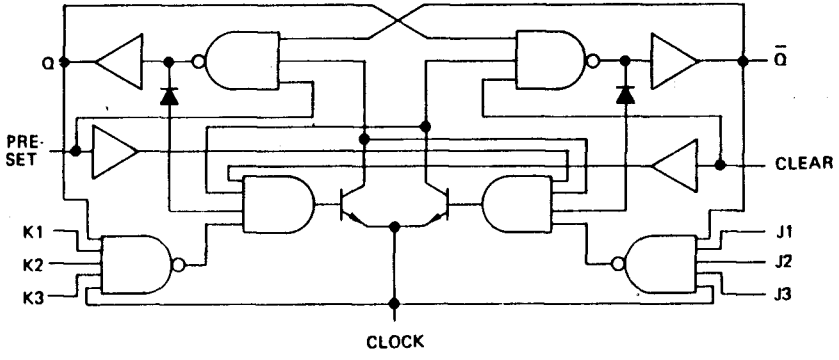


I_{IL} MAX	REG NOM
-2 MA	4K
-4.8 MA	1.3K
-9.6 MA	650

TYPICAL OF
ALL OUTPUTS



SCHEMATICS OF
INPUTS & OUTPUTS



FUNCTIONAL BLOCK DIAGRAM

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	**	L	L	Q_O	$\overline{Q}_O$
H	H	**	H	L	H	L
H	H	**	L	H	L	H
H	H	**	H	H	TOGGLE	
H	H	H	X	X	Q_O	$\overline{Q}_O$

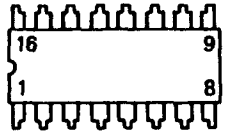
POSITIVE LOGIC: J = J1·J2·J3
K = K1·K2·K3

X = IRRELEVANT

FUNCTION TABLE

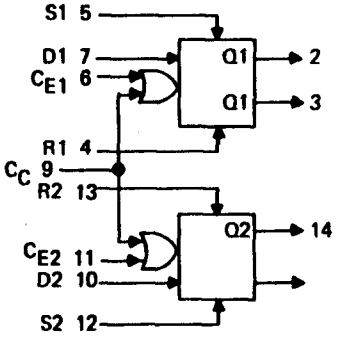
*THIS CONFIGURATION IS NONSTABLE; IT WILL NOT PERSIST WHEN PRESET & CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.
**TRANSITION FROM HIGH TO LOW LEVEL
"TOGGLE" = EACH OUTPUT CHANGES TO THE COMPLEMENT OF ITS PREVIOUS LEVEL ON EACH ACTIVE TRANSITION (PULSE) OF THE CLOCK.
"Q_O" = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

Figure 11-11. Edge-Triggered J-K Flip Flop Integrated Circuit (SN54H102J-00)

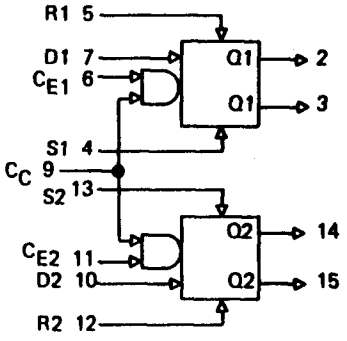


A CLOCK H IS A CLOCK TRANSITION FROM A LOW TO A HIGH STATE

POSITIVE LOGIC



NEGATIVE LOGIC



Vcc1 = PIN 1
Vcc2 = PIN 16
V_{EE} = PIN 8

RS TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = NOT DEFINED

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = DON'T CARE
$C = C_E + C_C$

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN

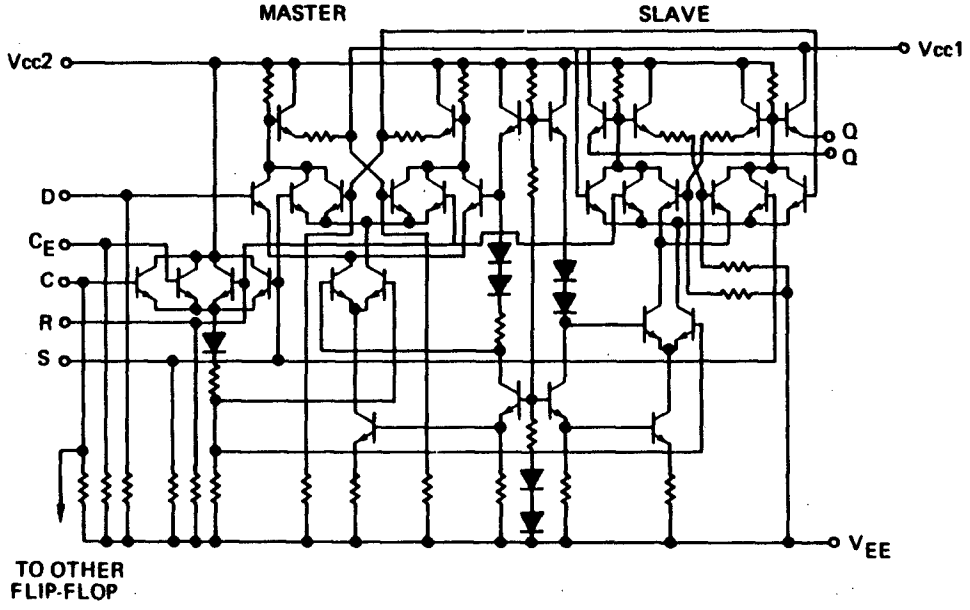
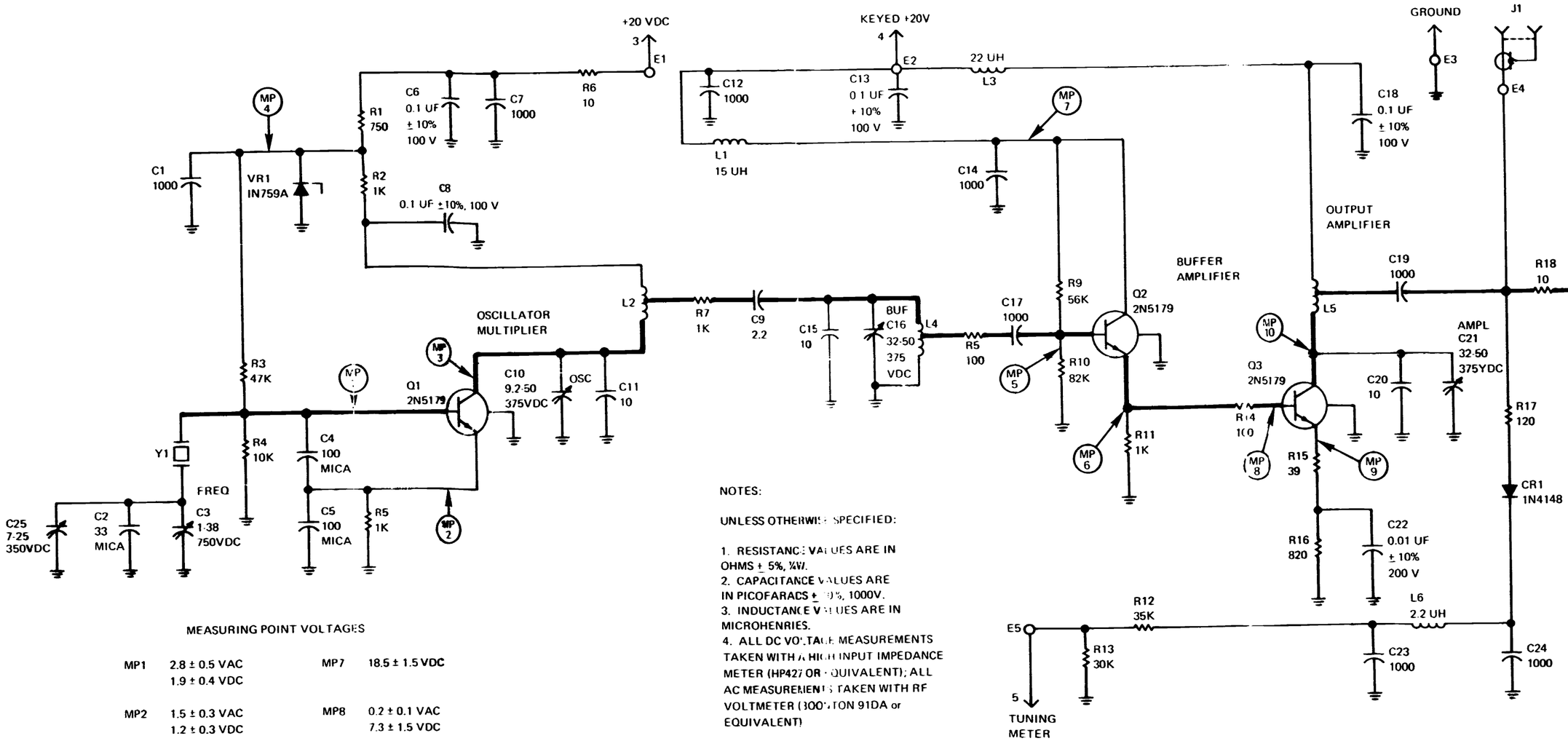


Figure 11-12. Dual Master-Slave (D-Type) Flip Flop Integrated Circuit (MC10531L)

Figure 11-13. Crystal Oscillator A1 G1 (This figure deleted)

Figure 11—14. Crystal Oscillator A1 G2 (This figure deleted)



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, ¼W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ± 10%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL DC VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT); ALL AC MEASUREMENTS TAKEN WITH RF VOLTMETER (BOONTON 91DA or EQUIVALENT)

EQUIPMENT MODIFICATIONS
ECP 571 CHANGE
C25 FROM 5.5-18 TO 7-25pF

MEASURING POINT VOLTAGES

MP1	2.8 ± 0.5 VAC 1.9 ± 0.4 VDC	MP7	18.5 ± 1.5 VDC
MP2	1.5 ± 0.3 VAC 1.2 ± 0.3 VDC	MP8	0.2 ± 0.1 VAC 7.3 ± 1.5 VDC
MP3	1.9 ± 0.4 VAC 9.0 ± 1.5 VDC	MP9	0.2 ± 0.1 VAC 6.6 ± 1.3 VDC
MP4	12 ± 1 VDC	MP10	4.6 ± 1 VAC 18.5 ± 1.5 VDC
MP5	0.3 ± 0.1 VAC 8 ± 1.6 VDC		
MP6	0.3 ± 0.1 VAC 7.3 ± 1.5 VDC		

NOTE: ALL BASE-EMITTER VOLTAGES MUST BE 0.7 ± 0.2 VDC

Figure 11-15. Oscillator-Multiplier A1(M)

OSCILLATOR-MULTIPLIER A1(M)

The oscillator-multiplier module is directly interchangeable with the oscillator-synthesizer module. The oscillator-multiplier module utilizes a fundamental crystal. Frequency accuracy is determined by "pulling" the crystal. Tuning to the exact frequency is accomplished by monitoring the frequency with a counter or frequency meter connected to J1.

The oscillator-multiplier module consists of a crystal-controlled oscillator and multiplier stage, a buffer amplifier stage, and an output amplifier stage. The oscillator-multiplier requires a fundamental mode crystal operating in the frequency range of 11.25 MHz to 99.975 MHz. The output frequency from the module is 5 times the crystal frequency.

Oscillator stage Q1 is a modified Colpitts circuit. Crystal Y1 operates in an antiresonant mode. Paralleled capacitor combination, C2, C3, and C25, in series with the crystal, controls the frequency. Capacitor C25 is internally adjusted at the factory so that the desired oscillator frequency falls at the C3 adjustment range midpoint. Capacitors C4 and C5 form the feedback divider characteristic of the Colpitts configuration. Transistor Q1 is biased into conduction by voltage divider R3 and R4. The Q1 emitter return is R5. The Q1 collector circuit is tuned to the oscillator fifth harmonic by the resonant circuit L2-C10, C11. Capacitor C10 is the front panel tuning element. The Q1 d.c. input is regulated at 12 volts by VR1. Oscillator power supply isolation is by R1, R6, C6, and C7. The tuned circuit RF ground is through C8. Collector circuit current limiting is provided by R2. Resistance R7 is impedance isolation between the oscillator-multiplier tuned circuit and buffer bandpass filter L4-C15, C16, tuned to the crystal fifth harmonic.

Buffer amplifier Q2 is an emitter follower that minimizes shunt loading on the L4-C15, C16 filter preceding it, and drives the output amplifier stage following it. Capacitor C16 is the front panel tuning element. Voltage divider R9, R10 provides base bias for Q2. Resistor R11 is the emitter load.

Stage Q3 is the output RF amplifier of the oscillator-multiplier module. The signal is applied to the Q3 base by direct coupling from the buffer amplifier via parasitic suppression resistor R14. Resistors R15 and R16 provide emitter bias. The collector circuit is tuned by L3-C20, C21 to the crystal fifth harmonic. Capacitor C21 is the front panel tuning element. The output passes through attenuator network R18, R19, which buffers the output to the driven stage, and stabilizes the output impedance to approximately 50 ohms.

The signal is branched from the output stage via R17 into diode detector CR1 for metering the signal level for tuning purposes. RF filtering is provided by network L6, C23, and C24. Resistors R12 and R13 determine the scale factor of the external indicating meter.

An external signal generator can be used if desired. To do so, crystal Y1 is removed, disabling the oscillator, and 1-2 V rms is applied to J1 from the external signal generator. The signal generator must be set to the desired output frequency, i.e., 5 times the crystal frequency. Front panel tuning capacitors C16 and C21 are then adjusted for maximum output on the meter.

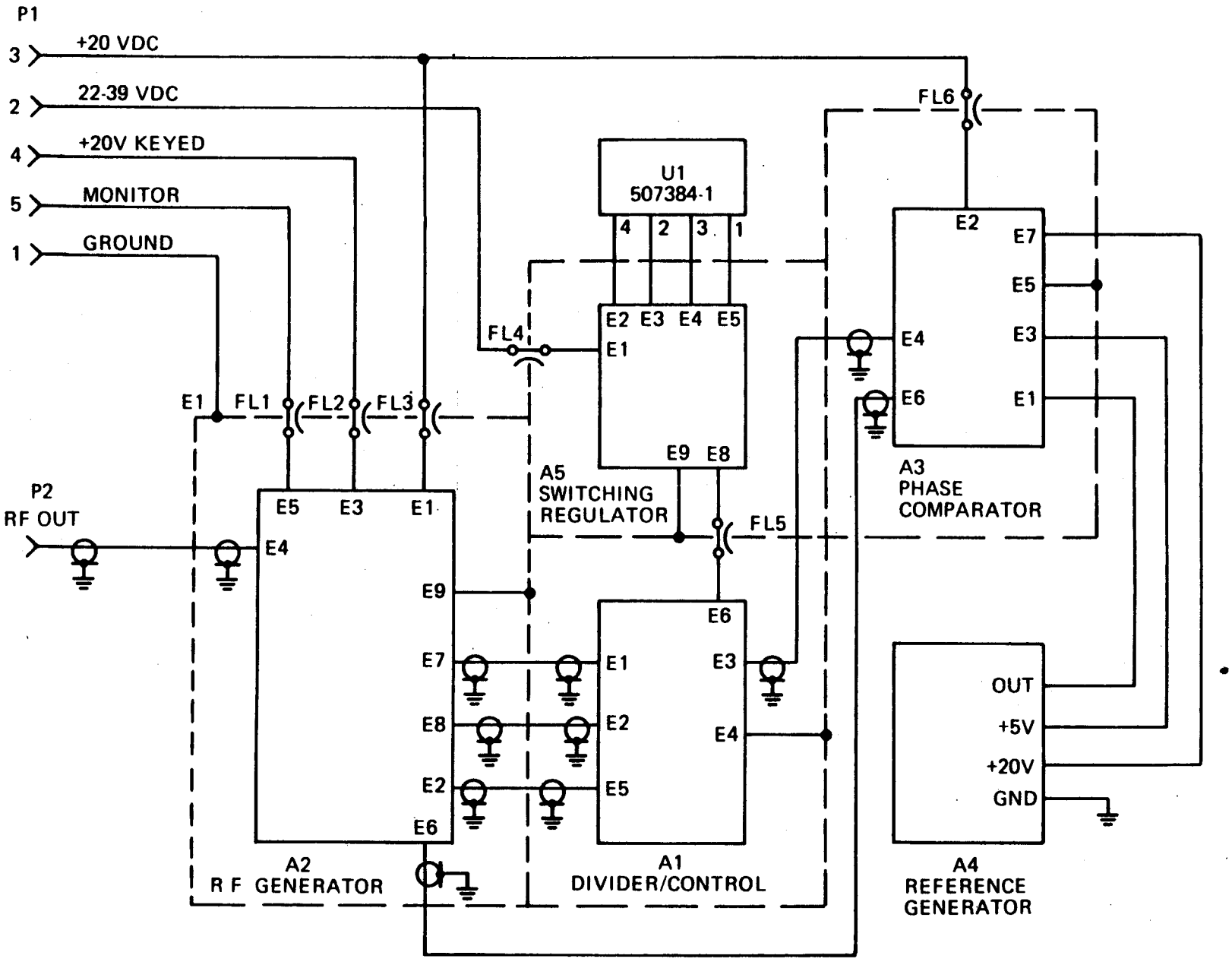
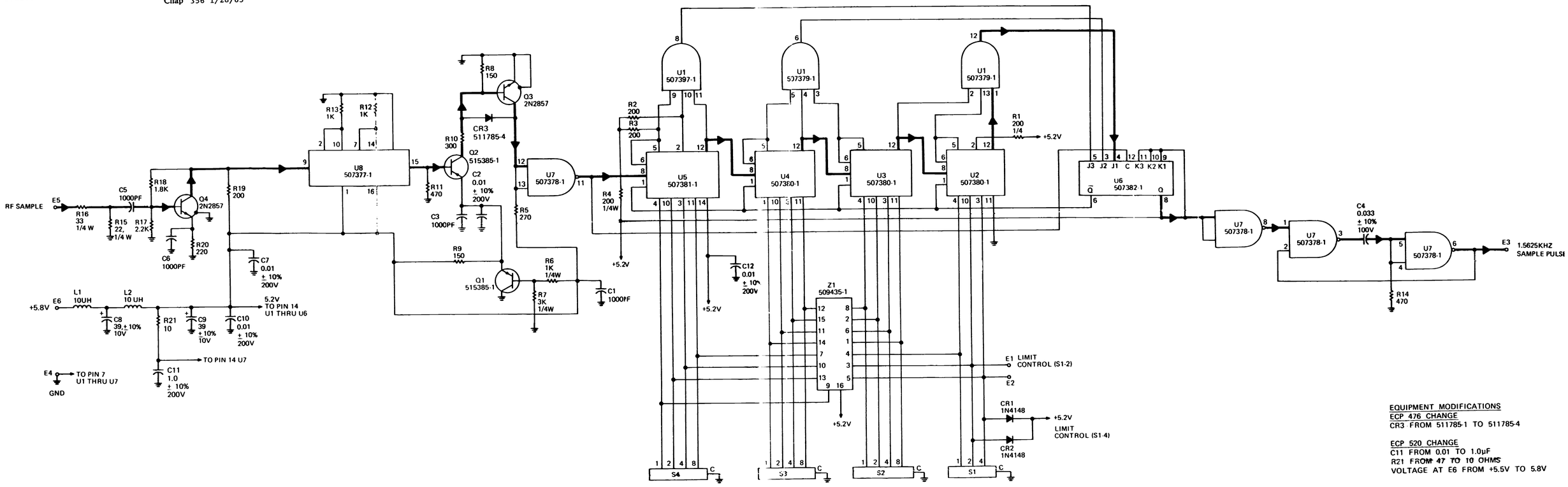


Figure 11-16. Oscillator-Synthesizer A1(S)

OSCILLATOR – SYNTHESIZER A1(S)

The oscillator-synthesizer generates selectable stable frequencies by a voltage-tuned oscillator. The selected oscillator output frequency is fed to a prescaler counter which divides the frequency by 4 and feeds it to a variable counter. The variable counter further divides the frequency by a ratio of 9,000 to 15,999 as determined by the settings of the frequency select thumbwheels. The division ratio of the counter is such that when the voltage-tuned oscillator is generating the correct frequency, the output of the variable counter is 1.5625 kHz. This output signal is fed to a phase detector and compared with a 1.5625 kHz reference signal. The 1.5625 kHz reference signal is derived from a precision crystal-controlled oscillator and a digital fixed-frequency divider counter. The phase difference between these two signals determines the d.c. voltage which controls the voltage-tuned oscillator such that phase lock with the reference oscillator is maintained. The nominal output level of the oscillator is + 14 dBm ± 3 dBm.



EQUIPMENT MODIFICATIONS
ECP 476 CHANGE
CR3 FROM 511785-1 TO 511785-4

ECP 520 CHANGE
C11 FROM 0.01 TO 1.0μF
R21 FROM 47 TO 10 OHMS
VOLTAGE AT E6 FROM +5.5V TO 5.8V

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8 W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 1000V

Figure 11-17. Divider/Control A1A1(S)

DIVIDER/CONTROL A1A1(S)

This board determines the output frequency. The board contains a prescaler (divide by 4) and a variable counter with its associated frequency selection switches. The RF sample from the RF generator board is fed through attenuator R15 and R16. C5 is a d.c. block which couples the RF to the base of amplifier Q4. This device places the RF at a d.c. level of about 3.2 volts (by virtue of bias resistors R17 and R18) which is the optimum input level for U8. U8 is an emitter-coupled logic dual-D flip-flop which is hooked up to divide the input RF signal (56.25 MHz to 99.9937 MHz) by 4. The output of U8 is fed to an emitter-coupled pair Q1 and Q2. This circuit amplifies the output of U8 and shifts the signal level to that of TTL (transistor-transistor logic). Q3 is used as a saturating switch which drives the first logic gate.

The variable counter number (divide by N) is essentially a chain of programmable counters constructed entirely with monolithic integrated circuits. The division ratio N ranges from 9,000 to 15,997 and is programmed by generating binary logic levels with the four-digit frequency selector thumbwheel switches. The first three switches are inverted "nines" complement binary coded decimal (bcd). Switch S4 is hexadecimal code which programs U5 (divide by 16). S1, S2, and S3 program U2, U3, and U4 respectively, which are divide by 10 counters. Assuming the thumbwheels are set to 99.9937, this means all switches are made placing a "low" on all the inputs, so the division ratio is 15,997. Thus the signal is coupled through the NAND gate (U7) following Q3 and into U5. This divides the input 24.9984375 MHz pulse train by 16. The output of U5 drives the input of U4 which divides by 10. This signal then drives U3, which drives U2, each of which divide by 10. When the counter reaches 99.9937 (by dial), or 15,997 pulses have been counted, the inputs to the U1 AND gates are all high, which drive a three-input AND gate in U6, causing it to change states. This resets U2, U3, U4, and U5, and causes a pulse out of pin 8 of U6 into a NAND gate of U7. This drives another NAND gate, whose output is shaped by C4 and R14 to drive another NAND gate, which is the output of the divider. These NAND gates are used to shape the output of U3 to a narrow pulse (approximately 10 μs) which drives the phase comparator.

If the thumbwheels are set to numbers other than 99.9937, the inputs to the divider counters are made high through the switch. Z1 is a resistor network consisting of 15 each 4.7-kilohm pull-up resistors with one lead common to pin 16 (B+). No change will occur until the data strobe drops to a logic zero (Q of U6 upon full count). At that time the data on the inputs will be transferred to their associated counters and the count will take up from there on the next clock pulse. Under these conditions, the count required will be shortened by the amount of the preset inputs.

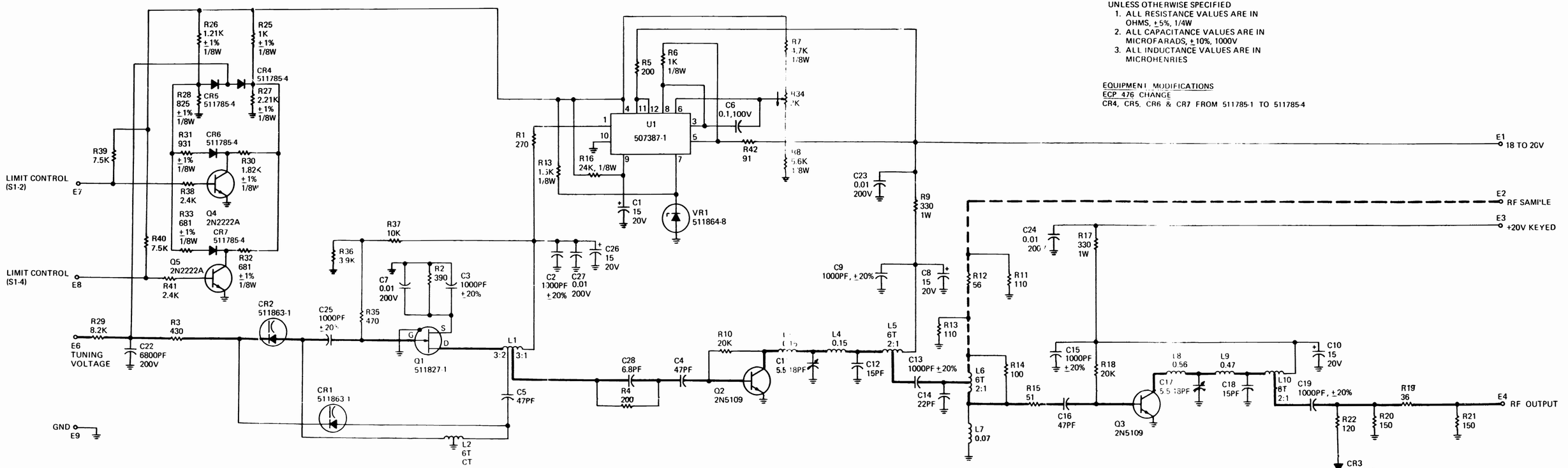


Figure 11-18. RF Generator A1A2(S)

RF GENERATOR A1A2(S)

The RF generator provides the output signal of the synthesizer, as well as driving the divider control prescaler. The printed wiring board contains the oscillator, limit controls for the oscillator, a buffer amplifier, a final amplifier, and a voltage regulator. The oscillator is basically a voltage-tuned Hartley circuit, with tank L2, CR1, and CR2. CR1 and CR2 are voltage variable capacitors (varactor diodes) whose capacity is dependent on the amount of reverse voltage. This control voltage is obtained from the output of the phase comparator, and is coupled through R29 and R3, with C22 used as a bypass. Q1 is a high-frequency field-effect transistor, with R1, R2, R35, R36, and R37 providing bias and feedback. C2, C3, C7, C26, and C27 are all bypass capacitors, and C5 and C25 are blocking capacitors. L1 is an autotransformer and is used to couple the signal out to the buffer amplifier Q2, through R4, C4, and C28.

R10 is a d.c. feedback resistor, and R9 is the collector load. L3, C11, L4, and C12 are low-pass filter sections to reduce the second harmonic, with C8, C9, and C23 used as bypasses. L5 is an autotransformer and couples the signal into signal splitter L6. R11, R12, and R13 are used to attenuate the signal which goes back to the divider control. L7, C16, and R15 match the input impedance of Q3, the final amplifier. R18 is the d.c. feedback with R17 the collector load. L8, C17, L9, and C18 are two low-pass filter sections to reduce harmonics, with C10, C15, and C24 bypasses. L10 is an autotransformer which couples the signal to C19, a d.c. block. R19, R20, and R21 are used to attenuate the signal to provide isolation from loading effects of the synthesizer output. R22, CR3, C20, R23, C21, and R24 form an RF detector which indicates the presence of RF on the receiver front panel L0 test point.

U1 is a transistor array of two individual transistors and two transistors internally connected as a Darlington circuit. U1 is used as a voltage regulator, with VR1 the zener reference. Q4 and Q5 are used to limit the control line voltage to the oscillator. They are tuned on by S1 on the divider control. This switch has binary coded decimal outputs, and depends on the frequency selected by the first thumbwheel switch. Either or both Q4 and Q5 may be turned on. When either is turned on, a voltage limit is developed across the precision resistors which are coupled to the control line. This voltage overrides the control voltage from the phase comparator and limits the oscillator range. This prevents the synthesizer from locking falsely on a harmonic.

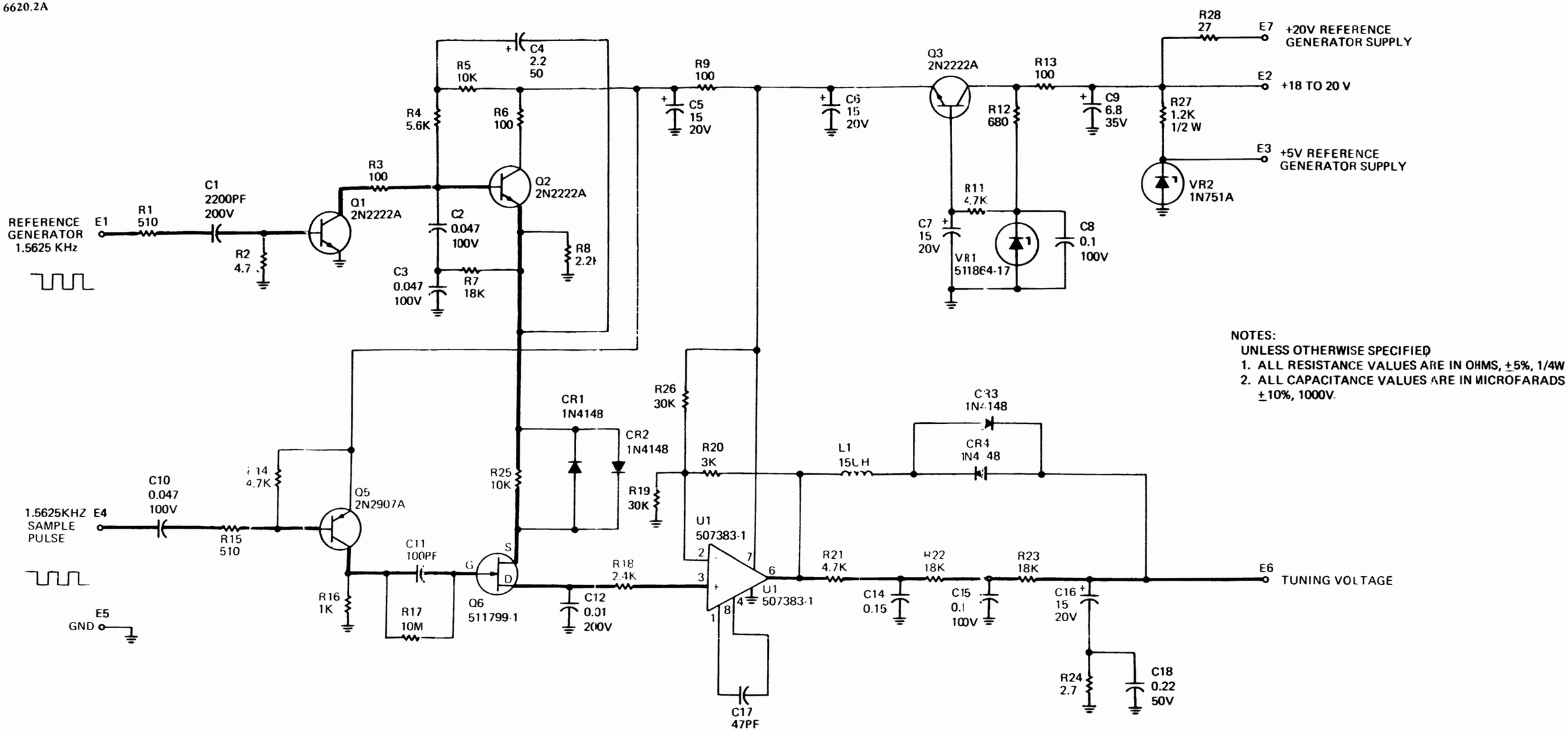


Figure 11-19. Phase Comparator A1A3(S)

PHASE COMPARATOR A1A3(S)

The phase comparator converts the difference between the phase of the variable counter and the reference generator to an error voltage. Note that the frequency of these two signals is the same, but they differ in phase. Q3 is a voltage regulator of the capacitor multiplier type. C9 and R13 are filters for the regulated 18 to 20 V d.c. input supply. VR1 is the zener diode which provides the reference voltage. C7 and C8 are bypass capacitors for VR1, with R11 and R12 the bias for Q3. C5, C6, and R9 are filters for the regulated output of Q3. R28 is a decoupling component to further filter the input voltage to the reference generator. R27 and VR2 establish the regulated +5V for the reference generator. Q1 is a switch for the square wave from the reference generator. R1, R2, and C1 differentiate the leading edge of the incoming square wave to cause a quick turn-on of Q1. This drives the ramp generator Q2. When Q1 conducts, it discharges C2 and C3, and pulls the base and emitter of Q2 toward ground. After Q1 turns off, C2, C3, R4, and R5 are used as an RC time constant to create a ramp. Since Q2 is an emitter follower, the output is bootstrapped back to the base to increase the ramp. R7 is used to linearize the ramp. R6 and R8 are bias resistors for Q2.

Q5 is a switch for the negative pulse from the divider control circuit which is differentiated by C10 and R15. R14 and R16 are bias resistors. C11 and R17 couple the leading edge of the signal to the gate of Q6 while also providing a high impedance. The ramp generator output is applied to the source of Q6 and is a varying d.c. voltage. When the sample pulse from the divider control is applied, Q6 conducts the d.c. level that is on the source at that particular instant, and this d.c. level is stored on C12. This level is held until the next sample pulse. Thus the circuit "samples" the d.c. level of the ramp, and "holds" it. This "hold" voltage is a continuous voltage that is proportional to the phase difference of the two input signals. During search mode (before phase lock occurs), CR1 or CR2 conduct because there is greater than 0.6 volt across them. After phase lock occurs, the voltage differential is low and R25 provides isolation for any noise that might be present. U1 is a high input impedance operational amplifier which is used as a d.c. level shifter to provide the proper d.c. level for the voltage-tuned oscillator. It has almost unity gain, with R19 and R26 providing the nominal operating level. R21, C14, R22, C15, R23, C16, R24, and C18 form a multisection low-pass filter which is used to remove any undesired a.c. signal from the control voltage to the voltage-tuned oscillator. During search mode, most of the filter is bypassed by L1 and CR2 or CR3, which conduct when the voltage differential is greater than 0.6 volt.

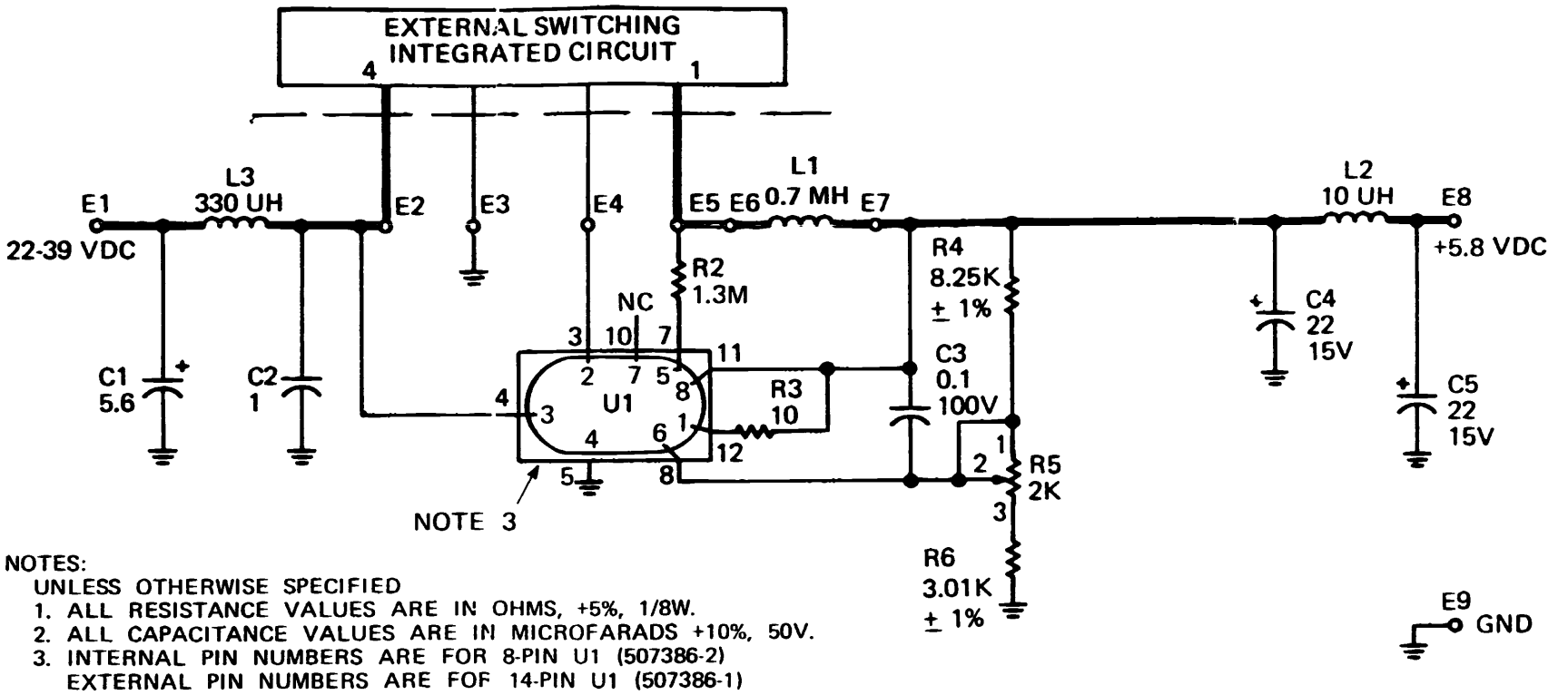


Figure 11-20. Switching Regulator A1A5(S)

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, +5%, 1/8W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS +10%, 50V.
3. INTERNAL PIN NUMBERS ARE FOR 8-PIN U1 (507386-2)
   EXTERNAL PIN NUMBERS ARE FOF 14-PIN U1 (507386-1)

EQUIPMENT MODIFICATIONS

ECP 470 CHANGES

DELETE VR1 (1N754A)
DELETE R7 (20 OHMS)
DELETE R8 (1K)
DELETE CR1 (2N2323)

ECP 520 CHANGES

CHANGE R2 FROM 1M TO 1.3M
CHANGE E8 VOLTAGE +5.5 Vdc TO 5.8 Vdc

ECP 648 CHANGE

CHANGE U1 TO BE EITHER
8-PIN (507386-2) or
14-PIN (507386-1)

ADD NOTE 3

SWITCHING REGULATOR A1A5(S)

This printed wiring board consists of an input filter, a power switch driver, an overvoltage shutdown circuit, and an output filter. The input filter consists of C1, C2, and L3. U1 is the switch driver, with R3 used as a short circuit protector. R4, R5, and R6 form a voltage divider string. L1 is an inductor which filters the d.c. pulses from the power switch. Operation consists of U1 being turned on by the feedback sensor after it drops to a sufficiently low value. It is an operational amplifier with its own internal reference diode. It operates as a switch and is either on or off. It drives an integrated circuit mounted on the back of the synthesizer which is a power switch. This switch conducts the unregulated d.c. for short pulses, operating at 40 kHz switching frequency.

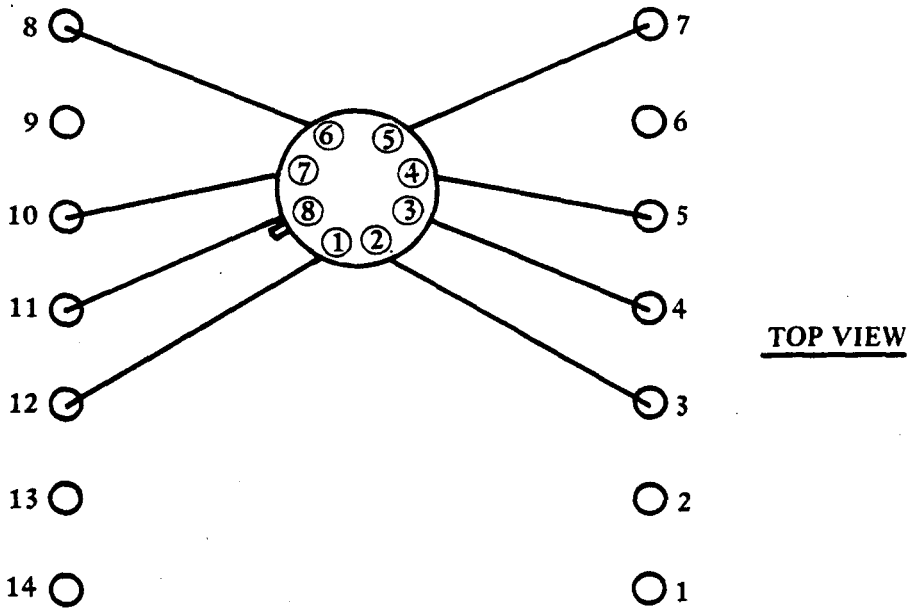


Figure 11-20A. T0-5/T0-99 Installation in 14-Pin Dual Inline Package (DIP) Socket

Voltage regulator U1 in the synthesizer switching regulator (A1A5) is no longer manufactured in the 14-pin dual inline package. U1 may be replaced with either the 14-pin DIP or with the 8-pin T0-5 or T0-99 package that is electrically equivalent. Use one or the other; do not install both on the sme circuit card. Figure 11-20A illustrates how the 8-pin T0-5 or T0-99 is to be installed to replace the 14-pin DIP in case of failure of the 14-pin DIP.

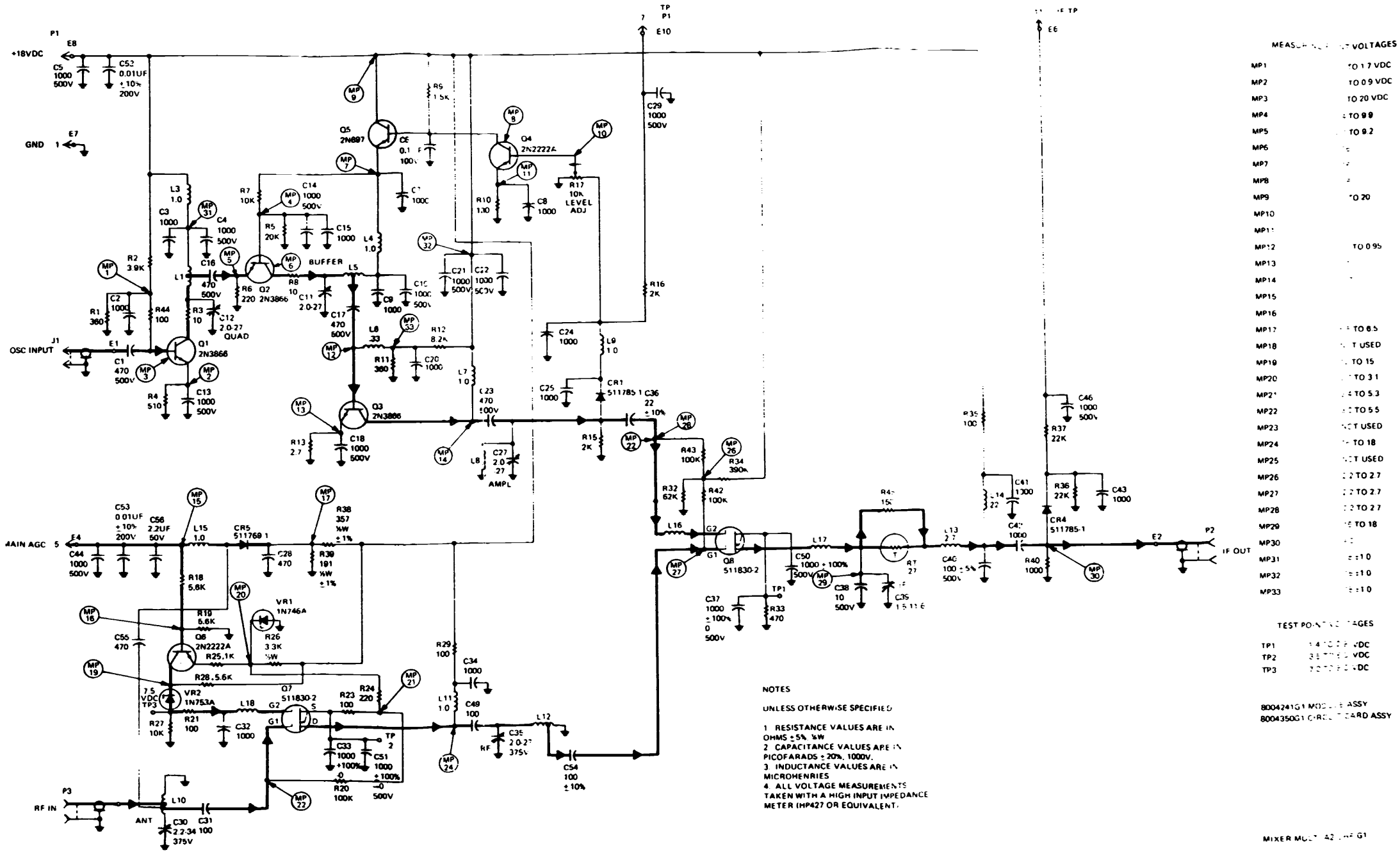


Figure 11-21. Mixer/Multiplier (UHF) A2 G1

11-42/11-41 (blank)

MIXER/MULTIPLIER (UHF) A2 G1

The uhf mixer/multiplier module consists of an agc-controlled RF stage, a mixer stage, a local oscillator frequency quadrupler stage, a buffer amplifier stage, an amplifier stage, a feedback amplifier stage and a series regulating stage for gain control. The RF input from the antenna is directly coupled to a tap on L10. The input tuned circuit consists of L10 and variable capacitor C30 which is peaked at the incoming RF. The input RF signal is coupled through C31 to gate 1 of the dual gate field effect transistor RF stage Q7. The source of Q7 is supplied through R23 and R24 from the cathode of zener diode VR1.

The voltage at gate 2 of Q7 is developed by the voltage divider consisting of R28, VR2, and R27 and is supplied to gate 2 of Q7 through R21 and L18. The agc input is connected through R18 to common emitter agc amplifier Q6. The agc input is also connected through L15 and pin diode CR5 to voltage divider R38 and R39. As the agc voltage level increases with increasing RF signal level, the pin diode is driven into conduction and thus attenuates incoming signals and prevents Q7 and Q8 from being overdriven. As the agc voltage increases, Q6 is driven harder into conduction and reduces the voltage supplied to gate 2 of Q7 by shunting VR2 and R27 in the voltage divider that provides bias for gate 2 of Q7.

The output at the drain of Q7 is coupled through C49 to parallel tuned circuit L12 and C35. C35 is adjustable to peak the signal at the received RF. The signal is then coupled through C54 to gate 1 of the dual-gate field effect transistor mixer stage Q8. The quadrupled crystal oscillator frequency is applied to gate 2 of Q8 and the intermediate frequency of 20.6 MHz is produced at the drain of Q8. Variable capacitor C39 is adjusted for maximum IF signal output. Impedance matching for the output circuit of Q8 is provided by matching network C38, C39, L13, and C40. Temperature compensation is provided by R45 and thermistor RT1. The IF signal is also detected by CR4 and applied through R37 to the receiver front panel major test point MIXER OUT as a positive voltage level.

The output from the oscillator module is coupled through C1 to the base of quadrupler Q1. Bias for Q1 is supplied through R44 from the voltage divider R1 and R2. C12 is adjusted to peak the signal in the collector of Q1 at four times the frequency applied to the base. The quadrupled frequency is coupled through C16 to the emitter of common base buffer amplifier Q2. C11 is adjusted to peak the signal at the collector of Q2 at four times the oscillator frequency. The signal is coupled through C17 to the base of amplifier Q3. C27 is adjusted to peak the signal at the collector of Q3 at four times the oscillator frequency. The signal is coupled from the collector of Q3 through C23, C36, and L16 to gate 2 of Q8. The voltage at the collector of Q3 is also detected by CR1 and applied through potentiometer R17 to the base of feedback amplifier Q4. The collector voltage of Q4 in turn controls the base to emitter bias for series regulator Q5. Q2 operates between cutoff and saturation. Q5 controls the output of Q2 by controlling the d.c. supply voltage to Q2 and thus the operating point of Q2. The detected voltage from CR1 is also applied to the front panel major test point MULT.

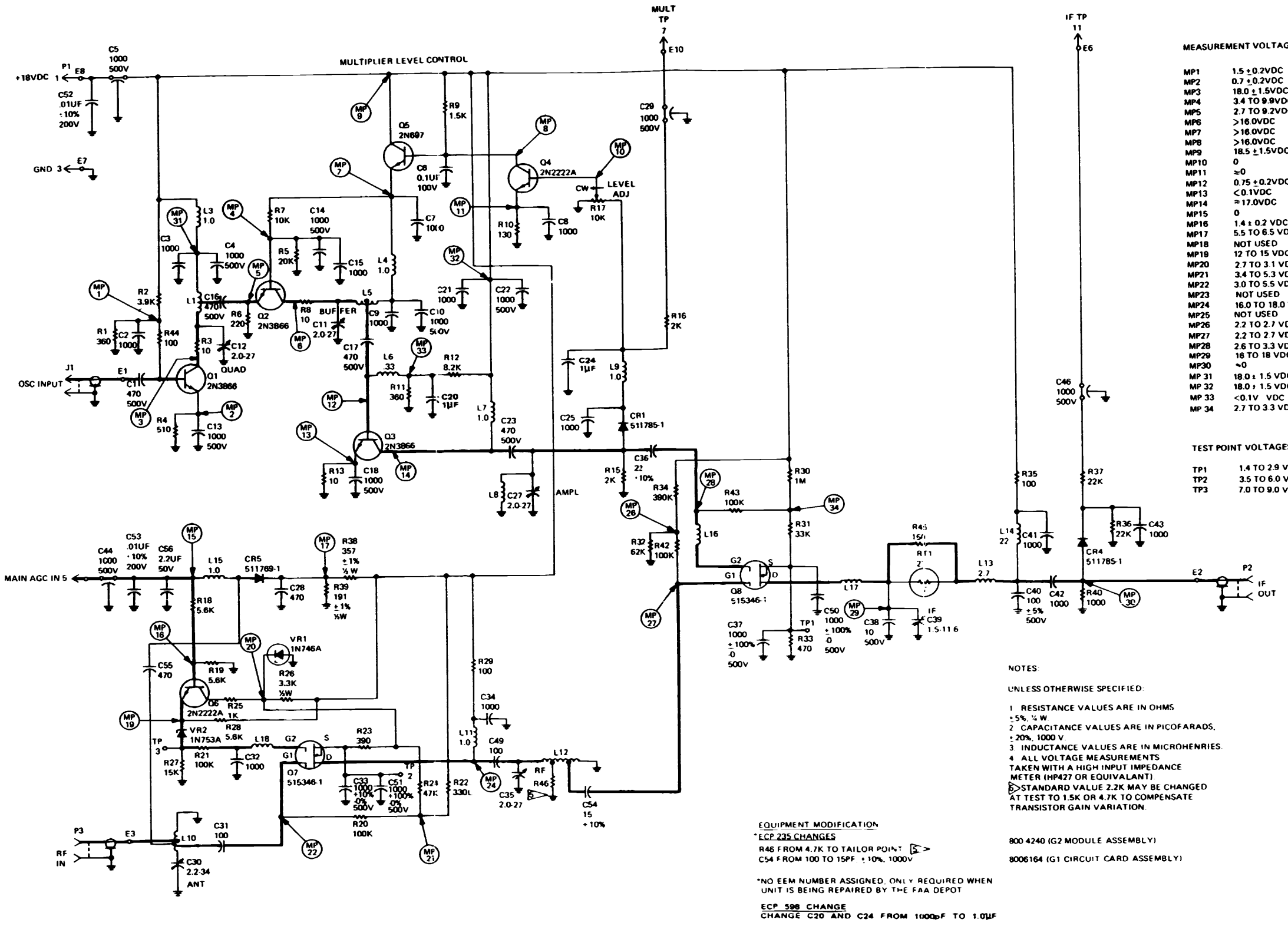


Figure 11-22. Mixer/Multiplier (UHF) A2 G2

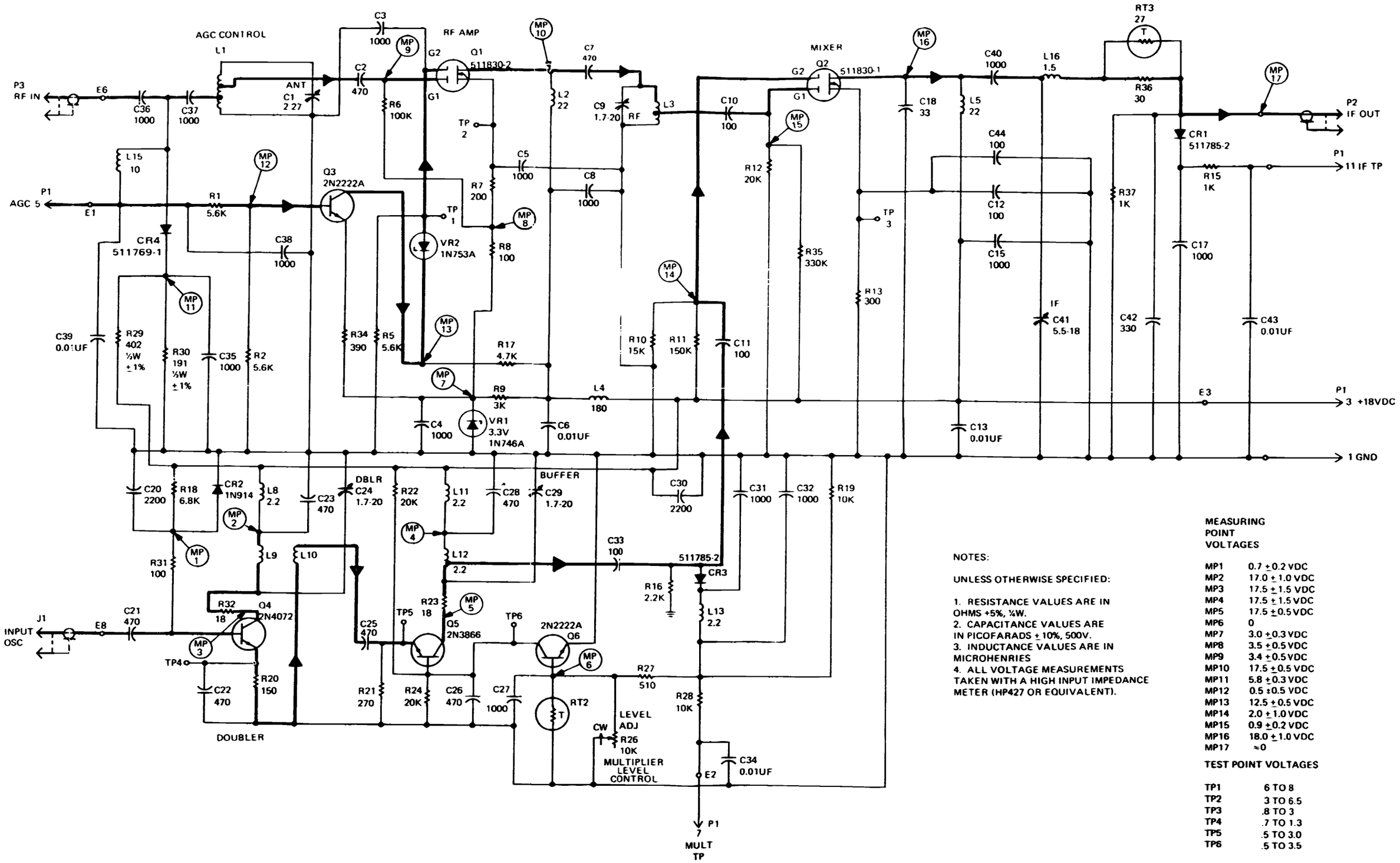
MIXER/MULTIPLIER (UHF) A2 G2

The uhf mixer/multiplier module consists of an agc-controlled RF stage, a mixer stage, a local oscillator frequency quadrupler stage, a buffer amplifier stage, an amplifier stage, a feedback amplifier stage, and a series regulating stage for gain control. The RF input from the antenna is directly coupled to a tap on L10. The input tuned circuit consists of L10 and variable capacitor C30 which is peaked at the incoming RF. The input RF signal is coupled through C31 to gate 1 of the dual gate field effect transistor RF stage Q7. The source of Q7 is supplied through R23 from the cathode of zener diode VR1.

The voltage at gate 2 of Q7 is developed by the voltage divider consisting of R28, VR2, and R27 and is supplied to gate 2 of Q7 through R21 and L18. The agc input is divided by R18 and R19 and applied to the base of common emitter amplifier stage Q6. The agc input is also connected through L15 and pin diode CR5 to voltage divider R38 and R39. As the agc voltage level increases with increasing RF signal level, the pin diode is driven into conduction and thus attenuates incoming signals and prevents Q7 and Q8 from being overdriven. As the agc voltage increases, Q6 is driven harder into conduction and reduces the voltage supplied to gate 2 of Q7 by shunting VR2 and R27 in the voltage divider that provides bias for gate 2 of Q7.

The output at the drain of Q7 is coupled through C49 to parallel tuned circuit L12 and C35. C35 is adjustable to peak the signal at the received RF. The signal is then coupled through C54 to gate 1 of the dual-gate field effect transistor mixer stage Q8. The quadrupled crystal oscillator frequency is applied to gate 2 of Q8 and the intermediate frequency of 20.6 MHz is produced at the drain of Q8. Variable capacitor C39 is adjusted for maximum IF signal output. Impedance matching for the output circuit of Q8 is provided by matching network C38, C39, L13, and C40. Temperature compensation is provided by R45 and thermistor RT1. The IF signal is also detected by CR4 and applied through R37 to the receiver front panel major test point MIXER OUT as a positive voltage level.

The output from the oscillator module is coupled through C1 to the base of quadrupler Q1. Bias for Q1 is supplied through R44 from the voltage divider R1 and R2. C12 is adjusted to peak the signal in the collector of Q1 at four times the frequency applied to the base. The quadrupled frequency is coupled through C16 to the emitter of common base buffer amplifier Q2. C11 is adjusted to peak the signal at the collector of Q2 at four times the oscillator frequency. The signal is coupled through C17 to the base of amplifier Q3. C27 is adjusted to peak the signal at the collector of Q3 at four times the oscillator frequency. The signal is coupled from the collector of Q3 through C23, C36, and L16 to gate 2 of Q8. The voltage at the collector of Q3 is also detected by CR1 and applied through L9 and potentiometer R17 to the base of feedback amplifier Q4. The collector voltage of Q4 in turn controls the base to emitter bias for series regulator Q5. Q2 operates between cutoff and saturation. Q5 controls the output of Q2 by controlling the d.c. supply voltage to Q2 and thus the operating point of Q2. The detected voltage from CR1 is also applied to the front panel major test point MULT.



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS +5%, ¼W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ±10%, 500V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

MEASURING POINT VOLTAGES

MP1	0.7 ±0.2 VDC
MP2	17.0 ± 1.0 VDC
MP3	17.5 ± 1.5 VDC
MP4	17.5 ± 1.5 VDC
MP5	17.5 ±0.5 VDC
MP6	0
MP7	3.0 ±0.3 VDC
MP8	3.5 ±0.5 VDC
MP9	3.4 ±0.5 VDC
MP10	17.5 ±0.5 VDC
MP11	5.8 ±0.3 VDC
MP12	0.5 ±0.5 VDC
MP13	12.5 ±0.5 VDC
MP14	2.0 ± 1.0 VDC
MP15	0.9 ±0.2 VDC
MP16	18.0 ± 1.0 VDC
MP17	≈0

TEST POINT VOLTAGES

TP1	6 TO 8
TP2	3 TO 6.5
TP3	.8 TO 3
TP4	.7 TO 1.3
TP5	.5 TO 3.0
TP6	.5 TO 3.5

8004240G1 MODULE ASSY.

8004351G1 CIRCUIT CARD ASSY.

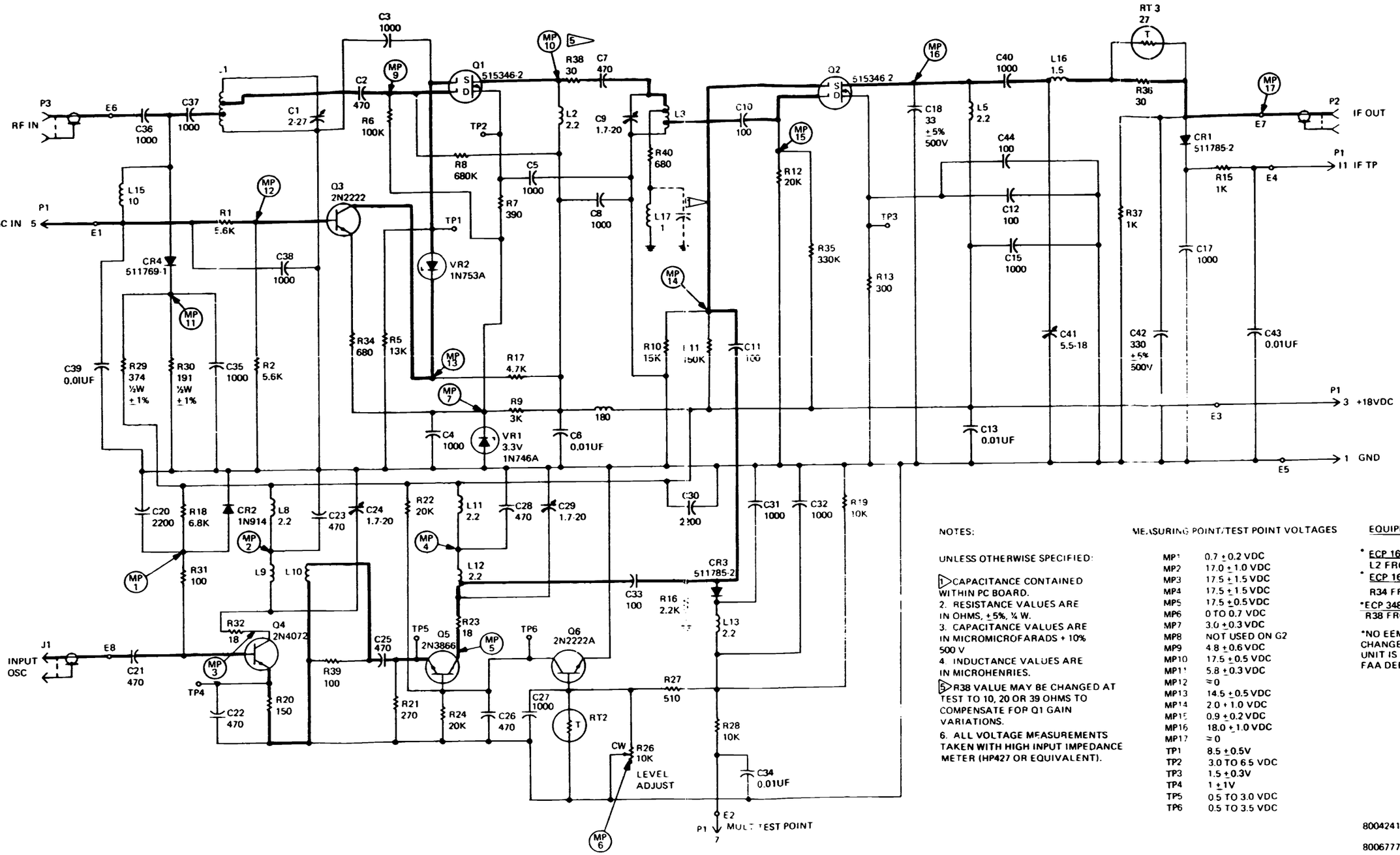
Figure 11-23. Mixer/Multiplier (VHF) A2 G1

MIXER/MULTIPLIER (VHF) A2 G1

The vhf mixer/multiplier module consists of a temperature-compensated and agc-controlled RF stage, a mixer stage, a local oscillator frequency doubler stage, and a buffer amplifier with a temperature compensated feedback stage. Optimum gain for the module is 12 to 14 dB. The RF input from the antenna is coupled through C36 and C37 to a tap on L1. Resonance at the received frequency is achieved by adjusting variable capacitor C1. The signal from a tap on L1 is coupled through C2 to gate 1 of dual-gate field effect transistor Q1. The source of Q1 is supplied through R7 and R8 from the cathode of zener diode VR1. The +3.3 volts established by the diode, is used to raise the source of Q1 sufficiently above ground so that the gates may be negatively biased relative to the source.

This voltage at gate 2 of Q1 is developed from the agc input to the module. The agc input is divided by R1 and R2 and applied to the base of common-emitter amplifier stage Q3. The agc input is also connected through L15 and pin diode CR4 to the voltage divider R29 and R30. As the agc voltage level increases with increasing RF signal level, the pin diode is driven into conduction and thus attenuates incoming signals and prevents Q1 and Q2 from being overdriven. The collector of Q3 becomes less positive as the input agc level becomes more positive. This voltage is a bias voltage direct coupled to gate 2 of Q1 after being level changed by zener diode VR2 allowing the agc input to control the level of the RF signal through Q1. The output at the drain of Q1 is coupled through C7 to parallel tuned circuit L3 and C9. C9 is adjustable to peak up the signal at the received RF frequency. The signal is then coupled through C10 to gate 1 of the dual-gate field effect transistor mixer stage Q2. The doubled crystal oscillator frequency is applied to gate 2 of Q2 and the intermediate frequency of 20.6 MHz is produced at the drain of Q2. Variable capacitor C41 is adjusted for maximum output at the IF signal. Impedance matching for the output circuit is provided by matching network L5, C18, C41, and C42. Temperature compensation is provided by thermistor RT3 and R36. The IF signal is also detected by CR1 and applied through R15 to the receiver front panel major test point MIXER OUT as a positive voltage level.

The output from the oscillator module is coupled through C21 to the base of doubler stage Q4. This signal is 0.6 to 1.0 volt rms. Approximately a +0.6 volt bias voltage is applied through R31 to the base of Q4. C24 is adjusted to peak up the signal in the collector of Q4 at twice the signal frequency impressed upon the base. This doubled frequency is induced from L9 into L10 and coupled through C25 to the emitter of buffer amplifier stage Q5. A feedback loop from Q6 establishes the voltage level on the base of Q5 thereby controlling the emitter-base bias of Q5 stabilizing its output. C29 is adjustable to resonate at the frequency produced by the preceding doubler stage. This output is coupled through C33 and C11 to gate 2 of mixer stage Q2 as previously discussed. The output is also detected by CR3 and applied through a low pass pi filter and R27 to the base of Q6. R26 provides level control by controlling the feedback voltage to Q5; temperature compensation is provided by RT2. The detected and filtered output is also applied through R28 to the receiver front panel MULT test point.



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. CAPACITANCE CONTAINED WITHIN PC BOARD.
2. RESISTANCE VALUES ARE IN OHMS, ±5%, ¼ W.
3. CAPACITANCE VALUES ARE IN MICROMICROFARADS ± 10% 500 V
4. INDUCTANCE VALUES ARE IN MICROHENRIES.
5. R38 VALUE MAY BE CHANGED AT TEST TO 10, 20 OR 39 OHMS TO COMPENSATE FOR Q1 GAIN VARIATIONS.
6. ALL VOLTAGE MEASUREMENTS TAKEN WITH HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

MEASURING POINT/TEST POINT VOLTAGES

MP1	0.7 ±0.2 VDC
MP2	17.0 ±1.0 VDC
MP3	17.5 ±1.5 VDC
MP4	17.5 ±1.5 VDC
MP5	17.5 ±0.5 VDC
MP6	0 TO 0.7 VDC
MP7	3.0 ±0.3 VDC
MP8	NOT USED ON G2
MP9	4.8 ±0.6 VDC
MP10	17.5 ±0.5 VDC
MP11	5.8 ±0.3 VDC
MP12	≈0
MP13	14.5 ±0.5 VDC
MP14	2.0 ±1.0 VDC
MP15	0.9 ±0.2 VDC
MP16	18.0 ±1.0 VDC
MP17	≈0
TP1	8.5 ±0.5V
TP2	3.0 TO 6.5 VDC
TP3	1.5 ±0.3V
TP4	1 ±1V
TP5	0.5 TO 3.0 VDC
TP6	0.5 TO 3.5 VDC

EQUIPMENT MODIFICATIONS

- ECP 169 CHANGES
  L2 FROM 22 to 2.2 MICROHENRIES
- ECP 169A CHANGES
  R34 FROM 390 TO 680 OHMS
- ECP 348 CHANGE
  R38 FROM 10 TO 30 OHMS

*NO EEM NUMBER ASSIGNED. CHANGES ONLY REQUIRED WHEN UNIT IS BEING REPAIRED AT THE FAA DEPOT.

8004241 G2 MODULE ASSEMBLY

8006777 G1 CARD ASSEMBLY

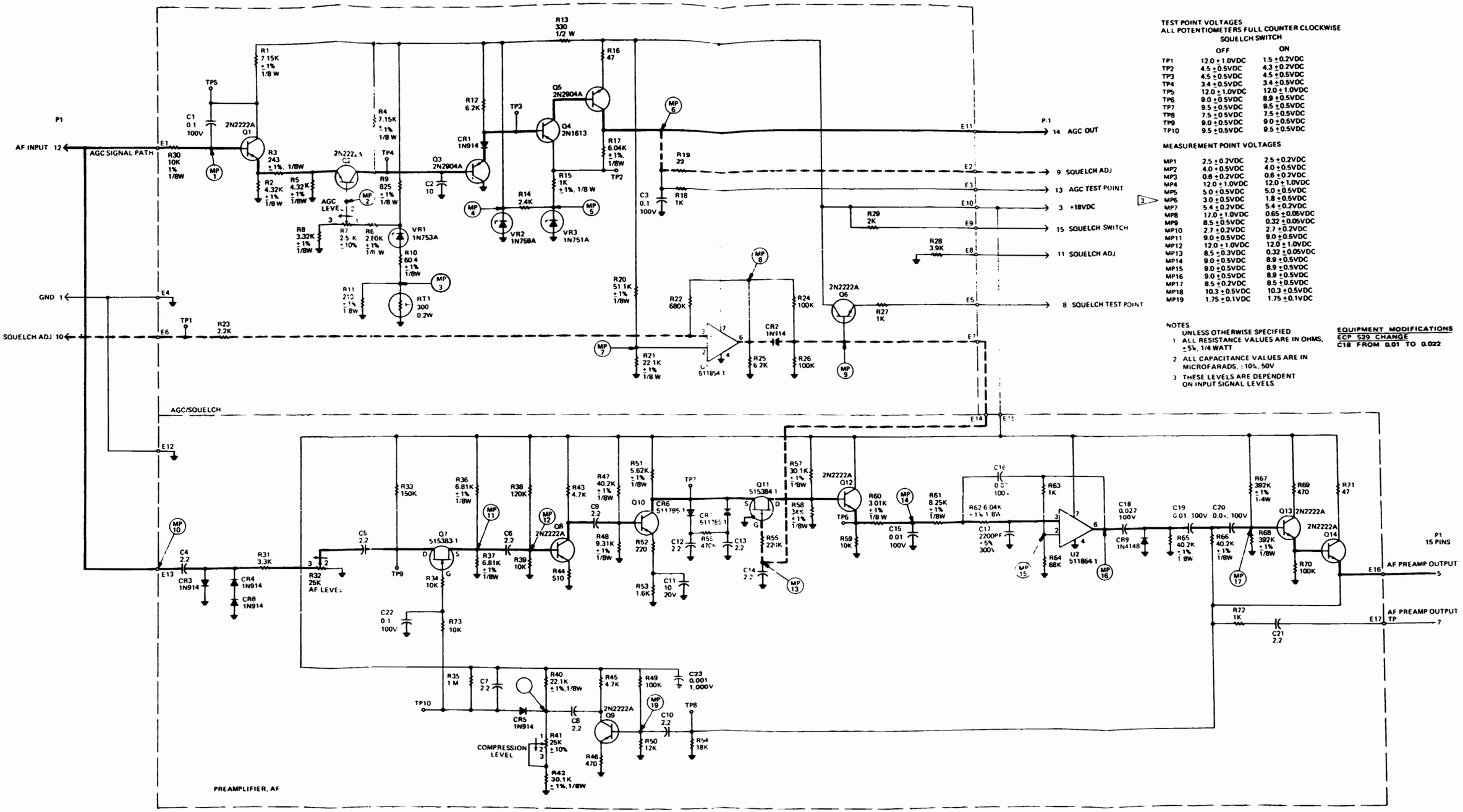
Figure 11-24. Mixer/Multiplier (VHF) A2 G2

MIXER/MULTIPLIER (VHF) A2 G2

The vhf mixer/multiplier module consists of a temperature-compensated and agc-controlled RF stage, a mixer stage, a local oscillator frequency doubler stage, and a buffer amplifier with a temperature compensated feedback stage. Optimum gain for the module is 12 to 14 dB. The RF input from the antenna is coupled through C36 and C37 to a tap on L1. Resonance at the received frequency is achieved by adjusting variable capacitor C1. The signal from a tap on L1 is coupled through C2 to gate 1 of dual-gate field effect transistor Q1. The source of Q1 is supplied through R7 from the cathode of zener diode VR1. The +3.3 volts established by the diode, is used to raise the source of Q1 sufficiently above ground so that the gates may be negatively biased relative to the source.

The voltage at gate 2 of Q1 is developed from the agc input to the module. The agc input is divided by R1 and R2 and applied to the base of common emitter amplifier stage Q3. The agc input is also connected through L15 and pin diode CR4 to the voltage divider R29 and R30. As the agc voltage level increases with increasing RF signal level, the pin diode is driven into conduction and thus attenuates incoming signals and prevents Q1 and Q2 from being overdriven. The collector of Q3 becomes less positive as the input agc level becomes more positive. This voltage is a bias voltage direct coupled to gate 2 of Q1 after being changed in level by zener diode VR2 allowing the agc input to control the level of the RF signal through Q1. The output at the drain of Q1 is coupled through R38 and C7 to parallel tuned circuit L3 and C9. R38 is a parasitic suppression resistor. C9 is adjustable to peak up the signal at the received RF frequency. The signal is then coupled through C10 to gate 1 of the dual-gate field effect transistor mixer stage Q2. The doubled crystal oscillator frequency is applied to gate 2 of Q2 and the intermediate frequency of 20.6 MHz is produced at the drain of Q2. Variable capacitor C41 is adjusted for maximum output at the IF signal. Impedance matching for the output circuit is provided by matching network L5, C18, C41, and C42. Temperature compensation is provided by thermistor RT3 and R36. The IF signal is also detected by CR1 and applied through R15 to the receiver front panel major test point MIXER OUT as a positive voltage level.

The output from the oscillator module is coupled through C21 to the base of doubler stage Q4. This signal is 0.6 to 1.0 volt rms. Approximately a +0.6 volt bias voltage is applied through R31 to the base of Q4. C24 is adjusted to peak up the signal in the collector of Q4 at twice the signal frequency impressed upon the base. This doubled frequency is induced from L9 into L10 and coupled through C25 to the emitter of buffer amplifier stage Q5. A feedback loop from Q6 establishes the voltage level on the base of Q5 thereby controlling the emitter-base bias of Q5 stabilizing its output. C29 is adjustable to resonate at the frequency produced by the preceding doubler stage. This output is coupled through C33 and C11 to gate 2 of mixer stage Q2 as previously discussed. The output is also detected by CR3 and applied through a low pass pi filter and R27 to the base of Q6. R26 provides level control by controlling the feedback voltage to Q5; temperature compensation is provided by RT2. The detected and filtered output is also applied through R28 to the receiver front panel MULT test point.



TEST POINT VOLTAGES
ALL POTENTIOMETERS FULL COUNTER CLOCKWISE
SQUELCH SWITCH

	OFF	ON
TP1	12.0 ± 1.0VDC	1.5 ± 0.2VDC
TP2	4.5 ± 0.5VDC	4.3 ± 0.2VDC
TP3	4.5 ± 0.5VDC	4.5 ± 0.5VDC
TP4	3.4 ± 0.5VDC	3.4 ± 0.5VDC
TP5	12.0 ± 1.0VDC	12.0 ± 1.0VDC
TP6	9.0 ± 0.5VDC	8.9 ± 0.5VDC
TP7	9.5 ± 0.5VDC	9.5 ± 0.5VDC
TP8	7.5 ± 0.5VDC	7.5 ± 0.5VDC
TP9	9.0 ± 0.5VDC	9.0 ± 0.5VDC
TP10	9.5 ± 0.5VDC	9.5 ± 0.5VDC

MEASUREMENT POINT VOLTAGES

MP1	2.5 ± 0.2VDC	2.5 ± 0.2VDC
MP2	4.0 ± 0.5VDC	4.0 ± 0.5VDC
MP3	0.6 ± 0.2VDC	0.6 ± 0.2VDC
MP4	12.0 ± 1.0VDC	12.0 ± 1.0VDC
MP5	5.0 ± 0.5VDC	5.0 ± 0.5VDC
MP6	3.0 ± 0.5VDC	1.8 ± 0.5VDC
MP7	5.4 ± 0.2VDC	5.4 ± 0.2VDC
MP8	17.0 ± 1.0VDC	0.65 ± 0.05VDC
MP9	8.5 ± 0.5VDC	0.32 ± 0.05VDC
MP10	2.7 ± 0.2VDC	2.7 ± 0.2VDC
MP11	9.0 ± 0.5VDC	9.0 ± 0.5VDC
MP12	12.0 ± 1.0VDC	12.0 ± 1.0VDC
MP13	8.5 ± 0.3VDC	0.32 ± 0.05VDC
MP14	9.0 ± 0.5VDC	8.9 ± 0.5VDC
MP15	9.0 ± 0.5VDC	8.9 ± 0.5VDC
MP16	9.0 ± 0.5VDC	8.9 ± 0.5VDC
MP17	8.5 ± 0.2VDC	8.5 ± 0.5VDC
MP18	10.3 ± 0.5VDC	10.3 ± 0.5VDC
MP19	1.75 ± 0.1VDC	1.75 ± 0.1VDC

NOTES
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT
2 ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 50V
3 THESE LEVELS ARE DEPENDENT ON INPUT SIGNAL LEVELS

EQUIPMENT MODIFICATIONS
ECP 539 CHANGE
C18 FROM 0.01 TO 0.022

Figure 11-25. Preamplifier, AF/AGC-Squelch A3

PREAMPLIFIER, AF/AGC-SQUELCH A3

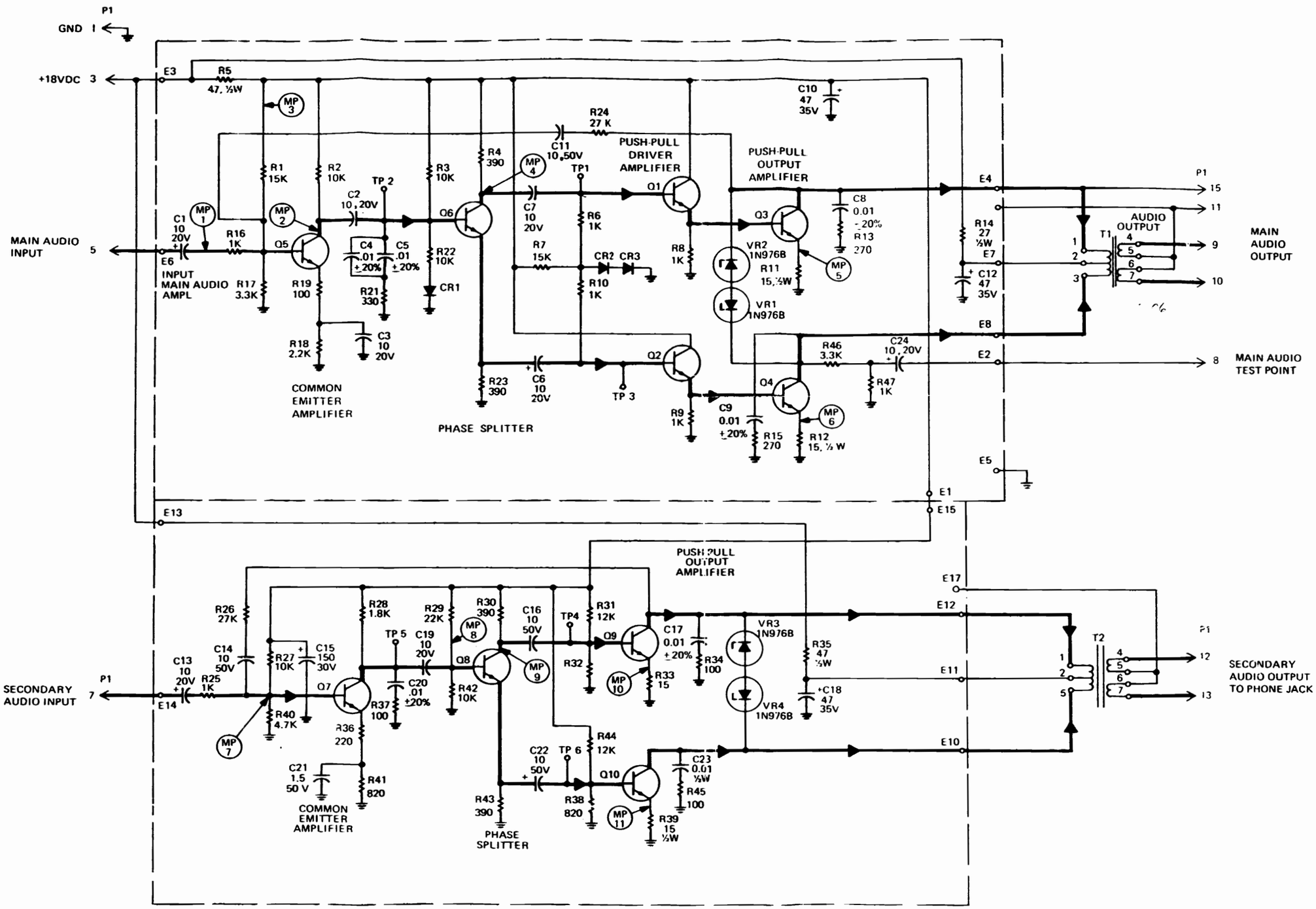
The audio input comes into P1 through pin 12 and is coupled through C4 to limiter diodes CR3, CR4, and CR8. This limiter clips noise and transients that occur on the audio input. The audio signal is then coupled through the voltage divider (R31 and R32), through capacitor C5 to the compression control FET Q7. The audio signal is fed through Q7, through capacitor C6 to the audio amplifier, Q8. Q8 amplifies the audio signal, coupling the amplified signal through C9 to amplifier Q10. Q10 further amplifies the audio signal and couples the output to a floating limiter consisting of CR6, CR7, R55, C12, and C13. This floating limiter provides limiting action around the d.c. bias level, and further limiting of unwanted noise pulses that occur in the audio passband. At this point in the circuit, the audio is compressed and maintains a near constant peak-to-peak signal level, and the floating limiter limits at levels just above and below the compression peak-to-peak audio level. The signal is then coupled through squelch control FET Q11 (described later) to emitter follower Q12. The output from Q12 is then coupled through the low-pass filter amplifier circuit consisting of R60, C15, R61, C17, R62, and C16, to operational amplifier U2. This low-pass filter and the high-pass filter (C18, C19, R65, R66, C20, R67, R68, Q13, Q14, R69, R70, and R71) maintain a receiver band pass of 300 to 3000 Hz within +1 to −2 dB of the reference frequency of 1000 Hz. The band pass of this filter rolls off the low end to at least 10 dB down at 100 Hz and at least 10 dB down at 10 kHz.

The audio output from the preamplifier path is coupled back to an amplifier consisting of transistor Q9 and associated biasing components. This stage amplifies the audio and detects and provides a d.c. bias to the compression FET Q7. Adjustment of the compression level is accomplished by an adjustment of R41 potentiometer which controls the amount of compression and the signal level output. This feedback compression circuit maintains a constant audio level output with varying audio input signals. The audio output from this module is coupled to the gain control on the front panel; consequently all compression takes place before the main audio gain control. Thus, compression is obtained at any audio signal level output. The compression detection takes place in diode CR5, and any ripple is filtered out by capacitor C7. This provides d.c. bias, proportional to the audio level, to the FET gate through resistors R73 and R34.

FET Q11 provides a series squelch switching action that turns the audio output on and off as a function of the agc amplifier. When the gate control voltage to Q11 is biased to a turn-off point, no audio signals pass through Q11. The source and the drain voltage potentials are nearly the same, thus providing no d.c. level shift when the transistor is turned off. When the transistor is turned on, the audio signal proceeds through Q11 with very little attenuation. It is the equipotential source and drain voltages that provide the quiet switching action of this squelch switch.

The automatic gain control amplifier consists of a differential amplifier, an emitter follower amplifier stage, and two additional amplifier stages. The detected carrier is coupled through R30 to the base of differential amplifier stage Q1. This transistor shares an emitter load network with Q2 consisting of R2, R3, and R5. The operating level of Q2 is adjusted by R7. The voltage at the junction of R6 and R9 is regulated by zener diode VR1. R11, RT1, and R10 are for temperature compensation. The adjustable voltage applied to the base of Q2 is established by the voltage divider composed of R6, R7, and R8. Direct coupling is used throughout the agc amplifier. The output from the differential amplifier, the collector of Q2, is applied to the base of emitter follower stage Q3. CR1 is used for temperature compensation. VR2 and R13 provide regulated +12 V for Q1, Q2, and Q3. Emitter follower Q3 output is applied to the base of Q4. The collector of Q4 is connected directly to the base of Q5. The agc output is taken from the collector of Q5. This output is also applied through R18 to the receiver front panel major test point AGC, to the squelch circuit (located in this same module) via R19, and the receiver front panel squelch control potentiometer.

The squelch circuit is essentially an electronic switch which turns on the preamplifier squelch FET when the detected signal reaches a certain level and turns off the FET when the detected signal is reduced to a certain level. With the receiver front panel squelch switch in the ON position, the agc voltage is applied across R19 and the front panel squelch adjust (R1 and R28). The wiper of front panel control R1 is directly coupled through resistor R23 to pin 3 of the operational amplifier U1. If the detected RF level increases, the output from operational amplifier pin 6 goes positive and turns on squelch FET Q11 in the preamplifier circuity. If the detector RF level decreases (as indicated by a decrease of the agc level) to the squelch level, the output from operational amplifier U1 decreases, thus turning off squelch FET Q11 in the preamplifier circuity. Complete and rapid switching is insured by the feedback path resistor R22 around the operational amplifier U1. Diode CR2 provides fast decay of squelch switch filtering capacitor C14 when the squelch switch turns off. When the receiver unsquelches, resistor R24 provides a short time constant action to charge C14 so that small squelch delay occurs to provide inhibiting of unwanted transients at the time of initial detection of input signals. Q6 provides a monitor output drive and serves as an isolation transistor for the squelch test point.



MEASUREMENT POINT VOLTAGES

MP1	2.7 ±0.6VDC
MP2	6.5 ±1.2VDC
MP3	16 ±2VDC
MP4	9.3 ±2VDC
MP5	0.55 +0.14VDC
MP6	0.55 ±0.14VDC
MP7	5.0 ±1.0VDC
MP8	4.0 ±0.5VDC
MP9	12.0 ±1.0VDC
MP10	0.25 ±0.1VDC
MP11	0.25 ±0.1VDC

TEST POINT VOLTAGES

TP1	1.0 V ±0.3 VDC
TP2	7.5 V ±0.5 VDC
TP3	1 V ±0.3 VDC
TP4	1 V ±0.2 VDC
TP5	8.5 V ±1 VDC
TP6	1 V ± 0. 2 VDC

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±5%, ¼ W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 2N1613.
5. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

Figure 11-26. Audio Frequency Amplifier A4

AUDIO FREQUENCY AMPLIFIER A4

The audio frequency amplifier consists of two separate audio amplifier systems. The main audio amplifier receives an input signal controlled by the AUDIO MAIN ADJ screwdriver adjustment on the receiver front panel, and supplies an output to a connector on the receiver rear apron for remote speaker operation. The secondary audio amplifier receives an input controlled by the PHONE ADJ control on the receiver front panel, and supplies an output to the PHONE OUTPUT jack on the receiver front panel.

The main audio amplifier consists of a common-emitter amplifier stage, a phase-splitter stage, a push-pull driver stage, a push-pull output stage, and an output transformer. The input audio signal is coupled through C1 and R16 to the base of common-emitter amplifier stage Q5. Degenerative feedback to this stage is employed to provide adequate regulation of the output signal voltage. This negative feedback signal is derived from output stage Q3 and is also coupled to the base of Q5 via R24 and C11. The signal from the collector of Q5 is coupled through C2 to the base of phase splitter Q6. The phase splitter provides signals of equal magnitude and opposite polarity to the output driver stage consisting of Q1 and Q2. Temperature compensation of bias for the driver stage is provided by CR2 and CR3.

The output signal from the emitters of driver stage Q1 and Q2 is direct coupled to the push-pull output stage at the base of Q3 and Q4. The collectors of Q3 and Q4 are connected to the primary of output transformer T1. The center tapped secondary of T1 is connected to a rear apron connector on the receiver. Signal voltage across T1 is limited to approximately 43 volts peak-to-peak maximum by the action of zener diodes VR1 and VR2. A compression output to the audio preamplifier/agc squelch module is provided from the collector of Q3. The signal from the collector of Q4 is divided by R46 and R47 and coupled through C24 to the receiver front panel major test point MAIN AF.

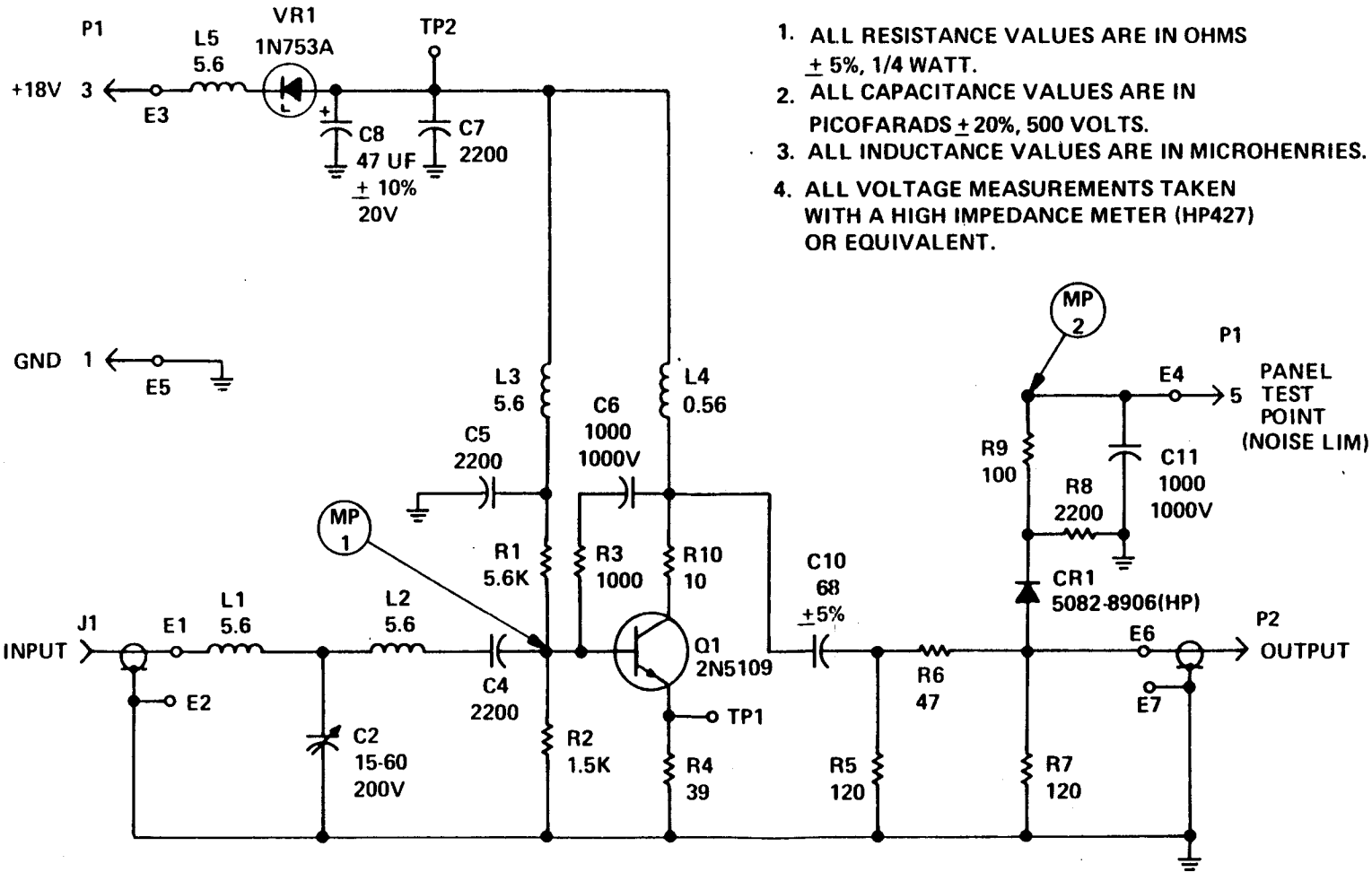
The secondary audio amplifier consists of a common-emitter amplifier stage, a phase splitter, a push-pull output stage and an output transformer. The input audio signal is coupled through R25 and C13 to the base of common-emitter amplifier stage Q7. Degenerative feedback from the collector of Q9 is also coupled to the base of Q7 via C14 and R26. The signal is coupled from the collector of Q7 through C19 to the base of phase splitter stage Q8. High frequencies are attenuated through the action of C20 and R37. Q8 provides signals of equal magnitude and opposite polarity to the push-pull output stage consisting of Q9 and Q10. The push-pull output stage drives the output transformer T2. The voltage across the primary of T2 is limited to a maximum of approximately 43 volts peak-to-peak by the action of zener diodes VR3 and VR4.

Surge protectors are provided to protect the audio amplifier output circuits from $\pm$ 1000 volts peak input pulses applied to each audio output. Protection for the main audio amplifier output is provided by surge protectors E1 and E2. These are mounted on terminal board TB1 adjacent to the rear apron connector J2. Protection for the secondary audio amplifier is provided by E8 mounted on the back of the receiver front panel PHONE OUTPUT jack.

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 WATT.
2. ALL CAPACITANCE VALUES ARE IN PICOFARADS ± 20%, 500 VOLTS.
3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH IMPEDANCE METER (HP427) OR EQUIVALENT.



MEASUREMENT/TEST POINT VOLTAGES

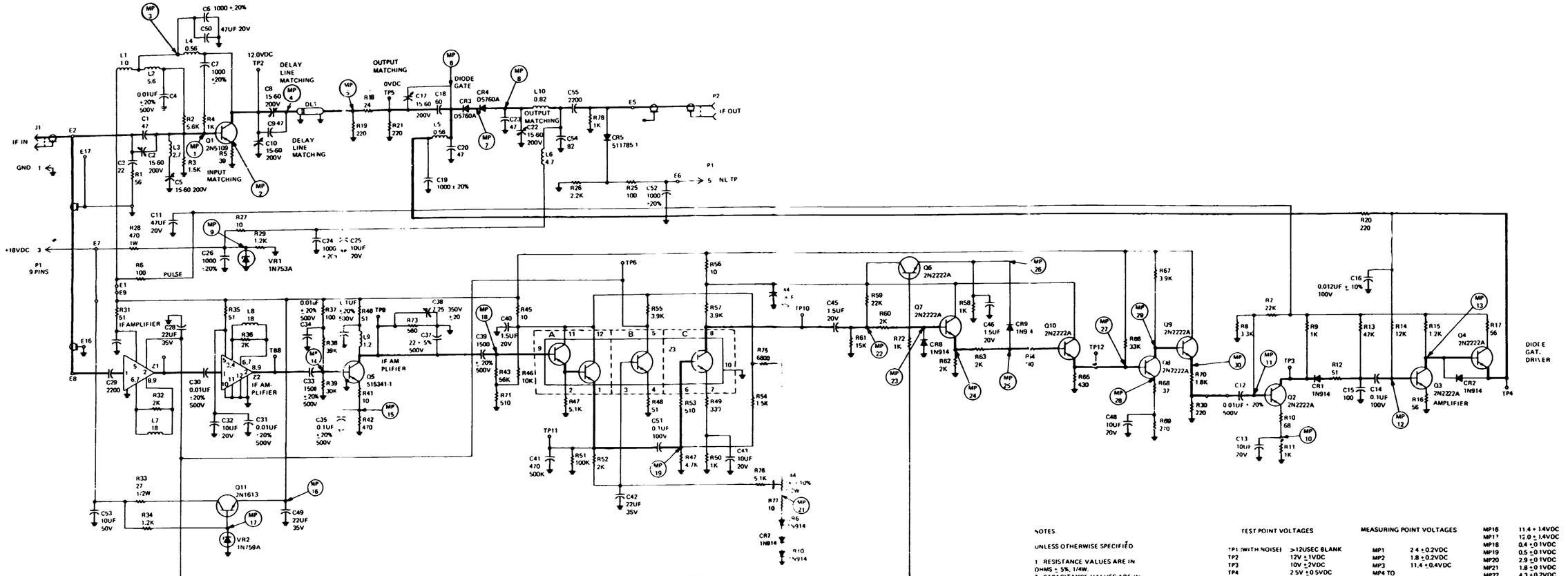
MP1	2 ±0.5VDC
MP2	0.46 ±0.1VDC
TP1	1.3 ±0.5VDC
TP2	11.5 ±1VDC

Figure 11-27. Buffer Amplifier A5

BUFFER AMPLIFIER A5

The function of the buffer amplifier is to provide a 50-ohm source impedance for the crystal filter and approximately a 50-ohm load to the mixer/multiplier module. The operating frequency is 20.6 MHz. The amplifier gain is 0 ± 1 dB and its 3-dB bandwidth is about 4 MHz. The tunable capacitance (C2) is adjusted for maximum gain at 20.6 MHz when J1 is fed from a 50-ohm generator and P2 is loaded with 50 ohms. The +18 V d.c. supplied to the module is regulated to about 12 V d.c. by VR1, a 6.2 volt zener diode. L5 prevents RF from leaving the module on the 18 V d.c. line and C7 and C8 provide a low a.c. impedance to keep the signal off the 12 V d.c. line.

L1, L2, and C2 are the input matching network. R1 and R2 bias Q1 so that its collector current is about 35 mA. L3 and C5 prevent any residual RF that may be on the 12 V d.c. line from appearing at the base of Q1. Both R4 and the series combination of R3 and C6 provide degenerative feedback for the amplifier, making it stable, and allowing interchangeability of transistors without gain change. L4 is the collector load. C10 accomplishes impedance stepdown from the collector impedance to the 50-ohm impedance of the 7.5 dB pad (R5, R6, and R7). R10 suppresses any tendency toward high frequency oscillations. When the signal at the output (P2) is large enough (greater than 0.5 V rms), CR1 rectifies a portion of the signal and C11 filters it to give a d.c. indication on the condition of the module at the NOISE LIM test point at the front panel of the receiver.



NOTES

UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ± 10%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES ± 10%.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPED ANCE METER (HP427 OR EQUIVALENT)

TEST POINT VOLTAGES

TP1 (WITH NOISE)	>12USEC BLANK
TP2	12V ±1VDC
TP3	10V ±2VDC
TP4	2.5V ±0.5VDC
TP5	0
TP6	1.5V ±0.5VDC
TP7	2V ±0.5VDC
TP8	1V ±0.2VDC
TP9	10V ±2VDC
TP10	11V ±1VDC
TP11	5V ±0.2VDC
TP12	1V ±0.2VDC

MEASURING POINT VOLTAGES

MP1	2.4 ±0.2VDC
MP2	1.8 ±0.2VDC
MP3	11.4 ±0.4VDC
MP4 TO MP5	1.9 ±0.5 OHMS
MP6	4.25 ±0.75VDC
MP7	5.25 ±0.75VDC
MP8	6.25 ±0.75 VDC
MP9	6.0 ±0.2VDC
MP10	0.75 ±0.25VDC
MP11	1.3 ±0.3VDC
MP12	1.4 ±0.2VDC
MP13	0.8 TO 2.5VDC
MP14	3.8 ±0.2VDC
MP15	3.2 ±0.2VDC
MP16	11.4 ± 1.4VDC
MP17	12.0 ± 1.4VDC
MP18	0.4 ±0.1VDC
MP19	0.5 ±0.1VDC
MP20	2.9 ±0.1VDC
MP21	1.8 ±0.1VDC
MP22	4.3 ±0.2VDC
MP23	4.2 ±0.2VDC
MP24	4.0 ±0.5VDC
MP25	0.5 ± 0.0VDC
MP26	0.5 TO 4.0VDC
MP27	1.5 ±0.2VDC
MP28	0.9 ±0.1VDC
MP29	1.0 ±0.2VDC
MP30	0.5 ±0.2VDC
E2	5 TO 10mV
E7	18.0 ±0.5VDC

Figure 11-28. Electrical Noise Limiter A5

ELECTRICAL NOISE LIMITER A5

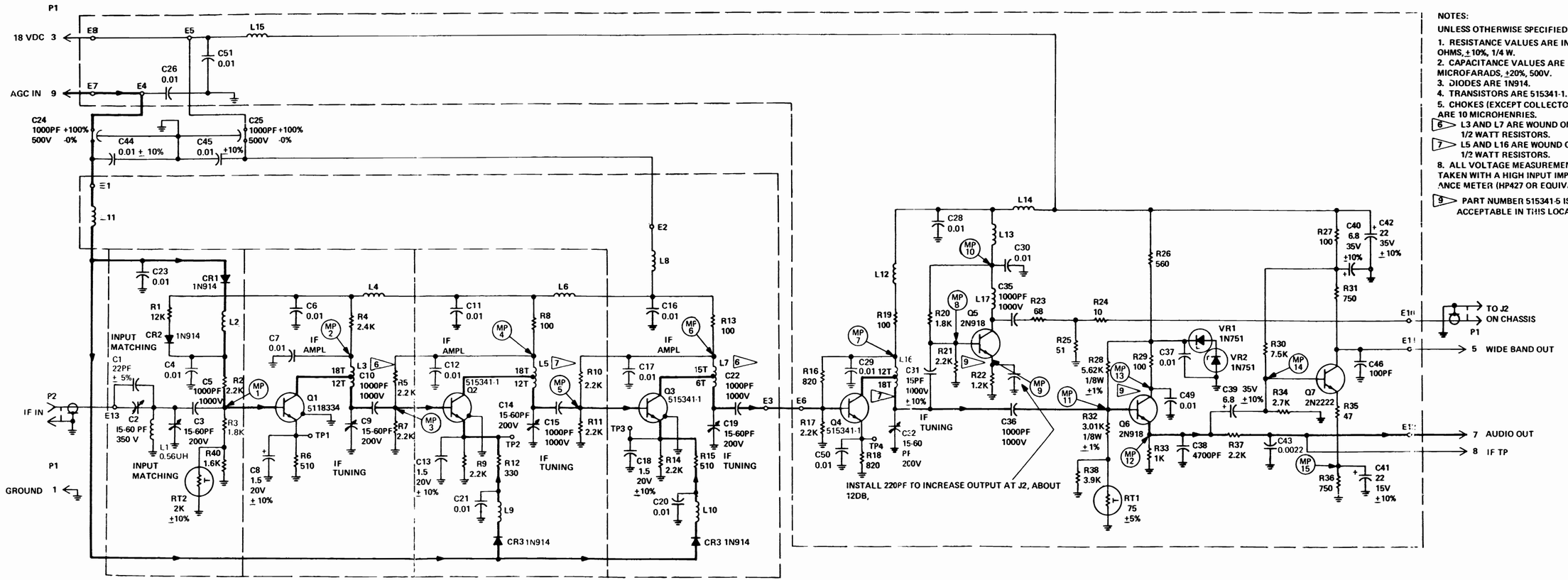
The signal applied to noise limiter module input J1 flows through an amplifier, a 0.2-μs delay line, and a gating circuit to output P2 with unity gain. The same signal applied to the input also flows into a circuit which establishes a d.c. voltage directly proportional to the amplitude of the intermediate frequency signal. If a pulse of noise occurs which is from 20 to 30 dB higher than the signal voltage, the gate is closed and the output signal is momentarily cut off. A pulse stretching effect occurs in this second loop so that the output signal is gated off for a slightly longer time than that occupied by the noise pulse. These signal blank out periods are of such short duration that they cause no adverse effect on the audio signal at the receiver output.

The IF input of J1 is applied through an impedance matching network to the base of amplifier stage Q1. C2 and C5 are adjustable to obtain the best impedance match between the 50-ohm input J1 and the amplifier input. Amplifier Q1 boosts the signal level to compensate for signal degradation in delay line DL1 and following circuitry, thereby maintaining a net gain of 1 for the module. The signal is coupled from the collector of Q1 to the 0.2-μs delay line by C8 and C9. C8 and C10 are adjustable for an impedance match with the 50-ohm delay line input impedance. The output of DL1 is applied through a pin diode gate made up of CR3 and CR4 to module output connector P2. Normally, with no noise pulse present, CR3 and CR4 are forward biased presenting minimum impedance to signal flow to the module output connector P2.

The signal input at J1 is also applied to the gate control loop consisting of an IF amplifier, a detector, an agc feedback loop, a pulse amplifier, and a gate driver. Z1 and Z2 are integrated-circuit IF amplifiers. These amplifiers are broadband tuned as a result of discrete components external to the integrated circuits. Z1 receives an agc input at pin 2. Amplifier stage Q5 is tuned to the IF of 20.6 MHz by C38. The collector of Q5 is coupled to the input of integrated circuit Z3 at pin 9. Z3 contains a detector, an agc output, and a pulse amplifier. The agc level is adjusted by R44 and is fed back from Z3 pin 5 to Z1 pin 2. Temperature compensation is provided by CR6, CR7, and CR10.

The detected signal, along with any noise that might be present, is clamped above ground level through the action of CR8 and applied to the base of emitter follower Q7. The signal from the emitter of Q7 is then applied through R63 and R64 to the base of Q10. However, the signal at the junction of R63 and R64 is clamped below a variable voltage level dependent upon the average peak signal. The agc from Z3 pin 5 is also applied through R72 to the base of Q6 allowing C46 to charge up to a value representing the level positive excursion of the detected signal. The base of Q10 is clamped below that level through the action of CR9. When a noise spike occurs extending more positive then the average signal level, it passes through emitter follower Q10 and is amplified by pulse amplifier Q8 and Q9. The noise spike is then coupled through C12 to the base of Q2. The action of CR1, R12, C15, R13, and C14 stretches and couples the pulse to the base of Q3. Q3 cuts off for the duration of the pulse and Q4 goes into conduction, applying +12 volts to the cathode of pin diode gate CR3 via R20 and L5. CR3 and CR4 are then back-biased for a time slightly longer than the duration of the noise pulse (+6 volts is applied to the anode of CR4 via R27 and L6) and the noise pulse is effectively removed from the receiver output.

At the end of the noise blanking pulse, Q3 resumes normal conduction and Q4 is cut off. This effectively connects the cathode of pin diode gate CR3 to ground via L5, R20, CR2, Q3, and R16, thus supplying forward bias to the pin diodes opening the gate. The +18 volts on P1-3 is decreased to +6 volts and +12 volts for use within the noise limiter module. The +6 volts is supplied by the regulator circuit consisting of R28, VR1, C26, and R29, and +12 volts is supplied by the regulator circuit consisting of Q11, R33, R34, VR2, and C49. The module signal output is also detected by diode CR5 and applied to receiver front panel major test point NOISE LIM.



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±10%, 1/4 W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 515341-1.
5. CHOKES (EXCEPT COLLECTOR COILS) ARE 10 MICROHENRIES.

6 > L3 AND L7 ARE WOUND ON 620 OHM, 1/2 WATT RESISTORS.

7 > L5 AND L16 ARE WOUND ON 300K, 1/2 WATT RESISTORS.

8. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

9 > PART NUMBER 515341-5 IS ACCEPTABLE IN THIS LOCATION

TEST POINT VOLTAGES

TP1	2V ±0.5VDC
TP2	8V ±1VDC
TP3	8V ±1VDC
TP4	11V ±1VDC

MEASURING POINT VOLTAGES

MP1	2.75 ±0.25VDC
MP2	7.75 ±1.25VDC
MP3	8 ±1VDC
MP4	17 ±1VDC
MP5	8.5 ±1VDC
MP6	17 ±1VDC
MP7	15.5 ±1VDC
MP8	9.5 ±1VDC
MP9	8.5 ±1VDC
MP10	17.5 ±1VDC
MP11	3 ±0.5VDC
MP12	3 ±0.5VDC
MP13	9 ±1VDC
MP14	2 ±0.5VDC
MP15	1.5 ±0.5VDC
E2	18 ±0.5VDC
E6	11.25 ±1.25VDC
E11	11 ±1.5VDC
E12	3 ±0.5VDC

EQUIPMENT MODIFICATIONS

ECP 474 CHANGE
R3 FROM 2K TO 1.8K

ECP 536 CHANGE
C1 FROM 47pF TO 22pF
L1 FROM 0.47 H TO 0.56 H

ECP 568 CHANGE
C43 FROM .022 TO .0022

Figure 11-29. IF Amplifier and Detector A6

IF AMPLIFIER AND DETECTOR A6

The intermediate frequency amplifier consists of four cascaded common-emitter IF stages followed by a detector and a low-gain IF stage base driven by the fourth stage. The low gain IF stage Q5 is an isolation amplifier whose output is coupled through J2 to the 50-ohm output connector J10 on the receiver rear panel. Detector Q6 is biased to perform the detection function and provide an audio signal to the audio preamplifier agc/squelch module. The detector also drives wideband audio amplifier Q7 and associated circuit components. The first amplifier, Q1, is a common-emitter configuration driven by the input IF signal through a matching network consisting of C1, C2, C3, and L1. C2 and C3 are provided to adjust the input impedance of the first stage to 50 ohms. The gain of this stage is controlled in a forward agc mode through the base bias resistor R2. The agc voltage controls the base drive through L2 and CR1. R1 and CR2 provide a fixed current to the bias network to maintain a high gain in the transistor in the absence of agc voltage.

The second and third stages, Q2 and Q3, are identical common-emitter stages driven in cascade by the first stage. The gain of each stage is controlled in a reverse agc mode by the injection of an agc voltage to the emitters of the transistors. The agc voltage is applied to the emitter of Q2 through R12, L9, and CR3. The agc voltage is applied to the emitter of Q3 through R15, L10, and CR4. The fourth stage, Q4, is a common-emitter stage, having no automatic gain control, which drives both the detector and the 50-ohm output isolation amplifier. Isolation amplifier Q5 is a low gain common-emitter stage which drives the 50-ohm output connector through a matching "T" network composed of R23, R24, and R25. The detector stage, Q6, uses its base-emitter junction to rectify the IF signal. C38, C43, and R37 filter out IF signal components and apply the filtered audio to the output connector. C39 couples the audio signal to the wideband audio amplifier which uses Q7 in a common-emitter output stage. The wideband amplifier has a 25-kHz passband.

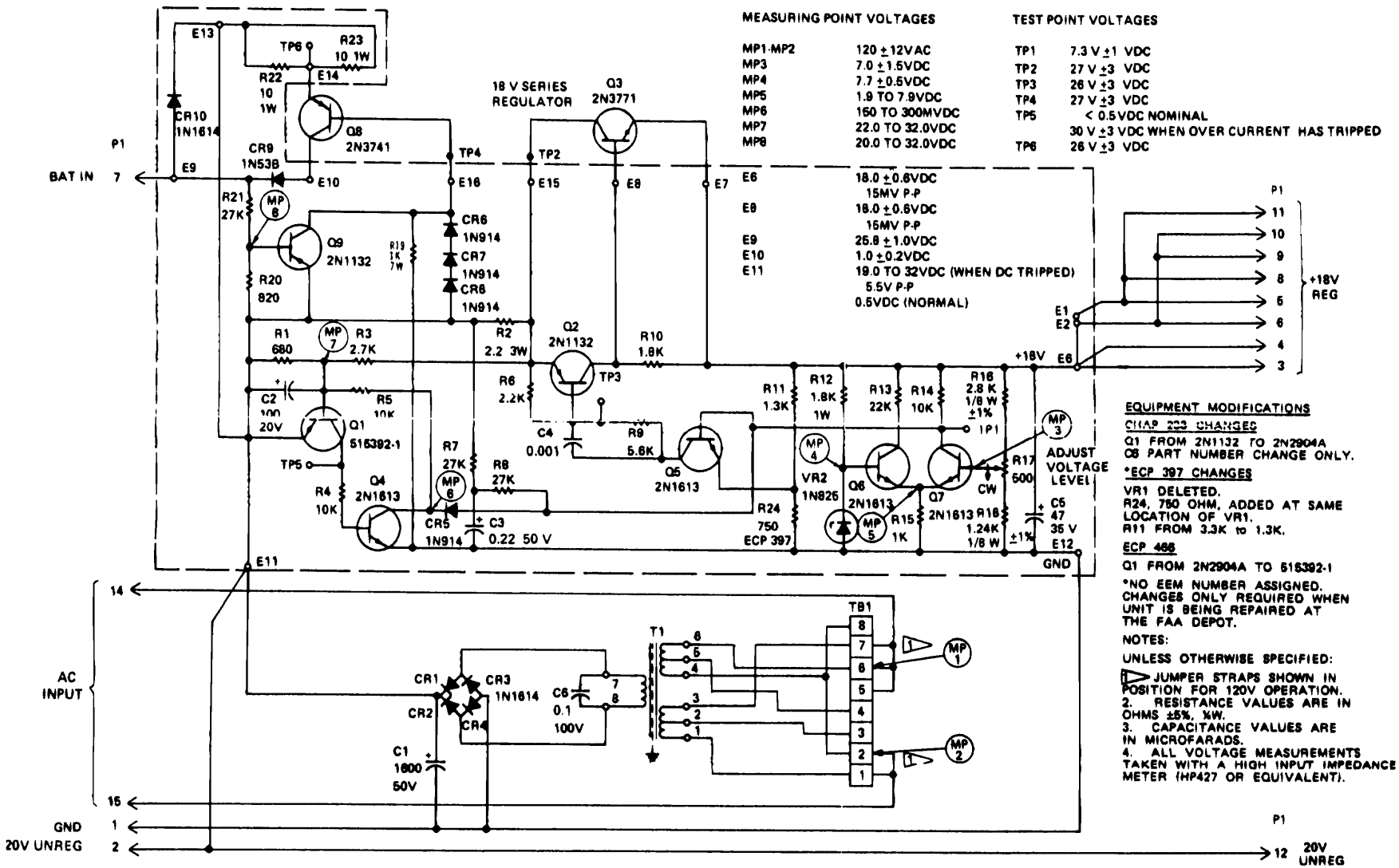


Figure 11-30. Power Supply PS1

POWER SUPPLY PS1

The power supply is designed to operate from either a.c. or d.c. voltages. Jumpers are provided on terminal board TB1 to allow the power supply to operate at any one of the following primary voltages: 105, 120, 210, or 240 V a.c. ±10%. Usable frquency for primary a.c. power is 47 to 420 Hz. In case of a.c. power failure, primary power is supplied to the power supply from an external battery (when available). With the supply operating on a.c., voltage is applied to the primary of transformer T1 via TB1. The secondary of T1 connects to the bridge rectifier (CR1, CR2, CR3, and CR4). An unregulated output of approximately +30 volts is provided at the junction of CR1 and CR2 for use as crystal oven heater power for the oscillator module. This same output flows through R2 and is reduced to +18 volts ±0.5% by series-pass transistor Q3 to supply the regulated voltage required by the receiver.

Q6 and Q7 form a differential amplifier driving emitter resistor R15. The regulator output voltage is applied across voltage divider R16, R17, and R18. A sample of the output from R17 is applied to the base of Q7. The level of the output voltage may be set by adjusting R17. A reference voltage established by zener diode VR2 is applied to the base of Q6 which is the other differential amplifier input. The output of the collector of Q7 is directly coupled to the base of common-emitter amplifier stage Q5. The voltage at the emitter of Q5 is held at a constant value by R11 and R24. A second input to the base of Q5 is applied by the short-circuit protection circuit via CR5. When the supply is operating with no short circuit present, CR5 will be back biased, effectively disconnecting the short-circuit protection input from the base of Q5.

The output of amplifier stage Q5, at the junction of resistors R9 and R6, is direct coupled to the base of common-emitter amplifier stage Q2. The collector of Q2 is direct coupled to the base of series-pass transistor Q3. The amplitude and polarity of this signal is such that a regulated +18 volts is produced at the emitter of Q3. Special circuitry is necessary to facilitate the start-up of the regulator. When power is turned on, capacitor C3 is charged up through resistor R7. The junction of R7 and C3 is connected to the base of Q5 through R8. When the voltage applied to the base of Q5 becomes positive enough, it overcomes the positive emitter voltage established by R24, and Q5 begins to conduct through R9 and R6. Current through R6 causes Q2 to start conduction which, in turn, allows conduction through series pass transistor Q3. When sufficient current flows on the regulated +18 volt line, the normal regulator takes control and the output is maintained at +18 volts. The relatively large value of R8 sufficiently isolates the start-up circuit to allow Q5 to be controlled by differential amplifier Q6 and Q7 when these transistors receive adequate operating voltage.

The battery is charged by a 300 mA nominal constant-current source when the power supply is operating from a.c. The battery charge path is from the junction of CR1 and CR2 through R22 and R23, Q8, and CR9 to the battery bus. Q8 is the series-pass transistor in the charging circuit. A constant voltage is applied to the base of Q8. This constant voltage is established by the voltage dropped across forward-biased diode string CR6, CR7, and CR8 (approximately 2 volts is dropped across the diodes). The charging current through emitter resistors R22 and R23 determines the emitter-base bias in Q8 and maintains the 300 mA nominal trickle charge rate. Reverse battery polarity protection is provided by stage Q9. With proper battery polarity, Q9 is in the cut-off region. However, if the battery is connected backward, a negative voltage will be applied to the base of Q9 causing heavy conduction. This eliminates the 2 volts dropped across diodes CR6, CR7, and CR8, and applies a back emitter-base bias to series pass transistor Q8. Transistor Q8 is then driven into the cut-off region and the battery charge path is interrupted.

When a short circuit occurs, a heavy current tends to flow through R2 and the series pass transistor Q3. An increase in current flow also occurs in R1 and R3. A forward emitter-base bias for Q1 is developed across R1 and Q1 starts to conduct. This applies forward bias to the emitter-base junction of Q4 which begins to conduct through R5. The collector of Q4 is connected through CR5 to the base of Q5 driving it into cutoff. Q5 is an amplifier stage in the regulator circuitry discussed in a previous paragraph. As a result of the regulator action, series pass transistor Q3 is cut off, removing the power supply regulated output from the receiver modules. C2 prevents extraneous activation of the short-circuit protection as a result of momentary changes in load. The short-circuit protection circuit is latching and once triggered by an overload, the regulated output is not reapplied until the receiver is turned off and then on again. Once an overload has occurred, current flows through Q4, R5, and R1. Current through R1 holds Q1 conducting which, in turn, maintains a forward bias on Q4 and holds it in conduction until primary power has been removed from the power supply.

In case of a.c. power failure, primary power will be supplied from the battery (when available). Current flow will be from the battery bus through isolation diode CR10, R2, and series pass transistor Q3 to all receiver modules requiring regulated voltage. The same regulator circuit is used regardless of whether using an a.c. or a d.c. power source.

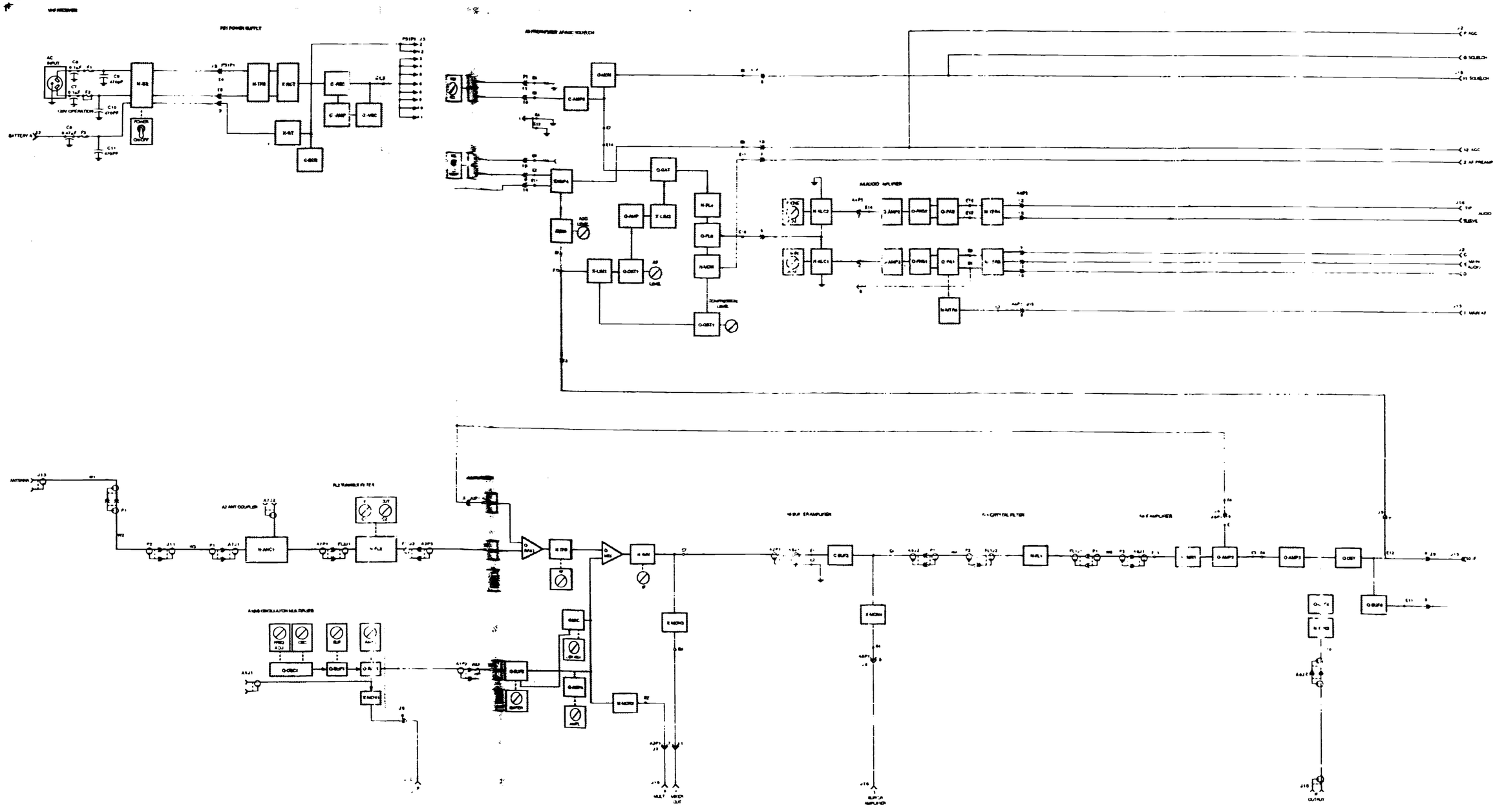


Figure 11-31. VHF Receiver Functional Blocked Diagram

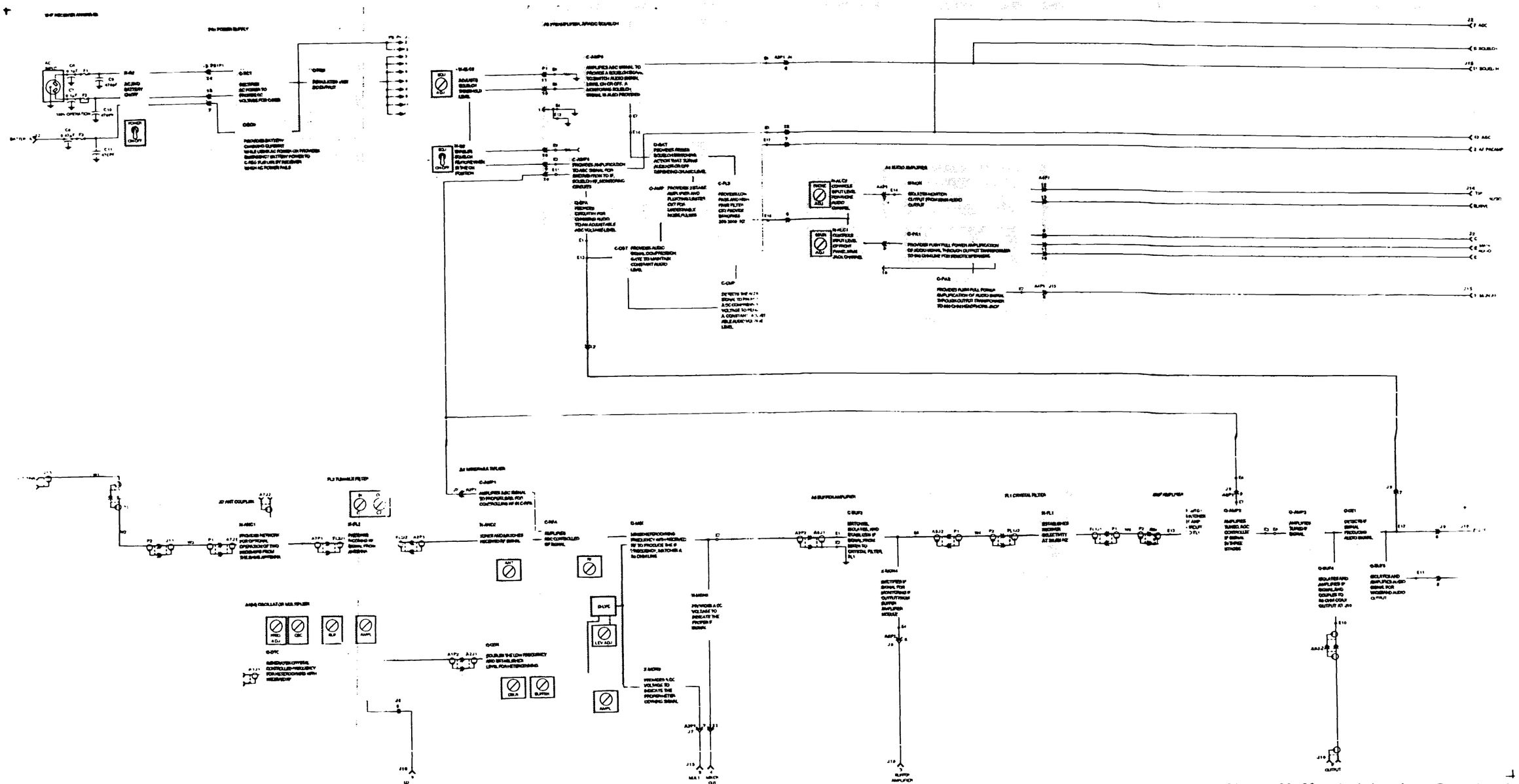
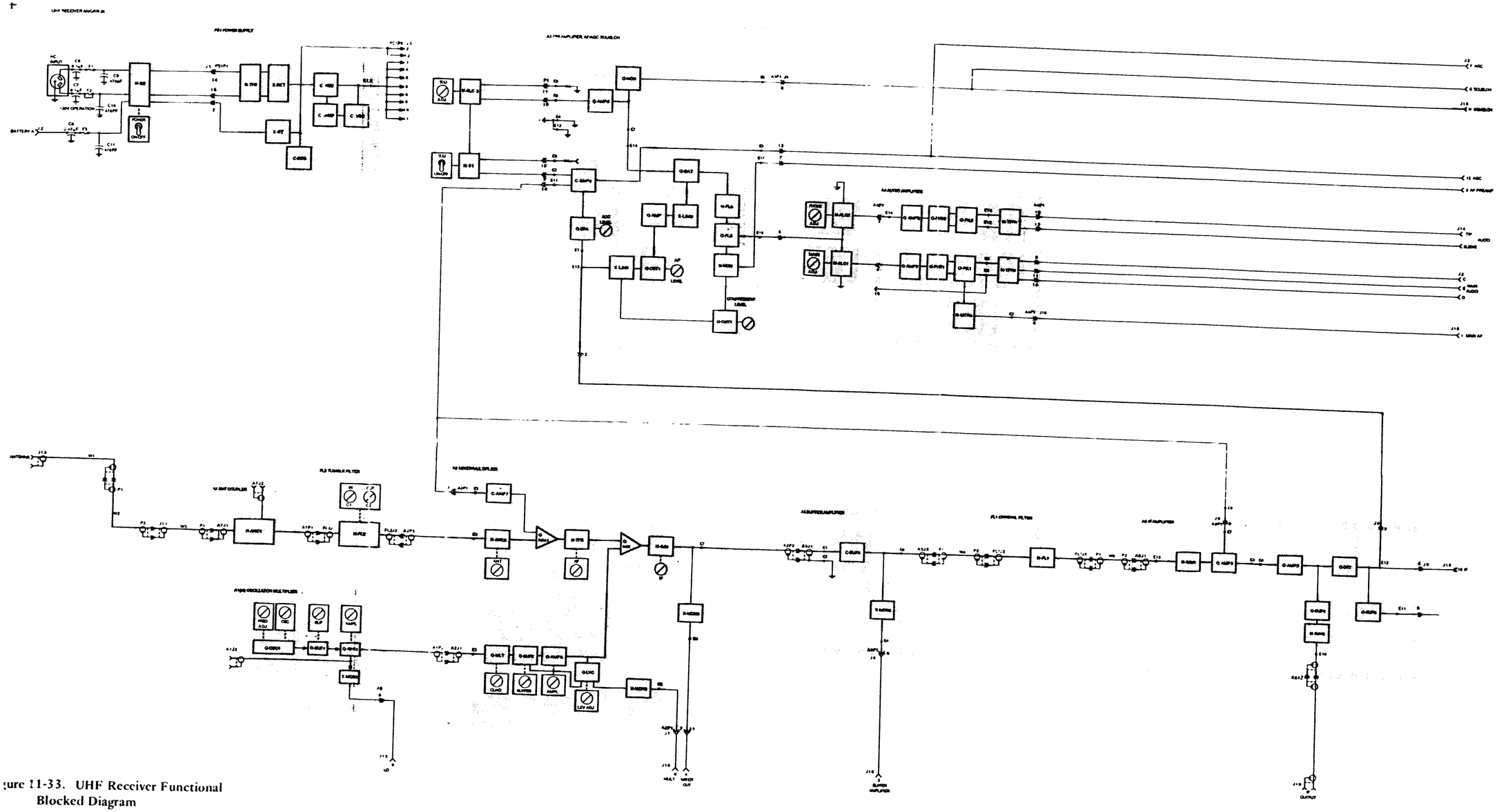


Figure 11-32. VHF Receiver Functional Block Diagram Text



ure 11-33. UHF Receiver Functional Blocked Diagram

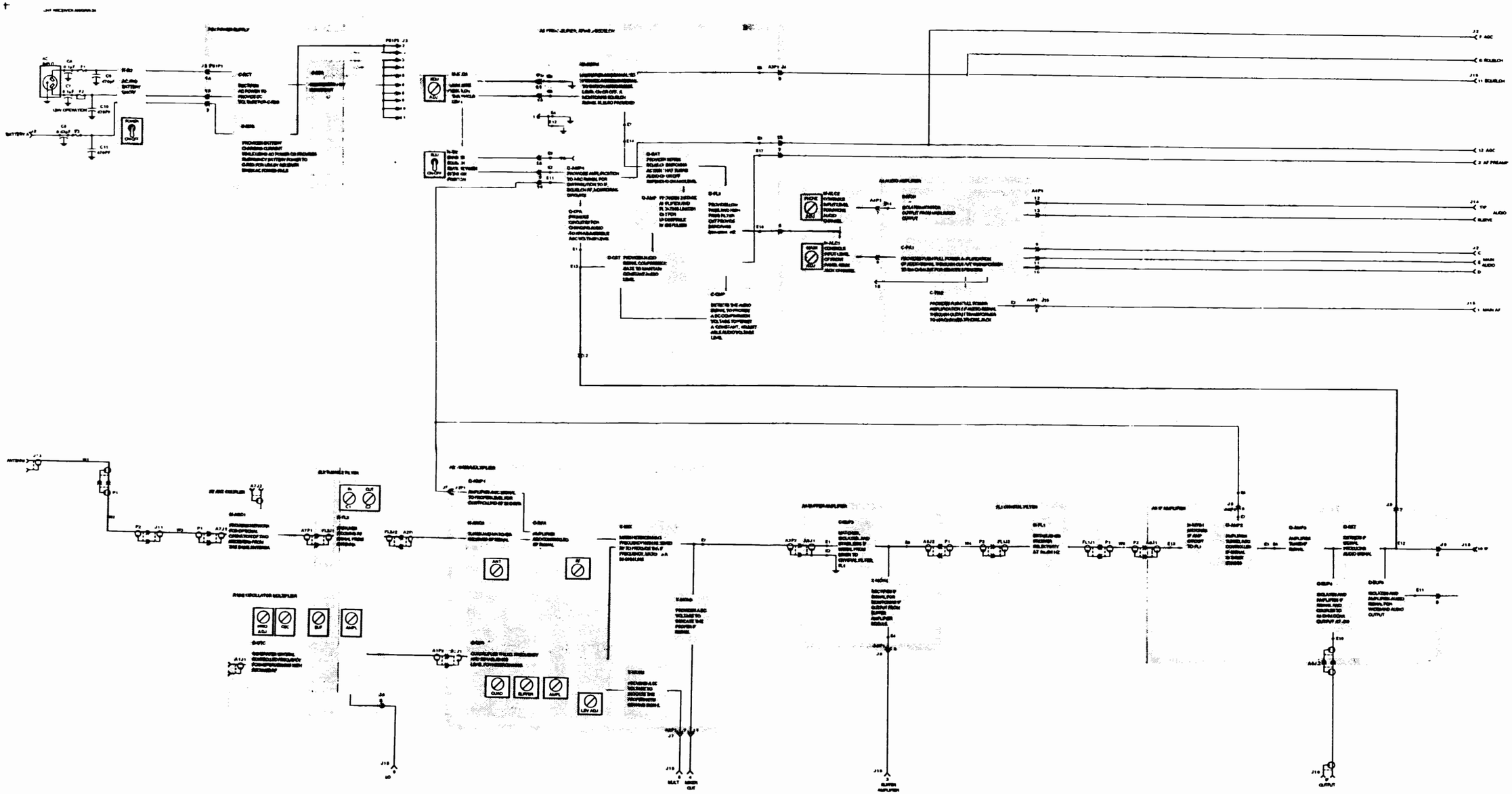


Figure 11-34. UHF Receiver Functional Blocked Diagram Text

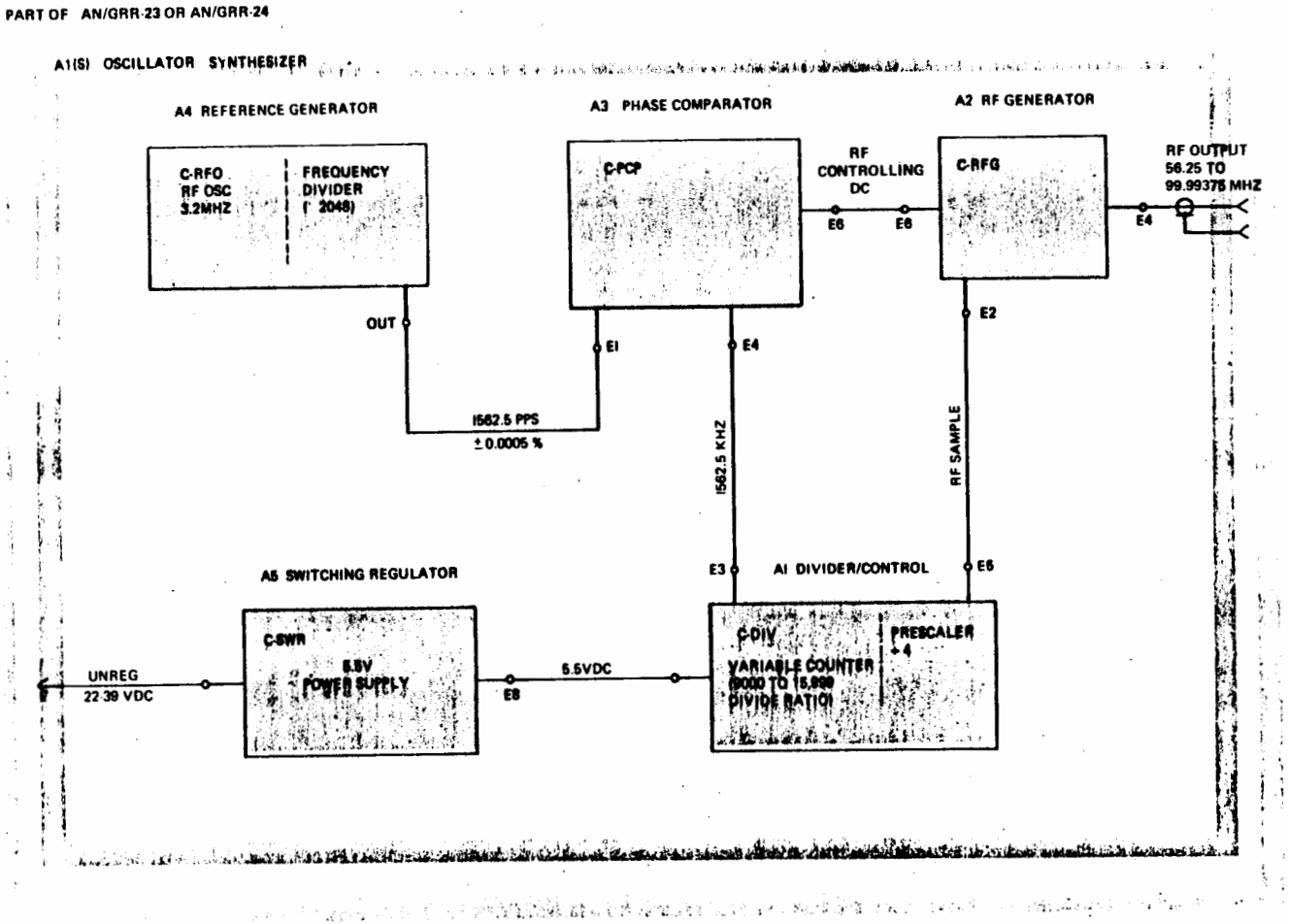


Figure 11-35. Oscillator-Synthesizer Functional Blocked Diagram

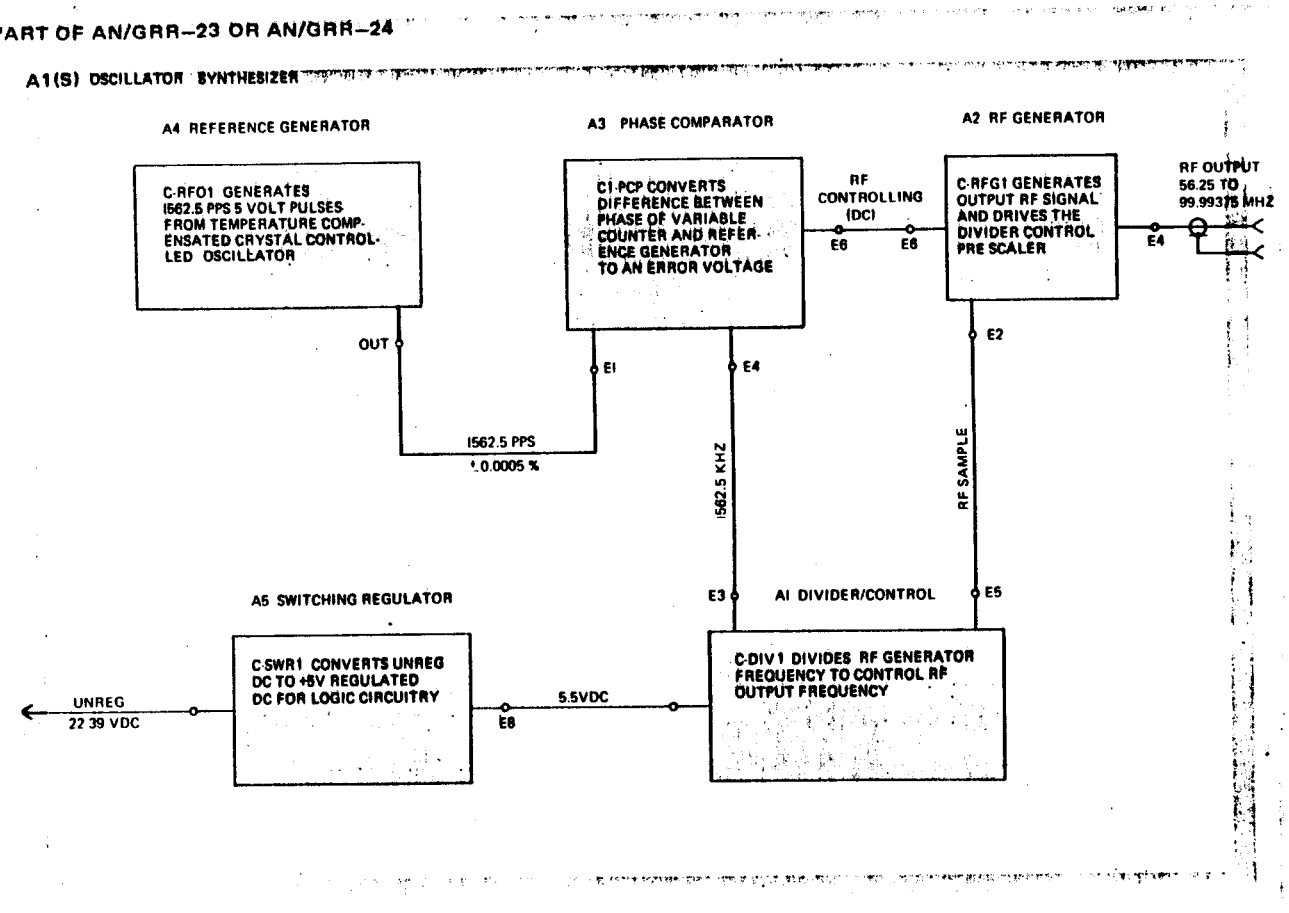


Figure 11-36. Oscillator-Synthesizer Functional Blocked Diagram Text

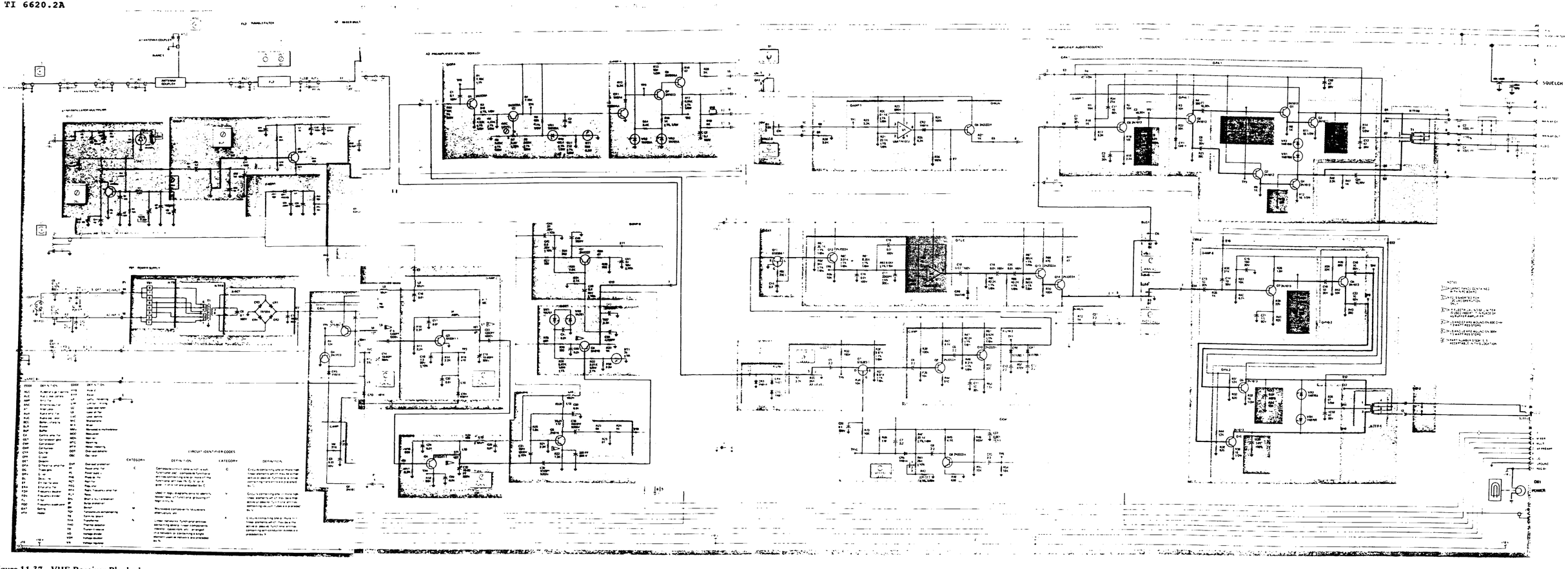


Figure 11-37. VHF Receiver Blocked Schematic Diagram

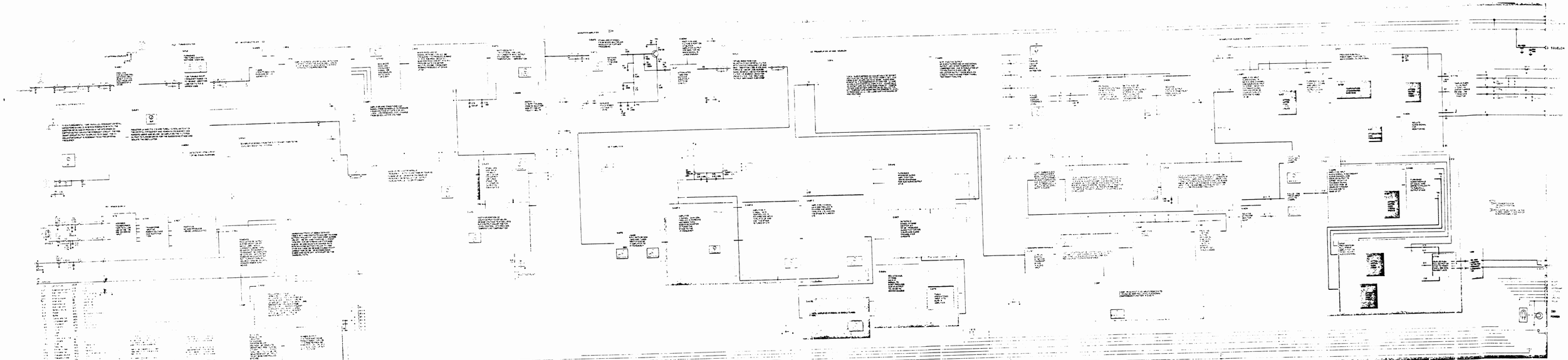


Figure 1-38. VHF Receiver Blocked Schematic Text

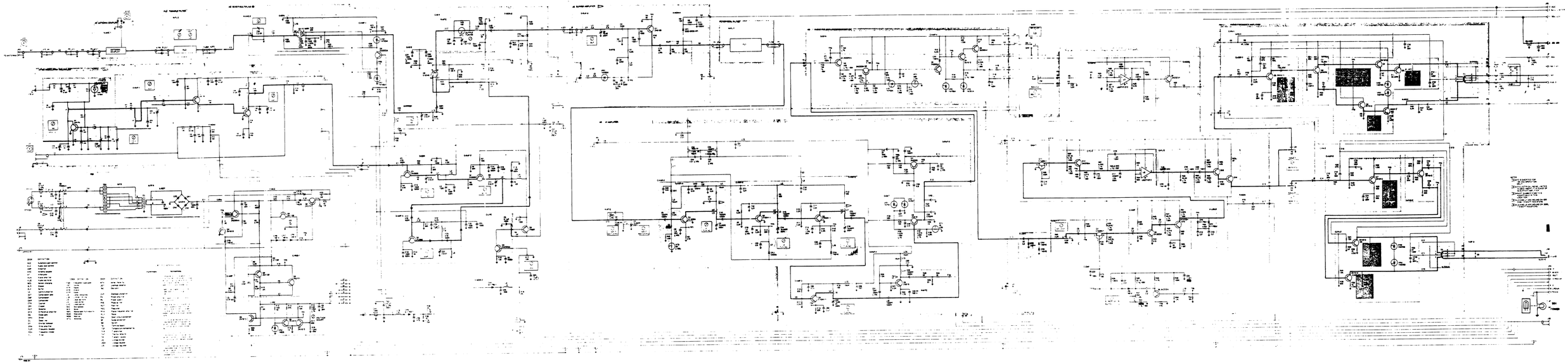


Figure 11-39. UHF Receiver Blocked Schematic Diagram

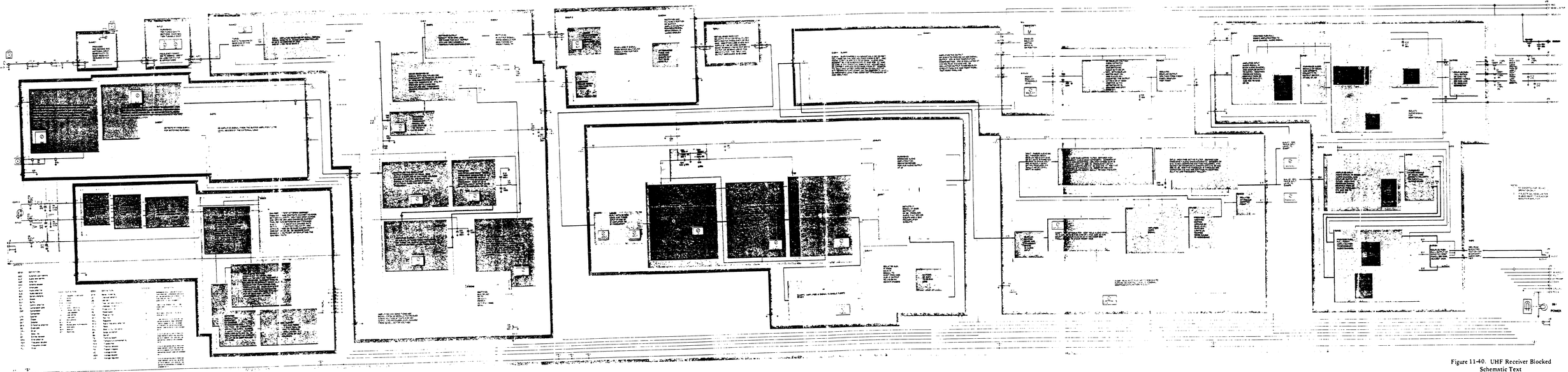


Figure 11-40. UHF Receiver Blocked Schematic Text

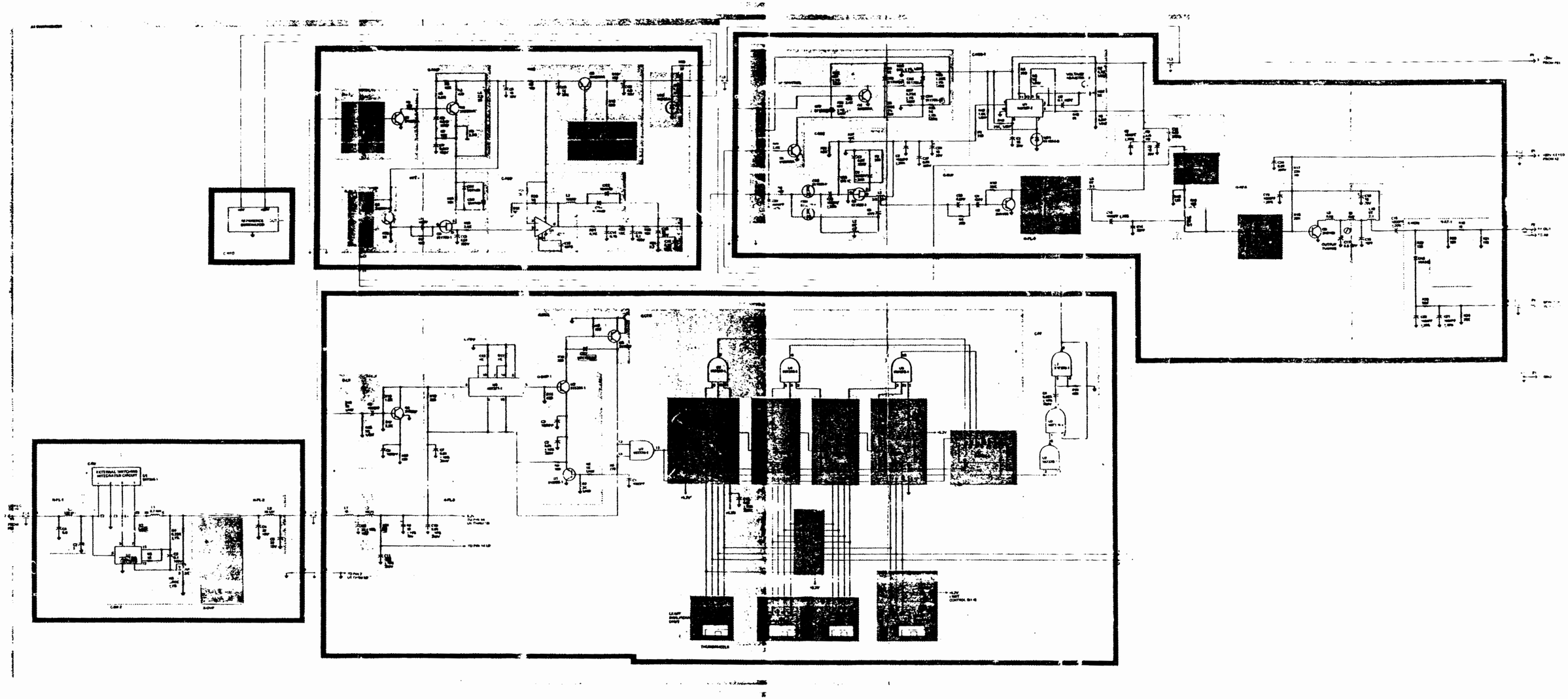


Figure 11-41. Oscillator-Synthesizer Blocked Schematic Diagram

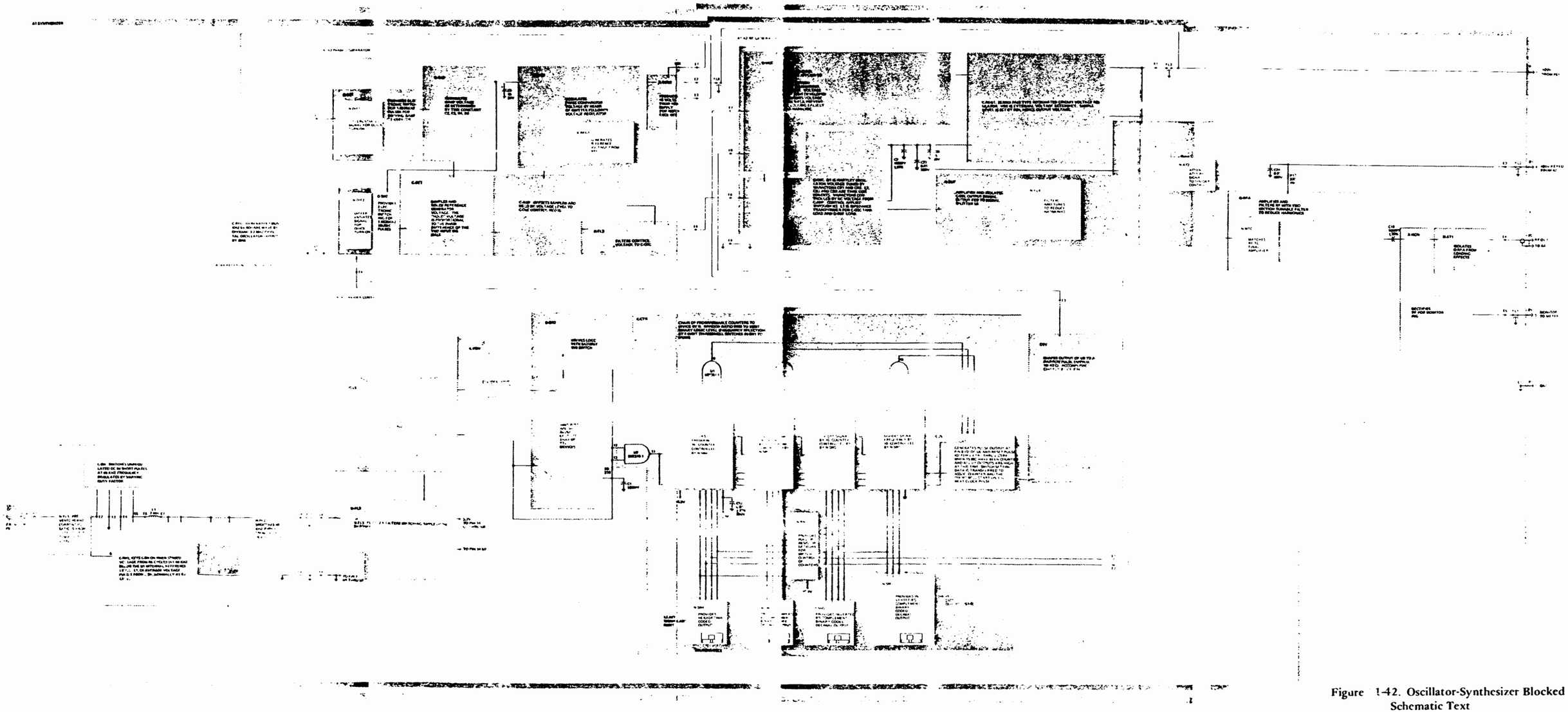


Figure 1-42. Oscillator-Synthesizer Blocked Schematic Text