## SECTION 20

## TIME-DELAY CIRCUITS

## PART A. ELECTRON-TUBE CIRCUITS

### PHANTASTRON CIRCUITS.

The phantastron-type circuit is considered to be a relaxation oscillator similar to the multivibrator in operation. Whereas the multivibrator derives its timing waveform from an R-C circuit, the phantastron uses a basic Miller-type sweep generator to generate a linear timing waveform, rather than the exponential waveform developed by the R-C circuit of the multivibrator. Thus, the output waveform is a linear function of the input (control) voltage, and the timing stability is improved.

The phantastron is usually triggered on by the leading edge of a gating or trigger pulse applied to the suppressor grid (or to the plate) of a pentode, and is shut off by an internally generated waveform. It can also be controlled by the trailing edge of the gate or trigger. It is basically a single pentode-type tube (pentagrid tubes are also used), with two or three diodes arranged to control linearity, turn-on or turn-off time, and operating level. Two types of phantastron circuits are used—the screen-coupled type and the cathode-coupled type. The screen-coupled circuit uses an internally generated waveform, generated in the screen circuit to control the suppressor electrode after the action is initiated by an input trigger. The cathode-coupled circuit utilizes an internally generated waveform developed across a resistor in the cathode circuit to control operation. Both circuits are classed as the slow-recovery type and use the basic Miller plate-to-grid feedback to provide reasonably fast turn-on and turn-off time. The fast-recovery type circuit uses a separate cathode follower to help speed up operation and provide a shorter recovery time.

The relationship between the screen-coupled and cathode-coupled circuits is analogous to that of the plate-to-grid and cathode-coupled multivibrators. Although the screen-coupled phanastron is considered to have the best timing accuracy, the cathode-coupled circuit has other advantages. For example, it does not require a negative supply and can provide both positive and negative outputs, and it is claimed that for **short** ranges the linearity of the time modulation is actually better.

### BASIC PHANTASTRON CIRCUITS.

### APPLICATION.

The phantastron circuit is used to generate a rectangular waveform, or linear sweep, whose duration is almost directly proportional to a control voltage. Because of its extreme linearity and accuracy, this waveform is used as a delayed timing pulse, usually in radar or display equipment. It is also used to produce time-delayed trigger pulses for synchronizing purposes and movable marker signals for display. For example, it is used as a time-modulated pulse, to indicate antenna position at any instant of rotation, or as a range strobe or delay marker.

### CHARACTERISTICS.

Operation is similar to the operation of a multivibrator.

Pulse width or delay varies linearly with the applied control voltage.

Requires an electron tube of the pentode or pentagrid type.

Output can be taken from the cathode, screen, or plate, and may be either positive or negative, as selected.

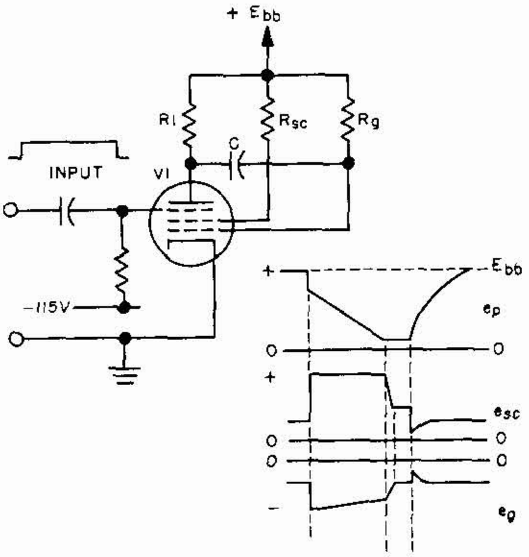
Provides either a low-impedance or high-impedance output, determined by output connections.

May be self-controlled or externally controlled.

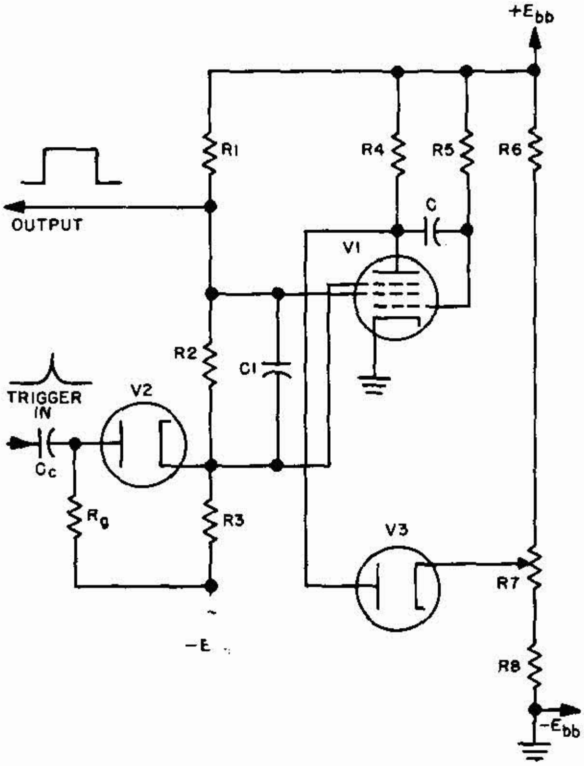
### CIRCUIT ANALYSIS.

**General.** The operation of the phantastron circuit is based on the use of a Miller-type linear sweep generator which uses a suppressor-gated pentode. In the Miller linear sweep generator, the suppressor grid is normally biased (negative) to prevent plate current flow, while the screen conducts heavily. The grid is returned to B+ through a resistor so that it is effectively at zero potential, and the cathode is grounded. When a positive gate is applied to the suppressor, plate current flows and produces a voltage drop across the plate load resistor. This negative-swinging plate voltage is fed back through a small capacitor to the grid, and quickly drives the grid negative; thus, it maintains the plate current at a small value, and also greatly reduces the screen current. Reduction of the heavy screen current produces a large positive swing on the screen, and the tube essentially remains in this condition, producing a positive screen gate. Meanwhile the plate current flows under control of the feedback voltage applied to the grid until no further feedback is produced. During this time the plate-current increase is linear, and the plate voltage continues to drop. (The normal discharge of C through $R_g$ would cause the current through the tube to increase in an exponential manner, thereby causing the plate voltage to drop exponentially. However, any exponential change is fed back to the grid 180 degrees out of phase with the normal discharge of C, thereby causing a linear increase in plate current.) At a point about 2 volts above ground, however, no further plate swing is possible, and the screen again conducts heavily, returning almost to the initial operating point. When the suppressor gate ends, the plate current is cut off, the screen returns to its initial operating point, and the cycle is ready to be resumed under control of the next gate. The following schematic shows the basic Miller circuit. Observe that the screen is not coupled, that a separate bias source is used for the suppressor, and that an external sweep gate is necessary. These are the main ways in which it differs from the phantastron.

From the circuit action described previously, it is clear that changing the applied plate voltage will determine the point, and the time, at which the plate voltage "bottoms" (with respect to the leading edge of the input waveform) and the screen resumes control. Changing the values of feedback capacitor C and grid resistor R will also determine the time of operation (by controlling the speed of the grid-plate feedback action). Both methods of controlling the time are used in phantastron circuits.



Miller Linear Sweep Generator

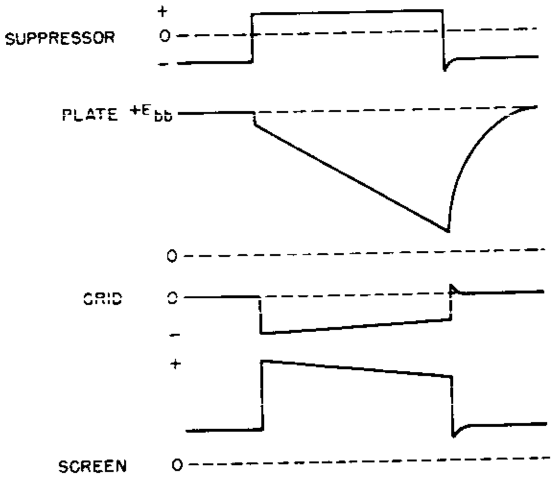


Basic Screen-Coupled Phantastron

**Circuit Operation.** As mentioned previously, there are two basic types of phantastron circuits in use – the screen-coupled and the cathode-coupled. The name is derived from the manner in which the gate for the suppressor is obtained. Recall that in the Miller circuit a positive gate is developed on the screen during operation; by coupling the screen to the suppressor, either directly or through a capacitor, this gate is used in the screen-coupled phantastron to control operation. A trigger pulse is needed only to start operation, because turn-off is automatic. By inserting a cathode resistor between the cathode and ground, a negative gate is developed and used to control the the cathode-coupled phantastron. Each of these circuits will be discussed more thoroughly in the following paragraphs.

**Screen-Coupled Circuit.** A typical monostable screen-coupled pentode circuit is shown in the accompanying figure. This circuit is started by a positive trigger applied to the suppressor grid, and at the end of operation it returns to the initial starting condition, ready to repeat the cycle of operation when the next trigger arrives. The output taken from the screen is a rectangular positive gate whose duration, or length, is controlled by R7. In the illustration, tube V1 is the basic phantastron, and diode V2 acts as a trigger injector and also as a disconnecting diode to effectively isolate the trigger circuit after the action is started. Diode V3 sets the maximum level of plate voltage as controlled by the position of R7, and, since the turn-off level is fixed, it effectively controls the time during which the circuit produces the linear gate or sweep. Operation occurs at the rate fixed by the discharge of C through R5. In some circuits R5 is made variable to set the maximum time delay, and R7 is provided as an external control to permit selection of the exact time duration required. Feedback capacitor C provides regenerative feedback from plate to grid, to allow quick response to any changes in the plate circuit. Capacitor C1 couples the positive gate from the screen to the suppressor, thereby holding the tube in a condition where plate current can flow.

Circuit operation can best be understood by referring to the waveforms developed in the tube elements shown in the following illustration, while reading the description of the circuit action. Three steps are involved in the circuit action--turn-on, linear sweep development, and turn-off. Before initiation of action, the circuit is resting with the plate current cut off, because a negative voltage is applied to the suppressor element through R3. Resistors R1, R2, and R3 form a combined suppressor and screen grid voltage divider connected between B plus and C minus. The values are such that the screen is positive and the suppressor is sufficiently negative to cut off plate current. Since they are directly connected, both elements are d-c coupled; also, through capacitor C1 they are a-c coupled. Therefore, both d-c and a-c voltages appearing on one element also affect the other element. Since the cathode is grounded and the grid is connected through R5 to B+, the grid remains near zero bias. Thus, although the plate current is cut off, the screen current is heavy. When a positive trigger is applied to the plate of disconnecting diode V2 through coupling capacitor $C_c$, the diode conducts, and the positive trigger appears across R3 and is applied to the suppressor of V1. The trigger is large enough to overcome the fixed negative bias and drive the suppressor positive. Therefore,



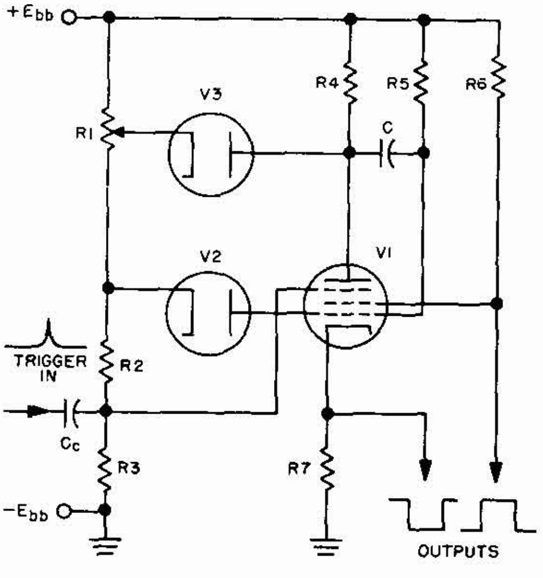
**Waveforms of Screen-Coupled Phantastron**

the plate current flows through R4. Since R4 is a relatively large-value resistor, the plate current quickly goes from zero to a low value, and simultaneously the negative swing produced across R4 is applied through C to the grid, driving it from zero to a negative value of only a few volts, but sufficiently negative to reduce the total cathode current. The grid is now in full control, and the reduction of screen current produces a large positive increase in screen voltage. Through C1 the positive-going screen voltage is fed back to the suppressor so that the action is regenerative; as a result, the tube is quickly triggered from the static condition to the operating condition, which produces a screen waveform with a sharp leading edge. The linear sweep development or timing cycle now begins, with the plate current of V1 increasing steadily. Since the grid is returned to B+, the grid voltage attempts to reach the zero bias level; however, it can change only slowly because the plate side of feedback capacitor C is steadily decreasing, so that any positive grid swing is immediately counteracted by a negative plate swing fed back to the grid. Therefore, capacitor C starts to discharge and electrons flow from the plate of V1, discharging C through R5. Thus C discharges at a rate determined by the time constant of C and R5 (in some circuits R5 is made variable to permit changing the rate of operation). In discharging, the grid side of capacitor C gradually becomes more positive, causing an increased current flow through R4 and producing a constant decrease in plate voltage. The positive increment on the grid is always slightly greater than the negative plate swing it produces; therefore, the grid potential gradually rises, and the plate potential gradually drops. When the plate reaches the point where a voltage change on the grid will produce no further plate-voltage change, the turn-off point is reached. Up to this time a positive gate has been produced in the screen circuit and coupled to the suppressor. A negative gate has been developed on the grid which is smaller in amplitude from the leading edge to the trailing edge by about a volt. (The amount is dependent upon the gain of the tube.)

Since the tube plate voltage is only a volt or so above zero and the plate current can no longer increase, but the grid voltage is still rising toward zero, causing an increase in current flow, the screen current increases. The moment the screen current increases, the screen voltage drops and feeds back a negative swing through C1 to the suppressor. The suppressor grid then resumes its original negative condition, stops any flow of plate current, and assumes control again. Since this action is regenerative, a sharp trailing edge is produced. Simultaneous with plate current cutoff, the plate voltage swings positive and feeds back to the grid a positive voltage, which helps the grid to return to normal zero bias condition. Since the charge on C cannot change instantly, the plate swing tapers off exponentially and the tube is not ready for another trigger cycle until it has completely recovered. Diode V3, a "plate-catching" diode (because of the way it "catches", or arrests, the positive excursion of the plate voltage), operates to catch the plate at a specific voltage, so that with a fixed bottoming point the length of the output pulse and its time duration depend on the plate voltage fixed by V3. The cathode of V3 is biased positive by the voltage divider consisting of R6, R7, and R8, as controlled by potentiometer R7. When the plate voltage of V1 is greater than the positive voltage applied to the cathode of V3, the diode conducts and quickly brings the plate voltage of V1 down to the level of the cathode voltage. Thus, the linear sweep action always starts at the voltage set by R7, and the duration of the phantastron gate (or the length of the sweep) is thereby determined. Because the amplitude of the plate sweep depends on the level at which it starts, R7 directly controls the amplitude. The amplitude of the screen gate is determined by the voltage applied and the screen current, and is only slightly affected by R7.

**Cathode-Coupled Circuit.** A typical cathode-coupled pentode is shown in the accompanying schematic. This circuit is also started by a positive trigger applied to the suppressor grid and turns itself off automatically like the screen-coupled circuit. The output can be taken from either the screen or cathode, or both. The screen output is a positive gate, and the cathode output is a negative gate.

In this circuit, tube V1 is the basic phantastron, with diode V3 operating to control the plate voltage level and determine the duration of the output gate. To minimize overshoot on the control grid, cathode, and screen grid (positive on the control grid and cathode, negative on the screen grid), diode V2 is connected between R1 and R2 on a voltage divider network consisting of R1, R2, and R3. (The voltage on the cathode of V2 is normally 1 or 2 volts less than the cathode voltage of V1.) Note that no negative supply is needed to bias the suppressor. Cathode bias is used, and the suppressor is held at a lower positive potential than the cathode; thus, it is effectively biased negative with respect to the cathode, cutting off plate current. The screen is drawing current, which produces a positive voltage on the cathode. When a positive input trigger appears across R3, it is applied to the suppressor. This trigger is prevented from affecting the control grid by automatically reverse-biasing diode V2. The grid is normally biased near



**Basic Cathode-Coupled Phantastron**

zero, being held by diode V2 at a potential determined by the voltage divider (R1, R2, and R3) connected between B+ and ground, and the cathode is positive with respect to the grid by approximately 1 or 2 volts. When the trigger is applied, it overcomes the bias between the suppressor and cathode, and plate current flows. The decrease in plate voltage, due to the flow of plate current, is fed back to the grid through capacitor C, causing the tube current to decrease and the cathode voltage to drop. This drop in cathode voltage further decreases the bias between the suppressor and cathode, and plate current increases further. Since the total tube current is decreasing and the plate current is increasing, the screen current must decrease. This action is regenerative, and plate current will jump from zero to a value determined by the tube characteristics. (Note that the bias between the cathode and suppressor is decreasing, which is regenerative, causing the plate current to increase. The bias between the cathode and grid is increasing. This action is degenerative, which decreases the total tube current. Therefore, there must be a point where these two effects are equal and the current will stabilize for an instant.) At this instant there is no further change in plate voltage, and the grid voltage increases in the positive direction at a rate determined by C and R5, since it is returned to $E_{bb}$ through resistor R5. This causes the plate current to increase. As the plate current increases, the plate voltage decreases, and this negative change is coupled through C to the grid. It can be seen that this signal is degenerative, and prevents the plate current from increasing rapidly. This action continues, providing a linear sweep until the plate voltage drops to a level at which it can no longer cause an increase in plate current. At this time, degenerative feedback to the grid stops, and the grid will go in a positive direction more quickly. This causes an increase in the total tube current, and thus an increase in cathode voltage, an increase in cathode-to-suppressor bias, and a decrease in plate current. With the total tube current increasing and the plate current decreasing, the screen current must be increasing. It can be seen that the action taking place is regenerative, as the plate will go positive, causing the grid to go positive, and the plate current will go rapidly to cutoff, leaving the tube in its pretriggered condition. The positive swing in the grid is limited by the "catching" diode, V2. Before the circuit is ready for the next cycle of operation, capacitor C must recharge through R3, R2, V2, and R4. As in the screen-coupled phantastron, this circuit is also of the slow-recovery type.

As stated previously, when the phantastron is triggered there is a large drop in the screen current. This produces a positive waveform on the screen with a steep leading edge. As the tube current gradually increases, producing the linear sweep in the plate circuit, the screen current increases in the same manner, but by a smaller amount, in proportion to the plate current. The screen waveform will therefore decrease linearly by a small amount until plate current cutoff (described previously) is reached. At plate current cutoff, the screen current increases abruptly, causing a steep trailing edge. Negative overshoots at the trailing edge of the waveform will be limited by the action of diode V2.

The resultant waveform across the cathode resistor can be visualized from the previous description of tube operation, by taking into account the changes in the total tube current. This waveform will be a negative gate with steep leading and trailing edges and with the flat portion falling off in amplitude at a linear rate. Any positive overshoot at the trailing edge will be limited by diode V2.

As in the screen-coupled phantastron, resistor R5 can be made variable to set the maximum width or delay. R1 is variable, and is connected to the plate of V1 through diode V3, thereby setting the level of plate voltage at which the phantastron begins its action (when triggered). It can be seen that this will determine the amplitude and thus the duration of the plate waveform. R1 is usually an external control to vary the width or delay, and R5 can be an internal adjustment to set the maximum width or delay.

In contrast to the screen-coupled phantastron, the cathode-coupled phantastron has a smaller range of operation. The maximum plate amplitude swing of V1 is limited by the value of the cathode resistor, in that "bottoming" of the plate voltage occurs at a more positive potential than in the case of the screen-coupled phantastron.

## FAILURE ANALYSIS.

**No Output.** Lack of plate or screen voltage because of an open bleeder resistor network (consisting of R1, R2, and R3) or open load resistors will prevent operation, as will a faulty electron tube. Loss of input trigger will also render the circuit inoperative. It is also possible for excessive bias to make the circuit inoperative because the trigger amplitude is not sufficient to overcome the bias and initiate operation. Such a condition is indicated when an input trigger can be seen on the suppressor with an oscilloscope and voltage appears on all tube elements, but either the grid or cathode voltage is higher than normal. This is most likely to occur in the screen-coupled circuit, where a negative fix supply is employed with a common bleeder to obtain bias. Since the cathode-coupled circuit develops its own bias, an excessive current drain or short-circuit condition would be needed to increase bias to the non-operating point.

**Distorted Output.** Distortion is indicated by a non-linear waveform or an inaccurate time delay. Linearity of sweep development is the basic property of this circuit, with the controlling elements being the applied d-c control voltage and the RC time constant in the feedback circuit. Control voltage trouble may occur when the circuit uses a separate external control from a separate power supply, as power supply fluctuations can easily change the operating level and hence the pulse duration. Failure of the plate-catching diode is usually indicated by lack of control over the entire range of operation, whereas partial control is more likely to result from changing power supply voltage or a defective control. Change of time constant due to changes in circuit values or to failure or partial shorting of the capacitor will change the rate of operation and hence the time delay. It should be most noticeable for the longer delay times. False triggering due to the pickup of noise or stray pulses in the control cabling (on remote units) may affect both the starting and stopping of the gate. If the disconnecting or triggering diode is used, however, such pickup will affect only the start unless it is coupled to the suppressor through stray capacitance, and this is rather unlikely to occur. Generally it is rather difficult to pinpoint trouble in this type of circuit unless an oscilloscope is used to observe the waveforms at each electrode, because there are four basic types of trouble, namely, starting trouble, stopping trouble, linearity, and recovery-time failure.

**Low or Unstable Output.** Low screen-gate output indicates improper screen voltage or current, which may be caused by a defective electron tube or a change in resistance value in the screen circuit. Low cathode-gate output indicates low cathode current, which is the sum of all element currents, and therefore may be due to any one of numerous causes. Usually a voltage check will indicate the defective component. Unstability in the form of jitter may be caused by power supply voltage fluctuations, noise, or false triggers picked up by unshielded wiring. An oscilloscope waveform check will reveal the cause of the unstability, which can then be traced to its source.

## FAST-RECOVERY PHANTASTRON CIRCUIT.

### APPLICATIONS.

The fast-recovery phantastron circuit is used to generate a linear sweep, or rectangular-wave output, whose duration is directly proportional to a control voltage. Because of its extreme linearity and accuracy, the phantastron output waveform is used as a delayed timing pulse, to produce time-delayed trigger pulses for synchronizing purposes, and movable marker signals for display.

### CHARACTERISTICS.

Operation is similar to that of monostable multivibrator.

Pulse width or delay varies linearly with the applied control voltage.

Requires an electron tube of the pentode or pentagrid type.

Circuit operation turn-on is by application of negative trigger or gate to the plate, or positive trigger or gate to the suppressor grid; turn-off is automatic by internally generated waveform.

Output can be taken from the cathode, screen, or plate, and may be either positive or negative, as selected.

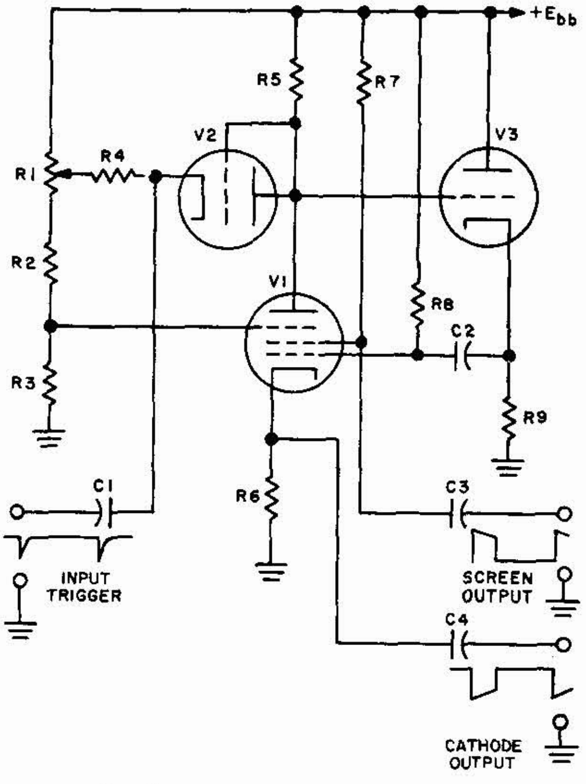
Provides either a low-impedance or high-impedance output, as determined by the output connections.

### CIRCUIT ANALYSIS.

**General.** The fast-recovery phantastron circuit is considered to be a relaxation oscillator similar to the multivibrator in operation. Whereas the multivibrator derives its timing from an exponential waveform developed by an R-C network, the phantastron uses a basic Miller-type sweep generator to produce a linear timing waveform. (The operation of the basic Miller linear sweep generator is described in the discussion of Basic Phantastron Circuits presented earlier in Section 20 of this Handbook.) The phantastron is usually turned on by the application of a gating or trigger pulse, and is turned off automatically by an internally generated waveform.

The rapid return to the stable operating condition at turn-off is the basic property of the fast-recovery phantastron circuit. The rapid recovery is accomplished by charging the feedback capacitor through the low cathode-to-plate conduction resistance of a cathode follower, rather than through the high-resistance plate-load resistor of the phantastron. The effect of the rapid charge path is to return the plate voltage of the phantastron circuit to its stable-condition level immediately in order to prepare the circuit, in as short a time as possible, for the next input trigger pulse. Although the cathode follower decreases the usable range of the control voltage and the linearity, it is necessary in order to reduce the recovery time when long-duration delays are desired. Whether the slow-recovery or fast-recovery phantastron circuit is used in a given application is determined by the recovery time requirements; otherwise, the circuits function in the same manner and serve the same purpose. Both a positive and a negative rectangular-wave output with well-defined leading edges may be obtained from the phantastron, depending on whether the output connection is made to the screen or cathode, respectively.

**Circuit Operation.** The accompanying schematic illustrates a typical pentode cathode-coupled fast-recovery phantastron circuit. The circuit is turned on by application of a negative trigger pulse to the plate; turn-off is automatic by an internally generated gate. Pentode tube V1 is the phantastron proper. This tube must have the capability of providing two control elements; that is, the suppressor grid must be capable of performing the function of another control grid. A suitable tube for use as a phantastron is the miniature-type 5725 pentode because of the sharp cutoff characteristic of its suppressor grid. Another suitable tube is the pentode type 6AS6. A pentagrid tube such as the 6SA7 can also be used in the phantastron circuit if certain modifications are incorporated in the circuit design . (A basic pentagrid tube phantastron multivibrator circuit is discussed in Section 8 of this Handbook.)

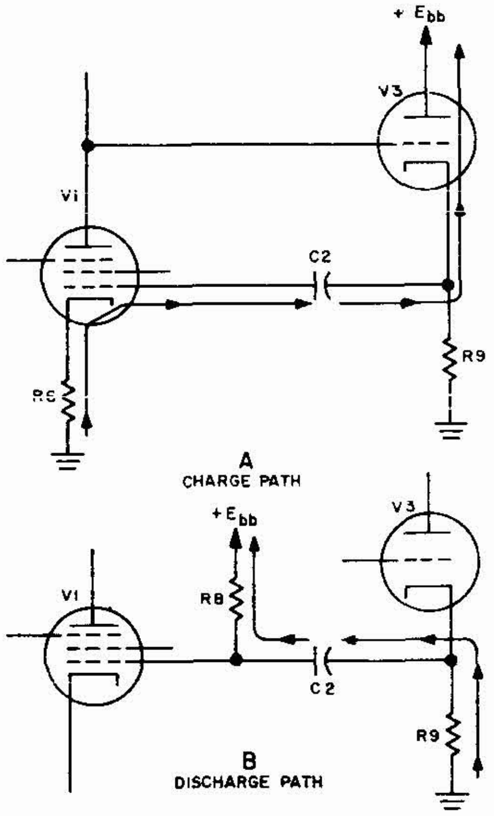


**Fast-Recovery Cathode-Coupled Phantastron**

The diode-connected triode, V2, functions as a trigger injector as well as a clamping diode for controlling the plate-voltage level and determining the duration of the output gate. The maximum value of operating plate voltage is clamped to a level determined by the setting of potentiometer R1 in the cathode of V2, and, since the turn-off level is fixed, the setting of this potentiometer effectively controls the time during which the circuit produces the linear gate or sweep. Triode V3 is the cathode follower circuit through which feedback capacitor C2 is rapidly charged in order to permit the phantastron plate voltage to rapidly return to the maximum operating level determined by trigger injector and clamping diode V2. Although the illustration shows two separate triodes for V2 and V3, in practical circuit applications a single twin-triode is frequently used for economy of tubes.

Potentiometer R1 and resistors R2 and R3 form a voltage divider from the positive voltage supply (+Ebb) to ground. The resistance values are such that the positive voltage developed across resistor R3 is less than the positive voltage developed across cathode-bias and load resistor R6; thus, the suppressor grid is effectively biased negative with respect to the cathode, and plate current is cut off. As mentioned previously, the setting of the wiper arm of potentiometer R1 establishes the voltage level at the phantastron plate, thereby determining the gate length. Resistor R4 is a decoupling resistor in the cathode of the trigger injector and clamping diode, V2. Resistor R5 is the phantastron plate-load resistor; R7 is the screen grid load resistor, and R9 is the cathode-load and coupling resistor for the cathode follower circuit.

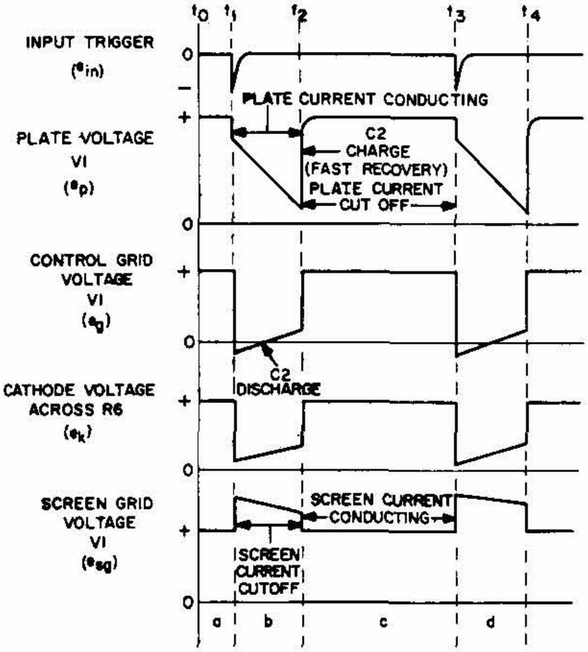
Resistor R8 returns the phantastron control grid to the positive voltage supply, setting the bias level that initially permits the screen grid to conduct heavily. Operation of the circuit occurs at the rate determined by the discharge of feedback capacitor C2 through resistor R8; in some circuits this grid-return resistor, which usually has a value exceeding 1 megohm, is made variable to set the maximum delay or pulse width of the output gate. The action of cathode follower V3 and capacitor C2 provides feedback from the phantastron plate to its grid, to allow rapid response to any change in the plate voltage. Capacitor C1 couples the input trigger to the cathode of trigger injector and clamping diode V2; this trigger initiates (or turns on) the phantastron action. Capacitors C3 and C4 are the output coupling capacitors for the screen grid and cathode, respectively; a positive gate is obtained from the screen grid, and a negative gate from the cathode. If desired, a linear sawtooth waveform can be obtained from the plate of the phantastron circuit.



**Charge and discharge Paths for Capacitor C2**

The following simplified schematic diagram shows the charge and discharge paths for capacitor C2. The charge path (part A of the illustration) is from ground through the phantastron cathode resistor, R6, and the low cathode-to-grid conduction resistance of V1 to the left side of the capacitor, and then from the right side of the capacitor through the low cathode-to-plate conduction resistance of the cathode follower and the positive voltage supply back to ground. This is the fast-recovery charge path for capacitor C2. That is, when the plate voltage of the phantastron rises, as it does at the end of the gate, it is free to do so without the interference of any lumped capacitance; tube interelectrode capacitance and stray wire capacitance are the only hinderances. The resistance in the charging path is also low at this time, since it consists mainly of the low conduction resistance of the cathode follower. The discharge path (part B of the illustration) for capacitor C2 is from its left side through grid-bias resistor R8 and the positive voltage supply to ground, and then from ground through the cathode-load resistor, R9, of the cathode follower to the right side of the capacitor. The long R-C time constant of this path causes capacitor C2 to discharge at a linear rate during the time that screen current is low (near cutoff) and the phantastron tube is drawing heavy plate current.

The operation of the fast-recovery phantastron circuit can best be understood by referring to the preceding circuit illustrations and the accompanying waveform illustration during the following discussion. When voltage is first applied, the plate section is in cutoff and there is heavy screen grid current. The conduction of screen current is a result of the fact that the operating voltage on this electrode is sufficiently positive to attract electrons emitted by the cathode as a result of the positive bias on the control grid (positive voltage return to B+ through resistor R8); this permits the flow of cathode current at this time. The current through cathode-bias resistor R6 produces a voltage drop across this resistor. The positive potential at the top of resistor R6 is now greater than the positive potential at the suppressor grid, which is obtained across voltage divider resistor R3. A bias voltage is therefore established between the suppressor grid and the cathode; this bias is sufficient to cut off the plate current while having no effect on the screen current.



**Theoretical Waveforms for Fast-Recovery Cathode-Coupled Phantastron**

Because there is no plate current, the plate voltage rises to the level determined by the setting of potentiometer R1 in the cathode of the trigger injector and clamping diode, V2. This same positive plate voltage is also impressed on the cathode follower control grid, since this grid and the phantastron plate are electrically identical. The cathode follower now conducts, and the flow of current through its cathode-load resistor, R9, develops a positive potential at the top of this resistor. This positive potential is coupled through capacitor C2 to the control grid of the phantastron, where it further increases phantastron conduction. The positive potential on the phantastron control grid also causes this grid to draw current and charge capacitor C2 through the path described previously. The foregoing action is instantaneous and causes the phantastron to assume its stable state, as depicted during time interval a on the waveform illustration. The circuit remains in this condition (heavy screen current and plate current cut off) until a negative trigger is applied to the phantastron plate through trigger injector and clampling diode V2 at instant $t_1$.

When the negative trigger ($e_{in}$) is applied through capacitor C1 to the cathode of V2, it forward-biases the diode and permits plate current to flow. This current, in turn, causes an immediate drop in the plate voltage developed across plate-load resistor R5. The negative-going signal is also on the grid of the cathode follower, V3, where it acts as a bias to reduce the conduction through V3, thereby reducing the voltage drop across its cathode-load resistor, R9. The negative-going signal at the top of resistor R9 is coupled through capacitor C2 to the control grid of the phantastron tube, V1, where it drives this grid sufficiently negative to reduce the conduction of the phantastron. Since the phantastron cathode current is reduced, the screen current is also reduced; thus a positive-going voltage is produced at the screen grid. Through cathode-follower action of the phantastron circuit, the negative-going signal on its control grid is coupled to the cathode, where it now reduces the bias between the cathode and suppressor grid. With a decrease in this bias voltage there is an increase in plate current, resulting in a further drop in plate voltage. The action just described is cumulative and instantaneous. Thus, when the negative trigger is applied to the cathode of V2 at $t_1$, there is an immediate fall in phantastron plate voltage and a sharp rise in plate current (the fall in plate voltage is fed to the grid through cathode follower V3 and capacitor C2 driving the control grid negative), there is a sharp rise in screen voltage and a decrease in screen current, and there is a decrease in total cathode current and a sharp decrease in cathode voltage. All of the voltage relationships are depicted at $t_1$ on the waveform illustration.

The fact that the phantastron plate current increases while the cathode current decreases is possible because the screen current is now decreasing. Therefore, the rise in plate current results from the fact that the plate draws current which had previously gone to the screen grid. That is, the bias between the cathode and the suppressor grid is decreasing, which is a regenerative action, causing the plate current to increase. Simultaneously, the bias between the cathode and the control grid is increasing, which is a degenerative action, causing the total tube current (and screen grid current) to decrease. The screen grid current is only reduced – not cut off completely; if it were cut off completely, plate current would also be cut off and the circuit would not function. Hence, there must be a point where the regenerative and degenerative effects are equal and the current stabilizes for an instant. This is the instant (at $t_1$, when the sharp drop in plate voltage ceases) at which capacitor C2 begins its discharge action.

As capacitor C2 discharges during time interval **b**, it loses electrons from its left side, in effect making this side of the capacitor (and the control grid of the phantastron) more positive to reduce the bias between the control grid and the cathode. The reduction in control grid bias permits a heavier flow of plate current through the phantastron, which gradually raises the voltage drop across cathode-bias resistor R6 ($e_k$ waveform), as illustrated during time in- interval **b**. The rate of change of tube current is governed by the discharge rate of capacitor C2 through resistor R8. Thus, in discharging, the control grid side of capacitor C2 gradually becomes more positive, causing an increase in plate current; this produces a constant decrease in plate voltage, which is fed back to the grid through cathode follower V3 and capacitor C2. The positive voltage increment on the control grid is always slightly greater than the negative-going plate signal it produces; therefore, the grid potential gradually rises and the plate potential gradually drops, as depicted by the respective control grid ($e_g$) and plate ($e_p$) waveforms during time interval **b**.

The action described during time interval **b** continues until the plate voltage becomes so low (only a few volts) that phantastron tube V1 can no longer amplify the changes in plate voltage. At this instant, $t_2$, capacitor C2 stops discharging and the control grid is rapidly driven positive, causing the tube current to increase at a very fast rate. The rapid rise of current through cathode-bias resistor R6 produces a high positive potential on the cathode, which, in relation to the positive potential on the suppressor grid, is a bias sufficient to cut off plate current. Since the total tube current is increasing at this instant, the additional current must flow in the screen grid circuit. The action now occurring is regenerative. As the plate voltage, whose swing is limited by trigger injector and clamping diode V2, goes positive because of plate current cutoff, the positive-going signal is coupled through cathode follower V3 and capacitor C2 to the phantastron control grid; this signal causes a further increase in tube current, thereby producing a higher voltage drop across cathode resistor R6 to increase the bias on the suppressor grid and further cut off plate current. The positive-going grid of the phantastron draws current and now rapidly charges capacitor C2 through the low cathode-to plate conduction resistance of the cathode follower. Thus, at instant $t_2$, the phantastron is rapidly returned to its original stable state of plate current cutoff and maximum screen grid current, as illustrated during time interval **c**, until the next trigger pulse at $t_3$ again causes a cycle of phantastron action.

As mentioned previously, when the phantastron is triggered (turned on) there is a sudden drop in screen current. This produces a positive-going voltage on the screen with a steep leading edge ($e_{sg}$ waveform). As the tube current gradually increases, producing the linear drop in plate voltage, the screen current increases in the same manner, but by a much smaller amount. The screen waveform will thus decrease linearly by a small amount until the point of plate-current cutoff (described previously) is reached. At the instant of plate-current cutoff, screen current increases sharply, causing a sharp drop in screen voltage, as depicted by the trailing edge of the $e_{sg}$ voltage waveform; this is the positive-gate output waveform coupled through capacitor C3 to the screen output terminals. The resultant negative-gate output, $e_k$, taken across phantastron cathode-load resistor R6, is coupled through capacitor C4 to the cathode output terminals. This negative-gate waveform also has steep leading and trailing edges, with the flat portion falling off in amplitude at a linear rate.

From the circuit action just described, it is evident that changing the value of the voltage applied to the plate will determine the point, and the time, at which the plate voltage "bottoms", with respect to the time of application of the input trigger. Potentiometdr R1 is connected to the phantastron plate through diode V2, thereby setting the level of plate voltage at which the phantastron begins its action when triggered. Changing the value of either feedback capacitor C2 or grid resistor R8 will also affect the pulse width by controlling the rate of discharge of capacitor C2. For example, increasing the value of capacitor C2 or resistor R8 will increase their R-C time constant, thereby causing capacitor C2 to discharge more slowly and increase the width of the delay gate. A decrease in the value of either capacitor C2 or resistor R8 will have the opposite effect on the width of the delay gate. In some phantastron circuits the grid resistor, R8 in this case, is made variable so as to control the maximum width of the delay gate. When made variable the grid resistor is usually an internal adjustment, whereas potentiometer R1 is usually an external control.

If it is desired to obtain several ranges of delay with the phantastron, the most satisfactory method is to leave the value of the grid return resistor (R8) fixed and switch in different values of capacitance for the feedback capacitor (C2). A cathode follower will provide a low-impedance point for the switching and minimize the effects of stray wire capacitance, in addition to providing a fast-recovery path. A disadvantage of using the cathode follower in the phantastron is that it increases the maximum error of the circuit. Ordinarily, the phantastron linearity is obtained by the feedback between plate and control grid, which tends to maintain a constant discharge of the feedback capacitor (C2). Since the gain of the cathode follower is less than unity, the compensation is not as linear as when the feedback occurs through the capacitor alone. However, a slight error (approximately 0.4 percent at a control voltage of 150 volts, for example) can be tolerated when it is necessary to reduce the recovery time of the circuit for long-duration output gate signals.

## FAILURE ANALYSIS.

**No Output.** The input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the cathode of trigger injector and clamping diode V2 can be due to an open input coupling capacitor, C1, or to failure of the external input-trigger source. It is also possible for a defective trigger injector and clamping diode tube, V2, as well as excessive bias, to make the circuit inoperative; the excessive bias will prevent the fixed-amplitude input trigger from overcoming this level and initiating the phantastron action. The foregoing conditions are indicated when an input trigger can be seen with an oscilloscope on the cathode of V2 and voltage appears on all tube elements, but either the phantastron control grid or cathode voltage is higher than normal. This is most likely to occur when a negative voltage source is used with a common bleeder network to obtain the bias (as in a screen-coupled circuit). Since this cathode-coupled pentode circuit develops its own bias, an excessive current drain or short-circuit condition would be needed to increase the bias to the nonoperating point.

Failure of the positive voltage supply, +Ebb, will disrupt the operation of the circuit, as will an open cathode circuit of either the phantastron or the cathode follower. With tubes installed in the circuit, the filament, plate, screen, and suppressor grid voltages should be measured, as well as the bias voltage developed across phantastron cathode resistor R6, to determine whether the applied voltages are within tolerance or whether an associated electrode resistor is open. If feedback capacitor C2 is open or cathode follower V3 is inoperative, there will be no feedback signal to promote the phantastron action. An open output coupling capacitor, C3 or C4, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective phantastron tube; however, a low screen gate output can also be caused by a decrease in applied voltage or a change in resistance value in the screen circuit. Low cathode gate output indicates low cathode current, which is the sum of all tube element currents, and thus may be caused by any one of numerous conditions (decreased tube conductance, reduced plate or screen voltage, etc). Usually, a voltage check will locate the defective circuit and component. A leaky or shorted output coupling capacitor, C3 or C4, will form a voltage divider with the input resistor of the following stage. If the input resistor of this next stage is returned to ground or to a negative supply, the voltage at the screen grid or cathode will be reduced, and the operation of the stage will be upset by the change in voltage applied to its grid.

**Distorted or Unstable Output.** Distortion is indicated by a nonlinear waveform or an inaccurate time delay. Linearity and accuracy of the output gate waveform development is the basic property of this circuit, with the controlling elements being the applied d-c control voltage and the R-C time constant in the feedback circuit. Control voltage trouble may occur when the circuit uses a separate external control from a separate power supply, since power supply fluctuations can easily change the operating level and, therefore, the gate duration. A change in time constant due to circuit values or to feedback capacitor failure or leakage will change the rate of operation and, hence, the gate length; this should be most noticeable for the longer gate lengths. False triggering due to pickup of noise or stray pulses in the control cabling (on remote units) may affect both the turn-on and turn-off of the gate. This instability, or jitter, can also be caused by power supply fluctuations. An oscilloscope waveform check at each electrode is usually the best method to checking for the cause of jitter, which can then be traced to its source.

**Incorrect Frequency.** The fast-recovery phantastron circuit has no components governing the frequency of its output gate signal; this frequency is governed by the input trigger applied to the circuit. Therefore, any change in the output gate frequency is a result of improper operation of the trigger generating circuits.

## ELECTROMECHANICAL (ACOUSTIC) DELAY LINES.

### APPLICATION.

An electromechanical or sonic delay line provides a means of retarding the passage of a signal or wave for a predetermined length of time without distorting the original composition of the signal or wave. This type of delay line is used in computers and in radar equipments such as moving target indicators (MTI).

### CHARACTERISTICS.

Delay line acts as a medium between electrical and sound impulses.

Delay line is composed of quartz crystal slabs and a mercury column.

Amount of time delay depends on length of mercury column.

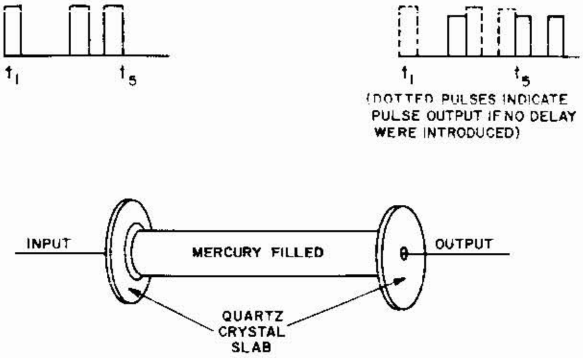
Time delay affected by temperature variations.

### CIRCUIT ANALYSIS.

**General.** The electromechanical (acoustic) delay line utilizes the piezoelectric effect of a quartz crystal slab to convert any electrical impulses within a circuit to sonic impulses. These sonic impulses traverse a column of mercury of specific length and are reconverted to electrical impulses by another quartz crystal slab at the opposite end of the mercury column. The overall effect is a resultant decrease in velocity relative to the velocity of electrical impulses traveling an equivalent distance. Therefore, by increasing the length of the mercury column, the longer the impulses will remain in the sonic state, and the greater will be the delay of the impulses.

### CIRCUIT OPERATION

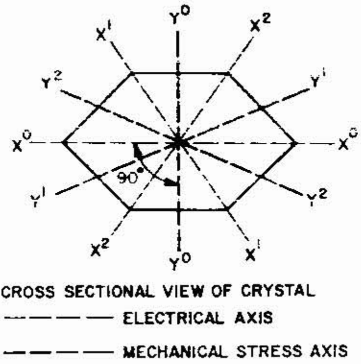
A pictorial representation of an acoustic delay line is shown in the following illustration. The delay line consists of two quartz crystal slabs and a column of mercury in a cylindrical container between the two crystal slabs. As electrical impulses are applied to the first crystal slab of the delay line, the piezoelectric effect associated with crystalline substances causes these impulses to be converted into corresponding mechanical expansions and contractions. One of the expanding and contracting surfaces of the crystal contacts the mercury column in such a way that these mechanical or sonic vibrations are conducted through the column in the same way that electrons are conducted through a wire. Sonic impulses travel at a considerably lower speed than electrical impulses and by increasing the length of the mercury column the time that is required for the impulses to travel from one end of the mercury column to the other becomes greater. The amount of time delay is proportional to the ratio of the velocity of sound in mercury to the velocity of electrical impulses through the conducting material used in the circuit, multiplied times the length of the mercury column.



(DOTTED PULSES INDICATE PULSE OUTPUT IF NO DELAY WERE INTRODUCED)

**Electromechanical (Acoustic) Delay Line**

Upon reaching the end of the mercury column, the sonic vibrations are converted to electrical vibrations by again applying the sonic vibrations to a crystal slab. This crystal, as the first crystal, contacts the mercury column along a plane of the crystal in which sonic or mechanical impulses can be applied or obtained (which happens to be perpendicular to the plane along which sonic impulses are applied or obtained).



**Crystal Axis**

## FAILURE ANALYSIS.

Since the sonic delay line is a single component the failure analysis can be simplified. If no signal is obtained at the output of the delay line and the proper signal is applied at the input, the mercury might have leaked from the cylinder which is supposed to contain it. Another cause of a no-output condition may be an open crystal or a crystal shorted to the metallic case containing it. It will not be necessary to determine which part of the delay line is at fault, since any defect will make it necessary for the entire delay line to be replaced.

A distorted output may be due to the effect of temperature changes within the area where the delay line is used. If extreme temperatures occur, there is a possibility that the crystals may be damaged. In order to prevent or correct this condition constant temperature monitoring should be provided.

## PART B. SEMICONDUCTOR CIRCUITS

Part B of this section is reserved for semiconductor time delay circuits, which may be included in another revision of this Handbook. No semiconductor time delay circuits are discussed in this issue.

## PART C. ARTIFICIAL DELAY LINES

## ELECTROMAGNETIC DELAY LINES.

### APPLICATION.

Artificial delay lines of the electromagnetic type are used to generate rectangular pulses of fixed duration (in radar receiver and transmitter applications); to produce a rectangular waveform from a step function of voltage (as used in starting and delay triggers for test equipment and video display units); to terminate a pulse produced by a regenerative device such as a blocking oscillator or multivibrator (as used in radar, timing circuits, and computers); and to duplicate an existing pulse at a later time (a simple case of time delay). These lines are commonly used for many types of waveshaping and pulse-forming applications.

### CHARACTERISTICS.

Provides a constant attenuation of signal, depending upon material and construction.

Consists of a number of equal sections (or half-sections) of lumped capacitance and inductance, providing a definite delay interval.

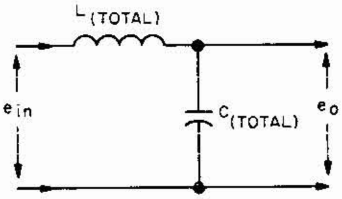
Provides a definite phase shift which can be repeated at specific intervals.

Possesses an inherent characteristic (surge) impedance which must be matched to input and output circuits for proper operation.

Similar in operation to a real transmission line, but greatly reduced in physical size.

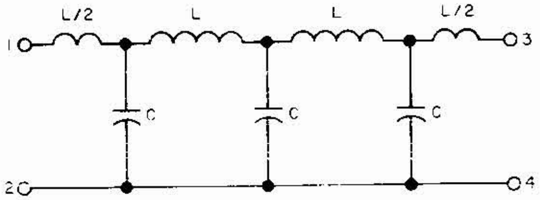
### CIRCUIT ANALYSIS.

**General.** Delay lines are simple to construct, reliable, permanent in their characteristics, and accurately reproducible in manufacture. The delay line operates by virtue of the finite velocity with which the signal travels along the delay line. For **open-wire** lines there is practically no difference in the velocity of propagation of the signal as compared with the velocity of propagation in free space, so that multiples of a physical quarter-wavelength of line must be used to produce the delay. This results in long and bulky lines. Even with the standard type of line, the delay is on the order of 0.003 microsecond per foot. A special coaxial delay line is produced with a spiral-wound center conductor (distributed-constant line) to provide better results; however, measured results at 5mc are only on the order of 0.042 microsecond per foot. Therefore, **artificial** lines consisting of lumped values of inductance and capacitance (which occupy a small space) are connected together in low-pass filter arrangements to provide the desired characteristics. Since a real transmission line has uniformly distributed inductance and capacitance, artificial lines can, in a small space, provide the electrical equivalent of a long line. The basic equivalent circuit of the **distributed-constant** artificial delay line is shown in the accompanying illustration. The functioning of this type of line is similar to that of the **lumped-constant** artificial delay line in all respects. It is used mainly for small delays of 1 microsecond or less where the total length of the line is conveniently held to a range of from 6 to 30 inches, depending upon the construction. Units have been manufactured with characteristic impedances of from 200 to 4000 ohms. The characteristic impedance (Z) is determined by the total distributed constants per inch, centimeter, or foot, by means of the standard formula $Z = \sqrt{L/C}$; the values are in ohms, henries, and microfarads. Time delay is given by the formula $T = \sqrt{LC}$; the values are in seconds, henries, and microfarads. For a given impedance and time delay, the inductance is determined by $L = TZ$, and the capacitance by $C = T/Z$. In actual practice, the manufacturer lists these values and the microseconds per unit length. Thus for a given delay only a specified length is required, avoiding any complicated calculations. Since the distributed-constant type of line is not as commonly used as the lumped-constant type of line, but functions similarly, for practical purposes the discussion of the lumped-constant type of line which follows applies to both types (neglecting end effects, temperature, and frequency response).



**Distributed-Constant Delay Line Equivalent**

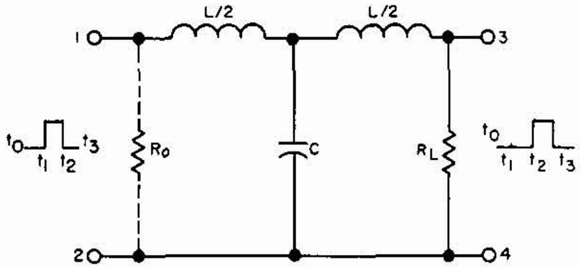
The schematic equivalent of a simple **lumped-constant** type of artificial transmission line is shown in the accompanying illustration. Basically, this circuit is that of a constant **k** low-pass filter with half T section terminations, utilizing one full T section of delay (plus the halves for a total delay of two sections). Actually, the number of sections varies with the design (usually from five to eight sections are sufficient).



**Lumped-Constant Equivalent Circuit**

The manner in which the artificial delay line is employed in a circuit determines how it functions. Generally speaking, there are three forms of operation to be considered. One form is that of a simple delay line which delays the input pulse or signal by a period of time equal to the time it takes to traverse the line; in this case the termination of the signal initiates circuit action after a predetermined delay time. In the second form, the reflected input pulse or signal is permitted to traverse the line, be reflected, and return to the origin; circuit action is initiated after 2n delay periods. In the third form, the line is charged to a specific storage level and is then discharged to form a precise pulse with a duration equal to the discharge-delay period. In each of these forms of operation, performance is generally based upon the theory of charge and discharge of an **ideal lossless** transmission line.

**Circuit Operation.** Consider now the case of the simple delay line. In this instance, the line is terminated in its characteristic impedance (the input need not be terminated unless power transfer is required, since there is no reflection). Assume the simple balanced T section equivalent circuit in the following figure. As far as the input circuit is concerned, the artificial transmission line appears as though it were a resistor equivalent to the characteristic (surge) impedance of the line ($R_o$). Assume that a rectangular 1-microsecond pulse is applied, and that a delay of 2 microseconds is desired. (The delay line is usually placed in series with the grid of a trigger circuit. Let us also assume that a negative trigger is required to initiate action.)



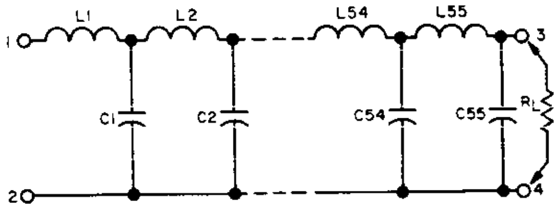
Properly Terminated Line Action

At the beginning of the cycle (time $T_1$), the positive pulse is applied to the line input at terminals 1-2. Immediately, the voltage across the line input rises to the pulse value (input is unterminated). At the load end of the line, however, no voltage as yet appears. Since the line constants are chosen for a 1-microsecond delay, it takes this length of time for the initial pulse to travel to the end of the line (because of the low velocity of propagation of the line). During this interval, capacitor C is being charged through left-hand inductor L/2. At time $T_2$ (1 microsecond later), capacitor C is charged and pulse voltage now appears at output terminals 3-4, across $R_L$. Note that this is still the leading edge of the initial pulse. At time $T_2$ the initial pulse terminates and the input voltage across terminals 1-2 drops to zero. Capacitor C now discharges through right-hand inductor L/2 until time $T_3$. When time $T_3$ is reached, the capacitor is completely discharged and the voltage across $R_L$ drops to zero. Thus, 2 microseconds after the start of the initial pulse, the negative trailing edge of the pulse appears at the grid of the trigger tube, and the trigger is initiated (by the trailing edge of the pulse) with a 2-microsecond delay. During the delay period, simple R-L-C charge and discharge action was postulated, as supported by simple transient theory.

In practice, a number of sections of L and C are required to provide pulse transfer and delay without distortion. All delay lines have resistance which distorts the pulse by causing a reduction of current as the line is charged, with a consequent slope in the top of the pulse. The inductance opposes the change in current and affects the circuit at the very beginning when the charging current quickly assumes a high value, and then acts to maintain the current flow after the maximum current value is reached and tends to decrease. With a large inductance the rise and fall of current is more gradual; with a smaller inductance the current rises and falls more rapidly. The addition of the capacitance to the circuit causes the current to reach a definite maximum value. The smaller the capacitance, the smaller the maximum value of current and the shorter the period of time required to reach maximum current. When both inductance and capacitance are combined, and the inductance is very small and the capacitance very large, the circuit action is controlled mainly by the resistance in the circuit. Under these conditions the charging current rises very quickly and remains constant for a relatively long period of time (because a relatively long time is necessary to charge the capacitor). Thus the response curve closely resembles the input step voltage. Ideally, as L approaches zero and C approaches infinity, so that only resistance is left in the circuit, the output waveform approaches the input waveform. This is theoretically true because a purely resistive circuit has no transient response and, therefore, does not change the shape of the input voltage waveform. With only resistance in the circuit, however, there would be no delay. Consequently, a practical compromise is reached by employing a number of L-C sections having a small inductance and a relatively large capacitance.

A detailed analysis of the operation of a typical distributed-constant type of delay line (chosen for ease of explanation) using actual values follows. As constructed, the line consists of very fine wire (No. 40 AWG, 0.0031 inch in diameter), wound on a plastic core. This continuously wound coil has a diameter of approximately 3/16 inch, and contains 109 turns per centimeter of length to provide a rated inductance of 20 microhenries per centimeter. An insulating sleeve is placed over the coil, and an external copper braid is used to provide a shielded outer conductor, which forms a capacitance of 16.5 picofarads per centimeter with the coil. The measured time delay is 0.018 microsecond per centimeter. To produce the 1-microsecond time delay mentioned in the previous discussion, a 55-centimeter length of this line is required. Therefore, we can consider the line to be made up of 55 sections (1 cm long), forming an equivalent ladder-type line as illustrated in the accompanying figure.

Although in the previous discussion an ideal pulse was assumed, with zero rise time, a practical square input pulse has a finite rise time. A value of 0.03 microsecond for a 1-microsecond pulse is representative of actual rise and fall time tolerances encountered in practice. When this pulse is applied to the input of the line at time $T_1$, terminals 1 and 2, coil L1 provides a counter emf which slows down or opposes the passage of current flow through it. The current through L1 is the charging current for capacitor C1 and the remainder of the line sections. Capacitor



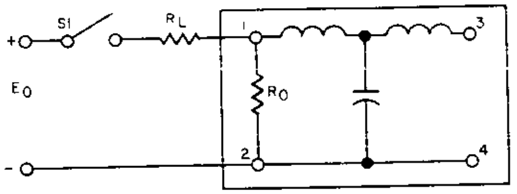
**Ladder-type Delay Line Equivalent**

C1 charges in accordance with the time constant L1C1 (0.018 microsecond). Since the rise time of the pulse is 0.03 microsecond, capacitor C1 charges quickly. During this period the voltage across L1 decreases while the voltage across C1 increases. In effect, the input voltage is applied to L2 after being delayed 0.018 microsecond. Since it takes 10 time constants to reach approximately full charge, the amplitude is less than that of the original pulse, and approximates a final value of about 0.6 that of the original value (at the end of the line). These line sections are effectively connected in series with the line, and the pulse travels progressively down the line from L1 through L55. Capacitor C55 is charged to the same value as L1 was after one time constant, and at a time ($T_2$) exactly 1 microsecond later. In other words, the leading edge of the pulse reaches the end of the line at that instant.

Since the duration of the pulse is 1 microsecond, the entire line is still charging. In the next instant, however, the input pulse terminates, and the negative-going trailing edge is applied to L1. At this time, C1 is fully charged and begins to discharge. The discharge path is the reverse of the charge path. The discharge action is similar to the charge action; that is, at the end of one time constant C1 is discharged substantially, and the effect is as if a negative voltage were applied between L2 and ground. The discharge pulse travels progressively down the line. During this time ($T_2$ to $T_3$) the amplitude of the output pulse remains constant, since the flat top of the input pulse is being reproduced by the constant charge voltage to which C55 is held. This action is the result of the small (fast) time constant per section (full charge is reached in approximately 0.09 microsecond). A slight rounding off of the leading edge is produced in practice (by exponential charging action); however, in the ideal case discussed previously, no such action was assumed. Practically, this rounding off effect is negligible, and the shape of the input pulse is retained as long as the pulse rise time is longer than the time constant per section. (When the rise time is less than the time constant per section, a noticeable rounding off or distortion of the pulse shape occurs.)

Once the discharge action is started by the trailing edge of the input waveform (time $T_2$), it continues until C55 is reached. The discharge of C55 through terminating resistor $R_L$ (at time $T_3$), connected across terminals 3 and 4, represents the trailing edge delayed 1 microsecond. Since the leading edge was also delayed 1 microsecond, the total delay from the leading edge to the trailing edge (or trigger) for the time period $T_1$ to $T_3$ is exactly 2 microseconds (within practical limits). A fewer number of sections or a change in the values of the inductance and capacitance used will change the delay time. In the case of the lumped-constant delay line, the action is identical. Instead of special construction, however, the delay line merely consists of a number of small inductors and capacitors connected in the ladder-type arrangement illustrated previously.

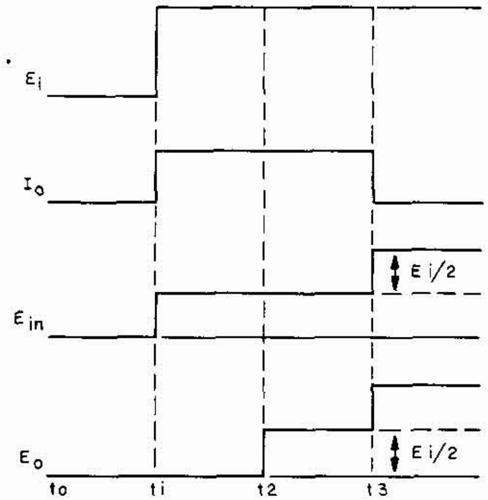
**Open-Circuited Line.** Consider now the case of the artificial delay line which is **not** terminated in its characteristic impedance. Let us assume that the line is open-circuited and is represented by the simple circuit shown in the following figure. The delay line is connected in series with load resistor $R_L$ and switch S1 to a d-c source of voltage $E_o$. Assume that the line at time $T_0$ is completely discharged, with S1 open. At time $T_1$, switch S1 is closed, and voltage $E_o$ is applied across load resistor $R_L$ and $R_o$ in series ($R_o$ is the surge or characteristic impedance of the delay line). Assuming that $R_L$ and $R_o$ are equal, the applied voltage divides equally, and half the applied voltage appears at terminals 1-2 (line input). The line is designed to have a velocity of propagation much less that of an open-wire line; thus, at time $T_2$ the voltage has just reached terminals 3-4. Since the line is open-circuited, the applied voltage is reflected back in phase (with the same polarity) toward the line input. Since current will not flow through the open circuit, the current polarity is reversed, and the reflected wave cancels the current of the incident wave to give a total zero current. Thus, the voltage at terminals 3-4 is effectively doubled, and a reflected voltage equal to $E_o$ travels back to the source. When the source is reached at time $T_3$, the input voltage and reflected voltage are equal, current flow ceases, and the pulse is terminated. At this time the line is charged to the applied voltage. While the output end of the line is not terminated, the input is usually matched with a resistor ($R_L$) equal to $R_o$ so that the reflected pulse is absorbed on its return. During the interval between pulses or signals (when S1 is open), the line discharges; thus it is ready to start another cycle of operation when S1 is again closed.



**Open Circuited Delay Line Equivalent**

The current and voltage relationships for the open-ended line are shown in the following figure.

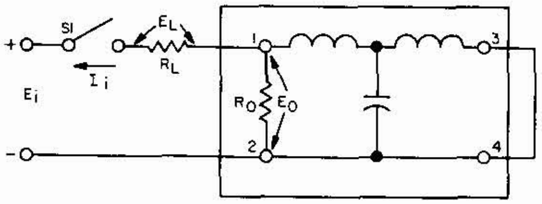
It can be seen that $E_i$ is the applied voltage or step function, which at the closing of S1 jumps to its maximum value. Simultaneously, charging current $I_o$ does likewise. Since the flow of $I_o$ through $R_o$ produces the voltage $E_{in}$ applied to the line, and since equal resistors $R_L$ and $R_o$



**Current and Voltage Relationships of Open-Circuited Line**

form a voltage divider across the input, the voltage $E_{in}$ is reduced to half of $E_i$, remains at this value during the time of two delay periods, and then returns to the source value when the line is fully charged and no further charging current flows. At the output of the line the step function $E_o$ rises to one-half maximum value after one delay period, and then to full value at the end of the remaining delay period. With the line fully charged at the end of two delay periods, it remains at the original applied value of $E_1$ until S1 is opened; the line then discharges. In practice, this is usually accomplished through the grid resistor of the stage which it triggers (the delay line is connected in parallel across the grid resistor in place of the conventional grid capacitor). Thus we can say that an open-ended delay line operates on a step function of voltage to produce a pulse of **current** equal in duration to twice the length of the line. The pulse across the characteristic impedance in series with the line has one-half the amplitude of the step function.

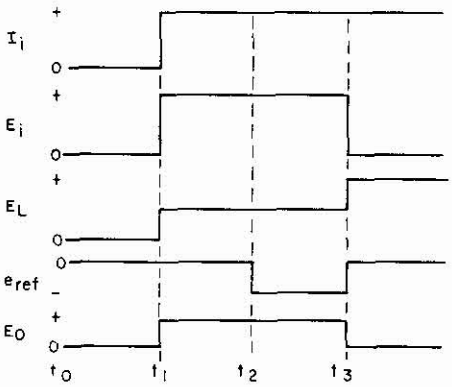
**Short-Circuited Line.** Consider now the case of an artificial delay line which is terminated by a short circuit at terminals 3-4, as shown in the accompanying figure.



**Short-Circuited Delay Line Equivalent**

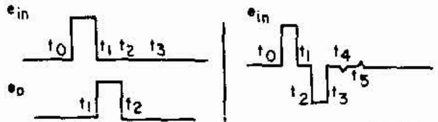
The illustration is identical to the illustration of the open-circuited line shown previously, except that the output is short-circuited. At time $T_1$ when S1 is closed, the applied voltage divides equally between $R_L$ and $R_o$. At time $T_2$ the voltage reaches terminals 3-4 and is inverted in polarity by the short circuit and sent back toward the source. Simultaneously, the current is reflected back in phase with the source wave. Therefore, the current doubles while the voltages of the reflected and incident wave cancel to produce zero voltage. The current wave then travels back to the source in coincidence with the oppositely polarized reflected voltage. When the source is reached at time $T_3$, the input voltage across $R_o$ is completely canceled and is therefore zero, while the current is double the starting value. In effect, the input to the line at this time is short-circuited also, and the line is completely discharged, ready for another cycle of operation.

The current and voltage relationships for the short-circuited line are shown in the following figure. In this case, $I_i$ is the step function, which at the closing of S1 jumps to its maximum value. Simultaneously, the applied voltage, $E_1$, does likewise. Because of voltage-divider action, $E_o$ (the voltage across $R_o$) is half the source value, or $E_i/2$. It remains at this value for the time of two delay periods, and returns to zero when the out-of-phase reflected pulse reaches the input and produces cancellation. Voltage $E_L$ across $R_L$ is produced at half amplitude since it is equal to the input voltage across $R_o$; it remains at this value for two delay periods and then rises to the source value at the termination of the pulse. The voltage $e_{ref}$ is the reflected voltage, which does not exist until time $T_2$; it is negative and equal in amplitude to $E_o$. Once started by the reflection, it continues to flow back to the source until time $T_3$, when it reaches the start ($T_1$) and terminates output pulse $E_o$. Output pulse $E_o$ originates at time $T_1$ at half the amplitude of source voltage $E_1$, continues for the time of two delay periods, and is then terminated.



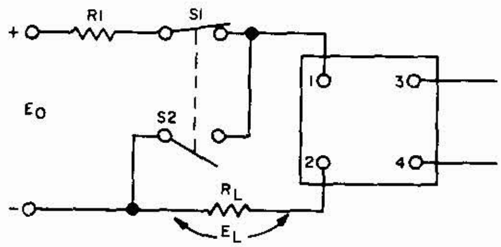
**Current and Voltage Relationships of Shorted Line**

In the case of the shorted line, then, we can say that it operates on a step function of current to produce a pulse of **voltage** equal in duration to twice the length of the line. The voltage produced has half the amplitude of the step of current multiplied by the characteristic impedance. Thus, there is complete duality between open lines charged from a constant-voltage source, and short-circuited lines charged from a constant-current source. The choice of the method depends upon the characteristics of the switch used to produce the step function. A thyratron switch has an impedance of less than 10 ohms and, therefore, effectively constitutes a constant voltage source. A pentode switch, on the other hand, may have an impedance of a megohm when closed, and yet switch appreciable currents. While the discussion above has assumed ideal step function operation, in actual practice there is an effect produced by the steepness of the grid pulse and stray capacitance, which determine the slope of the leading edge of the pulse. Line attenuation also produces phase distortion; the characteristic impedance of the line and the line resistance produce a slope on the trailing edge of the pulse, and determine the total amplitude of the pulse. Accidental resonances in the line can cause oscillation following both edges of the pulse. Unterminated open or shorted lines will tend to produce another reflection at the input end, and cause a following pulse of lower amplitude until attenuated by the losses in the line (this is effectively an oscillatory condition). The following figure shows some typical waveforms taken with different line terminations, and is indicative of typical responses of artificial delay lines. The pulse length is 1-microsecond, and the delay time is also 1 microsecond. Part A of the figure shows both input ($e_{in}$) and output ($e_o$) waveforms with the delay line properly terminated both at the input and the output. Part B shows the input waveform with the input properly terminated and the output short-circuited. Note that between times $T_1$ and $T_2$ the output pulse is effectively cancelled by the negative inverted pulse, whose leading edge appears at $T_2$ and lasts until $T_3$. Since the amplitude of the inverted pulse is not exactly equal to that of the input pulse, slight pips appear at $T_4$ and $T_5$, even though the input is properly terminated. Part C shows a partially shorted line, that is, with the load only one-half the value of the line characteristic impedance, and with the input properly terminated. In this case, since the mismatch is approximately 50% there is a reflection of approximately 1/4th the amplitude, with the remainder being absorbed. Note that because the resistance or impedance is lower than that of the line, the signal is inverted as with the short-circuited line. Part D shows a more nearly matched condition, at about 20% mismatch. While the reflection is still inverted, because the impedance of the load is lower than that of the line, its amplitude is very small. Part E shows the input waveform with the input and output both properly terminated. In this case the output is absorbed by the proper termination, and no reflection occurs; hence, the input pulse stands alone. Part F shows the condition for a 50% mismatch, with the load impedance twice the line impedance. In this case the reflected pulse is of the same polarity as the input, acting as an open line, since the load impedance is higher than the surge impedance of the line. The amplitude is not half of the input, but approximately one-quarter, exactly as in the opposite case of 50% mismatch shown in part C. Part G shows the waveform at the input with the output open-circuited and with the input properly terminated. In this case the open line creates a complete reflection, which is not quite equal in amplitude to the input signal because of line attenuation; therefore, there is a slight reflection, causing the minor pips at $T_4$ and $T_5$, even though the input is properly terminated. The final case is with the output short-circuited and the input terminated in a lower impedance than that of the line. Part H shows the input waveform for this case. Since the line is shorted, the reflected pulse is inverted, and, since it is improperly terminated at the input, reflection occurs, with each succeeding waveform being further reduced in amplitude. This is equivalent to an oscillatory condition or an undamped transient response.



**Typical Delay Waveforms for Various Terminations**

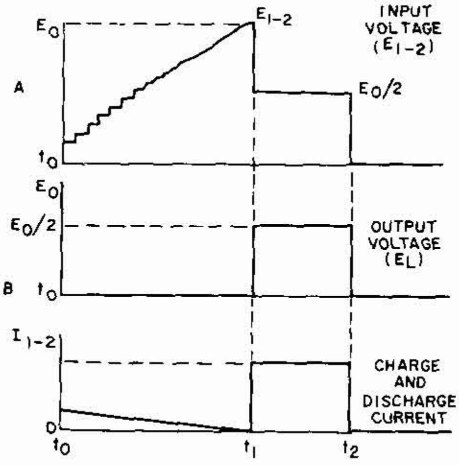
**Pulse-Forming Line.** In the two preceding cases of open and shorted delay lines, the action was considered with the line discharged and a pulse applied. In the third and final case involving the use of a delay line, the line is first charged to a specific level, is then disconnected and discharged, and finally forms a pulse with steep leading and trailing edges and with a time duration equal to the delay time. The accompanying figure shows a simple schematic equivalent of such a pulse-forming circuit. As shown, the line is connected through R1, S1, and $R_L$ to the d-c source voltage, $E_o$. Switch S2 is linked mechanically with S1 so that when S1 is closed S2 is open, and vice versa. The line is not terminated, but rather is open-circuited. At time $T_0$ switch S1 is closed and the line is permitted to charge until it reaches a steady-state condition with the line charged to voltage $E_o$. (This charge consists mostly of electrostatic energy stored in the capacitors.) At time $T_1$, switch S2 is closed, opening S1, and the line dis-



**Line Discharge Equivalent Circuit**

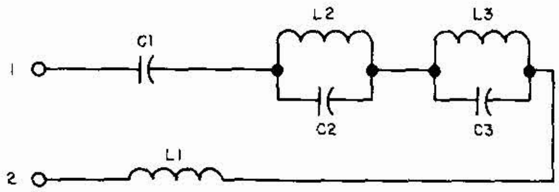
charges through $R_L$. The discharge current through $R_L$ produces voltage $E_L$, which is the desired output voltage. The flow of current through $R_L$ produces a voltage wave which travels from terminals 1-2 of the delay line toward open end 3-4. Since the load resistor is placed in series with the line and the line is now acting as the source of voltage, this voltage divides between the characteristic impedance of the line and $R_L$, which is of the same resistance. Therefore, the initial discharge voltage is half of the value to which the line is charged. Because the flow of current is now reversed, the polarity of the voltage wave is opposite that to which the line was initially charged. As this induced wave travels down the line, it cancels out the original charge by one-half the maximum charge voltage. Thus, the discharge current which flows through $R_L$ is equal to $E_o/2R_o$. When the wave reaches terminals 3-4, reflection occurs. The reflected wave is now of the same polarity as the induced voltage wave and, since current cannot flow in an open circuit, the voltage doubles, becoming equal to $E_o$. The polarity of the discharge (induced) wave is opposite the original polarity of $E_o$; thus both voltages are equal and cancel. Since the current cannot flow further, it is inverted in polarity and travels back to the source, wiping out the current wave as it travels. When the reflected wave reaches the input terminals, all the electrostatic energy stored in the line is completely discharged, and neither current nor voltage exists anywhere along the line. Switch S2 is then opened and S1 is closed, starting a new cycle of operation. In this instance the discharge of the line has resulted in a rectangular pulse with a duration equal to twice the delay time.

Current and voltage relationships for the charge and discharge of the delay line are shown in the following figure. At time $T_0$, when S1 is closed and S2 is open, the source voltage is applied to the line through charging resistor $R_1$ in series with $R_0$ and $R_L$. In the absence of $R_1$ the line would have half the source voltage applied. However, $R_1$ is a large-value resistor (where the $I^2R$ loss in this resistance is undesirable a choke is used instead), and only a small voltage is applied to the line. The initial voltage is reflected again and again (as shown in part A) until the line is finally charged up to the source voltage (assuming that the period of time between $T_0$ and $T_1$ is sufficient). At time $T_1$, when switch S1 is open and S2 is closed, the discharge commences and the charge voltage immediately drops to half the maximum value. The line voltage remains at this value until time $T_2$ is reached, when the discharge ceases. Thus, from part B of the figure it can be seen that between $T_1$ and $T_2$ the line discharges at a constant current with a voltage equal to one-half the initial charge voltage.



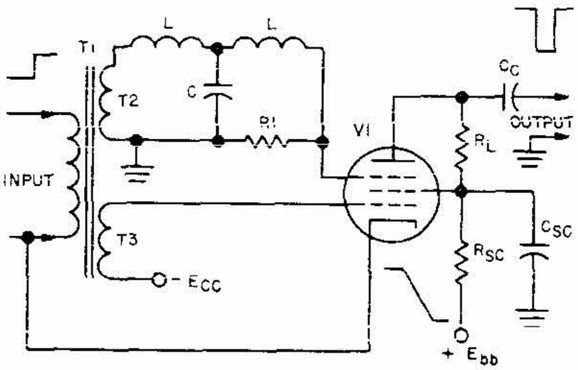
**Current and Voltage Relationships for Discharge Line**

The ladder-type LC networks used for the delay lines discussed previously are sometimes replaced by a more sophisticated type of line which uses a two-terminal series arrangement instead of the four-terminal parallel arrangement, as shown in the following simplified schematic. In this arrangement the two sections have different values of L and C. This type of construction is similar to the *m*-derived filter. The theory of operation is identical to that of the ladder-type of delay line; the different construction merely provides equivalent or better pulse response characteristics with fewer sections.



**Two-Terminal Delay Network**

An artificial delay line used with a typical pulse generator to produce an output pulse equal to the delay time is shown in the following schematic. In this application a step function of voltage is applied to a delay line (which is connected to a tube element) at the same time the input pulse (step function) is applied to another tube element. The inverted and delayed pulse stops circuit action at the end of the delay period. Transformer T1 has two



**Typical Pulse Generator**

secondary windings, T2 and T3. Winding T3 is connected to the bias source and the control grid of the tube. When a positive input pulse is applied to the primary, the induced pulse in the secondary of T3 causes the tube to conduct. Secondary T2 is connected across the delay line, forming a shorted line, with the opposite end properly terminated by R1 and connected to the suppressor grid. In the absence of a pulse and for the initial delay period, the suppressor is essentially at ground potential, being connected through the winding to ground. When the initial pulse is applied to primary T2, a positive pulse travels along the line, is inverted, and appears as a negative shut-off gate at the suppressor grid. Conduction occurs only during the time delay period. By tube action the plate current pulse produces an inversion of the positive input pulse, and provides a negative output pulse across $R_L$, which appears at $C_c$; this pulse is equal to the delay period. Because of the numerous variations in circuitry, no attempt will be made to cover any other practical circuits. The operation of the various circuits is essentially the same, with the output of the delay line controlling the circuit action.

## FAILURE ANALYSIS.

Since the artificial delay line consists of inductors and capacitors, a simple resistance or continuity check will determine whether the line is open or short-circuited. Basically, the line either works or it does not work. If it does not, the end result is that the controlled circuit produces a pulse of the wrong width and shape. Therefore, it is necessary to observe the circuit waveforms with an oscilloscope. Usually, the delay line is applied to the grid circuit of a tube, in which event the plate waveform, being an inverted and amplified replica, may be observed to avoid shunting the line with the oscilloscope input. If the rise time is slow, it may be because the input pulse shape has too much slope. If not, the line inductance is probably excessive. When the top of the pulse slopes excessively, the resistance in the line is excessive. Normally, a slight slope is expected since the line resistance can never be zero. Usually, the line resistance will also place a slight tail on the pulse in short-circuited lines. Adding additional sections will tend to sharpen the rise and fall time, but will also make the delay time longer. Therefore, in such case, the total inductance per section will necessarily have to be reduced. In practice, a defective delay line is usually replaced with a new one. Otherwise it will be necessary to accurately measure the individual components in inductance and capacitance bridges to determine whether they are defective. While insertion or removal of a component or section may temporarily restore the line to proper operating condition, this will be no assurance that other components have not been damaged by the cause of the previous failure, and will themselves soon fail and cause a similar condition. Failure of the associated tube and circuit is more common than delay line failure. Replace the suspected tube with a known good one and check the values of the resistors in the circuit. Failure of the terminating resistor is usually indicated by the presence of additional reflections or by an oscillatory condition.