SECTION 16

CLAMPER (D-C RESTORER) CIRCUITS

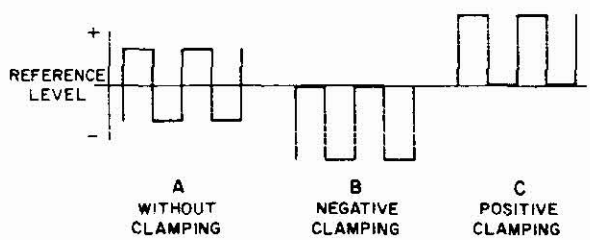
PART A. ELECTRON-TUBE CIRCUITS

DIODE CLAMPER.

General. Diode clampers, also referred to as **d-c restorers and baseline stabilizers,** are used in electronic circuits to hold either amplitude extreme of a waveform to a given reference level. The name **d-c restorer** is somewhat misleading in that the d-c component present in the output waveform has nothing to do with any d-c component that may be associated with the input waveform. The diode clamper circuit can be arranged to "clamp" either amplitude extreme and thereby permit the waveform to extend in only one direction from the reference level. Thus, the circuit can be used to hold either the positive extreme or the negative extreme of a waveform to a desired reference-voltage level.

Diode clampers which hold the positive extreme of the waveform to a desired reference level are called **negative** clampers because the entire waveform is shifted negatively with respect to the reference level; those which hold the negative extreme to a desired reference level are called **positive** clampers because the entire waveform is shifted positively with respect to the reference level.

The accompanying waveform illustration shows the variation of signal voltage with respect to a reference potential without clamping and when negative and positive clamping are used.



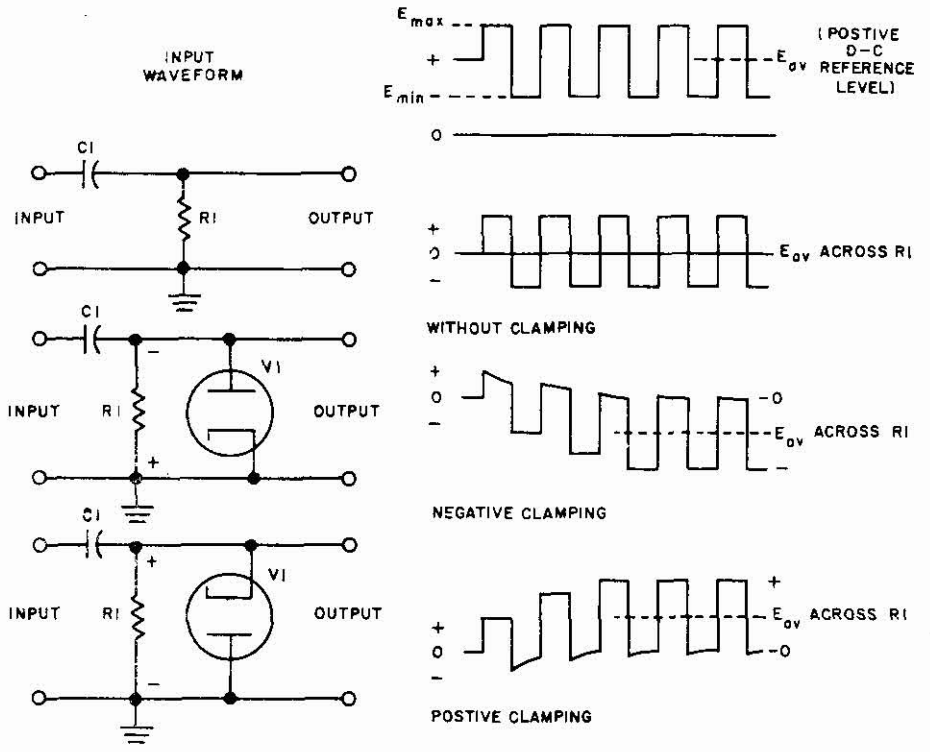
Signal-Voltage Variation With Respect to a Reference Level

R-C coupling is commonly used between stages; in this coupling method, the coupling capacitor also serves as a blocking capacitor, to keep any d-c potential that may be present from affecting the following stage. (The methods used to couple one stage to another were discussed in Section 2.) The varying component of the voltage applied to the R-C coupling network is transmitted to the following stage as a signal waveform (in this case, a square wave) which varies above and below some fixed reference level, as shown in part A of the accompanying waveform illustration. If the resistor of the R-C coupling network is grounded, then the reference level is said to be at ground potential, or at zero reference level, and the signal waveform varies above and below ground (zero reference level) as shown. If the resistor is returned to a fixed potential, as for example a bias voltage, then the reference level is the level of the fixed potential, and the signal waveform varies above and below the fixed potential.

In certain electronic circuits, it is desirable to confine the signal waveform to voltages which lie either above or below the fixed reference voltage established for the circuit. For these circuit applications the clamper circuit is used to hold either the positive or negative extreme of the signal waveform to the desired reference level.

In the following discussion, it is assumed that the input waveform is obtained from the plate circuit of a previous stage and, therefore, varies about a positive d-c voltage reference level. The output waveform obtained from an R-C coupling network is normally centered about an established reference voltage level at or near ground potential. However, if the coupling capacitor can be made to charge to the **maximum** positive d-c value of the input waveform and remain at this value, then any signal swing must occur in a negative direction; therefore, the output waveform varies between the established reference level and some negative value, depending upon the peak-to-peak amplitude of the input signal. Conversely, if the coupling capacitor can be made to charge to the **mimimum** positive d-c value of the input waveform and remain at this value, then any signal swing must occur in a positive direction; thus, the output waveform varies between the established reference level and some positive value, depending upon the peak-to-peak amplitude of the input signal. In the case where the capacitor charges to the maximum positive d-c value, the top of the output waveform is clamped to the reference level, as shown in part B of the accompanying illustration, and the action is termed **negative clamping.** In the case where the capacitor charges to the minimum positive d-c value, the bottom of the output waveform is clamped to the reference level, as shown in part C, and the action is termed **positive clamping.**

The accompanying illustration shows two simple diode clampers and the output waveform associated with each circuit when a square wave is applied to the input of the clamper circuit. The shift of waveform axis with respect to the zero reference level occurs because diode V1 can conduct only when its plate is positive with respect to its cathode. Thus, capacitor C1 charges through a very short time constant (resistance of diode V1 when conducting) on alternate half cycles of the waveform when the plate of the diode is positive with respect to its cathode; the capacitor tends to discharge through a long time constant, the resistance of R1, when the plate of the diode is negative with respect to its cathode (diode V1 nonconducting). This rapid charge and slow discharge action continues until the charge builds up on the capacitor to shift the waveform from the original zero axis. Resistor R1 permits some discharge of capacitor C1 during alternate half cycles of the waveform when diode V1 is nonconducting. This effect causes the waveform to have a slight overshoot at the zero axis, instead of exactly coinciding with the zero axis. Regardless of the presence of a d-c component in the input waveform to the clamper circuit, one polarity extreme or peak (either positive or negative), of the output waveform will approximate the zero axis; whether the positive or negative extreme approaches the zero axis is determined by the manner in which diode V1 is arranged in the circuit.



Negative and Positive Diode Clamper Circuits and Output Waveforms

Although the preceding general discussion has assumed that a positive d-c potential exists as the reference level for the input waveform to the clamper circuit and ground as the reference level for the output waveform, the circuit operation is essentially the same, no matter what respective levels exist at the input and output of the circuit. Several clamper circuits are discussed later in this section which are purposely arranged and "biased" to produce an output waveform clamped at a given d-c reference level (other than ground potential).

Typical negative and positive diode clamper circuits are discussed in the circuit descriptions which follow in this section.

NEGATIVE DIODE CLAMPER.

APPLICATION.

The negative diode clamper (or d-c restorer) is used when it is desired to hold, or "clamp", the positive extreme of a waveform to a zero reference level (ground potential).

CHARACTERISTICS.

Input signal waveform contains both positive and negative amplitude extremes.

Output signal waveform varies between the reference level (ground) and some negative value, which is determined by the peak-to-peak amplitude of the input waveform.

Input and output signals are in phase with one another.

Uses diode in conjunction with an R-C coupling network; cathode of diode is at ground (chassis) potential.

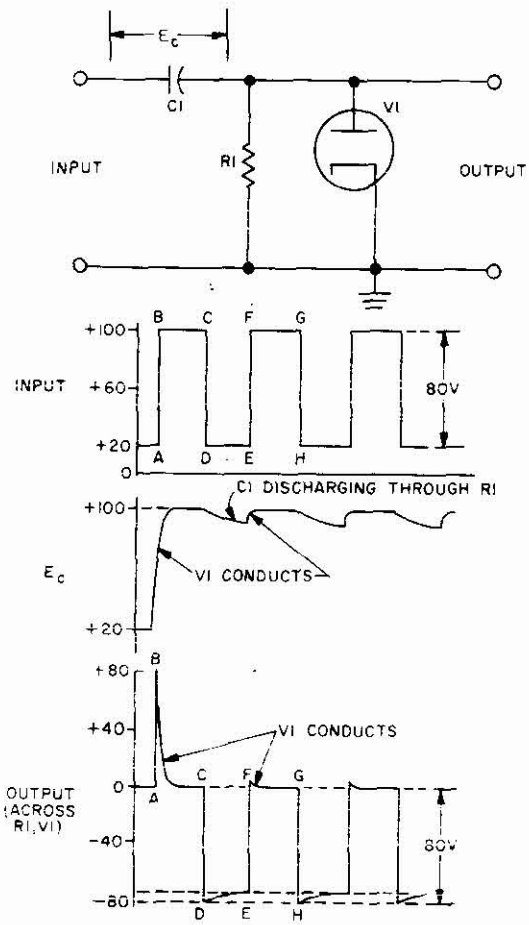
CIRCUIT ANALYSIS.

General. The negative diode clamper circuit consists essentially of a diode connected in parallel with the resistor of a conventional R-C coupling network. The diode is connected so that whenever the waveform swings in a positive direction the diode conducts to produce a short R-C time constant; whenever the waveform swings in a negative direction the diode does not conduct, and this results in a long R-C time constant. Thus, two different time constants are produced — a short time constant during the positive half cycle of the input waveform, and a long time constant during the negative half cycle. It is this difference in time constants that produces the clamping action for the output waveform.

Circuit Operation. A negative diode clamper is shown in the accompanying illustration, together with typical input and output waveforms. Capacitor C1 and resistor R1 form an R-C coupling network and determine the long time

constant of the circuit. Electron tube V1 is an indirectly heated cathode-type diode; it is the clamper diode and, together with capacitor C1, determines the short time constant of the circuit. The filament (heater) circuit for the diode is not shown in the schematic.

The input waveform shown in the accompanying illustration is typical of a square wave generated at the plate of a multivibrator stage. The waveform can be considered as the plate-voltage variation which is applied to the input of the clamping circuit. Initially the plate voltage of the multivibrator stage is low (+20 volts) while the tube is conducting heavily; the plate voltage rises to a high value (+100 volts) when the tube is non-conducting, or cut off. Thus, when the stage is in operation, a square wave is produced which has an 80 volt peak-to-peak amplitude. Coupling capacitor C1 of the R-C network is initially charged to a potential of +20 volts, which is the plate voltage of the multivibrator stage when the tube is conducting heavily.



Negative Diode Clamper Circuit and Waveforms

The circuit conditions at this time are indicated by point A on the input and output waveforms of the accompanying illustration. Immediately following point A on the input waveform, the input to the clamper circuit suddenly rises 80 volts (from +20 volts to +100 volts) to point B. Since the charge on capacitor C1 cannot change immediately, the 80-volt change appears across resistor R1 and also across diode V1. This makes the plate of diode V1 80 volts positive with respect to its cathode, and the diode conducts to charge capacitor C1 through a short time constant path. When conduction begins, the output voltage drops from point B on the output waveform to zero (reference level).

At point C on the input waveform, the input signal drops 80 volts (from +100 volts to +20 volts), but capacitor C1 is charged to +100 volts and cannot change instantaneously; therefore, an 80-volt drop in signal voltage appears across resistor R1, causing the output to drop from zero (reference level) to —80 volts. Thus, between points C and D on the waveforms, the input voltage drops from +100 to +20 volts, and the output voltage drops from zero (reference level) to —80 volts. During the time interval between points D and E on the waveforms, capacitor C1 will discharge slightly through the long time-constant path offered by resistor R1 until point E is reached.

At point E on the input waveform, the input signal again rises 80 volts (from +20 volts to +100 volts) to point F on the input waveform. Once again the charge existing on capacitor C1 cannot change immediately, and the 80-volt change appears across resistor R1. However, an 80-volt change causes the output voltage to overshoot the zero reference level slightly because of a slight discharge of capacitor C1 which has occurred during the time interval between points D and E. Therefore, because of the voltage overshoot, a small positive voltage exists across resistor R1 and diode V1. The plate of the diode is positive with respect to its cathode, and the diode conducts momentarily to replace the slight loss of charge on capacitor C1. The output quickly drops and remains at zero (reference level) until point G is reached. The input signal again drops (from +100 volts to +20 volts), and an 80-volt drop in signal voltage appears across resistor R1, again causing the output to drop from zero to —80 volts. Thus, between points G and H on the waveforms, the input voltage drops from +100 to +20 volts, and the output voltage drops from zero to —80 volts. Once again, capacitor C1 begins to discharge through resistor R1 to complete another cycle.

The output waveform has purposely been drawn to show a substantial decrease in voltage caused by the discharge of capacitor C1 during the period of time the input waveform is at its negative extreme (point D to point E). In practice, however, the value of resistor R1 is relatively large, and very little distortion results from the discharging of capacitor C1 through R1, or from its charging through diode V1 (at point F).

From the explanation of the negative clamper operation given above, it is seen that the positive extreme of the input waveform has been held, or clamped, to the desired zero reference level and the entire waveform has been shifted negatively with respect to the reference level.

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FAILURE ANALYSIS.

General. Because of the relative simplicity of the negative diode clamper circuit, the failure analysis is also relatively simple and is limited to several possible failures.

Initially, the input signal should be checked to determine whether it is present and of the correct waveshape and amplitude. The diode, V1, should be checked to determine whether it is in satisfactory condition and whether the correct filament (heater) voltage is applied to the tube. In many cases, a d-c potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage-divider action to occur. Since capacitor C1 is in series with resistor R1, a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. Furthermore, in this case it is likely that diode V1 will conduct at all times. A quick check to determine whether coupling capacitor C1 is leaky (or shorted) is to remove diode V1 from the circuit and check for the presence of voltage developed across resistor R1.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. As a result, distortion will occur during the time required for capacitor C1 to reach a new reference level, which results from a change in signal amplitude. If the value of resistor R1 decreases considerably, distortion of the output waveform will occur because of the decreased R-C time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since only three components are involved in the circuit (resistor R1, capacitor C1 and diode V1), these components are easily checked to determine whether they are defective. Resistor R1 can be measured with an ohmmeter to determine its resistance, capacitor C1 can be checked with a suitable capacitance analyzer, and diode V1 can be checked in a tube tester or, as an alternative, a diode known to be good can be substituted and the operation of the circuit noted.

POSITIVE DIODE CLAMPER.

APPLICATION.

The positive diode clamper (or d-c restorer) is used when it is desired to hold, or "clamp", the negative extreme of a waveform to a zero reference level (ground potential).

CHARACTERISTICS.

Input signal waveform contains both positive and negative amplitude extremes.

Output signal waveform varies between the reference level (ground) and some positive value, which is determined by the peak-to-peak amplitude of the input waveform.

Input and output signals are in phase with one another.

Uses diode in conjunction with an R-C coupling network; plate of diode is at ground (chassis) potential.

CIRCUIT ANALYSIS.

General. The positive diode clamper circuit consists essentially of a diode connected in parallel with the resistor of a conventional R-C coupling network. The diode is connected so that whenever the waveform swings in a negative direction the diode conducts and produces a short R-C time constant; whenever the waveform swings in a positive direction the diode does not conduct, and this results in long R-C time constant. Thus, two different time constants are produced — a short time constant during the negative half cycle of the input waveform, and a long time constant during the positive half cycle. It is this difference in time constants that produces the clamping action for the output waveform.

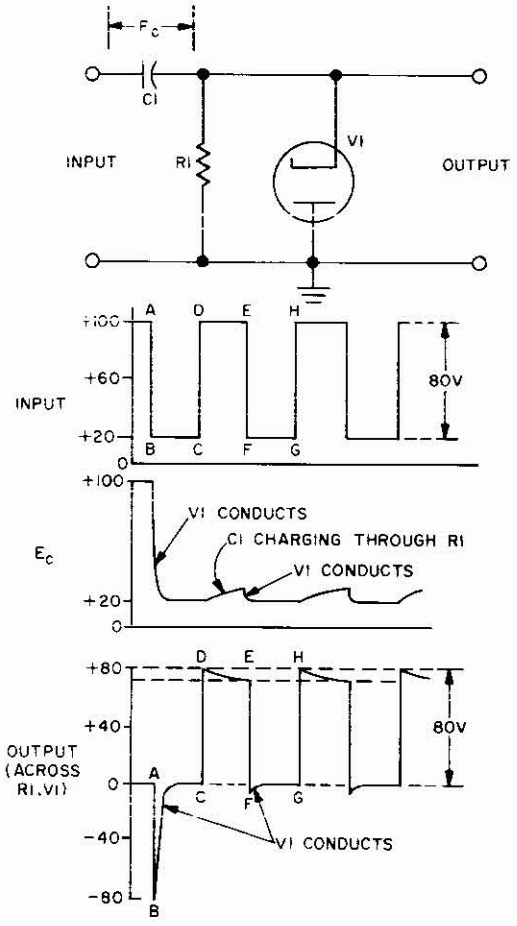
Circuit Operation. A positive diode clamper is shown in the accompanying illustration, together with typical input and output waveforms. Capacitor C1 and resistor R1 form an R-C coupling network and determine the long time constant of the circuit. Electron tube V1 is an indirectly heated cathode-type diode; it is the clamper diode and, together with capacitor C1, determines the short time constant of the circuit. The filament (heater) circuit for the diode is not shown on the schematic.

The input waveform given in the accompanying illustration is typical of a square wave generated at the plate of a multivibrator stage. The waveform can be considered as the plate-voltage variation which is applied to the input of the clamping circuit. Initially the plate voltage of the multivibrator stage is high (+100 volts) while the tube is cut off (nonconducting); the plate voltage drops to a low value (+20 volts) when the tube is conducting heavily. Thus, when the stage is in operation, a square wave is produced which has an 80-volt peak-to-peak amplitude. Coupling capacitor C1 of the R-C network is initially charged to a potential of +100 volts, which is the plate voltage of the multivibrator stage when the tube is cut off (nonconducting).

The circuit conditions at this time are indicated by point A on the input and output waveforms of the accompanying illustration. Immediately following point A on the input waveform, the input to the clamper circuit suddenly drops 80 volts (from +100 volts to +20 volts) to point B. Since the charge on capacitor C1 cannot change immediately, the 80-volt change appears across resistor R1 and also across diode V1. This makes the cathode of diode V1 80 volts negative with respect to its plate, and the diode conducts to discharge capacitor C1 through a short time constant path. When conduction begins, the output voltage rises from point B on the output waveform to zero (reference level).

At point C on the input waveform, the input signal rises 80 volts (from +20 volts to +100 volts), but capacitor C1 is charged to +20 volts and cannot change instantaneously; therefore, an 80-volt increase in signal voltage appears across resistor R1, causing the output to rise from zero (reference level) to +80 volts. Thus, between points C and D on the waveforms, the input voltage rises from +20 to +100 volts, and the output voltage rises from zero (reference level) to +80 volts. During the time interval between points D and E on the waveforms, capacitor C1 will charge slightly through the long time-constant path offered by resistor R1 until point E is reached.

At point E on the input waveform, the input signal again drops 80 volts (from +100 volts to +20 volts) to point F on



Positive Diode Clamper Circuit and Waveforms

the input waveform. Once again the charge existing on capacitor C1 cannot change immediately, and the 80-volt change appears across resistor R1. However, an 80-volt change causes the output voltage to overshoot and drop below the zero reference level slightly because of a slight charge of capacitor C1 which has occurred during the time interval between points D and E. Therefore, because of the voltage overshoot, a small negative voltage exists across resistor R1 and diode V1. The cathode of the diode is negative with respect to its plate, and the diode conducts momentarily to discharge capacitor C1. The output quickly rises and remains at zero (reference level) until point G is reached. The input signal again rises (from +20 volts to +100 volts), and an 80-volt increase in signal voltage appears across resistor R1, again causing the output to rise from zero to +80 volts. Thus, between points G and H on the waveforms, the input voltage rises from +20 to +100 volts, and the output voltage rises from zero to +80 volts. Once again, capacitor C1 begins to charge through resistor R1 to complete another cycle.

The output waveform has purposely been drawn to show a substantial decrease in voltage caused by the charging of capacitor C1 during the time the input waveform is at its positive extreme (point D to point E). In practice, however, the value of resistor R1 is relatively large, and very little distortion results from the charging of capacitor C1 through R1, or from its discharging through diode V1 (at point F).

From the explanation of the positive clamper operation given above, it is seen that the negative extreme of the input waveform has been held, or clamped, to the desired zero reference level and the entire waveform has been shifted positively with respect to the reference level.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the positive diode clamper circuit, the failure analysis is also relatively simple and is limited to several possible failures.

Initially, the input signal should be checked to determine whether it is present and of the correct waveshape and amplitude. The diode, V1, should be checked to determine whether it is in satisfactory condition and whether the correct filament (heater) voltage is applied to the tube. In many cases, a d-c potential exists at the input to the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage-divider action to occur. Since capacitor C1 is in series with resistor R1, a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. A quick check to determine whether coupling capacitor C1 is leaky (or shorted) is to remove diode V1 from the circuit and check for the presence of voltage developed across resistor R1.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. As a result, distortion will occur during the time required for capacitor C1 to reach a new reference level, which results from a change in signal amplitude. If the value of resistor R1 decreases considerably, distortion of the output waveform will occur because of the decreased R-C time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since only three components are involved in the circuit (resistor R1, capacitor C1, and diode V1), these components are easily checked to determine whether they are defective: resistor R1 can be measured with an ohmmeter to determine its resistance, capacitor C1 can be checked with a suitable capacitance analyzer, and diode V1 can be checked in a tube tester or, as an alternative, a diode known to be good can be substituted and the operation of the circuit noted.

NEGATIVE-BIASED DIODE CLAMPER.

APPLICATION.

The negative-biased diode clamper is used when it is desired to shift and hold the reference level (negative extreme for positive diode clamper, or positive extreme for negative diode clamper) of the applied signal to some negative value.

CHARACTERISTICS.

Establishes a d-c reference level of a signal, but does not affect its amplitude.

The reference level is always a negative value equal to the bias voltage.

Input and output voltages are in phase.

Uses a diode, an r-c network, and a bias voltage supply.

A negative-biased diode clamper may be used as either a positive or negative clamper.

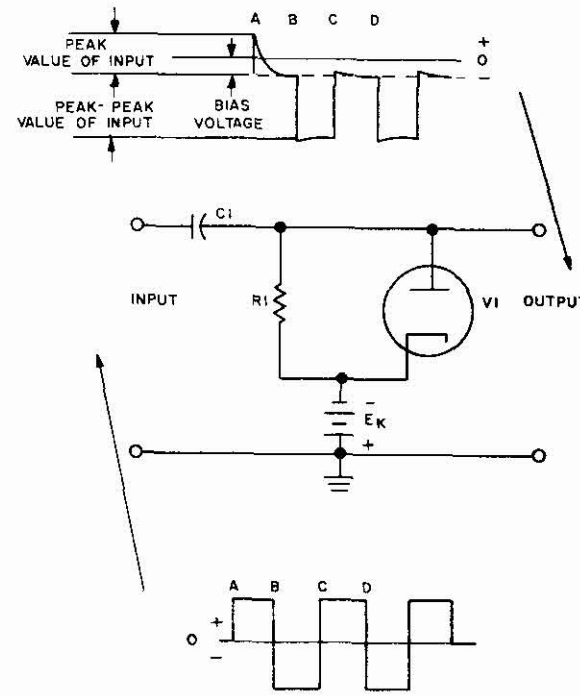
CIRCUIT ANALYSIS.

General. A diode clamper (positive or negative) is connected so that whenever the signal swings in one direction (positive direction for negative clamping—negative direction for positive clamping) diode V1 conducts to produce a short r-c time constant; whenever the signal swings in the opposite direction diode V1 does not conduct, and this results in a time constant dependent on a resistor in parallel with the diode and coupling capacitor C1, which is long with respect to the time constant of the resistance of the diode and the coupling capacitor. Thus, two different time constants are produced; a short time constant when V1 is conducting and a long time constant when V1 is not conducting.

The output voltage is obtained across the parallel combination of the diode and the resistor. During the short time constant all of the input signal voltage is developed across the coupling capacitor and none is developed across the diode and resistor, and thus no output is developed. During the long time constant, practically none of the signal voltage is developed across the coupling capacitor and practically all of the signal voltage is developed across the resistor and diode, and thus practically all of the signal appears at the output.

The clamping level is dependent on the input voltage value; normally the clamping occurs at a zero voltage reference level and extends in a positive or negative voltage direction to a voltage value equal to the peak to peak input voltage. With the insertion of a negative bias voltage the reference level is shifted in a negative direction. A negative or positive diode clamper having a negative bias will have the minimum negative voltage of the output at a reference level equal to the value of the bias voltage.

Circuit Operation. A negatively biased negative diode clamper is shown in the accompanying illustration. Capacitor C1 and resistor R1 form an r-c coupling network and determine the long time constant associated with the circuit. Electron tube V1 is an indirectly heated cathode type of diode. This diode during the time of its conduction, shunts R1 and together with capacitor C1 determines the short time constant of the circuit. Voltage source E_K provides a negative bias voltage which alters the reference level from zero to a negative reference level equal to the bias potential.



Negatively Biased Diode Clamper

The input waveform shown in the accompanying illustration is a typical square wave. Prior to point A on the signal voltage waveform there is no input voltage. Prior to point A on the output voltage waveform, the output voltage is maintained at the bias voltage value. At point A the first leading edge of the input square wave occurs. Since C1 cannot instantaneously charge to this value, the full signal voltage appears on the plate of V1. The output voltage at point A is the algebraic addition of the voltage across V1 and the negative bias voltage. Capacitor C1 charges rapidly, however, because of the very small time constant (with respect to the frequency of the input signal) of C1 and the small resistance of V1 during its conduction. The output voltage diminishes to the bias voltage at the same rate that C1 charges. This voltage diminishes well before point B is reached. Then the input signal reaches point B, capacitor C1 again cannot change its charge instantaneously, and a high negative voltage appears on the plate of V1. Therefore, diode V1 does not conduct and all the voltage appears across R1. The output voltage at

point B is the algebraic sum of the negative voltage across R1 and the negative bias voltage.

During the pulse period between points B and C, capacitor C1 discharges slightly through R1 for the duration of the negative pulse. Since the time constant of R1 and C1 is large, however, only a slight amount of this voltage leaks off. The amount of the voltage that discharges through R1 subtracts from the voltage originally applied across R1 at point B. Hence, at point C the initial negative charge is less than at point B, accounting for the dip in the waveform.

When point C is reached and the input signal rises in a positive direction V1 conducts, and capacitor C1 again cannot respond instantaneously to the rapid change. Hence the full voltage appears across the diode. The output voltage this time, however, is not only the voltage across V1 plus the bias voltage but it is this algebraic addition minus the voltage that is present across R1. Since the voltage across R1 has been reduced by the discharge of C1, the voltage across R1 is less than the voltage across V1 by the amount of voltage that has leaked off C1 at point C. The output voltage at point C is then slightly more positive than the bias. This produces the slight positive peak on the waveform at point C, since the anode of V1 is more positive than the cathode, V1 conducts and quickly charges, removing the small pip caused by the initial surge across V1. The output voltage then drops to that of the bias voltage for the remainder of the pulse width, period C to D on the waveform. When point D is reached the action is the same as that occuring at point B and the cycle repeats.

By reversing the diode in the illustrated circuit, the circuit becomes a negatively-biased positive diode clamper. The positive diode clamper normally has a positive output with a zero reference level. By inserting the negative bias, the reference is shifted to a negative voltage value equal to the bias voltage.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the negatively biased negative or positive diode clamper circuit, the failure analysis is limited to several possible failures. Before checking for failures within the clamper circuit, check the input signal to determine whether it is present and of correct waveshape and amplitude. If the signal is present and correct, the fault must exist in the clamping circuit. In many cases, a d-c potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage divider action to occur. Since capacitor C1 is connected in series with resistor R1 a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. Furthermore, in this case it is likely that diode V1 will conduct at all times. Check coupling capacitor C1 for leakage.

If the bias supply were to open, no output would be obtained. If the bias supply voltage became shorted, an output would exist, but the reference level would be shifted to zero instead of some negative value.

If the resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input signal is subject to changes in amplitude. If the resistor R1 decreases considerably, distortion of the output waveform will occur because of the decreased r-c time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since there are only four components in the circuit there should be little difficulty in determining the faulty component. Resistor R1 may be measured with an ohmmeter to determine if its value is within the acceptable tolerance. Capacitor C1 may be checked with a capacitor analyzer or by measuring the voltage from one plate of C1 to ground and then the other plate of C1 to ground (if the voltages measured are equal the capacitor is shorted). Bias voltage source E_K may be checked with a voltmeter. If after all known good bias supply, or with a voltmeter. If after all the components have been checked the trouble still persists, diode V1 must be at fault. A low reverse resistance is also an indication of a defective diode.

POSITIVE-BIASED DIODE CLAMPER.

APPLICATION.

The positive-biased diode clamper is used when it is desired to shift the reference level of the applied signal in a positive direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Output waveform varies between the positive reference level and a voltage equal to the sum of, or the difference between, the peak to peak amplitude and the positive reference voltage.

Establishes a d-c reference level for the waveform, but does not affect its amplitude.

Input and output voltages are in phase.

Uses a diode, an r-c network, and a bias supply.

A positive bias may be used with both positive and negative clampers.

CIRCUIT ANALYSIS.

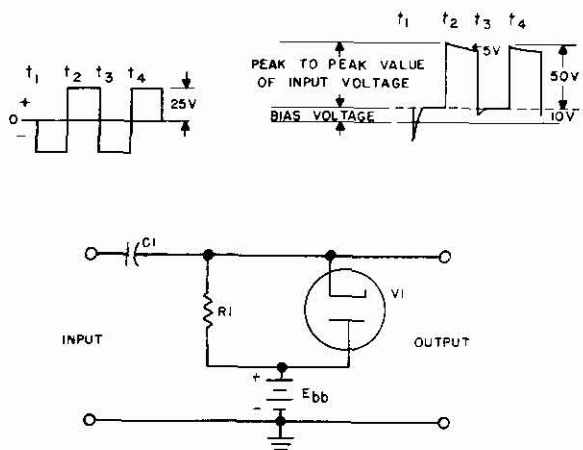
General. A diode clamper (of either positive or negative type) is connected so that whenever the waveform swings in one direction (positive direction for negative clamping and negative direction for positive clamping) the diode conducts to produce a short r-c time constant; whenever the waveform swings in the opposite direction the diode does not conduct, and this results in a time constant dependent on the r-c network which is very long with respect to the short time constant formed by diode V1 and capacitor C1.

The output voltage is taken across the parallel combination of the diode and the resistor to ground. During the short time constant, all of the signal voltage appears

across the coupling capacitor and no voltage appears across the diode, or the resistor, and thus no voltage appears at the output. During the long time constant practically none of the signal voltage appears across the coupling capacitor and practically all of the signal voltage appears across the resistor, and thus practically all of the signal appears at the output.

The clamping level is dependent upon the input voltage value, normally being clamped at a zero voltage reference level and extending in a positive or negative voltage direction to a voltage value equal to the peak to peak input voltage. With the insertion of a positive bias voltage the reference level is shifted in a positive direction. A positive diode clamper (biased positive) will have its lowest positive value as the reference level. A negative diode clamper (biased positive) will have its highest positive value as the reference level. The reference level will be, in any case, a value equal to the value of the bias voltage.

Circuit Operation. A positively biased positive diode clamper is shown in the accompanying illustration.



Basic Biased-Positive Diode Clamper

Capacitor C1 and resistor R1 form an r-c coupling network and determine the long time constant associated with the circuit. Electron tube V1 is an indirectly heated cathode-type of diode. This diode, during the time of its conduction shunts R1, and together with C1 determines the short time constant associated with the circuit. Voltage source Ebb provides a bias voltage which changes the reference level from zero to a positive level equal to the bias potential. The illustrated input waveform is a typical square wave with times t_1, t_2, t_3 and t_4 occurring at the leading and trailing edges of the waveform where the signal changes from positive to negative levels and vice versa. Prior to application of the input voltage at time t_0 the output voltage is maintained at the positive bias voltage level, that is at, say +10 volts. At time t_1, the negative-going leading edge of the square wave input pulse occurs. Since coupling capacitor C1 cannot change its charge instantly the total input voltage appears across resistor R1, and produces a negative spike of output voltage. Since V1's cathode is now driven negative with respect to the anode, diode V1 conducts. The amplitdue of the output signal at this instant is a -25 volt peak of input voltage plus a positive 10 volts bias, which add algebraically to an effective -15 volts output amplitude. When V1 conducts, the short time constant quickly discharges C1 and the negative spike drops to the bias level remaining at this value for the remainder of the pluse width. In this instance the effective zero level is not zero but is the positive bias level. Meanwhile, diode V1 is conducting lightly because of the positive bias, and creating the flat (bottom) portion of the output pulse for the time remaining between t_1 and t_2. At time t_2, the input waveform becomes positive-going and swings to the full 50 volt peak value. Again C1 cannot change its charge instantly, so the full voltage appears across R1. The output voltage now rises to +60-volts, the sum of the peak input voltage (+50) and the bias (+10). During this time the cathode of V1 is now more positive than the anode and conduction ceases. During the period between t_2 and t_3, C1 charges slowly through the long time constant supplied by R1. At time t_3 the second input pulse ends and the negative-going trailing edge causes the output voltage to drop 50 volts. Because of the small charge through the long time constant circuit, this voltage overshoots the bias level, and drops to +5 volts instead of the normal bias value of +10 volts. This occurs because capacitor C1 is charged 5-volts during the pulse width because of the long time constant. Hence, although the initial output voltage is 60 volts at time t_2, it drops to 55 volts by time t_3, due to the charging of C1. Therefore, when the negative 50 volt swing occurs at t_3, the output level drops to +5 volts. Thus an effective 5-volt negative overshoot is produced at the bottom of the waveform. The negative overshoot drives diode V1 into conduction which quickly discharges C1 to the bias level and eliminates the overshoot pip. The out put now remains at the +10 bias level for the remainder of the flat (bottom) portion of the waveform. At time t_4 the waveform again changes direction and a positive-going signal is applied. The cycle now repeats, and thus the negative portion of the waveform is held clamped to the positive bias level for the duration of the input signal. The distortion shown in the illustration of the waveform is exaggerated to facilitate the understanding of circuit action. In practice, the time constant of C1 and R1 is sufficiently large that very little distortion of the waveform occurs.

By reversing the diode in the illustrated circuit, the circuit now becomes a positively biased negative diode clamper. The negative diode clamper normally has a negative output with a zero reference level. By inserting the positive bias the reference level is shifted to a positive voltage value equal to the bias voltage.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the positively biased positive or negative diode clamper circuit, the failure analysis is also simple and is limited to only a few possible failures.

Initially, the input signal should be checked to determine whether it is present and of correct waveshape and amplitude. If the bias battery or supply voltage should become open no output would be obtained. If the bias supply voltage should become shorted, an output would exist but the reference level would be shifted to zero instead of some positive value. In many cases, a d-c potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage divider action to occur. Since capacitor C1 is in series with resistor R1 a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. If the value of R1 decreases considerably, distortion of the output waveform will occur because of the decreased r-c time constant, and as a result, undesirable spikes will be present in the output waveform.

There should be little difficulty in determining the component at fault, since there are only four components in the circuit. Resistor R1 may be measured with an ohmmeter to determine if the value is within tolerance. Capacitor C1 may be checked with a capacitor analyzer or by measuring the voltage from each plate of C1 to ground (if the voltages measured are equal, the capacitor is shorted). If every other component has been checked and the trouble still exists, diode V1 must be at fault.

TRIODE CLAMPER.

A clamping circuit, which is sometimes referred to as a d-c restorer, or a base line stabilizer in other publications holds either extreme of a waveform to a given reference level.

All clamper circuits are dependent on two time constant circuits required to establish the reference level to which the output is clamped, one a long time constant circuit and the other a short time constant circuit. The long time constant circuit is developed by the input coupling capacitor and a resistor, which is shunted by a diode. The short time constant circuit is developed by the input coupling capacitor and the resistance of the diode during the time of its conduction. Whether the clamper is clamped in the positive or negative direction depends upon to which element of the diode the coupling capacitor is connected. If the capacitor is connected to the cathode of the diode the clamping circuit will clamp in a positive direction. If the capacitor is connected to the plate of the diode the clamping circuit will clamp in a negative direction.

Although a diode is sufficient to provide clamping action, is relatively inexpensive, and requires less space and associated circuitry than tubes with more elements, it sometimes become advantageous to use triodes in certain applications. A basic single-tube triode clamper, will provide a higher peak to peak output voltage for a given input voltage

It is necessary that in a basic single-tube triode clamper as in most other triode circuits, that an input coupling capacitor be connected to the grid of the tube in order to prevent d-c coupling. In the case of the basic single-tube triode clamper, the grid of the tube acts as the plate of an effective diode in a diode clamping circuit. Thus with the input coupling capacitor connected to the effective plate of the diode, negative clamping is obtained. However, due to the phase inversion of the input and output signals of an electron tube, positive clamping is obtained at the plate of the triode.

Another type of triode clamper, which uses two triodes, rather than one is the synchronized triode clamping circuit. This is used in rotating radial sweep radar applications, where a trapezoidal voltage is needed to produce the sweep. The trapezoidal sweep voltage varies above and below a reference line. In addition, the voltage that occurs between sweeps varies in magnitude, from cycle to cycle. As a result, each sweep occurs at a different point on the screen due to the effect of this difference in voltage between sweeps. The synchronized clamper prevents this condition. It is necessarily a two-way clamping circuit because the voltage to be clamped must be clamped both above and below a reference line. The circuit is made inoperative during sweeps, by synchronizing pulses, so that no clamping occurs during the sweep time. Between sweeps, the clamper operates and clamps these undesirable variations in voltage to a reference line from a positive and negative direction. The sychronized triode clamper, and the single triode clamper are discussed separately in the following paragraphs.

BASIC SINGLE-TUBE CLAMPER.

APPLICATION.

A basic single-tube clamper is used where it is desired to obtain amplification of the input signal as well as clamp one extreme of the signal.

CHARACTERISTICS.

Clamping is accomplished between the grid and the cathode, the grid acting as a diode plate.

Clamping between the grid and the cathode can only be in a negative direction, since the coupling capacitor must be connected to the grid of the triode.

Output taken from the plate of the triode will be clamped in a positive direction.

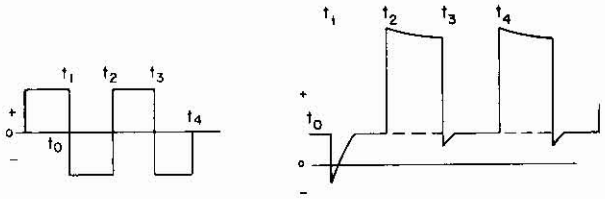
CIRCUIT ANALYSIS.

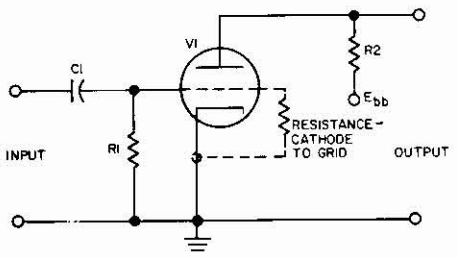
General. The circuit operation of the basic single-tube triode clamper is largely similar to that of the diode clamper. In the triode clamper, the control grid serves the

same function as the diode plate in the diode clamper circuit. The grid-leak bias resistor and coupling capacitor in conjunction with the grid to cathode resistance of the triode provides a means by which two time constants may be produced. These time constants enable a certain bias level to be established, which fixes the reference level to which the output level is clamped.

The grid is maintained at a negative voltage, and since the plate voltage varies inversely and is of opposite polarity, the output voltage is clamped at a positive reference level. The action of the triode also provides amplification of the input signal.

Circuit Operation. A basic single-tube triode clamper is shown in the accompanying illustration. C1 and R1 are the input coupling capacitor and the grid leak bias resistor, respectively. They form the long time constant circuit associated with the clamper. The cathode to grid resistance of triode V1 during the time of maximum conduction along with C1 form the short time constant circuit associated with the clamper. R2 is the plate load resistor, which also provides the proper dc plate voltage to the plate of V1.

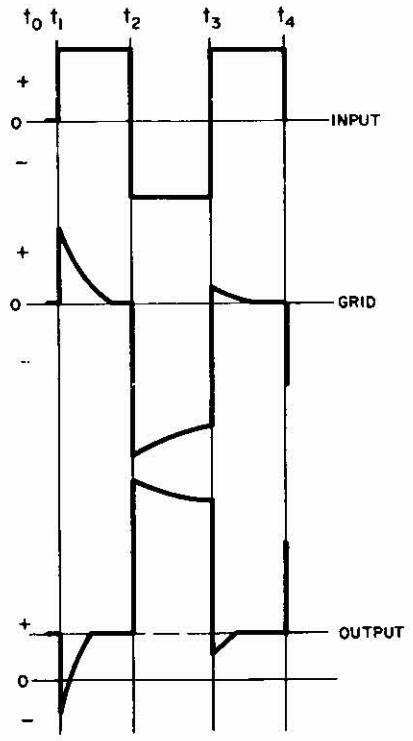




Basic Single-Tube Triode Clamper

The input signal is a typical square wave, having equal positive and negative amplitudes as shown in the accompanying illustration. Prior to the application of the square wave at time t_0, the output voltage is held at a certain level due to the plate voltage being developed across the plate load resistor R2. This voltage value constitutes the reference or clamping level of the output voltage. Times t_1 and t_3 represent the leading edges, and times t_2 and t_4 represent the trailing edges of the input square wave.

At time t_1, the first positive-going leading edge occurs and appears at the grid of V1. Since capacitor C1 cannot



Clamper Waveforms

immediately change its charge the entire voltage appears across R1. Grid current immediately flows from cathode to grid and begins charging capacitor C1. The time required to charge C1 is very short because of the low cathode to grid resistance of V1. As C1 becomes fully charged, the grid side of C1 becomes negative, and the grid is at the same negative potential. This charging action continually reduces the amount of tube conduction from the time of the initial application of the leading edge of the square wave to the time where C1 becomes fully charged. This varies the plate output voltage from some negative value to some positive value (the reference level) where it remains constant for the duration of the pulse, until the trailing edge of the input waveform is reached at time t_2. At t_2, the negative-going trailing edge of the input signal causes a negative voltage to appear across R1 and on the grid of V1. The negative grid swing causes the plate current to reduce, and the plate output voltage, therefore, rises to nearly the full value of the supply (goes positive). At this time, the input signal reaches its maximum negative swing and the output voltage reaches its maximum positive swing. For the duration of the pulse to time t_3 a long time constant path is offered through R1 to discharge C1, since V1 is no longer conducting from grid to cathode (no grid current is flowing). Because

of the long time constant and the relatively short pulse width time, C1 discharges only slightly before the next positive leading edge of the input signal appears at t_4. Thus the output signal drops a few volts. At time t_3 the positive-going input signal drives the grid of V1 positive so that grid current flows. Meanwhile the increased plate current causes the plate voltage to drop below the clamping level because of the slight loss of voltage during the discharge period. Actually, during this period, the grid voltage is driven above zero bias into the positive region and conduction through the short time constant path through the grid to cathode current quickly charges C1 to the clamping level, and removes the overshoot dip on the grid waveform. Thus, the dip in current below the clamping level in the plate circuit is minimized by grid current drawn by V1, and the plate current then remains constant until the trailing edge of the input pulse at t_4. At t_4 the cycle again repeats, and action is the same as described for the period between t_2 and t_4. Actually, the distortion shown in the illustration of the output waveform is exaggerated to facilitate understanding circuit action. In practice the time constant of C1 and R1 is sufficiently large that very little distortion of the waveform occurs.

FAILURE ANALYSIS.

No Output. If a square wave signal within the design limitations of the triode clamping circuit is applied to the input of the circuit a "no output" condition may be the result of no plate voltage existing at the plate of V1. This may be due to a faulty plate supply voltage source or due to an open plate load resistor, R2. The only other faulty component that would result in a "no output" condition is a faulty triode V1.

In order to determine which component is the cause of the "no output" condition, first check to see, with an oscilloscope, if the correct input signal is applied. If a correct signal is applied, check for the presence of plate voltage. If no plate voltage is present, check resistor R2 with an ohmmeter. If R2 is an acceptable value of resistance, check the plate supply voltage source with a high resistance voltmeter to determine if any plate supply voltage exists. If there is no plate supply voltage, try to adjust the source for the correct voltage value. If all these components have been checked and the "no output" condition still exists the triode must be faulty.

Low or Distorted Output. If a "low or distorted output" condition exists it may be due to the square wave input signal not being within the design limitations of the triode clamping circuit. This condition may also be due to any of the following component failures: open or shorted input capacitor C1, open or shorted grid leak resistor R1, shorted plate load resistor R2, incorrect value of plate EBB, or a defective triode V1.

To determine why the output is low or distorted, first check the square wave input signal with an oscilloscope. Check the capacitor C1 with an in-circuit capacitor checker to determine if it is open, or measure the voltage from both sides of C1 to ground to determine if C1 is shorted. (If the measured voltages are equal the capacitor is shorted.) Check resistor R1 with an ohmmeter. If resistor R1 has an acceptable resistance value, check resistor R2 with an ohmmeter. If resistor R2 has an acceptable resistance value, measure, the value of the plate voltage supply, Ebb, with a high resistance voltmeter. If the plate supply voltage is incorrect, try to adjust the plate voltage supply source for the correct voltage value. If all these components have been checked and the "low or distorted" condition still exists, the triode must be defective.

SYNCHRONIZED TRIODE CLAMPER.

APPLICATION.

A synchronized triode clamper is used in television and radar circuitry where it is desired to hold a signal voltage to a zero reference level and allow the signal to vary both positively and negatively from the zero reference level.

CHARACTERISTICS.

Uses two triodes connected in series.
Clamping occurs between input signal variations.
Synchronizing pulses are required.

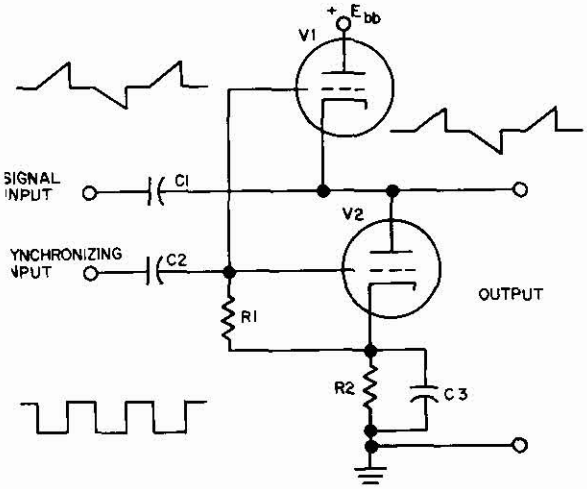
CIRCUIT ANALYSIS.

General. A synchronized triode clamper utilizes the conduction of two triodes to maintain a specific reference level during the time that no signal is present. At the time that the input signal occurs, a negative synchronizing pulse drives the triodes into a nonconducting state for the duration of the synchronizing pulse. The duration of the synchronizing pulse and the duration of the input signal are the same. Any variation in the voltage between input signals (when the triodes are conducting) changes the amount of conduction of the triodes and changes the amount of plate voltage and plate resistance of the triodes. The change in plate voltage and plate resistance is such that the output voltage is maintained at the reference level.

Circuit Operation. A typical triode clamping circuit is shown in the accompanying illustration. The input is coupled through capacitor C1 directly to the output. The series combination of triode V1, triode V2, and cathode bias resistor R2 intersects this input line (between capacitor C1 and the output) at the point where the cathode of V1 and the plate of V2 are connected. Capacitor C2 couples a series of negative synchronizing pulses to the grids of triodes V1 and V2. Resistor R1 provides a potential difference (bias) between the cathode and the grid of V2 during the time of the synchronizing pulse. Capacitor C3 is the bypass capacitor for cathode bias resistor R2.

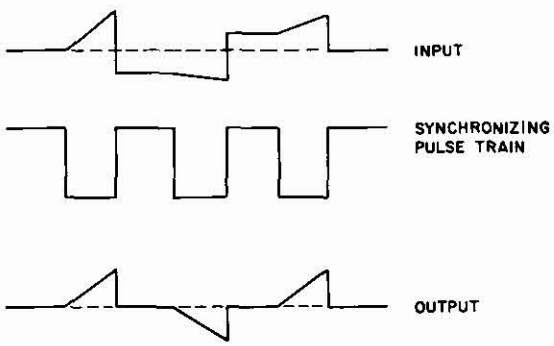
The input signal, in this case, is a series of positive and negative going sawtooth waveforms extending from the zero voltage reference line. There is a steady-state period with no signal variation between the sawtooth waveforms.

A synchronizing pulse signal is applied to capacitor C2. This synchronizing pulse signal consists of negative pulses equal in duration to and occurring at the same time



Synchronized Triode Clamper

as the sawtooth waveforms. The period between each sawtooth, therefore, is equal to the period between each synchronizing pulse. A diagram of the corresponding time and amplitude relationships of the input, synchronizing, and output waveforms is shown in the accompanying illustration.



Clamper Waveforms

At the time either a positive or negative sawtooth waveform is applied to the input of capacitor C1, a negative synchronizing pulse is applied to the synchronizing input through capacitor C2 and applied to the grids of triodes V1 and V2. This synchronizing pulse cuts off the triodes V1 and V2 for the duration of the pulse, which is equal to the period of the sawtooth waveform. When the duration of the sawtooth waveform ends, the duration of the synchronizing pulse is likewise completed, and triodes V1 and V2 return to conduction, forming a voltage divider network. This voltage divider consists of the two triodes and a cathode bias resistor R2 in a series connection, extending between plate voltage supply Ebb and ground.

If there should be any voltage at the input that varies from the zero reference line, at this time, the conduction of the triodes will vary in such a way as to compensate for the voltage variation and to maintain the output at the zero reference. If this voltage variation is positive, the voltage at the cathode of V1 and the voltage at the plate of V2 is made more positive. The increased plate voltage of V2, in most cases, is relatively ineffective in changing the amount of conduction of V2. The increased voltage at the cathode of V1, however, causes the grid voltage to appear more negative, thereby increasing the bias. (This positive increase in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2). The conduction of V1 is then reduced causing the plate resistance of V1 to increase, thereby causing a greater voltage drop across V1. With the increased voltage drop across V1, there will be less voltage available at the plate of V2, and thus at the output. This voltage decrease at the plate of V2 and at the output is equal to the positive voltage variation occurring at the input. The output voltage is, therefore, maintained at the zero reference level.

If the voltage variation, at the time that triodes V1 and V2 are in the state of conduction, is negative, the voltage at the plate of V2 and at the cathode of V1 is negative. The voltage decrease at the cathode of V1 causes the grid voltage to appear more positive, thereby decreasing the bias. (This decrease in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2.) The conduction of V1 is increased causing the plate resistance of V1 to decrease and causing the voltage drop across V1 to decrease. A more positive voltage is then present at the cathode of V1, at the plate of V2 and at the output. This voltage increase is equal to the negative voltage variation at the input. Thus output voltage is maintained at the zero reference level for a negative voltage variation as well as a positive voltage variation.

FAILURE ANALYSIS.

No Output. A "no output" condition may be due to any of the following failures: an open coupling capacitor C1, an open synchronizing pulse capacitor C2, no input signal, or no synchronizing pulse train. These failures may be located by measuring capacitors C1 and C2 with an in-circuit capacitor checker, and by observing the input signal with an oscilloscope. If either the input signal or the synchronizing pulse train is not present at the respective inputs, check the input signal source or the synchronizing pulse source with an oscilloscope. If the "no-output" condition still exists after these checks have been made, a bad connection somewhere in the circuit must be the cause.

Low or Distorted Output. A low or distorted output may be due to any of the following defects (provided the proper input signal is applied): low or no plate supply voltage, improper synchronizing pulse, open or shorted resistor R2,

open or shorted resistor R1, open or shorted capacitor C3, shorted capacitor C1, shorted capacitor C2, or, if the condition still exists after checking these components, triode V1, or triode V2, or both triodes must be defective.

To determine which of these components is at fault, first check the input signal with an oscilloscope. If the input signal is correct, proceed to the synchronizing pulse input and check the synchronizing pulse train with an oscilloscope. If either the input signal or the synchronizing signal is incorrect the trouble is not in the clamping circuit, but is in some stage prior to the clamper. If the synchronizing pulse train is correct, check the plate supply voltage with a high resistance voltmeter. If the plate supply voltage is correct, check resistors R1 and R2 with an ohmmeter. Check capacitor C3 with an in-circuit capacitor checker, or by measuring the voltage from both plates of C3 to ground. If both voltages are equal the capacitor is shorted. If all components are found to be satisfactory the fault must be in either triode V1 or triode V2, or in both triodes.

PART B. SEMICONDUCTOR CIRCUITS

DIODE CLAMPERS.

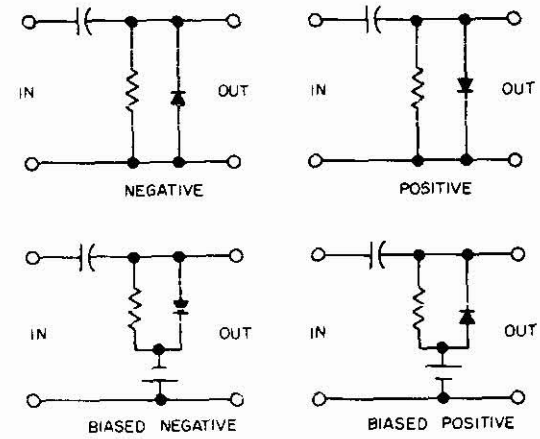
The semiconductor diode clamper is practically identical to the electron tube clamper, both circuitwise and functionally. Before proceeding, the reader should review the material on Diode Clampers in Part A — Electron Tubes in this section, as it is generally applicable to this discussion.

Like the electron tube, the semiconductor diode clamper is used to hold the input signal at a predetermined level, either above, below, or at ground level. When the positive extreme of the input waveform is held at the desired reference level, the entire waveform is effectively shifted in a negative direction from the reference level, and such action is called **negative** clamping. When the negative extreme of the input waveform is held at the fixed reference level, the entire waveform is effectively shifted in a positive direction, and such action is called **positive** clamping. When the input signal is unclamped and is symmetrical, both the positive and negative portions of the waveform vary equally above and below the reference level.

To effect clamping, the semiconductor diode is operated as a simple switch controlled by the polarity of the input waveform. In the direction of forward conduction it passes the signal, but in the direction of reverse conduction it is in effect an open circuit and blocks the signal. Although the forward resistance of the semiconductor diode is low, the reverse resistance is not infinite like that of an open switch. In fact, the reverse resistance of a semiconductor diode can be as low as 50,000 ohms. In practice, however, such low values are never used to any large extent because of the loading they present to the circuit across which they are connected. Design practice is to employ diodes with a back resistance more nearly equal to that of the conventional electron tube, which is in the megohm region. Although the almost infinite resistance of the electron tube cannot be obtained in the present type of semiconductor diode without adversely affecting the forward resistance and overall performance, fairly high reverse resistances can be obtained. As a general rule, reverse resistances of the order of hundreds of thousands of ohms are obtainable and are used.

In addition to the inherent disadvantage of a relatively low reverse resistance, the semiconductor diode also has a capacitive effect which varies with applied voltage, physical size, and composition. In most cases this capacitive effect is small enough to compare favorably with that of the electron tube diode. However, when the semiconductor diode is used as a d-c restorer at video and higher frequencies, the shunting capacitance may affect the waveform of the signal. For these reasons, the semiconductor diode is generally restricted in use to d-c bias circuits and low-frequency pulse operation.

Since the diode may be connected to operate on positive or negative signals and may also be biased positively or negatively, four basic circuit variations of the diode clamp exist, as shown in the accompanying illustration. Generally speaking, the unbiased diode circuits are not used extensively because the reverse leakage of the diode



Types of Diode Clamping Circuits

adversely affects performance; furthermore, these simple circuits are restricted to holding either the positive or the negative peak of the waveform to zero level. Thus, if it is desired to clamp the waveform at a particular point other than zero level, the biased type of clamping circuit must be used. Biased diode clamping circuits are used extensively in transistor switching circuits which operate at levels less than the limits of cutoff and saturation to obtain more precise switching. Each type of diode clamper circuit is discussed in the circuit descriptions which follow in this section.

NEGATIVE DIODE CLAMPER.

APPLICATION.

The negative diode clamper (or d-c restorer) is used where it is desired to hold, or "clamp", the positive extreme of a waveform to a zero reference level (the reference level for this circuit must be ground potential). This circuit is commonly used in radar, television, telemetering and pulse code communications equipments, and computers.

CHARACTERISTICS.

Input signal contains both positive and negative portions, but output signal consists of only a negative-going signal similar to the input signal.

Output waveform amplitude varies between ground (reference level) and some negative value as determined by the peak-to-peak amplitude of the input signal.

Input and output signals are in phase with each other.

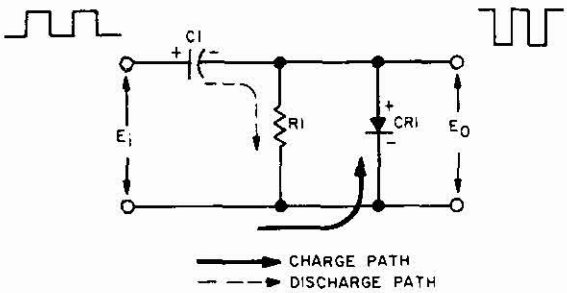
Used in conjunction with an R-C coupling network.

CIRCUIT ANALYSIS.

General. The unbiased diode clamp is usually employed as a shunt across the resistor portion of an R-C coupling circuit. By providing a low-resistance path during conduction periods and a high-resistance path during nonconducting periods, the diode provides different charge and discharge times for the coupling capacitor. When the posi-

tive portion of the input waveform causes the diode to conduct, negative clamping is produced, as described in the following paragraph.

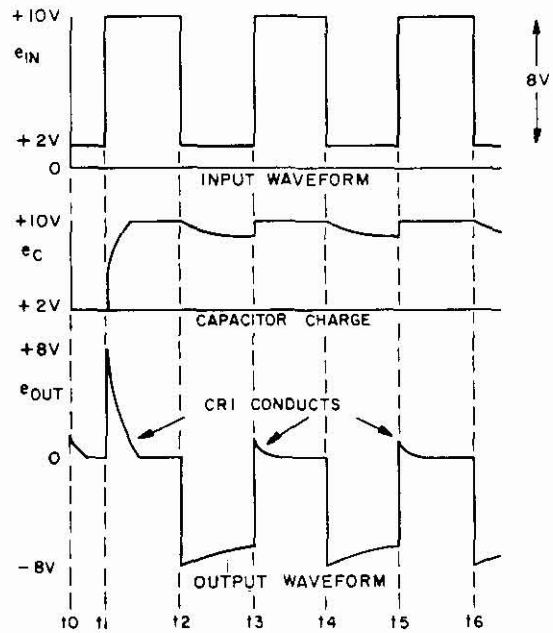
Circuit Operation. The schematic of a basic unbiased diode clamp is shown in the following illustration. As shown, C1 is the coupling capacitor of an RC coupling network. Resistor R1 is the input resistor of the network and determines the long time constant (discharge period) of the circuit. Clamping diode CR1 connected in shunt with R1 determines the short time constant (charging time) of the circuit. When a positive input signal is applied it causes CR1 to conduct, and C1 is quickly charged to the input potential. Since the output is taken from across R1 which is effectively short circuited by the conducting diode (forward resistance is only a few ohms), little or no output appears for the positive portion of any applied signal. During the negative portion of the input signal CR1 does not conduct (except for reverse leakage current) consequently the negative portion of the input signal appears as the output across R1. This circuit acts to effectively shift the entire waveform in a negative direction by holding the positive peak of the input signal to the zero level. Therefore the input waveform can only appear as a negative output. Thus the positive portion is effectively eliminated by the clamping diode.



Negative Clamp

In the accompanying illustration the input waveform is shown as a square wave for ease of explanation. Likewise, the input waveform level is considered to vary from +2 to +10 volts. Such an input signal is typical of the waveform generated at the collector of an NPN transistor multivibrator (or an electron tube). Although a square wave is used in the following explanation of detailed circuit operation, any wave shape applied to the clamper input will be negatively clamped without appreciably changing the shape of the wave (provided the R1C1 time constant is long with respect to the pulse duration).

Capacitor C1 is charged as indicated in the above illustration to a potential of +2 volts at the negative peak of the input waveform (t_0). At time t_1, the input to the clamper circuit rises 8 volts to a +10 volts. Since capacitor C1 cannot change its charge immediately, the 8 volt change appears across R1 and CR1, producing a positive spike on the output waveform. Since the anode of CR1 is now 8 volts positive with respect to its cathode, CR1 conducts and



Clamper Input and Output Waveforms

charges C1 to +10 volts. The charging of C1 occurs rapidly because of the low forward resistance of the diode, and the low forward resistance of the diode shunting R1 causes any output voltage appearing across R1 to drop to zero during time t_1 to t_2. Simultaneously, the diode stops conducting, and capacitor C1 remains in its charged condition for the duration of the pulse.

At t_2 the input signal drops 8 volts (from +10 volts to +2 volts). Since C1 is charged to +10 volts and cannot discharge immediately through the long time constant circuit created by R1, this negative-going voltage appears across R1 as a negative 8 volt output. (CR1 cannot conduct because its anode is now negative with respect to its cathode.) Thus at point t_2 on the waveform, the input voltage drops from +10 volts to +2 volts, and the output drops from zero to -8 volts. During the time interval between t_2 and t_3, capacitor C1 discharges slightly (from 8 volts to 7 volts, for example) through the long time constant path of R1.

At point t_3 of the input waveform, the input signal again rises 8 volts (from +2 to +10). Once again the charge on C1 cannot change immediately and the 8 volt positive change appears across R1. Because of the assumed 1 volt discharge through R1 between times t_2 and t_3, the 8 volt change now exceeds the capacitor charge voltage. Therefore, the output voltage overshoots the zero reference level and a positive (approximately 1 volt) signal appears across R1 and CR1. With the anode of CR1 positive with relation to its cathode, the diode conducts momentarily to replace the slight loss of charge on C1. As a result, the output voltage quickly drops to zero and remains at zero level until the end of the pulse at time t_4.

At time t_4, the input signal again drops from +10 to +2 volts. The 8 volt drop appears as a negative output across R1 causing the output voltage to drop from zero to −8 volts. Once again, C1 begins to discharge through the long time constant circuit as explained previously.

The output waveform has been purposely drawn to show a substantial decrease in voltage caused by the discharge of C1 during the duration of the negative peak of the input waveform (times t_3 to t_4 and t_4 to t_5). In practice, however, the value of R1 is relatively large so that little distortion results from the discharging of C1 or from its charging through CR1. The semiconductor diode, however, does have a much lower reverse resistance that of the electron tube. Since this back resistance is effectively connected in parallel with R1, it lowers the overall output resistance and reduces the value of the long time constant. Therefore, more distortion is produced by the semiconductor diode clamper than the tube diode.

From the explanation of circuit operation given above, it is seen that the positive extreme of the input waveform has been held or clamped to zero reference level, and that the entire waveform has been shifted negatively with respect to this reference level.

FAILURE ANALYSIS.

General. Because of the extreme simplicity of the negative diode clamper circuit, there are only a few possibilities of trouble. The capacitor, resistor, and diode can be checked for shorted or open-circuited conditions with an ohmmeter. Circuit functioning, however, must be checked with an oscilloscope to determine whether the waveform is correct and the operation is normal.

No Output. An open-circuited capacitor, a lack of input signal, or a shorted or defective diode can cause a no-output indication. Use an oscilloscope to determine whether the proper input signal is present and whether it appears across R1.

Low Output. A leaky or partially shorted capacitor can cause other than normal output. Usually such a condition will be indicated by a change in the d-c voltage measured across R1, assuming a normal input signal. A defective diode can also cause this condition, and is usually indicated by a much-lower-than-normal reverse resistance.

Distortion. Normally there should be no distortion of the output signal. Any distortion visible on an oscilloscope (with a frequency response high enough for the pulse used) indicates a change in circuit time constants due to defective components. Use an "in-circuit" type of capacitor checker to determine whether the capacitor is leaky. The remaining elements can be checked with an ohmmeter. (Be certain to observe the proper polarity when checking the diode; otherwise, an erroneous indication will be obtained.)

Clamping Level Changes. A change in the clamping level could be caused by a defective diode, a leaky coupling capacitor, C1, or a change of input pulse amplitude. As long as the input pulse amplitude is constant clamping will occur as described above. If, however, the pulse amplitude varies from pulse to pulse, the low amplitude pulses will not be properly restored. This action occurs because the low amplitude pulse is unable to reach the zero level or rise above it. Thus the diode can not operate to restore the charge lost in the discharging of capacitor C1 through the long time constant circuit between pulses. Hence the following pulse will start at some point below the zero level. If excessive, it may be possible to read a negative voltage across R1.

In the case of a leaky capacitor, the diode will conduct constantly for a positive voltage (NPN collector polarity) applied to the anode, or with a constant negative voltage (PNP collector polarity) applied it will act as a biased type clamp. This condition may be determined by making a voltage check with a VTVM connected across the output of the clamp.

POSITIVE-DIODE CLAMPER.

APPLICATION.

The positive diode clamper (or DC restorer) is used where it is desired to hold, or "clamp", the negative extreme of a waveform to a zero reference level (the reference level for this circuit must be ground potential). This circuit is commonly used in radar, television, telemetering, and computers.

CHARACTERISTICS.

Input signal contains both positive and negative portion, but output signal consists only of a positive-going signal similar to the input signal.

Input and output signals are in phase with each other.

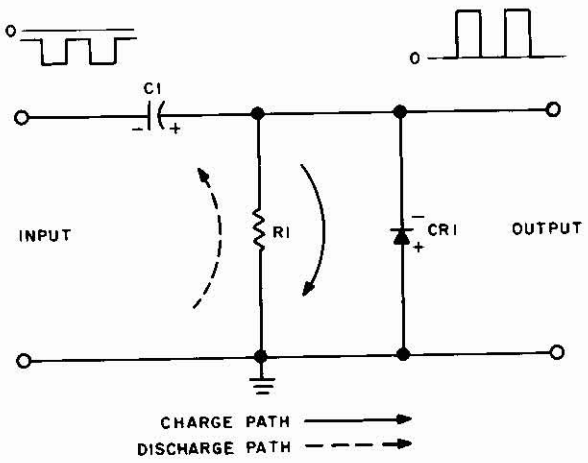
Used in conjunction with an RC coupling network.

CIRCUIT ANALYSIS.

General. The unbiased diode clamp is usually employed as a shunt across the resistor portion of an RC coupling circuit. By providing a low resistance path during conduction periods and a high resistance path during nonconducting periods, the diode provides different charge and discharge times for the coupling capacitor. When the negative portion of the input waveform causes the diode to conduct, positive clamping is produced, as described in the following paragraph.

Circuit Operation. The schematic of a basic unbiased diode clamp is shown in the accompanying illustration. As shown, C1 is the coupling capacitor of an RC coupling network. Resistor R1 is the input resistor of the network and determines the long time constant (discharge period) of the circuit. Clamper diode CR1, connected in shunt with R1 determines the short time constant (charging time) of the circuit. When a negative input signal is applied it causes CR1 to conduct, and C1 is quickly charged to the input potential. Since the output is taken from across R1, which is effectively short circuited by the conducting diode (forward resistance is only a few ohms), little or no output appears for the negative portion of any applied signal. During the positive portion of the input signal CR1 does not conduct (except for reverse leakage current) consequently

the positive portion of the input signal appears as the output across R1. This circuit acts to effectively shift the entire waveform in a positive direction by holding the negative peak of the input signal to the zero level. Therefore, the input waveform can only appear as a positive output. Thus the negative portion is effectively eliminated by the clamping diode.

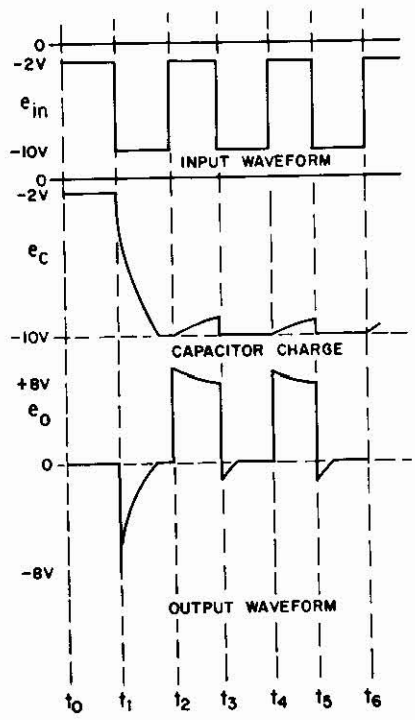


Positive Clamper

In the following waveform illustration the input waveform is shown as a square wave for ease of explanation. Likewise, the input waveform level is considered to vary from -2 to -10 volts. Such an input waveform is typical of the waveform generated at the collector of a PNP transistor multivibrator. Although a square wave is used in the following explanation of detailed circuit operation, any waveshape applied to the clamper input will be positively clamped without appreciably changing the shape of the wave (provided that the R1-C1 time constant is long with respect to the pulse duration).

Capacitor C1 is charged as indicated in the waveform illustration to a potential of -2 volts at the positive peak of the input waveform (t_0). At time t_1 the input to the clamper circuit drops 8 volts to a -10 volts. Since capacitor C1 cannot change its charge immediately the 8 volt change appears across R1 and CR1 producing a negative spike on the output waveform. Since the anode of CR1 is now effectively 8 volts positive with respect to its negative cathode, CR1 conducts and charges C1 to -10 volts. The charging of C1 occurs rapidly because of the low forward resistance of the diode, and the low forward resistance of the diode shunting R1 causes any output voltage to drop to zero during time t_1 to t_2. Simultaneously, the diode stops conducting, and capacitor C1 remains in its charged condition for the duration of the pulse.

At t_2 the input signal rises 8 volts (from -10 volts to -2 volts). Since C1 is charged to -10 volts and cannot discharge immediately through the long time constant circuit created by R1, this positive-going voltage appears across R1 as a positive 8 volt output. (CR1 cannot conduct because its cathode is now positive with respect to its anode.) Thus at point t_2 on the waveform, the input voltage rises from -10 volts to -2 volts and the output rises from zero to +8 volts. Between pulses, during the time interval from t_2 to t_3, capacitor C1 discharges slightly (say from -10 volts to -9 volts) through the long time constant path of R1.



Clamper Input and Output Waveforms

At point t_3 of the input waveform the input signal again falls 8 volts (from -2 volts to -10 volts). Once again the charge on C1 cannot change immediately and the 8 volt negative change appears across R1. Because of the previously assumed discharge of 1-volt through R1 between time t_2 and t_3, the 8 volt change now exceeds the capacitor charge voltage. Therefore, the output voltage overshoots the zero reference level, and a negative (approximately 1-volt) signal appears across R1 and CR1. With the cathode of CR1 negative with respect to its anode, the diode conducts momentarily and replaces the slight loss of charge on C1. As a result, the output voltage quickly drops to zero and remains at zero level until the end of the pulse at time t_4.

At time t_4, the input signal again increases from -10 to -2 volts. The 8 volts increase appears as a positive output across R1 causing the output voltage to rise from zero to +8

volts. Once again C1 begins to discharge through the long time constant circuit as explained previously.

The output waveform has been purposely drawn to show a substantial decrease in voltage caused by the discharge of C1 during the duration of the positive peak of the waveform (times t_2 to t_3 and t_4 to t_5). In practice, however, the value of R1 is relatively large so that little distortion results from the discharging of C1 or from its charging through CR1. The semiconductor diode, however, does have a much lower reverse resistance than that of an electron tube. Since this back resistance is effectively connected in parallel with R1, it lowers the overall output resistance and reduces the value of the long time constant. Therefore, more distortion is produced by the semiconductor diode clamper than the tube diode.

From the explanation of circuit operation given above, it is seen that the negative extreme of the input waveform has been held or clamped to the zero reference level, and that the entire waveform has been shifted positively with respect to this reference level.

FAILURE ANALYSIS.

General. Because of the extreme simplicity of the negative diode clamper circuit, there are only a few possibilities of trouble. The capacitor, resistor, and diode can be checked for shorted or open-circuited conditions with an ohmmeter. Circuit functioning, however, must be checked with an oscilloscope to determine whether the waveform is correct and the operation is normal.

No Output. An open circuited capacitor C1, a lack of input signal, or a shorted or defective diode can cause a no-output condition. Use an oscilloscope to determine whether the proper input signal is present and whether it appears across R1.

Low Output. A leaky or partially shorted capacitor, C1, can cause other than normal output. Usually such a condition will be indicated by a change in the dc voltage measured across R1, assuming a normal input signal. A defective diode can also cause this condition, and is usually indicated by a much-lower-than-normal reverse resistance.

Distortion. Normally, there should be no distortion of the output signal. Any distortion visible on an oscilloscope (with a frequency response high enough for the pulse used) indicates a change in circuit time constants due to defective components. Use an "in-circuit" type of capacitance checker to determine whether the capacitor is leaky. The remaining elements can be checked with an ohmmeter. (Be certain to observe the proper polarity when checking the diode; otherwise, an erroneous indication will be obtained.)

Clamping level Changes. A change in the clamping level could be caused by a defective diode, a leaky coupling capacitor, C1, or a change of input pulse amplitude. As long as the input pulse amplitude is constant clamping will occur as described above. If, however, the pulse amplitude varies from pulse to pulse, the low amplitude pulses will not be properly restored. This action occurs because the low amplitude pulse is unable to reach the zero level or drop below it. Thus a diode cannot operate to restore the charge lost in the discharging of capacitor C1 through the long time constant circuit between pulses. Hence the following pulse will start at some point above the zero level. If excessive, it may be possible to read a constant positive voltage across R1.

In the case of a leaky capacitor, the diode will conduct constantly for a negative voltage (PNP collector polarity) applied to the cathode, or for the opposite case (NPN transistor) it will act as a biased type of clamp. This condition may be checked by making a voltage check with a VTVM connected across the output of the clamp.

BIASED-NEGATIVE DIODE CLAMPER

APPLICATION.

The biased-negative diode clamper is used in transistorized equipment when it is desired to shift the reference level of the applied signal in a negative direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Establishes the d-c reference level of the waveform, but does not affect its amplitude.

Uses a diode in conjunction with an R-C coupling circuit.

Can clamp either extreme of the input waveform to the negative reference level, by reversing the diode.

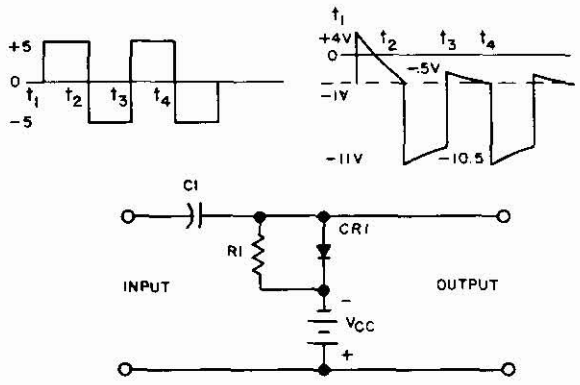
Reference level established by the amount of negative bias used.

CIRCUIT ANALYSIS.

General. The biased negative diode clamper may be of either the positive or negative type, depending upon the relative connection of the diode with respect to the bias. Under all circumstances, the reference level of the negatively-biased diode clamper will be at some negative value. If it is a negatively-biased positive diode clamper, the output waveform will start at this negative value and extend in a positive direction. If it is a negatively-biased negative diode clamper, the output waveform will start at this negative reference level, and extend in a negative direction. The circuit is comprised basically of a diode and an RC network. The diode acts as a switch, closing on one half cycle to provide a very short RC time for the capacitor, and opening on the alternate half cycle, to provide a long time constant which depends upon the size of a resistor in conjunction with the capacitor. The overall result at the output is a reproduction of the input, but shifted to a new reference level.

Circuit Operation. A typical negatively-biased negative diode clamper is illustrated below.

Capacitor C1 and resistor R1 form an RC coupling network and determine the long time constant associated with the circuit. Diode CR1, during the time of its conduction, together with C1, determine the short time constant associated with the circuit. The bias supply, VCC, alters the reference level from zero to a level equal to the bias.



Negatively-Biased Negative Diode Clamper

When the circuit is initially energized and with no signal applied to the input, the diode begins conducting because of the negative potential (Vcc) applied to the cathode. As CR1 conducts, capacitor C1 begins charging, and when its charge is equal to Vcc, the diode cuts off, since its anode and cathode potentials are now equal. The voltage at the output is at this time equal to the bias voltage Vcc, or -1 volt.

When a signal is applied, as illustrated, the following action occurs. At time t_1, the voltage increases almost instantly from 0 volts to a +5 volts. (The voltages used here are only for ease of explanation). Capacitor C1 cannot change its charge immediately (because of the property of capacitors), and the anode of CR1 suddenly becomes more positive than its cathode and begins conducting. Because C1 cannot immediately change its charge, the entire input voltage is developed across the diode, and the output, taken from across the diode, increases 5 volts in a positive direction. Because it does not start at 0 volts, but at 0 -1 volt, as shown on the illustration, the output rises to +4 volts. The conducting state of CR1 provides a very short time constant for the capacitor, however, and C1 rapidly charges to the new voltage. As C1 charges, the voltage drop across CR1 decreases, and once again reaches -1 volt when C1 is fully charged.

The output remains at this voltage until the negative swing of the input signal at time t_2. At this time the input swings from a +5 volts to a -5 volts. Again, C1 cannot immediately change its charge, but this time the diode cannot conduct, because its anode is negative with respect to its cathode. The entire input voltage is therefore developed across R1, and the output voltage changes 10 volts in a negative direction from the -1-volt reference level, or to -11 volts. Because the diode is not conducting, R1 provides a long time constant for C1 and the capacitor begins charging very slowly to the -5 volts of the input signal. The capacitor charges very slowly because of the long RC time constant, and when the input signal reaches t_3, the total output has only decreased to, for example, from -11 to -10.5 volts (the capacitor has charged to .5 volt). At time t_3, the input again rises to +5 volts, bringing CR1 into conduction. This sudden +10 volt rise also produces a +10 volt increase in the output. Since the total output is 10.5 volts at this time, a +10 volt increase brings it up to -.5 volts, which accounts for the small positive-going peak at t_3 in the output waveform. Because of the short RC time provided by CR1, the capacitor quickly charges again to -1 volt eliminating the peak, and the output remains a -1 volt until time t_4, when the cycle again repeats.

By reversing the diode, the circuit can be converted into a negatively-biased, positive diode clamper. The difference at the output then will be that the entire output waveform will be clamped above the negative bias voltage, instead of below it as in the negative clamper.

Because the reverse resistance of a semiconductor diode is lower than that of an electron tube, the type of diode used is selected to have a very high reverse resistance. This is necessary to keep the shunting effect of the reverse resistance to a minimum.

FAILURE ANALYSIS.

No Output. The absence of an input signal, or an open C1 are the only probable causes of a no-output condition. Check for the presence of the input signal with an oscilloscope. If signal is not present, the fault lies in a preceding stage, and the clamper is probably not defective. If a signal is present, check C1 with an in-circuit capacitor checker. There is also the possibility that two components such as CR1 and Vcc, or R1 and Vcc, are both shorted at the same time, thus producing a short circuit across the output. Check the bias supply with a high resistance voltmeter for proper voltage, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the special case where the diode is not completely shorted, but reads a very low resistance of, say 2000-ohms or less, it can be considered to be defective.

Low or Distorted Output. A partially shorted CR1, a leaky C1, or R1 decreasing in value can cause a low output condition to exist. Actually, the output will not be low without being distorted, nor will it be distorted without being low. Check C1 with an in-circuit capacitor checker, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the case where the diode is not completely shorted, but reads a very low resistance of, say 2000-ohms or less, it can be considered to be defective.

Change in Clamping Level. A change in the bias supply voltage, Vcc, will cause the output clamping level to change. Check for the proper value of voltage with a high resistance voltmeter.

BIASED-POSITIVE DIODE CLAMPER.

APPLICATION.

The biased-positive diode clamper is used in transistorized equipment when it is desired to shift the reference level of the applied signal in a negative direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Establishes the d-c reference level of the waveform but does affect its amplitude.

Uses a diode in conjunction with an R-C coupling circuit.

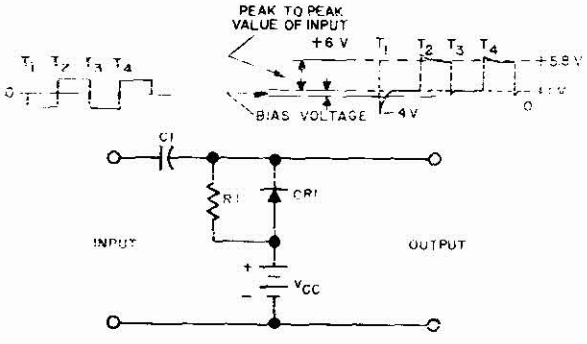
Can clamp either extreme of the input waveform to the positive reference level, by reversing the diode.

Reference level established by the amount of positive bias used.

CIRCUIT ANALYSIS.

General. The biased positive diode clamper may be of either the positive or negative type, depending upon the relative connection of the diode with respect to the bias. Under all circumstances, the reference level of the positively-biased diode clamper will be at some positive value. If it is a positively-biased positive diode clamper, the output waveform will start at this positive value and extend in a positive direction. If it is a positively-biased negative diode clamper, the output waveform will start at this positive reference level, and extend in a negative direction. The circuit is comprised basically of a diode and an RC network. The diode acts as a switch, closing on one half cycle to provide a very short RC time for the capacitor, and opening on the alternate half cycles, to provide a long time constant which depends upon the size of a resistor in conjunction with the capacitor. The overall result at the output is a reproduction of the input, but shifted to a new reference level.

Circuit Operation. A typical positively-biased positive diode clamper is illustrated below.



Positively-Biased Positive Diode Clamper

Capacitor C1 and resistor R1 form an RC coupling network and determine the long time constant associated with the circuit. Diode CR1, during the time of its conduction, together with C1, determine the short time constant associated with the circuit. The bias supply, VCC, alters the reference level from zero to a level equal to the bias.

When the circuit is initially energized and with no signal applied to the input, the diode begins conducting because of the positive potential (VCC) applied to the anode. As CR1 conducts, capacitor C1 begins charging, and when its charge is equal to VCC, the diode cuts off, since its anode and cathode potentials are now equal. The voltage at the output is at this time equal to the bias voltage VCC, or +1 volt.

When a signal is applied, as illustrated, the following action occurs. At time t_1, the input voltage increases almost instantly from 0 volts to a -5 volts. (The voltages used here are only for ease of explanation). Capacitor C1 cannot change its charge immediately (because of the property of capacitors), and the anode of CR1 suddenly becomes more positive than its cathode and begins conducting. Because C1 cannot immediately change its charge, the entire input voltage is developed across the diode, and the output, taken from across the diode, increases 5 volts in a negative direction. Because it does not start at 0 volts, but at the bias level of +1 volt, as shown on the illustration, the output decreases to only a negative 4 volts. The conducting state of CR1 provides a very short time constant for the capacitor, however, and C1 rapidly charges to the new voltage. As C1 charges, the voltage drop across CR1 decreases, and once again reaches +1 volt when C1 is fully charged.

The output remains at this voltage until the positive swing of the input signal at time t_2. At this time the input swings from a -5 volts to a +5 volts. Again, C1 cannot immediately change its charge, but this time the diode cannot conduct, because its anode is negative with respect to its cathode. The entire input voltage is, therefore, developed across R1, and the output voltage changes 5 volts in a positive direction from the +1 volt reference level, or to +6 volts. Because the diode is not conducting, R1 provides a long time constant for C1 and the capacitor begins charging very slowly to the +5 volts of the input signal. The capacitor charges very slowly because of the long RC time constant, and when the input signal reaches t_3, the total output has only decreased, for example, from +6 volts to +5.8 volt. (The capacitor has charged to .2 volt). At time t_3, the input again changes to -5 volts, bringing CR1 into conduction. This sudden change to -5 volts also produces -5 volts at the output. Since the total output is +5.8 volts at this time, a -5 volt change brings it down to +.8 volt, which accounts for the small negative going peak at t_3 in the output waveform. Because of the short RC time provided by CR1, the capacitor quickly charges again to +1 volt, eliminating the peak and the output remains at +1 volt until time t_4, when the cycle again repeats.

By reversing the diode, the circuit can be converted into a positively biased, negative diode clamper. The difference at the output then will be that the entire output waveform will be clamped above the positive bias voltage, instead of below it as in the negative clamper.

Because the reverse resistance of a semiconductor diode is lower than that of an electron tube, the type of diode used is selected to have a very high reverse resistance. This is necessary to keep the shunting effect of the reverse resistance to a minimum.

FAILURE ANALYSIS.

No Output. The absence of an input signal, or an open C1 are the only probable causes of a no-output condition. Check for the presence of the input signal with an oscilloscope. If the signal is not present, the fault lies in a preceding stage, and the clamper is probably not defective. If a signal is present, check C1 with an in-circuit capacitor checker. There is also the possibility that two components such as CR1 and Vcc, or R1 and Vcc, are both shorted at the same time, thus producing a short circuit across the output. Check the bias supply with a high resistance voltmeter for proper voltage, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the special case where the diode is not completely shorted, but reads a very low resistance, of say 2000 ohms or less, it can be considered defective.

Low or Distorted Output. A partially shorted CR1, a leaky C1, or R1 decreasing in value can cause a low output condition to exist. Actually, the output will not be low without being distorted nor will it be distorted without being low. Check C1 with an in-circuit capacitor checker, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the case where the diode is not completely shorted, but reads a very low resistance of, say 2000 ohms or less, it can be considered defective.

Change in Clamping Level. A change in the bias supply voltage, Vcc, will cause the output clamping level to change. Check for the proper value of voltage with a high resistance voltmeter.

TRIODE, BASIC COMMON-BASE CLAMPER.

APPLICATION.

The basic common-base triode clamper maintains between specific voltage levels the maximum positive and negative voltages developed at the collector of the transistor used in the clamping circuit. This circuit is usually used as a switching amplifier to maintain a constant output pulse amplitude.

CHARACTERISTICS.

Common base transistor configuration provides an output with no current amplification and no phase inversion.

Collector voltage is clamped, not the output voltage.

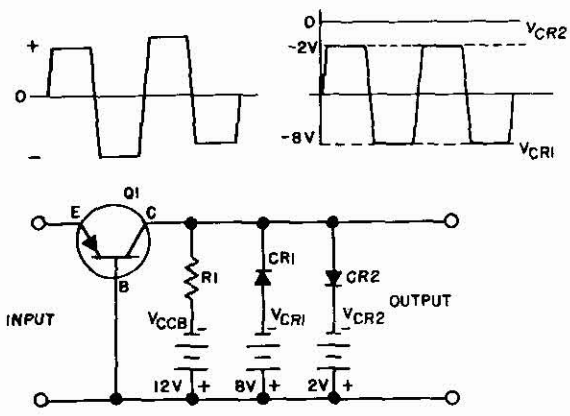
Two diodes provides clamping action.

Diode bias potentials establish minimum and maximum clamping levels.

CIRCUIT ANALYSIS.

General. The clamping action to be discussed occurs in the collector circuit of the common base connected transistor. Normally, the signal voltage in conjunction with the series combination of the collector load resistor and the collector supply voltage develops a certain collector voltage. If the input signal varies above some level, however, one of two diodes begins conducting. These diodes are connected in parallel with each other and with the collector supply and load. The conduction of the diode maintains or clamps the collector voltage at the bias value. If the signal varies below some level in the opposite direction the other diode conducts, causing the collector voltage to be maintained or clamped at another lower voltage level. During the time that the signal is between clamping levels, the collector voltage varies in accordance with the input signal voltage variation.

Circuit Operation. The circuit of the triode, basic common-base clamper used in this application is shown in the accompanying illustration.



Triode, Basic Common Base Clamper

The input signal voltage, as illustrated, is a square-wave pulse type signal which may vary from maximum to minimum amplitudes. It is applied to the emitter of transistor Q1, connected in a common base configuration. The collector voltage variation corresponds to the input voltage variation and is developed across the collector load resistor, R1, by the collector supply voltage V_{CCB}. Diode CR1 and its base voltage V_{CR_1} establish a negative clamping level, below which the collector voltage cannot go. Diode CR2 and the bias voltage V_{CR_2} establish a positive clamping level above which the collector voltage cannot go.

The input signal applied to the emitter of Q1 is amplified and in-phase when it appears as the output voltage at the collector of Q1. If the output voltage developed at the collector of Q1 is between the voltage limits of V_{CR_1} and V_{CR_2} the diodes cannot conduct. The collector voltage varies in accordance with V_{CCB} minus the output voltage developed across R1 (V_{R_1}), which depends upon the collector current. Once the input signal varies enough to cause the positive collector voltage swing to exceed the value of V_{CR_2} (assumed to be -2 volts), diode CR2 conducts because the anode is driven positive and forward-biases the diode. The collector voltage is then maintained at the value of V_{CR_2} until the signal voltage drops to a point at which the positive collector voltage swing becomes less than the voltage V_{CR_2}, at which time CR2 becomes reverse biased, stops conducting, and the collector voltage is again dependent on V_{CCB} minus V_{R_1}.

If the input signal varies enough in the opposite (negative) direction to cause the collector voltage to become the same as, or more negative than the value V_{CR_1} (assumed to be -8 volts) diode CR1 is forward-biased and conducts. The collector voltage is then maintained at the value of V_{CR_1} until the signal voltage increases to a value where the collector voltage becomes more positive than the voltage V_{CR_1}, at which time diode CR1 is reverse biased, stops conducting, and the collector voltage is again dependent on V_{CCB} minus V_{R_1}.

By clamping both the positive and negative levels, the transistor is prevented from saturating and causing hole storage effects which would increase the pulse length, or from being driven to cutoff when the input is in the other direction. It also has the advantage of not requiring special selection of transistors at the time of replacement, since the operating limits are made such that any transistor of the same type will operate satisfactorily in this circuit. This circuit is not used with sine-wave inputs except where clipping effects are desired.

FAILURE ANALYSIS.

No-Output. A no-output condition may prevail due to any of the following defects: no input signal present at the emitter of Q1, an open or shorted collector supply voltage V_{CCB}, an open collector load resistor, R1, or a defective transistor, Q1.

The location of the cause of the no-output condition may be found by first determining if an input signal is present with an oscilloscope. If the input signal is present, check collector supply voltage, V_{CCB}, with a voltmeter. If the collector supply voltage is present check resistor R1 with an ohmmeter. If all other possibilities have been checked and a no-output condition still exists, transistor Q1 can be considered defective.

Low or Distorted Output. This condition may be due to a faulty input signal. If the input signal is found to be correct by an oscilloscope the low or distorted output condition may be due to any of the following conditions: improper voltage values for, collector supply voltage V_{CCB}, bias voltage V_{CR_1}, or bias voltage V_{CR_2}; shorted or open diodes CR1 or CR2; or a load resistance (R1) which is not the proper resistance value; or a defective transistor, Q1.

To determine which of the possible causes of the low or distorted output condition is responsible; first, check the voltage values V_{CCB}, V_{CR_1}, and V_{CR_2} with a high resistance voltmeter. If any of these values is incorrect adjust the particular voltage source for the proper value. If these voltages are correct, check diodes CR1 and CR2 with an ohmmeter. If the diodes are good, the ohmmeter will read zero resistance when placed across the diode in a forward direction, and will read infinite resistance or a very high resistance when placed across the diode in the reverse direction. If the diodes are good, check resistor R1 with an ohmmeter. If all of the preceding items have been checked and found satisfactory, transistor Q1 must be the faulty component.