NAVAER 16-1-519
SUPPLEMENT NO. 2

N-44599
Supp 2

1

Handbook
PREFERRED CIRCUITS
Navy Aeronautical Electronic Equipment

PREPARED BY [redacted]

4608 NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
FOR
BUREAU OF AERONAUTICS
DEPARTMENT OF THE NAVY

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SUPPLEMENT NO. 2 (DATED APRIL 1, 1959) HANDBOOK PREFERRED CIRCUITS

INSTRUCTION SHEET

INSTRUCTIONS FOR INSERTING SHEETS DATED APRIL 1, 1959 IN HANDBOOK PREFERRED CIRCUITS AND REMOVING INCORRECT OR OBSOLETE SHEETS

REMOVE	INSERT
Table of Contents, pp. xi and xii, dated Aug. 1, 1958.	Table of Contents, pp. xi and xii, dated April 1, 1959.

PART 1. PREFERRED CIRCUITS MANUAL

PC 79, pp. 79-2—79-9, dated April 1, 1959.
PC 101, pp. 101-2—101-9, dated April 1, 1959.
PC 102, pp. 102-2—102-10, dated April 1, 1959.
PC 250, pp. 250-2—250-6, dated April 1, 1959.
PC 251, pp. 251-2—251-4, dated April 1, 1959.

PART 2. NOTES TO THE PREFERRED CIRCUITS MANUAL

16. Crystal Oscillators, pp. N16-1—N16-4, dated April 1, 1959.

POWER SUPPLY VOLTAGES FOR TRANSISTORS

A supplement to MIL-STD-706,* which will include regulated power supply voltages for transistors, is under consideration. The voltages which appear most likely to be adopted are 1.5, 3, 6, 12, 25, 50, and 100 volts, positive or negative. These are the power supply voltages which are used in the transistor circuits in this manual.

*MIL-STD-706, 23 December 1958, establishes nominal values for regulated direct current power supply voltages within the range of 100 to 500 volts for use in military electronic equipment. This standard provides in part as follows: "Nominal values of all regulated direct current voltages within the range of 100 to 500 volts, positive or negative, shall be selected from the following list: 100 volts, 150 volts, 250 volts, 300 volts, and 450 volts."

ERRATA
TO SUPPLEMENT 1
OF
HANDBOOK PREFERRED CIRCUITS
NAVAER 16-1-519

Page 1–2, on schematic diagram:
Add "A" to make V1 read "6080WA"

Pages 3–2, 4–2, and 5–2, under "Notes" at bottom of each page:
Change Note 1 on each page to read: "Either output terminal may be grounded; however, the positive input terminal must not be grounded."

Page 6–2, under the heading "Components," lines 3 and 4:
Change the first word of each line to "All"

Page 6–3, figure 6–1:
Delete: Scale—2″=1″

Page 7–3, under "Operating characteristics, Input voltage, E_1:"
Change "Minimum 290 volts dc" to "Minimum 300 volts dc"

Page 7–3, under "Notes" at bottom of page:
Change Note 2 to read: "Either output terminal may be grounded; however, the positive input terminal must not be grounded."

Page 8–3, under "Notes" at bottom of page:
Change Note 3 to read: "Either output terminal may be grounded; however, the positive input terminal must not be grounded."

Page 8–6, right column, last sentence:
Change "An input voltage ripple of 1 volt" to read: "An input ripple of 10 volts together with a screen-supply ripple of 1 volt"
The sentence should read: "An input ripple of 10 volts together with a screen-supply ripple of 1 volt results in an output ripple of less than 1 millivolt."

Page 53–2, under the heading "Output", last 3 lines:
Right column: Before "dc", insert the word "variable"
Right column: Change "20 to 150 volts" to "±10 to ±75 volts"
Left column: Change "Range center" to "Average level"

Page 53–7, right column, line 9 of text:
Change "first" to "second"

Page 53–11, left column, next to last line of text:
Change "—250" to "—230" so that the text reads: "(—50 to —230 volts)"

Page 53–13, left column, second equation from bottom and third line from bottom, and in right column, second equation from top:
Change "mc/sec^2" to "megacycles-per-second per second"

Page 70–3, under "Notes:"
In Note 2, change "fixed winding" to "fixed phase winding"

Page 71–2, under "Notes:"
In Note 2, change "a gain" to "an amplification"

Page 74–7, right column, line 7:
Change "and 74–6" to "or 74–6"

Page 74–9, figure 74–10:
In the box, add "PC 74" so that the label in the box reads: "PC 70 AND PREAMPLIFIER PC 74."

Page 74–10, left column, last paragraph of section 4.3, line 5:
After the sentence ending in the word "point," add the sentence: "C1 is a polystyrene or other low leakage capacitor."

April 1, 1959

Page 74–10, figure 74–12:

In the box, add "PC 72" so that the label in the box reads: "PC 70 AND PREAMPLIFIER PC 72."

Page 74–10, left column, heading of section 4.4:

Add "DC" so that the heading reads: "DC Differentiating Servo"

Page 74–11, right column, lines 9 and 10:

Delete "produce a voltage which is in phase with the error signal" and substitute "be small"

Page 201–2, under "Operating characteristics," lines 11 and 12:

Change to read: "Maximum amplification variation with temperature of +150° C and −50° C, respectively.[4]"

Page 202–3, figure 202–1:

Delete: Scale −2″ =1″

Page 204–4, left column, line 12:

Change "misroammeter" to "microammeter"

Page 202–6, right column, line 3:

After "60 ohms" add the word "maximum"

Page N13–1, right column, sec. 13.2(a), line 1:

Delete the words "mixers and"

Page N13–3, right column, 3rd, 9th, and 11th lines from bottom:

In each line, change "2D21" to "search stopper"

Page N13–4, left column, 5th line from bottom:

Change "2D21" to "search stopper"

Page N13–7, right column, line 10:

Change "one-fifth" to "one-fiftieth"

Page N13–8, figure N13–4(f):

Change labeling on curves as follows:

T_1, change 30.42 to 30.22

T_0, change 30.35 to 30.15

ERRATA TO ORIGINAL HANDBOOK PREFERRED CIRCUITS.

The following changes should be made in the original Handbook Preferred Circuits, NAVaer 16–1–519. (A previous list of changes for incorporation in the Handbook was issued under date of June 22, 1956.)

Page 64–2, under "Notes:"

In Note 1, change "potentionmeter" to "potentiometer"

Page N2–7, figure N2–13:

In the ordinate, transpose the words "maximum" and "minimum" so that the ordinate reads: "Ratio of minimum to maximum plate current"

Page N2–8, right column, equation for $K_2{}^{2/3}$:

Change "(2.6)" to "(3.6)"

Page N7–6

Change this page number to "N7–5."

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*Issued in Supplement No. 1.
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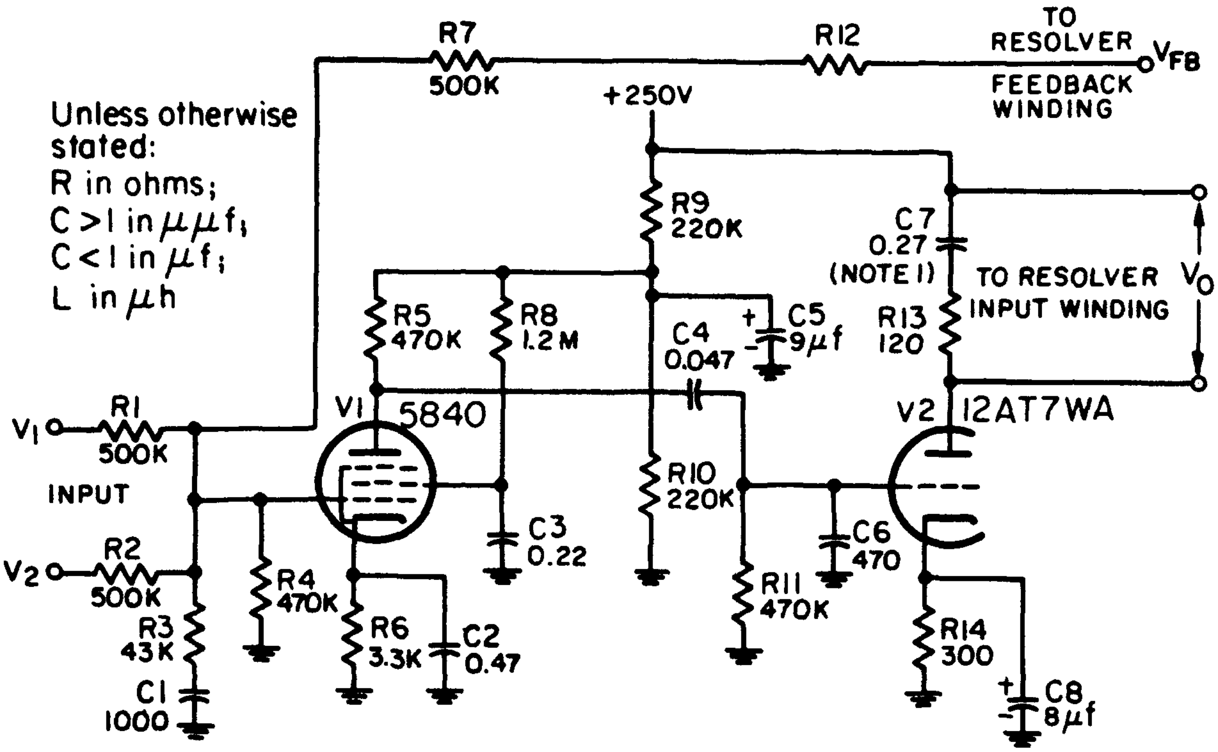
*Issued in Supplement No. 1.

†Issued in Supplement No. 2.

NBS PREFERRED CIRCUIT NO. 79
RESOLVER DRIVER

NBS PREFERRED CIRCUIT NO. 79
RESOLVER DRIVER



Components:

R1, R2, R7: The relative stability must be such that the ratio R7/R1 and R7/R2 does not change more than 0.05%.

R12=[1/300+(1−a)] R7, where a is the resolver transformation ratio.

R3,R4,R6,R12: ±5% limits; R9,R10: ±10% limits; all other R: ±20% limits.

C1,C2,C7: ±5% limits; all other C: ±20% limits. (Note 2)

Operating characteristics:

$$V_o \approx -\left(V_1 \frac{R7}{R1} + V_2 \frac{R7}{R2}\right)$$

Maximum output (5% distortion): 50 volts rms.

Stability: (Note 3)

	Lower	*Upper*
Amplification margin	14 db	12 db
Phase margin	50°	60°

Power requirements:

250 volts dc ±10% at 8.7 ma.

6.3 volts ac ±10% at 450 ma.

(For Notes, see next page)

Notes:

1. The values of C7 and R13 are determined by the operating frequency and by the resolver used. Values shown are for the Mark 4 Mod 0 resolver operating at 500 cps. (See sec. 2.2.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. Amplification and phase margin were measured with both inputs open and with the combination of tube characteristics and supply voltages which resulted in the highest value of forward amplification.

PC 79 RESOLVER DRIVER

1. APPLICATION

PC 79 was designed to drive an ac resolver having compensating windings. It is an ac operational amplifier used as an isolation amplifier and employing feedback which includes the compensating winding of the resolver. With the resolver, it is useful as a computing element in problems involving coordinate conversion, coordinate rotation, and resolution of vectors when accuracies of 0.5 percent are sufficient. The component values given (p. 79-2) are for operation at 500 cps; operation at other frequencies requires change in six component values. (See section 2.2.)

2. DESIGN CONSIDERATIONS

Compensated resolvers are readily available with a functional accuracy of ± 0.1 percent. The use of a compensating winding for the feedback places the resolver excitation loss in the feedback loop. This results in a low over-all phase shift and a constant amplification, even when the resolver copper loss changes with temperature. In addition, by proper loading of the feedback winding, the effects of any load on the rotor can be compensated.

If the resolver is to be operated at a frequency other than 500 cps, the values of C1, C2, C7, R3, R6, and R13 must be changed. In addition, the values of C7 and R13 are a function of the input impedance of the resolver. When long leads are employed between the amplifier and the resolver, and/or when the trimming resistor, R12, is included in the resolver, the resistors R1, R2, and R7 should be changed to 100KΩ. In this case, R4 should also be 100KΩ, R3 8.2KΩ, and C1 5000$\mu\mu f$.

2.1 *Feedback*: An open loop amplification [1] of 300 is obtained by adjustment of the passive feedback network between the resolver compensating winding and the grid of V1. The only component of this network that is not determined by other considerations is the grid return of V1, since the values of the input and feedback resistances (R1, R2, R7, and R12) are determined by the application of the circuit. If the desired result were achieved by the selection of the value of R4 alone, the amplitude response would fall to unity at a frequency of 7500 cps or above, with the risk that additional stray capacitance might cause the circuit to oscillate at a frequency near this point.

The lag network, R3,C1, shapes the response so that the desired amplitude and phase characteristics are obtained. The equivalent circuit for the lag network, together with its amplitude and phase characteristics, is shown in figure 79-1. The desired response is obtained by choosing values for R3 and C1 that will cause only a small phase shift at the 500 cps operating frequency and at the upper crossover frequency of 7500 cps (the frequency at which the open *loop amplification* would be 1 if the amplification fell off at a constant rate of 12 db per octave). As a result of the lag network the amplification falls to 1 at about 7500 cps with a total phase shift of 120° using nominal tubes and supply voltages. (Fig. 79-3.)

Trimmer resistor R12 is used to compensate for the finite amplification of the amplifier and for the transformation ratio of the resolver compensating winding when it is less than 1. By proper selection of the trimmer resistor, the output to the resolver can be made almost exactly equal to the sum of the input voltages (assuming that the input and feedback resistors are equal).

If *the transformation ratio* of the resolver is 1 and R12 is zero, the output of the amplifier (input to the resolver) is

$$V_o = -\left(\frac{V_1}{R1} + \frac{V_2}{R2}\right) R7 \left(\frac{A'}{1+A'}\right)$$

[1] The open loop amplification is defined as the amplification around the complete loop from any point in the circuit back to the same point; for instance, from amplifier input back to amplifier input again.

where $A'=300=\frac{R_p}{R7}A$ = open loop amplification defined in footnote 1.

A = voltage amplification between V1 grid and V2 plate

R_p = the parallel combination of R1, R2, R7, and the input impedance of the amplifier.

If R7 is now increased one three-hundredth by making R12 = R7/300, R_p will be changed very little and $A'/(1+A')$ remains $300/301 \approx 299/300$. The output of the amplifier is now

$$V_o = -\left(\frac{V_1}{R1}+\frac{V_2}{R2}\right)\frac{301}{300}\,R7\,\frac{299}{300}$$

$$= -\left(V_1\frac{R7}{R1}+V_2\frac{R7}{R2}\right)\frac{300^2-1}{300^2}$$

The error has been reduced from 1/301 to about $1/300^2$. The compensation for the finite amplification of the amplifier has no effect on the stability of the amplification with changes in the open loop amplification, A′. In either case the open loop amplification would have to decrease 23% to cause a 0.1% decrease in the output voltage.

For a resolver transformation ratio of 1, R12 should be 1.6KΩ when R7 is 500KΩ, and 330Ω when R7 is 100KΩ. When the transformation ratio is less than 1, R12 must also increase R7 by the percentage that the transformation ratio is less than 1. For a transformation ratio of 0.98, R12 must be increased by an additional 2% of R7 to give R12 = 12KΩ when R7 = 500KΩ, and R12 = 2.4KΩ when R7 = 100KΩ. R12 need not be a precision resistor since its resistance is only a very small percent of the total feedback resistance. When a number of resolver drivers are to be used interchangeably with several resolvers, the usual procedure is to make the trimmer resistor a part of the resolver. The resolvers must be trimmed individually because even a 0.01 difference in transformation ratio can change the required trimmer resistance by 100%.

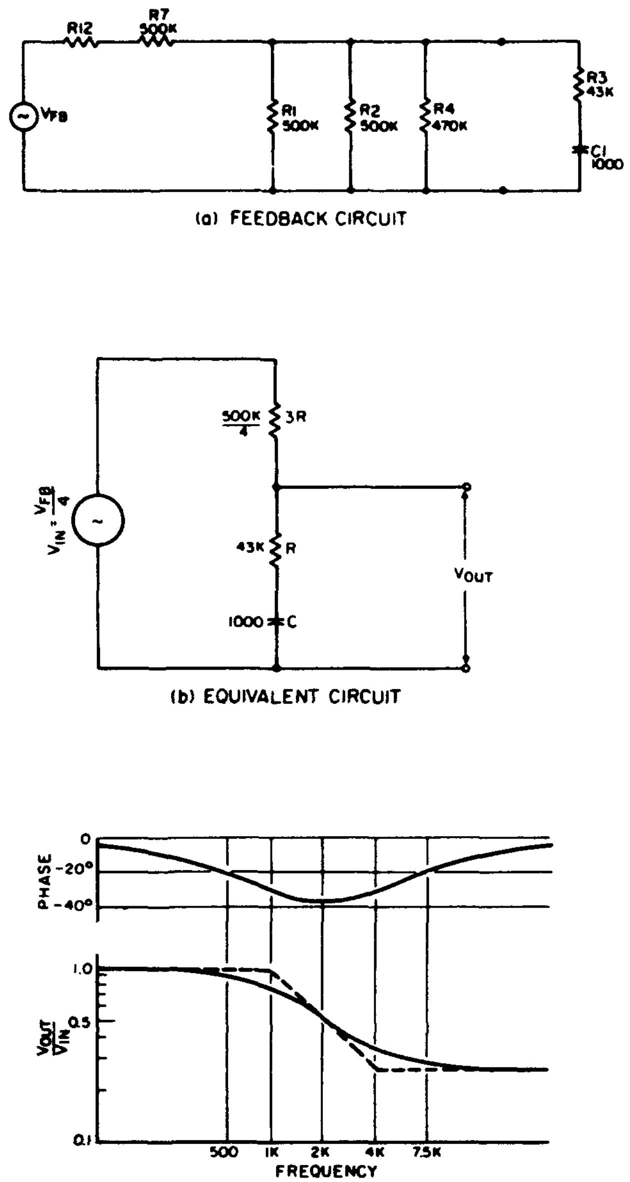


Figure 79–1.—Effect of lag network, R3,C1, on phase and amplitude response.

2.2 *Amplifier:* The amplifier circuit is basically an ac operational amplifier with minor modifications to adapt it to the resolver load.

Capacitor C7 and resistor R13 are used to obtain a unity power factor load with a Q of approximately 4 at the operating frequency. The given values of C7 and R13 (see preferred circuit, p. 79–2) are for the Mark 4 Mod 0 resolver operating at a frequency of 500 cps. For other resolvers and/or for other operating frequencies, values must be calculated to obtain the Q of 4 and unity power factor at the operating frequency for the inductance and resistance of the resolver in use. Placing the loading resistance in the capacitive branch of the circuit produces a phase response which reaches a maximum of less than 90° at a frequency about a decade above the operating frequency and then drops back to 0°. This lessens the possibility that additional stray capacitance at the higher frequencies will cause instability.

The cathode bypassing of V1 is ineffective at frequencies lower than 100 cps. This reduces the stage amplification by a factor of 4 at low frequencies and minimizes the possibility of low frequency oscillations. The value of the bypass capacitor, C2, is selected so that the angular frequency (1/R6,C2) is 0.2 of the operating frequency. The over-all effect on the phase response of the stage is similar to that of a lead network (fig. 79-2). The phase lead is about 20 degrees at the operating frequency, increases to a maximum of about 40 degrees between one

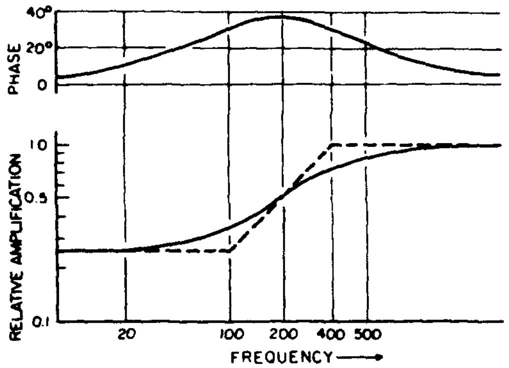


Figure 79-2.—Effect of cathode bypass capacitor, C2, on the phase and amplitude response of the first amplifier stage.

and two octaves below the operating frequency, and then falls to less than 10 degrees at the lower crossover frequency. The 20 degree lead at the operating frequency is offset by the 20 degree lag caused by the lag network, R3,C1.

3. PERFORMANCE

PC 79 was tested with the Norden-Ketay 105D2K size 15 resolver, and with minor modifications can be used with the American Electronics IR15W4-405 size 15 resolver. PC 79 can also be used with the American Electronics IR11W4-103 size 11 resolver, if R13 is changed to 240Ω and C7 is changed to 0.16μf.

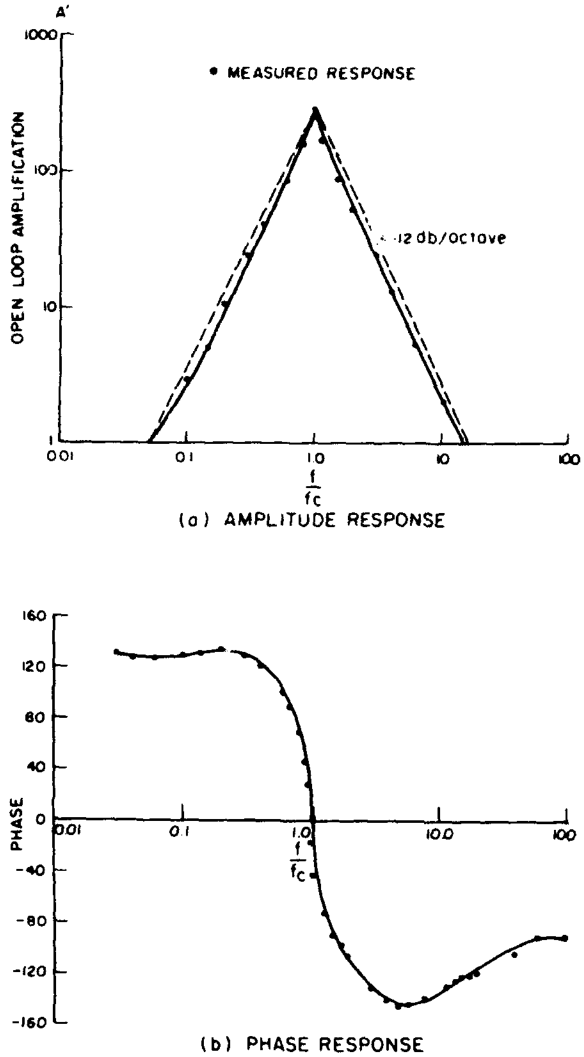


Figure 79-3.—Open loop characteristics of PC 79.

3.1 *Frequency Response:* The open loop amplification was measured by breaking the circuit at the connection to the feedback winding, inserting a signal in series with the feedback resistors, R7 and R12, and measuring the output across the resolver feedback winding. Both inputs were grounded during this measurement, representing the condition when voltage sources are connected to inputs V_1 and V_2. This is also the condition for the lowest value of open loop amplification using nominal components and voltages.

Figure 79-3 is a Bode diagram of the open loop amplification obtained under the above conditions; figure 79-4 shows the closed loop response. In the latter figure, the solid circles show the measured values of the factor $A'/(1+A')$; the open circles are values calculated using the values of A' obtained from figure 79–3. At frequencies of about 0.75 and 1.4 times the carrier frequency, the open loop amplification A' is down by a factor of 2 and distortion appears in the output at high signal levels. These frequencies are well outside the normal operating range of the amplifier. Capacitor C4 is the principal contributor to the low frequency peak, while C6 and R13 account for the rise in the response at the higher frequencies. Decreasing the resistance of R13 increases the amplitude of the peak. Shielded leads between the amplifier and the resolver contribute little to the peaks.

The gain and phase margins were measured with both inputs open, and with the combination of tubes and supply voltages that resulted in the highest forward amplification. The errors, on the other hand, were determined for the lowest forward amplification by using tubes which had reached the minimum end-of-life transconductance permitted by MIL–E–1 and supply voltages which were 10% low. At the operating frequency, the forward amplification was reduced 37.5% by the low limit tubes and an additional 12.5% by the low supply voltages. The resulting change in the open loop amplification from both causes was calculated to be 0.35% based on a 50% change in a nominal open loop amplification of 300. Since the resolver accuracy is 0.1%, applications of PC 79 are limited to those in which 0.5% accuracy is sufficient.

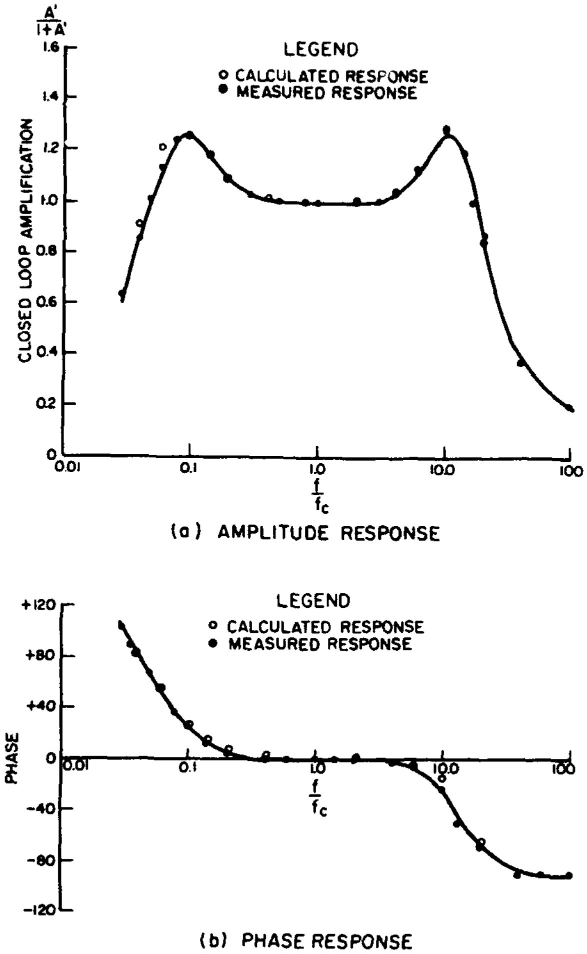


Figure 79–4.—Closed loop characteristics of PC 79. A Mark 4 Mod 0 resolver was used to complete the feedbuck loop.

3.2 *Error and Null Voltages:* The output of the resolver when compared with the input gives the performance indicated in figure 79–5. The comparison was made using the preferred circuit with voltage applied to input 1, with input 2 grounded, and with maximum coupling between stator and rotor. Under these conditions the input and output voltages are theoretically equal. The deviation of the output from the input is partly static error as a result of manufacturing tolerances and partly due to quadrature and harmonic components which are present even at null. The amplitude of these errors is a function of the resolver input voltage and may be the determining factor in selecting the operating voltage of the resolver. The solid lines in figure 79–5 are for the nominal operating frequency of 500 cps, and the dashed lines are for 475 cps. The curves given are for the 105D2K resolver; the results for other resolvers will differ.

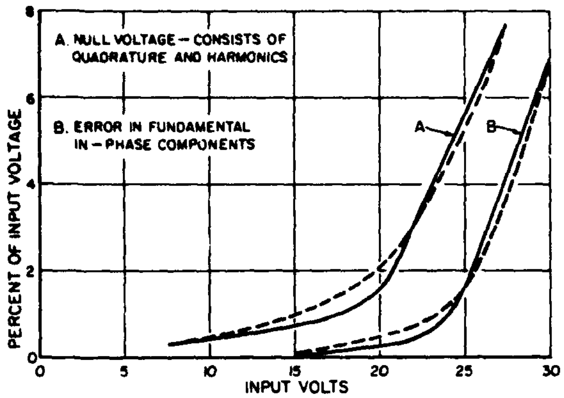


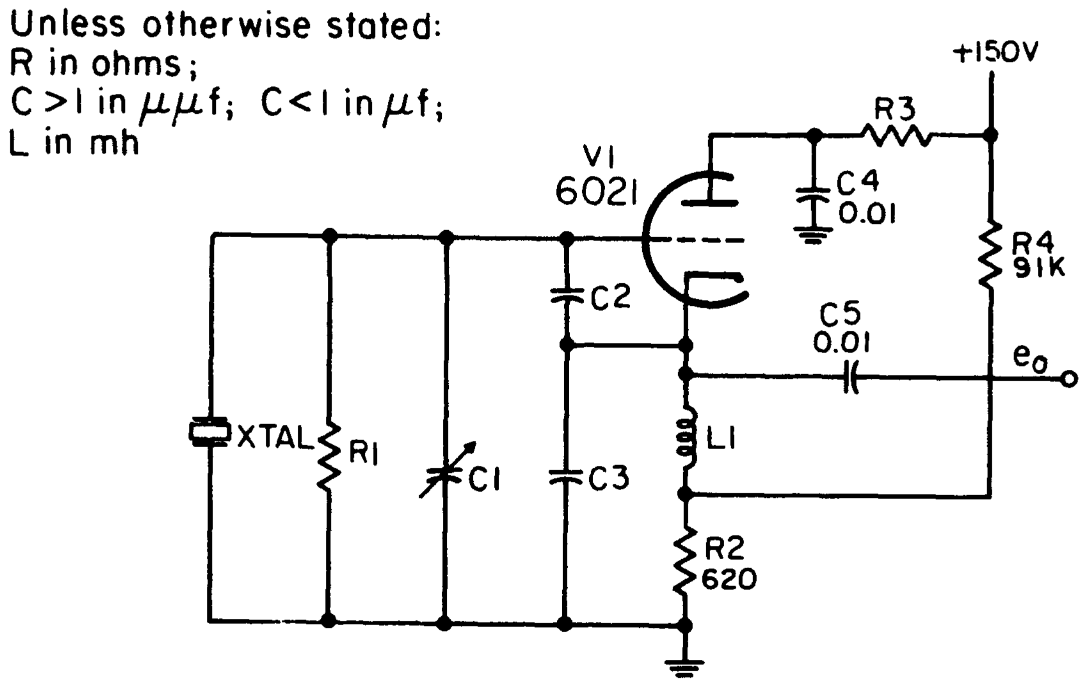
Figure 79–5.—Performance of PC 79 used with a Mark 4 Mod 0 resolver operating at 500 cps. The dashed curves show the effect of a 5% decrease in input frequency.

NBS PREFERRED CIRCUIT NO. 101

0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR

NBS PREFERRED CIRCUIT NO. 101

0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR



Component data:

Preferred crystal types: CR–18/U, CR–36/U. (See Note 1.)

Frequency range mc	R1 Ω	R3 Ω	C1 μμf	C2 μμf	C3 μμf	C1′	C2′	C3′	L1 mh
						Distributed "C" μμf (See Note 2)			
0.8–5	560K	33K	10. 7	15	100	6. 3	2	12. 5	7. 0
3–11	47K	39K	12. 4	15	33	6. 3	2	12. 5	0. 8
5–20	33K	33K	8. 4	24	24	6. 3	2	12. 5	0. 3

R2, R4: ±10% limits; R1, R3: ±20% limits. C1, C2, C3: ±10% limits; C4, C5: ±20% limits, or guaranteed minimum value. (See Note 3.)

Power requirements:

150 volts dc at 4 ma (plate supply); 6.3 volts at 300 ma (heater supply).

Operating characteristics:

For output voltage and crystal dissipation as a function of crystal resistance, frequency, and oscillator tube transconductance, see figures 101–1 through 101–3. (See Notes 4 and 5.)

Factors affecting absolute frequency accuracy:	*CR–18/U* *ppm*	*CR–36/U* *ppm*
(a) Manufacturing tolerance (within temperature range)	50	20
(b) Frequency correlation (See Note 6)	10	10
(c) Frequency stability for 10% change in plate and heater voltage	<3	<3
(d) Frequency variation for a 10% change in a single capacitor	<8	<8
(e) Frequency variation for a 20% change in a single resistor	<1	<1

(For Notes, see next page)

NOTES:

1. CR-36/U is a temperature-controlled unit. (See MIL-C-3098B.)

2. The distributed capacitance values shown are typical of those obtained by use of conventional wiring in the test units. Lead dress, tube sockets versus direct lead soldering, etc., will cause these values to vary; therefore, they should be checked and the lumped capacitors C1, C2, and C3, shown in the circuit diagram, changed to keep the total capacitances the same as listed, i.e., the sum of C2+C2′ to remain constant. In most cases adjustment of C1 to keep C_t (defined in section 2.1) equal to 32 $\mu\mu$f will be satisfactory. Note that C3 is paralleled by 15 $\mu\mu$f of load capacitance.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. The crystal drive equals I^2R_e where I is the rms current through the crystal, and R_e is the crystal resistance as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.) The current through the crystal can be equated to the current through the 32 $\mu\mu$f of capacitance which is in parallel with the crystal, since the crystal circuit is high Q. The current through the 32 $\mu\mu$f is E/X_c where E is the rms voltage across the crystal, and X_c is the capacitive reactance of 32 $\mu\mu$f at the operating frequency. The crystal drive therefore equals $(E/X_c)^2R_e$.

5. The output voltage is measured with a load of 10KΩ paralleled by 15 $\mu\mu$f.

6. Frequency correlation is defined as the difference between the circuit operating frequency (operating at 25° C with circuit values as shown in the diagram) and the antiresonant frequency of the crystal unit as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.)

PC 101 0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR

1. APPLICATION

PC 101 provides the designer with a stable frequency source of minimal complexity. Operation at any frequency in the 0.8 to 20 mc range may be accomplished by substituting different crystals on a plug-in basis, with no retuning required. The twin-triode 6021 provides a triode section for use as a mixer, buffer, and/or frequency multiplier. Use of a single or twin-triode miniature or subminiature equivalent requires changes in the lumped capacitances to compensate for changes in tube and distributed capacitances. The electron-coupled pentode circuit of PC 102 should be used to obtain higher output, immunity from the effects of load changes, greater harmonic content, and better frequency correlation. However, this will increase circuit complexity, and may increase the physical size of a unit due to the use of a single tube per envelope.

2. DESIGN CONSIDERATIONS

2.1 *Symbols:*

(*a*) P_x: Power dissipated in the crystal unit, or crystal drive level.

(*b*) C_t: The total grid to ground capacitance, due to C1, C2, C3 and associated distributed and stray capacitance.

(*c*) R_t: The total crystal circuit resistance consisting of the sum of the crystal resistance as measured in the appropriate crystal impedance meter and the additional resistance connected in series with the crystal to simulate a higher resistance crystal.

2.2 *Crystal Circuit:* The crystal equivalent circuit consists of a very large inductance (in the order of henries), in series with a very small capacitance (in the order of hundredths of a micromicrofarad) and a resistance ranging from a minimum of 5 ohms at the high-frequency end of the circuit range to a maximum of 1000 ohms at the low-frequency end. In addition, due to the crystal holder, etc., there is a small capacitance in the order of 5 $\mu\mu f$[1] in parallel with the crystal. In the Colpitts circuit, the crystal operates at a frequency higher than the series resonant frequency (which is determined by the constants of the series arm alone) and lower than the parallel resonant frequency[2] (which is a function of the parallel capacitance and the inductance of the crystal together with the external parallel capacitance). This total external parallel capacitance is a fixed value for any given MIL crystal. The crystal, together with the associated parallel circuit capacitance, acts as an inductance whose effective reactance varies very rapidly with changes in frequency. The oscillator circuit adjusts its frequency so that the effective reactance of the crystal at the operating frequency is just enough for the loop gain to be 1 with a phase shift of 180° between input voltage (grid-cathode) and output voltage (plate-cathode). The crystal is tested for antiresonance with 32 $\mu\mu$f of external parallel capacitance. This specification allows the user to design a circuit which will oscillate at a frequency close to the antiresonant frequency of the crystal. In general, this frequency correlation should be better than 10 parts per million. The antiresonant frequency of the crystal can differ from the frequency stamped on the crystal holder by a maximum number of parts per million as specified in MIL-C-3098B for the particular crystal involved. This maximum deviation includes the combined effects of manufacturing tolerance and temperature coefficient within the temperature range for which the crystal is designed.

The effective series resistance of the crystal is a measure of the "activity" of the crystal. It is a controlling factor in the determination of output-voltage amplitude and crystal dissipation.

2.3 *Oscillator Configuration:* A Colpitts grounded plate circuit was chosen because it

[1] The maximum value of this capacitance is set by MIL specifications as 7 $\mu\mu$f.

[2] The parallel resonant frequency referred to is that frequency for which zero phase shift is measured when the crystal is inserted in the specified crystal impedance meter. (See MIL-C-3098B.)

allows frequency changing on a crystal plug-in basis, with greater stability and better frequency correlation than provided by the nearest alternative, the Miller oscillator. Use of the Colpitts circuit, however, results in sacrifice of output amplitude for the same magnitude of crystal dissipation obtained with the Miller oscillator.

The Colpitts oscillator is difficult to start when used with high resistance crystals. Adjustment of the capacitor voltage divider C2, C3 to insure starting tends to reduce output voltage or increase crystal dissipation. These effects can be mitigated by providing an initial negative bias to the oscillator tube. This negative bias reduces grid loading during initial oscillator buildup and allows oscillator operation with a more favorable capacitor divider ratio. The capacitor C1 in many applications is composed mainly of lead and switch capacitances when switches are used for frequency changing.

The voltage divider R2,R4 provides the initial bias to the oscillator tube. This circuit also increases frequency stability. The oscillator circuit without this fixed bias will experience a larger change in frequency as a function of a given change in plate voltage than will this circuit with a fixed bias. The improvement in frequency stability is an added advantage obtained from the use of a fixed bias. The mechanism involved is the reduction in the plate resistance of the tube with an increase in supply voltage which is counteracted by the increase in plate resistance caused by the increase in bias across the bias network R2, R4.

The choke L1 keeps the oscillator output from being loaded by the cathode resistor. It is chosen of sufficient size to resonate with C3 at a frequency lower than half the lowest frequency of the particular band in use. This insures negligible inductive effect on the capacitor divider C2, C3.

The range of crystal resistances allowed by MIL–C–3098B appears to be much wider than necessary in view of present manufacturing techniques. Because of this wide range, design compromises must be made in order to insure operation of the circuit with the entire range of crystal resistance allowed by specifications and yet keep crystal dissipation within the recommended limits.[3]

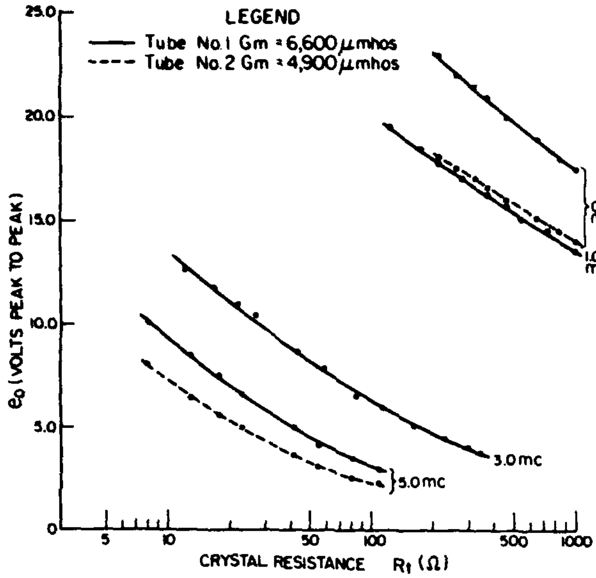
2.4 *Oscillator Tube:* The 6021 twin-triode has a medium μ (35) and sufficient transconductance (5400 μmhos) for use as the oscillator stage and as a buffer or frequency multiplier stage. It is a MIL preferred tube and is frequently used in associated circuits in the same type of equipment as would employ PC 101, thus allowing for a reduction of tube types in an equipment.

3. PERFORMANCE

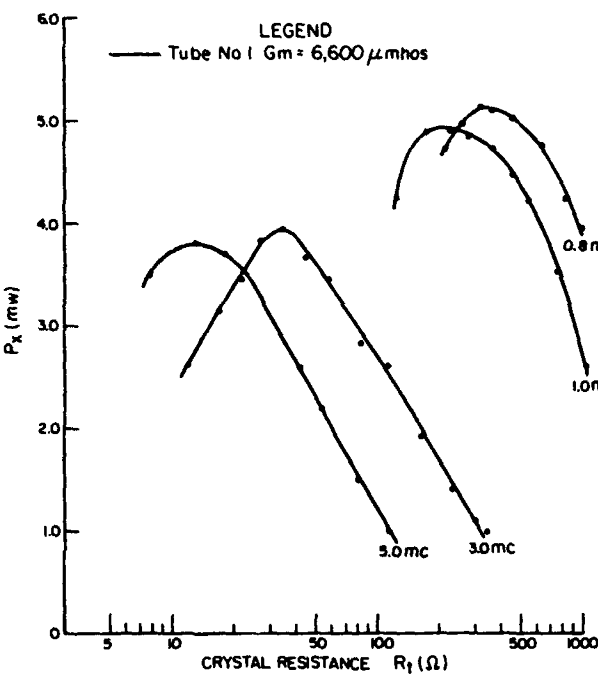
3.1 *Output Voltage Amplitude and Crystal Dissipation:* Figures 101–1 through 101–3 are graphs of output voltage and crystal drive level versus crystal resistance for the three frequency bands of PC 101. All voltages shown are peak to peak as measured on an oscilloscope. Typical waveforms for the frequency extremes of PC 101 are shown in figure 101-4. The essentially sinusoidal waveform of the higher frequency output is due to the lowered impedance of the RC load (10KΩ in parallel with 15 $\mu\mu$f) at these frequencies.

Because limit crystals were not available, the performance data were plotted using the lowest resistance crystals available and simulating higher resistance units by adding resistance in series with the crystal. The circuit used in making the measurements is shown in figure 101–5, where R_x is the added resistance. The validity of this simulation technique was checked by making measurements on two crystals, one a low resistance and the other a high resistance crystal. Resistance was added to the low resistance crystal to bring its resistance up to that of the high resistance unit, and the operation of the two crystals was compared in the test circuit of figure 101–5. The output voltage and computed crystal dissipation checked within 5%. Further checks were

[3] There is no restriction on crystal drive in MIL–C–3098B. These specifications serve merely to delineate acceptance test procedures. Recommended operating limits for crystals in military equipment are listed in section II of WADC Technical Report 56–156, ASTIA Document No. AD 110448, "Handbook of Piezoelectric Crystals for Radio Equipment Designers," Oct. 1956.

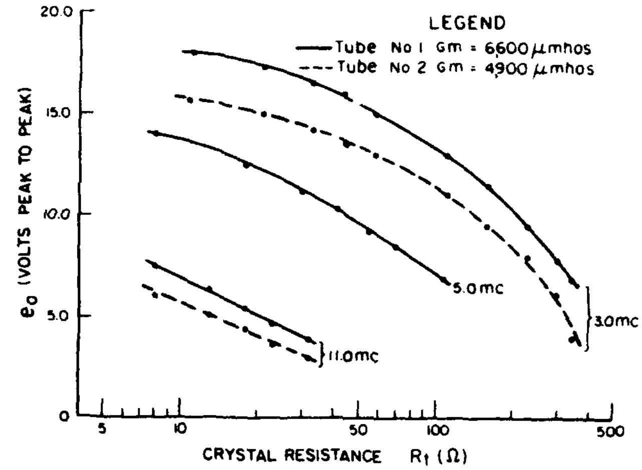


(a) Output voltage.

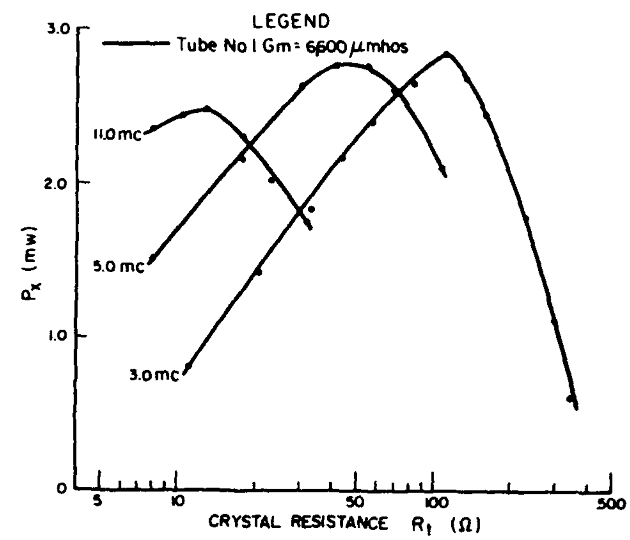


(b) Crystal dissipation.

Figure 101–1.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the low frequency band (0.8 to 5.0 mc).



(a) Output voltage.

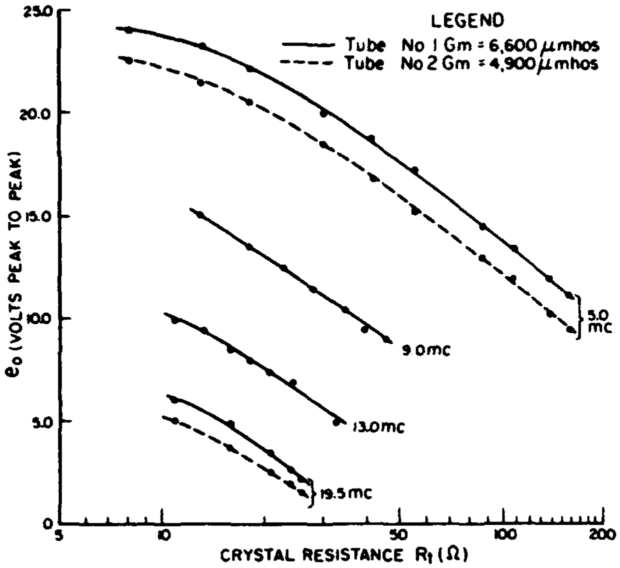


(b) Crystal dissipation.

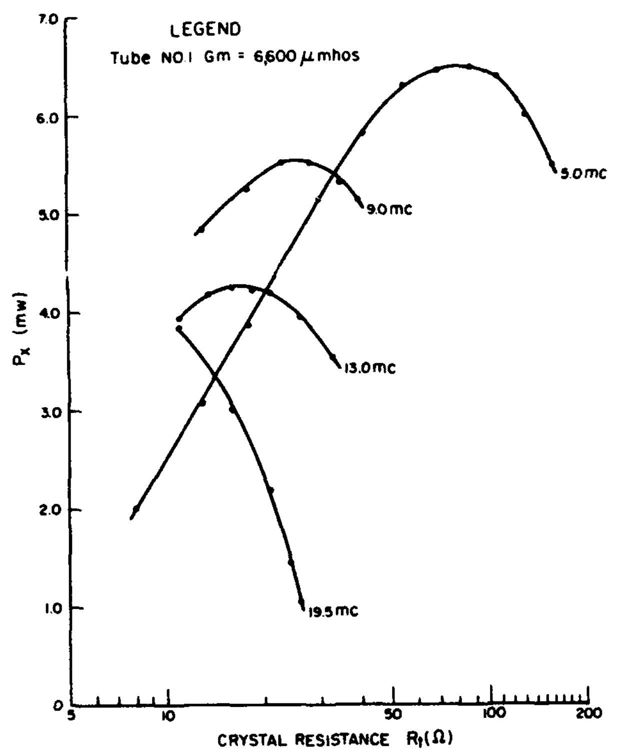
Figure 101–2.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the middle frequency band (3.0 to 11.0 mc).

made by inserting a crystal with a resistor in series with it in the appropriate crystal impedance meter (see MIL–C–3098B). The readings erred on the pessimistic side, i.e. the readings were higher than would be expected to result from the addition of the crystal and external resistance values. Here again the difference was less than 5%.

In the tests discussed above, the results of which are shown in figures 101–1(b), 101–2(b) and 101–3(b), all dissipation curves go through a peak, except at the high end of the high-frequency band. The peak indicates that the use of lower resistance crystals than were obtainable for these measurements will not result in greater than maximum recommended crystal dissipation (see footnote 3) at any frequency, with the possible exception of the high end of the high-frequency band.

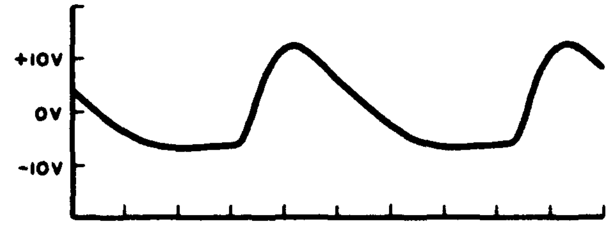


(a) Output voltage.

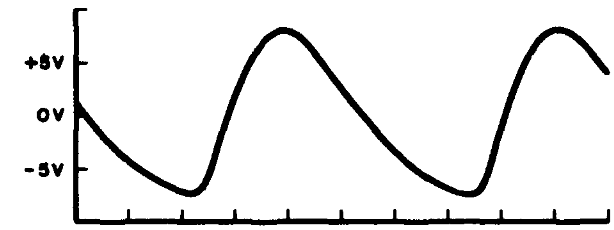


(b) Crystal dissipation.

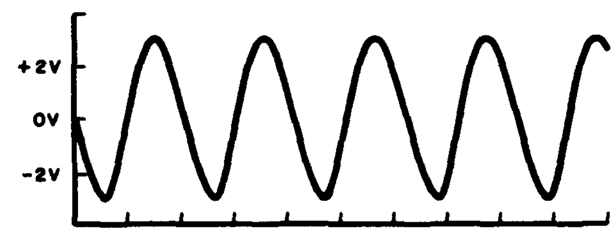
Figure 101-3.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the high frequency band (5.0 to 20 mc).



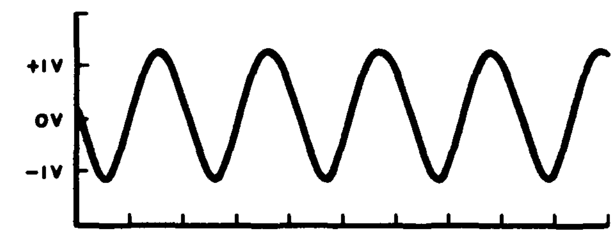
(a) 0.8 MC, R_t = 230Ω



(b) 0.8 MC, R_t = 1000Ω



(c) 19.5 MC, R_t = 11Ω



(d) 19.5 MC, R = 26Ω

Figure 101-4.—Output voltage waveforms across a 10KΩ resistive load.

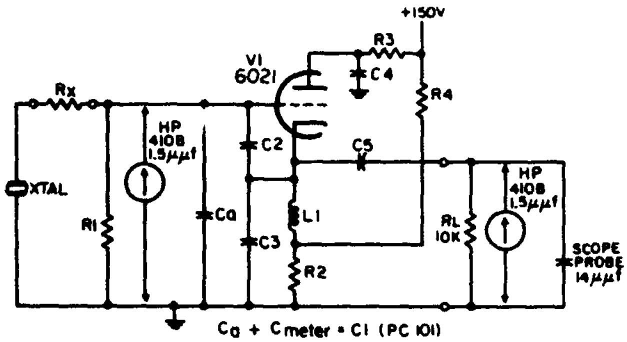


Figure 101-5.—Test circuit used for measuring the performance of PC 101. The crystal resistance R_t, figures 101-1 through 101-4, is equal to the crystal resistance R_e plus the added fixed resistor R_x.

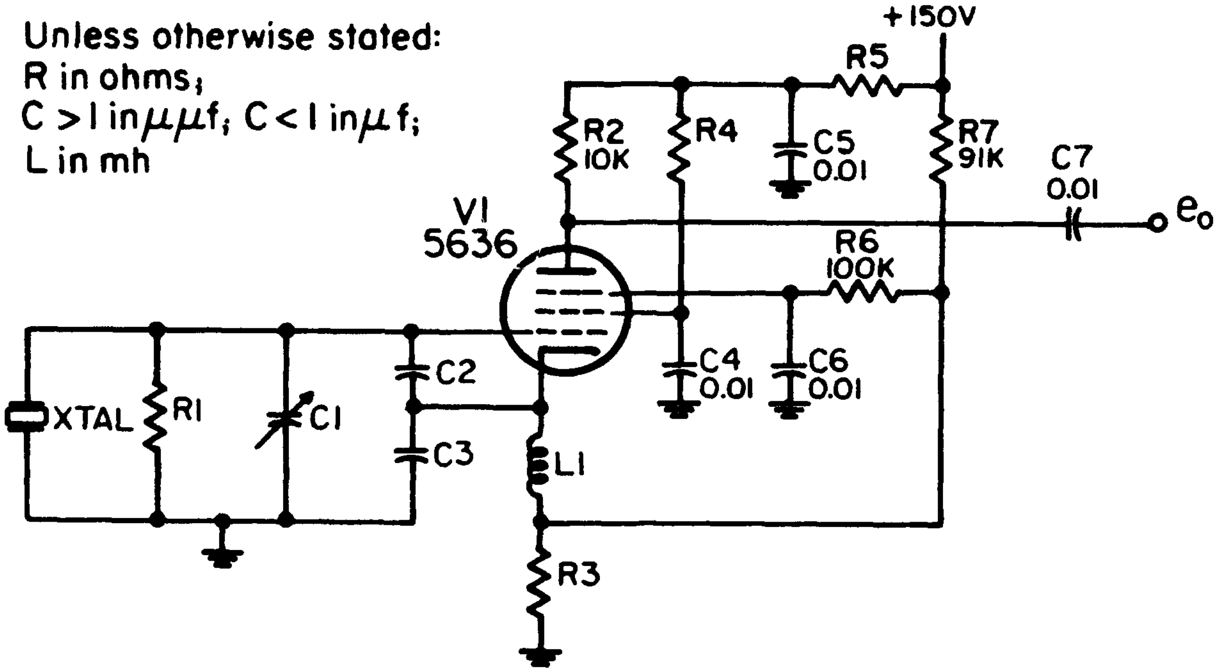
In figures 101-1(a), 101-2(a), and 101-3(a) the solid lines represent data taken using a 6021 with a transconductance near the maximum permitted by MIL-E-1. Data were also taken at the high and low ends of each band using a low transconductance tube; these data, plotted as broken lines, indicate the deterioration of output voltage with decreased transconductance. Deterioration of output voltage with decreased transconductance for other frequencies within each band can be interpolated visually from this data. The crystal dissipation shown in figures 101-1(b), 101-2(b), and 101-3(b) was plotted for the high transconductance tube only, since maximum crystal dissipation would occur when the highest transconductance tube was used.

3.2 *Frequency Stability:* The value of the crystal oscillator as a system component is dependent on its frequency stability. Two major causes of frequency variation are changes in circuit component values and temperature. In general, the least critical components are resistors. For a ±20% variation in value of a single resistor, the frequency deviation is less than one part per million. For a ±10% change in a single capacitor, however, the frequency may change by approximately 8 ppm. Throughout the mean temperature range of −55° C to +90° C, the mean frequency of a typical CR-18/U crystal unit changes by about 15 ppm. This change, together with frequency variations caused by temperature changes of the component parts, can cause a total frequency deviation over the operating temperature range of as much as 35 ppm. For temperature-controlled crystal units, such as the CR-36/U, the total is less than 22 ppm.

NBS PREFERRED CIRCUIT NO. 102
0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR

NBS PREFERRED CIRCUIT NO. 102
0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR

Unless otherwise stated:
R in ohms;
C >1 in $\mu\mu$f; C<1 in μf;
L in mh



Component data:
Preferred crystal types: CR-18/U, CR-36/U. (See Note 1.)

Frequency range mc	R1 Ω	R3 Ω	R4 Ω	R5 Ω	C1 $\mu\mu$f	C2 $\mu\mu$f	C3 $\mu\mu$f	C1′	C2′	C3′	L1 mh
								Distributed "C" $\mu\mu$f (See Note 2)			
0.8–5	330K	620	47K	12K	10.3	15	150	6.3	2	12.5	7.0
3–11	100K	620	68K	6.8K	8.7	18	100	6.3	2	12.5	0.8
5–20	47K	470	110K	150	8.6	22	47	6.3	2	12.5	0.3

R3, R7: ±10% limits; all other R: ±20% limits. C1,C2,C3: ±10% limits; all other C: ±20% limits, or guaranteed minimum value. (See Note 3.)

Power requirements:
150 volts dc at 4 ma (plate and screen supply); 6.3 volts at 150 ma (heater supply).

Operating characteristics:
For output voltage and crystal dissipation as a function of crystal resistance, frequency, and oscillator tube transconductance, see figures 102–1 through 102–3. (See Notes 4 and 5.)

Factors affecting absolute frequency accuracy:	*CR-18/U* *ppm*	*CR-36/U* *ppm*
(a) Manufacturing tolerance (within temperature range)	50	20
(b) Frequency correlation (see Note 6)	10	10
(c) Frequency stability for 10% change in plate and heater voltage	<3	<3
(d) Frequency variation for a 10% change in a single capacitor	<8	<8
(e) Frequency variation for a 20% change in a single resistor	<1	<1

(For Notes, see next page)

NOTES:

1. CR-36/U is a temperature-controlled unit. (See MIL-C-3098B.)

2. The distributed capacitance values shown are typical of those obtained by use of conventional wiring in the test units. Variation of capacitance due to lead dress, the difference in tube socket capacitance versus direct tube leads soldering, etc., will cause these values to vary; therefore, they should be checked and the lumped capacitors C1, C2, and C3, shown in the circuit diagram, changed to keep the total capacitances the same as listed, i.e., the sum of $C2+C2'$ to remain constant. In most cases adjustment of C1 to keep C_t (defined in section 2.1) equal to 32 $\mu\mu$f will be satisfactory.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. The crystal drive equals I^2R_e where I is the rms current through the crystal, and R_e is the crystal resistance as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.) The current through the crystal can be equated to the current through the 32 $\mu\mu$f of capacitance which is in parallel with the crystal, since the crystal circuit is high Q. The current through the 32 $\mu\mu$f is E/X_c where E is the rms voltage across the crystal, and X_c is the capacitive reactance of 32 $\mu\mu$f at the operating frequency. The crystal drive therefore equals $(E/X_c)^2R_e$.

5. The output voltage is measured with a load of 10KΩ paralleled by 15 $\mu\mu$f.

6. Frequency correlation is defined as the difference between the circuit operating frequency (operating at 25° C with circuit values as shown in the diagram) and the antiresonant frequency of the crystal unit as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.)

PC 102 0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR

1. APPLICATION

PC 102 provides the designer with a stable frequency source that is relatively immune to changes in output loading. Selection of this circuit is generally based on its ability to provide harmonics of the fundamental frequency to its load. This circuit also provides isolation of the oscillator section from the plate circuit output. Operation at any fundamental frequency in the 0.8 to 20 mc range is accomplished by substituting crystals on a plug-in basis. Tuned circuits are required for the selection of any particular harmonic. This oscillator is particularly useful in electronic equipment requiring operation on a number of separate channels.

2. DESIGN CONSIDERATIONS

2.1 Symbols:

(*a*) P_x: Power dissipated in the crystal unit, or crystal drive level.

(*b*) C_t: The total grid to ground capacitance, due to C1, C2, C3 and associated distributed and stray capacitance.

(*c*) R_t: The total crystal circuit resistance consisting of the sum of the crystal resistance as measured in the appropriate crystal impedance meter and the additional resistance connected in series with the crystal to simulate a higher resistance crystal.

2.2 *Crystal Circuit:* All considerations given in PC 101 apply to this circuit, as the oscillator portion is that of PC 101. Only deviations and additional performance characteristics will therefore be discussed here.

2.3 *Oscillator Configuration:* The Colpitts grounded plate circuit of PC 101 readily adapts itself to electron coupling, since the plate operates at ac ground potential. When a pentode tube is used, the screen grid operated at ac ground potential acts as the anode of the oscillator. The output voltage of PC 102, which is obtained from the pentode plate circuit, is a complex waveform of repetition rate equal to the fundamental frequency of the crystal unit, provided the plate is untuned. When a tuned circuit is added, the fundamental or harmonic of interest may be selected.

Overlapping frequency ranges are provided to assist the circuit designer in the selection of a single oscillator to operate over a range of frequencies without a change of circuit configuration.

2.4 *Oscillator Tube:* A 5636 subminiature pentode tube is used in PC 102. Equivalent miniature tubes such as the 5725/6AS6W miniature pentode tube may be used. Because the separate, externally-connected suppressor lead allows separate dc biasing of the suppressor, the decoupling between the oscillator and the output portion of the circuit is improved.[1] Use of an internally-connected suppressor would increase the reaction of output load changes on the oscillator frequency. A further consideration in the choice of the 5636 was the applicability of a pentode with a high transconductance suppressor to other portions of an equipment using PC 102. This tends to reduce the number of tube types present in an equipment and therefore aids logistic simplification. For each application of PC 102, the capacitors C1, C2, and C3 should be changed where necessary to compensate for distributed capacitances differing from the ones shown in the table on page 102-2. In many cases a variable C1 provides sufficient coverage.

3. PERFORMANCE

Figures 102-1 through 102-3 are graphs of output voltage and crystal drive level versus crystal resistance for the three frequency bands of PC 102. All voltages shown are peak to peak as measured on an oscilloscope.

Figure 102-4 shows typical output voltage waveforms across a 10KΩ load resistor at the frequency extremes covered by PC 102. Al-

[1] See discussion in Notes to the Preferred Circuits Manual, section 16.3(d).

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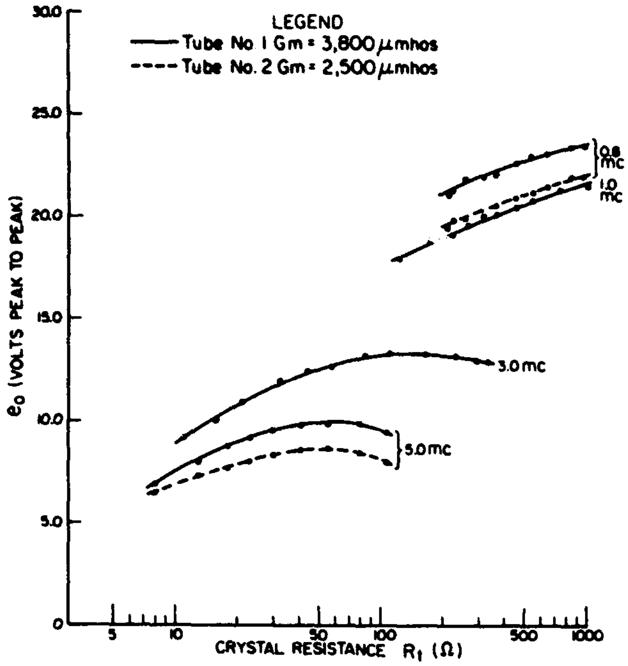
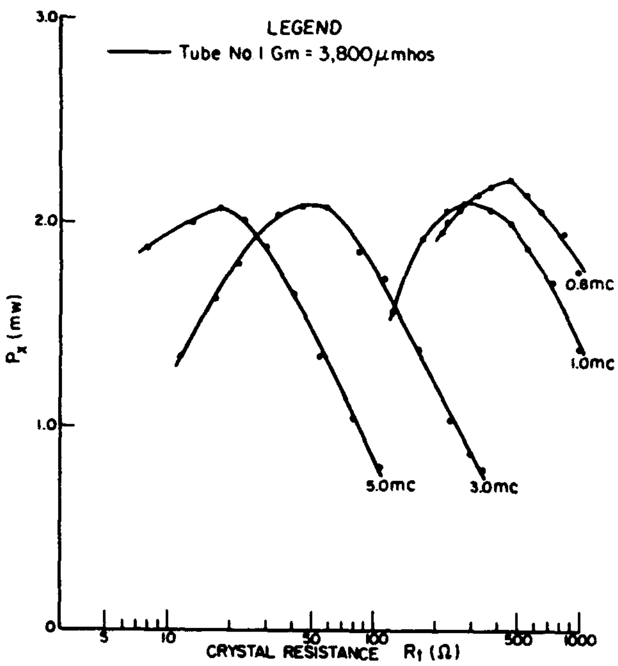
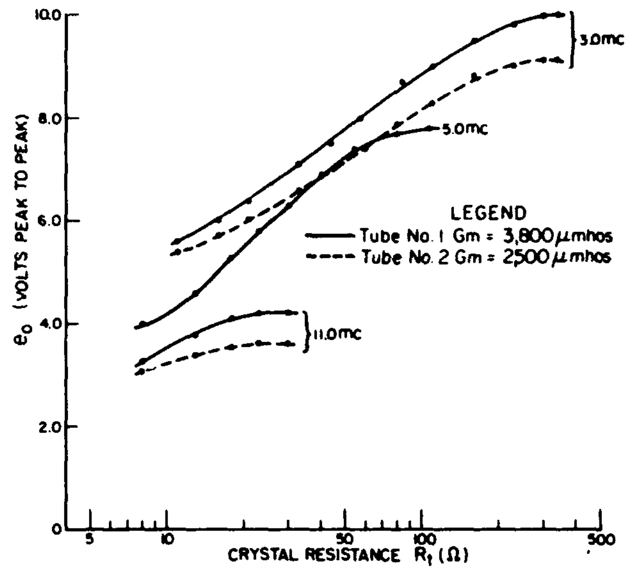


(a) Output voltage.

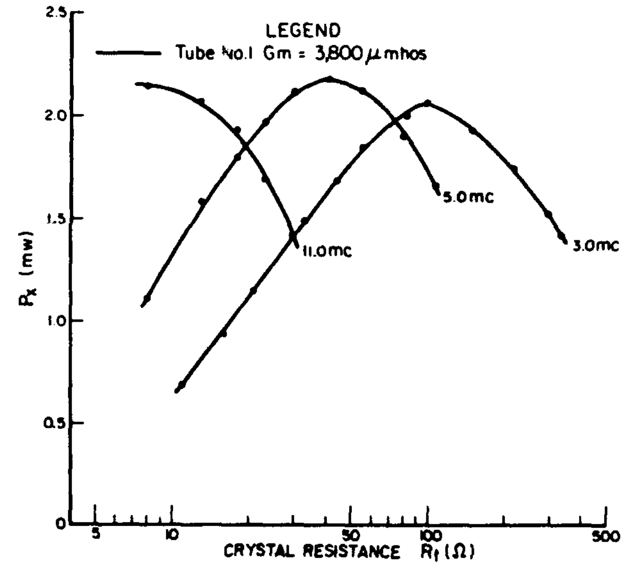


(b) Crystal dissipation.

Figure 102-1.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the low frequency band (0.8 to 5.0 mc).



(a) Output voltage.

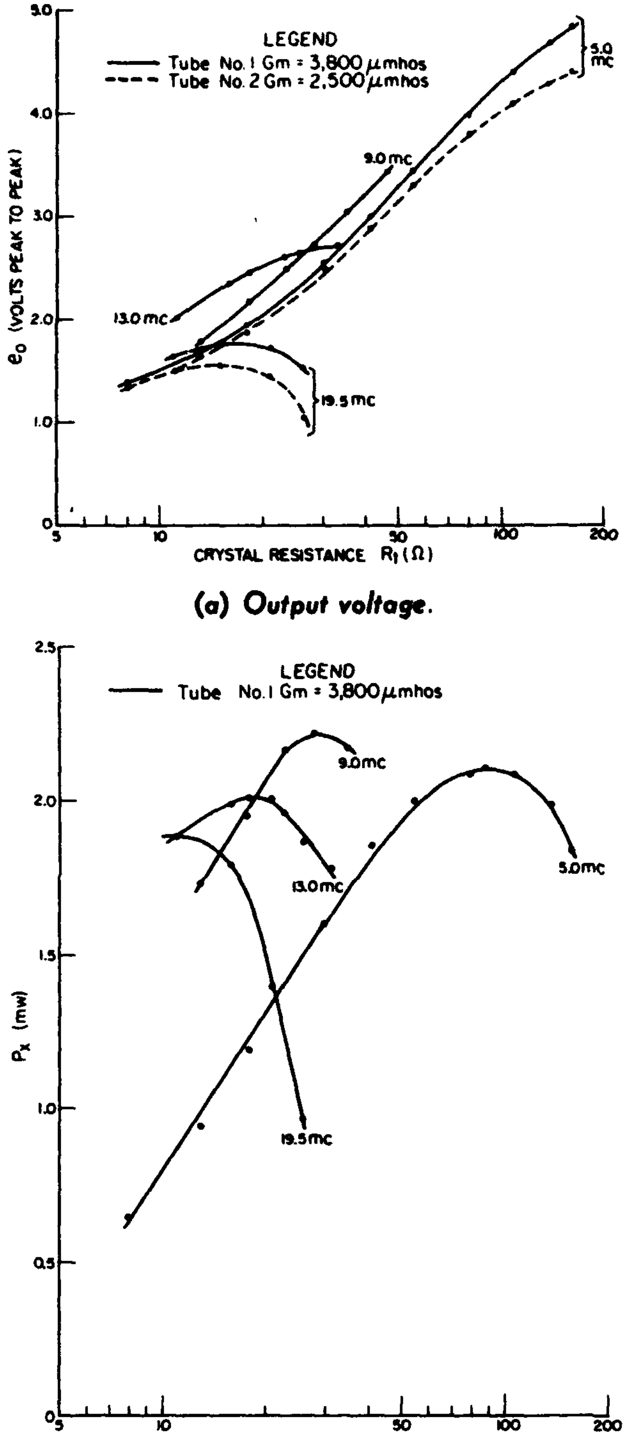


(b) Crystal dissipation.

Figure 102-2.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the middle frequency band (3.0 to 11.0 mc).

though the output current at the high end of the high-frequency band is actually non-sinusoidal, it appears to approach a sinusoid when viewed on an oscilloscope, because the higher harmonics are attenuated by the load capacitance. The test circuit used to make these measurements is shown in figure 102-9.

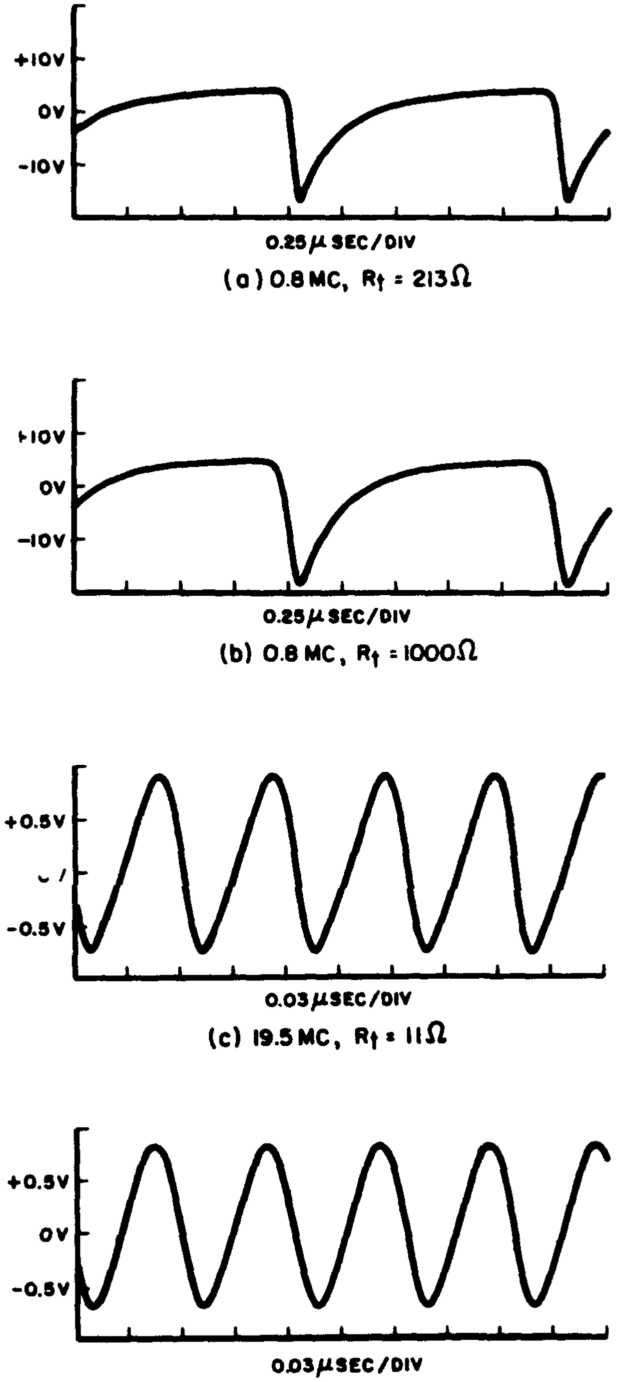
Figure 102-5 contains reproductions of the voltage waveforms measured across a 100 ohm resistor (RB in fig. 102-10). This resistor was inserted bteween the plate and the 10KΩ load resistor to reduce the effect of shunt capacitance and thereby provide a more precise representa-



(a) Output voltage.

(b) Crystal dissipation.

Figure 102–3.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the high frequency band (5.0 to 20 mc).



(a) 0.8 MC, R_t = 213 Ω

(b) 0.8 MC, R_t = 1000 Ω

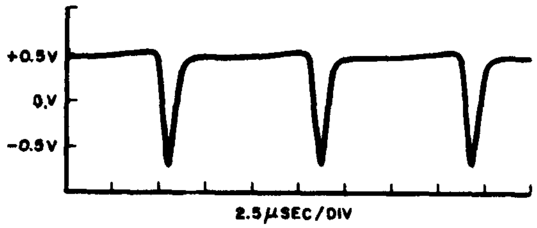
(c) 19.5 MC, R_t = 11 Ω

(d) 19.5 MC, R_t = 26 Ω

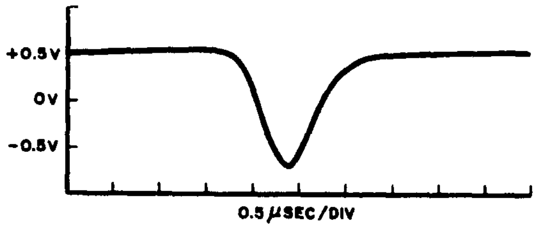
Figure 102–4.—Output voltage waveforms across a 10KΩ resistive load.

tion of the plate current waveform. The circuit arrangement used to make the measurements of plate current waveform is shown in figure 102–10.

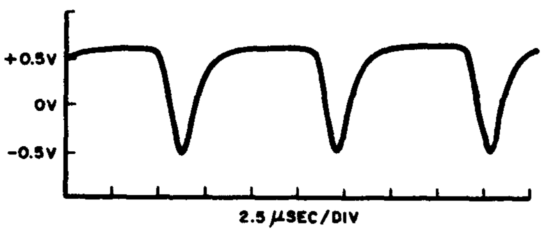
The output voltage of each harmonic was measured by replacing the 10KΩ plate load resistor with a 5KΩ resonant impedance circuit tuned to that harmonic frequency. The har-



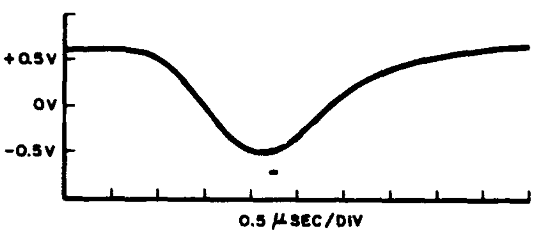
(a) WAVEFORM WITH LOW RESISTANCE CRYSTAL ($R_t = 11\Omega$)



(b) SAME AS (a). SWEEP SPEED INCREASED TO SHOW GREATER DETAIL



(c) WAVEFORM WITH HIGH RESISTANCE CRYSTAL ($R_t = 341\Omega$)



(d) SAME AS (C). SWEEP SPEED INCREASED TO SHOW GREATER DETAIL

Figure 102–5.—Example of plate current waveform for midband 3 mc fundamental frequency showing the increased angle of current flow caused by an increase in crystal resistance.

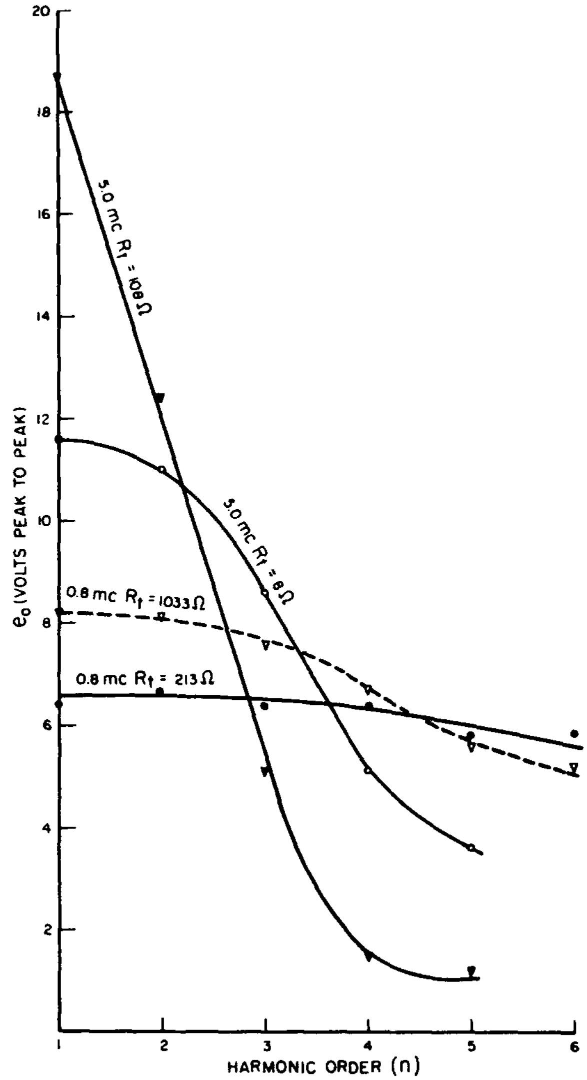


Figure 102–6.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the low frequency band (0.8 to 5.0 mc).

monic voltage developed across each tuned circuit is plotted in figures 102–6 through 102–8 as a function of harmonic order, n, where n = 1 is the crystal fundamental frequency.

3.1 *Output Voltage (Resistive Load):* As in PC 101, high limit crystals were simulated by connecting resistors in series with low-resistance crystals. The circuit used in making the performance measurements is shown in figure 102–9, where R_x is the added resistance. In the tests made using PC 101, output across a 10KΩ load resistor decreased as crystal resistance increased. However, with PC 102, output voltage across a 10KΩ load resistor increases as crystal resistance increases. (See figs. 102–1(a), 102–2(a), and 102–3(a).) In each circuit the peak to peak voltage was measured. In PC 101, the output voltage is developed between cathode and ground, and the grid drive is developed across the crystal between grid and ground. This is a cathode follower type of output, and the output voltage is an

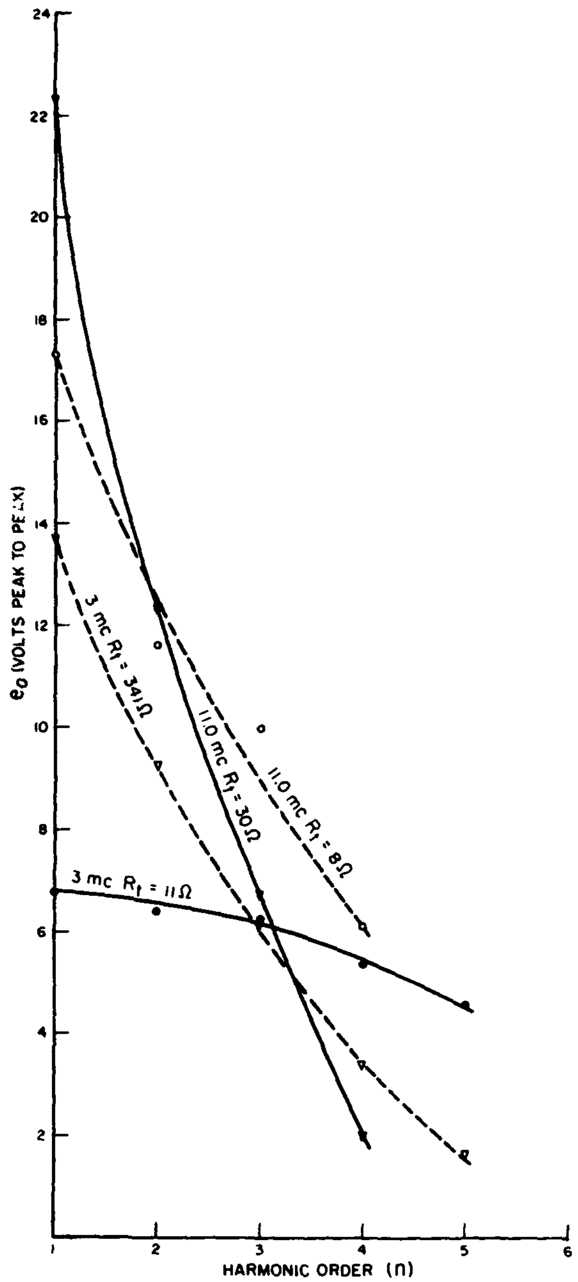


Figure 102-7.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the middle frequency band (3.0 to 11.0 mc).

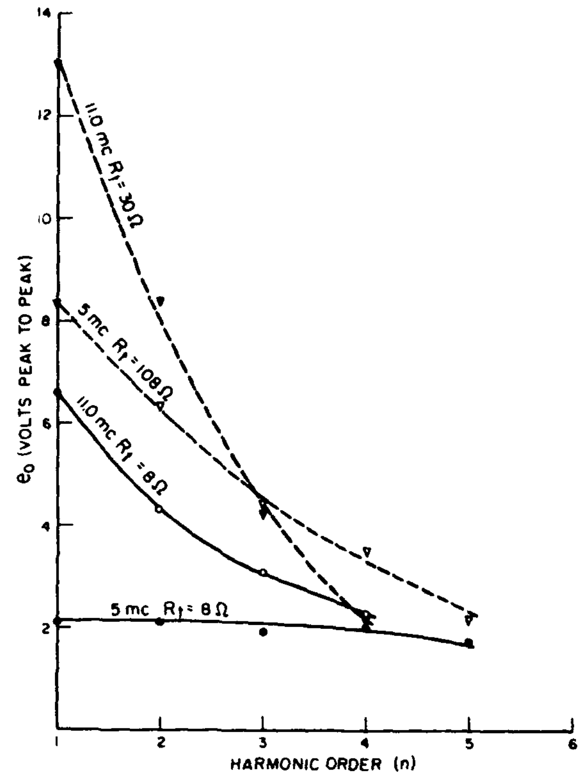
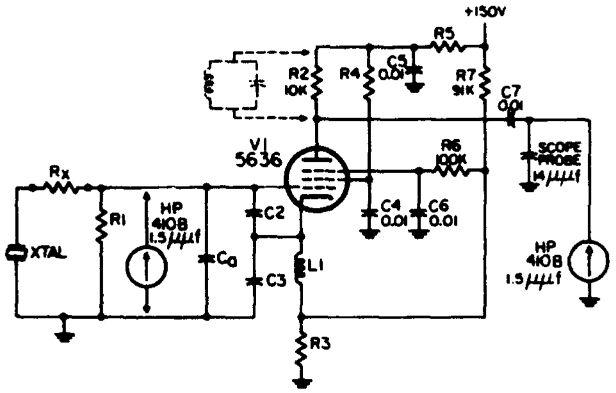


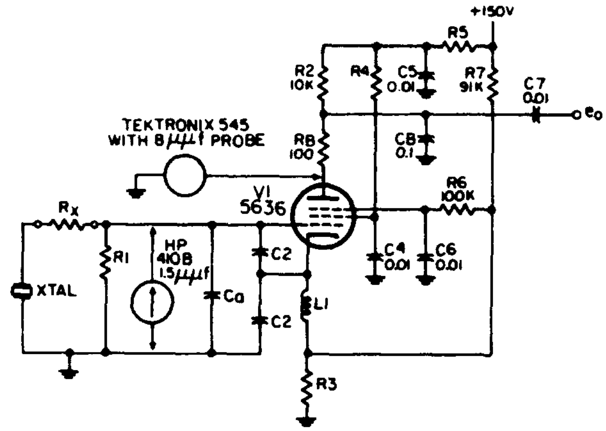
Figure 102-8.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the high frequency band (5.0 to 20 mc).

essentially fixed percentage of the crystal voltage for any one frequency. It is not an exact fixed percentage, because changes in output voltage waveform do occur as a function of grid drive. In PC 102, however, the output voltage is a function of plate current flowing through the plate load impedance. When a low resistance crystal is used, the crystal voltage and consequently the grid drive are larger (as in PC 101) than when a high resistance crystal is used. However, the larger grid drive causes a higher grid leak bias and results in a small angle of current flow. (See fig. 102-5.) This smaller angle of current flow produces a current pulse in which the relative magnitude of the higher harmonics is larger than it is for the higher resistance crystal with the larger angle of current flow. Thus (see fig. 102-5), the peak current is greater for the low resistance crystal than it is for the high resistance crystal, although the peak to peak voltage across a 10KΩ load is lower (see figs. 102-1(a), 102-2(a), and 102-3(a). This is caused by the attenuation of the higher order harmonics of the current pulse through the 25 μμf (load plus distributed) parallel capacitance across the 10KΩ load resistor. The difference in harmonic content of the high and low resistance crystals for a given frequency is evident from the curves of figures 102-6, 102-7, and 102-8.



Ca + Cmeter = C1 (PC 102)

Figure 102–9.—Test circuit used for measuring the performance of PC 102. The crystal resistance R_t, figures 102–1 through 102–8, is equal to the crystal resistance R_o plus the added fixed resistor R_x.



Ca + Cmeter = C1 (PC 102)

Figure 102–10.—Circuit used to obtain plate current waveforms shown in figure 102–5.

3.2 *Harmonic Output* (*Tuned Load*): Because of the widespread use of the Colpitts electron-coupled crystal oscillator as a source of harmonic voltages, measurements of output voltage generated across a tuned load were made for selected frequencies in all three bands of PC 102. The tuned circuits used for these measurements were selected to have an impedance in the vicinity of 5000 ohms. No attempt was made to build tuned circuits of exact impedance for each harmonic. Instead, the actual impedance in the circuit was measured using the parallel resistor method.[2] All output voltages were then normalized with respect to 5000 ohms, on the assumption that the pentode oscillator was a current generator and that therefore the output voltage was directly proportional to the impedance of the output tuned circuit for any given grid drive condition. The results of these measurements are shown in figures 102–6, 102–7, and 102–8, where the solid lines are graphs of a frequency with a low resistance crystal in the circuit, and the dotted lines show the results with a high resistance crystal in the circuit. The inversion of amplitude relations between the high and low frequency of each band as compared to the voltages measured across an output load resistor (see figures 102–1(a), 102–2(a), and 102–3(a) is accounted for by the effect of the capacitance in parallel with the load resistor which bypasses more of the energy in the high frequency current pulses than in the low frequency current pulses.

3.3 *Crystal Dissipation:* As shown in figures 102–1(b), 102–2(b) and 102–3(b), the crystal dissipation does not exceed the recommended maximum[3] for the temperature-controlled crystal CR-36/U. All measurements on high resistance crystals were made by adding resistance in series with a low resistance crystal to simulate a higher resistance crystal.

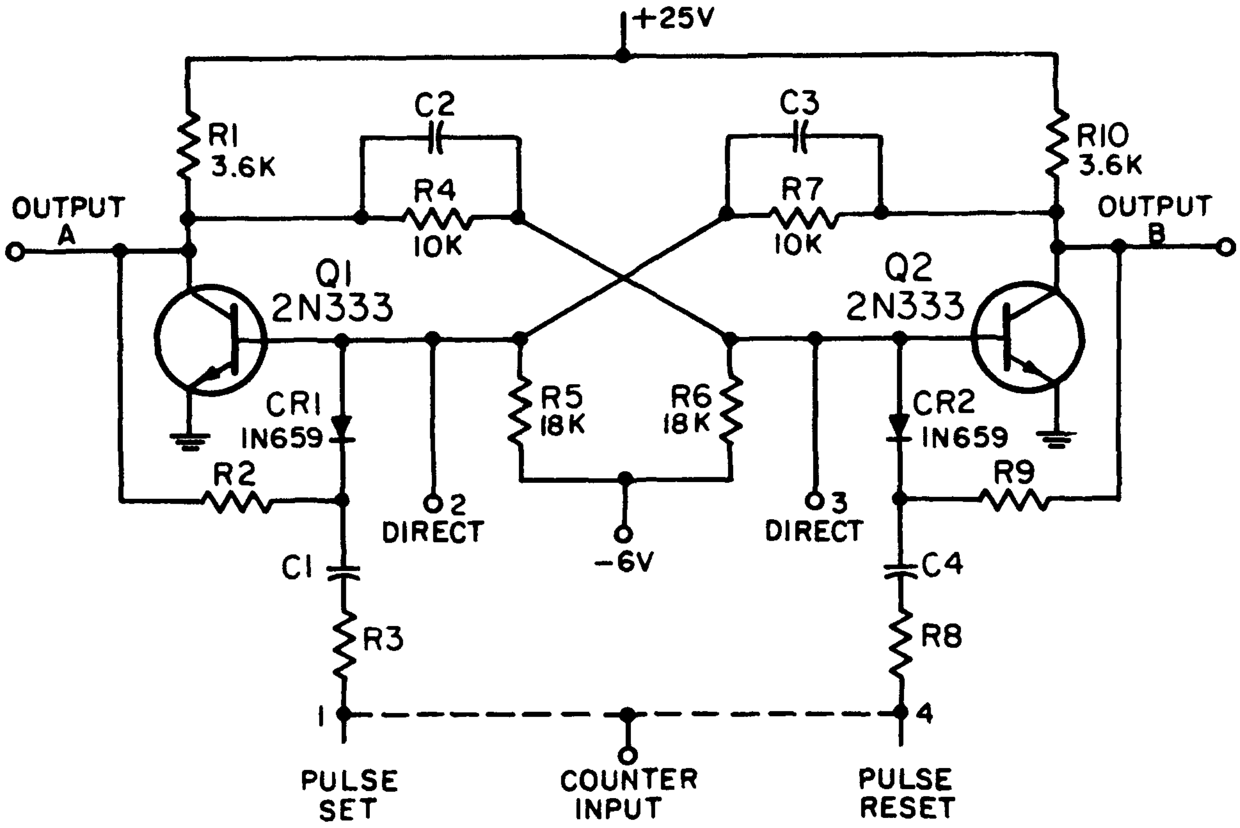
[2] Assuming that the tuned circuit at resonance is resistive, the impedance of the tuned circuit equals $(e_1/e_2-1)R_p$, where e_1 is the output voltage with no resistor connected across the tuned circuit, and e_2 is the output voltage with a resistor R_p connected across the tuned circuit.

[3] 5 mw to 9,999.999 kc; 2.5 mw from 10,000 kc to 20,000 kc. For the CR-18/U, the maximum recommended drive level is 10 mw to 9,999.999 kc, and 5 mw from 10,000 kc to 20,000 kc. See WADC Technical Report 56–156, "Handbook of Piezoelectric Crystals for Radio Equipment Designers," October 1956, p. 464 (ASTIA Document No. AD 110448.)

NBS PREFERRED CIRCUIT NO. 250
SATURATING BISTABLE MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 250

SATURATING BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C in $\mu\mu f$

Components:

R1, R4, R5, R6, R7, R10: ±5% limits; R2, R3, R8, R9: ±10% limits. All C: ±10% limits. (See Note 1.) For component values not specified on the schematic diagram of PC 250, see table 250–1, page 250–4.

Operating characteristics:

Input levels and minimum durations:

Counter or pulse: 7 volts negative, 3 μsec duration at −7 volt level. Direct: +1 ma for 10 μsec, or −4 ma for 5 μsec.

Maximum pulse repetition frequency: 40 kc.

Delay time: 2 to 5 μsec.

Output levels, both A and B: 18 ±3 volts for 10% supply voltage variation.

Output impedance:

Positive-going waveform: 2.5KΩ.

Negative-going waveform: Less than 500 Ω.

Power requirements: +25 volts, 10 ma; −6 volts, 0.7 ma.

Temperature range: −65° C to 125° C with temperature stable resistors and capacitors.

NOTE:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 250 SATURATING BISTABLE MULTIVIBRATOR

1. APPLICATION

PC 250 is a slow-speed, stable, saturating multivibrator for use as a counter, shift register, gate, or switch. It provides transitional stages between electromechanical readout and higher speed nonsaturating bistable counters. The design was optimized to accept wide tolerance transistors and should be employed when selection is to be avoided.

2. DESIGN CONSIDERATIONS

The circuit is triggered by turning off the on transistor and allowing the resulting transient to regenerate, holding the circuit in the new state. In the rest condition the dc voltages applied to the diode terminals are such that the diode associated with the off transistor is biased off by approximately 20 volts. The diode associated with the on transistor is biased off by less than the collector saturation voltage of the on transistor, approximately one-half volt. A negative pulse with the specified amplitude will, when applied to the counter input, be steered to the base of the on transistor and cause a change of state. A positive pulse will not be passed by the steering diodes.

The input circuit must furnish to the base circuit of the on transistor a negative pulse of sufficient voltage and time duration to drive the transistor out of saturation. The required voltage and width of the applied pulse are related. Experimental measurements show that at a given impedance level the product of the two is very nearly constant for the minimum trigger level.

Three sets of part values for input connections 1 and 4 are listed in table 250-1. When PC 250 is driven from a low-impedance pulse source, the component values and performance specifications of Adaption 1 apply. When PC 250 is driven from a higher impedance source, such as a non-saturating bistable multivibrator or a time delay multivibrator, the component values and performance specifications of Adaption 2 apply. When successive stages of PC 250 are cascaded, the first stage is either Adaption 1 or Adaption 2, and the successive stages should have the component values specified for Adaption 3. Instead of buffer amplifiers being used to prevent reaction on prior stages, various values are used for the resistors and capacitors listed without sacrifice of ultraconservative performance.

2.1 *Circuit Operation:* The bias circuit permits one transistor to conduct in saturation while the other transistor is held in the off condition. The dc circuit elements have been chosen so that transistors with low limit values of dc current gain, h_{FE}, will saturate. Higher gain transistors will consequently be driven further into saturation.

In the design of this circuit care was taken to use the extreme lower limit value of h_{FE}. This value has been found to be approximately 7 for the 2N333.

The output voltage swing is expressed as

$$\Delta V_2 \approx V_{CC}\frac{\text{R7}}{\text{R7}+\text{R10}} - V_{CE(sat)2}$$

where V_{CC}=collector supply voltage and $V_{CE(sat)2}$=collector to emitter saturation voltage. From this relationship it is readily determined that the output amplitude depends on the transistor saturation resistance. This is one of the most important advantages of saturating type switching circuits.

2.2 *Impedance:* Some changes in the circuit impedance can be made. Only the relative values of the circuit resistances are of importance, except that for a fixed supply voltage the value of R5 and R6 is limited by the I_{CBO} and the $V_{CE(sat)}$ characteristics of the transistor, rather than by the other circuit elements. It is recommended that R5 and R6 not exceed 20,000 ohms; larger values of the other resistances may be chosen.

The resistor values should not be scaled down beyond that point where either the collector current ratings or the power dissipation of the transistors are exceeded. The resistors in

TABLE 250–1.—*Component values and performance of PC 250*

Adaption No.	Signal source	Max. source imped.	R2 R9	R3 R8	C2 C3	C1 C4	Input imped.	Input: Max. rep. rate	Input: Trigger voltage range	Output: Rise time (tr)	Output: Fall time (tf)	Number of set-reset loads	Minimum circuit recovery time
		ohms	ohms	ohms	μμf	μμf	ohms	kc	volts	μsec	μsec		μsec
1	Operation from low impedance pulse source	[1] 500	2.2K	[1] 500	1200	1500	1K	[3] 40	3–5	15	2.5	0	[3] 20
								[3] 40	3–5	25	3.0	2	[3] 25
								25	7–25	40	5.0	5	40
								12.5	7–25	80	7.5	10	80
2	Operation from non-saturating multivibrator or from either output of time delay multivibrator	[2] 1K	5.6K	[2] 1K	680	1000	1.5K	20	7–25	15	1.5	0	50
								20		25	2.0	2	50
								20		40	3.0	5	50
								12.5		80	5.0	10	80
3	Cascaded operation of identical stages or from either of above adaptions	500	5.6K	2.2K	680	560	3K	40	14–25	15	1.0	0	25
								40		25	1.5	2	25
								25		40	3.0	5	40
								12.5		80	7.0	10	80

[1] Total of source and isolating resistance is 500 ohms, ±10%.
[2] Total of source and isolating resistance is 1000 ohms, ±10%.
[3] With input pulse width of 3–5 μsec duration.

PC 250 may be reduced to approximately one-half of the values given without exceeding the ratings of the 2N333 up to a case temperature of 125° C. However, input circuit Adaption 2 is not recommended for use with resistance values lower than those given. Note that the saturation resistance of the transistor is not affected by this scaling down, so that the output impedance for a negative-going signal does not change.

2.3 *Transistor Type*: The transistor characteristics of greatest importance to the circuit operation are: (1) collector voltage, power, and current ratings; (2) dc and high-frequency current gain; (3) base-to-emitter voltage required to sustain saturated conduction; (4) collector-to-emitter voltage during saturated conduction; and (5) maximum I_{CBO} to be encountered.

The transistor power dissipation is dependent on the saturation collector voltage, as well as on the saturation collector current. The power loss in the transistor is particularly low if transistors having a low value of saturation resistance are used.

3. PERFORMANCE

3.1 *Pulse Input:* The input circuit may be used for either set-reset or counter operation. The characteristics required of the input signal are dependent on the values of R2, R9, R3, R8, C1, and C4. Values of these components have been chosen to provide operation from three general types of input, as outlined below and in table 250–1.

(a) Adaption 1 will operate from pulse inputs occurring at frequencies up to 40 kc. The highest frequency response is obtained when the pulse width of the negative-going input signal is 3 to 5 μsec. Pulse widths less than 3 μsec do not provide reliable operation, while pulses wider than 5 μsec do not allow the input circuit sufficient recovery time at 40 kc.

Generally, the duration of the more positive portion of the input signal should be a minimum of 16 μsec. For this circuit, the specified value of R3, as well as that of R8, is the sum of the source resistance and the physical isolating resistance.

(b) Signal sources for driving Adaption 2 can be a non-saturating flip-flop or either output of a time delay multivibrator. In this operation, only two set-reset (or one counter connection) inputs per source are recommended. A typical recovery time of the input circuit is approximately 50 μsec.

(c) Adaption 3 is intended for cascaded operation. Signal sources for driving Adaption

3 can be either Adaption 1, 2, or 3. The recovery time of the input circuit is approximately 20 μsec.

The minimum input required for reliable triggering of the three adaptions is plotted in figure 250-1 as a voltage of a given amplitude and rise time. The curves for the three adaptions show that for rise times below a certain value, dependent on the circuit, each circuit requires a minimum amplitude for triggering.

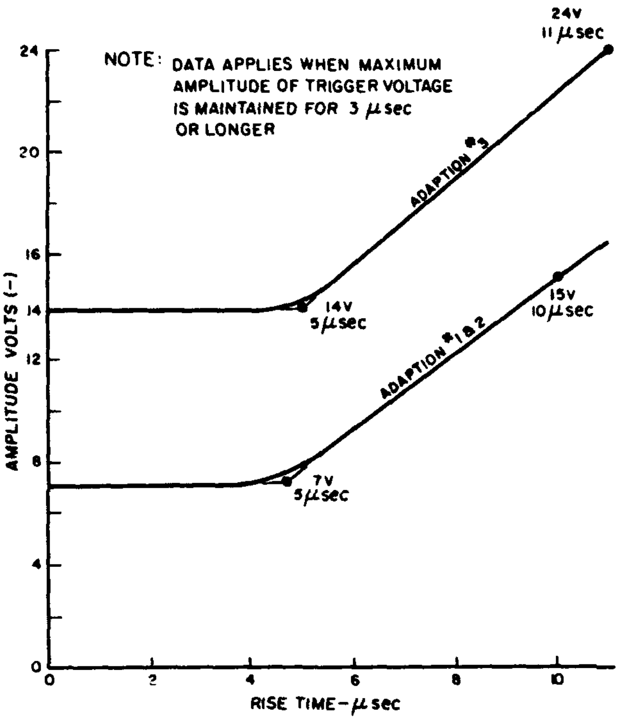


Figure 250-1.—Amplitude required for triggering vs. rise time.

The minimum duration of the applied trigger pulse, or the rest time after a negative-going ramp is applied, should not be less than 3 μsec, although shorter pulses of greater amplitude will cause triggering.

3.2 *Direct Input:* The direct input can be used for reset of the transistor by applying to the base a negative voltage source that will cause a current of 4 ma to ground for 5 μsec. Alternatively, a positive pulse from a source that will cause a current of 1 ma for 10 μsec may be used. The positive voltage resets the opposite transitor to the "off" condition.

The direct connection can also be used for the insertion of blocking pulses from a subsequent counter stage to provide other than binary counting operation, as illustrated in figure 250-2.

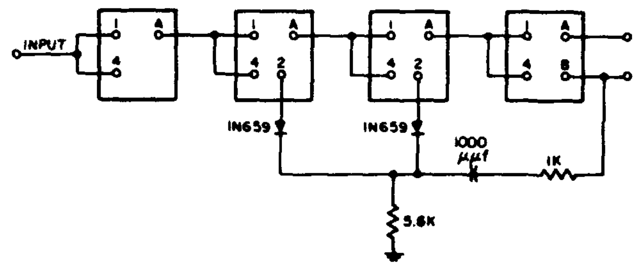


Figure 250-2.—Four stages of PC 250 connected for operation as a decade counter.

3.3 *Output:* The two outputs are complementary voltages of either 1 or 19 volts. The maximum circuit switching time is 2 to 5 μsec.

Figure 250-3 shows the output waveform. The irregularity on the more positive portion of the waveform is caused by the recovery of the input circuit from a positive-going input. Usually the spike is absorbed in the rise time of Adaption 1. In Adaptions 2 and 3 the height of the spike does not exceed 2 volts.

The rise and fall times of the outputs, which are dependent on the loading, are tabulated in table 250-1 for various combinations.

3.4 *Cascaded Operation:* Stages may be directly cascaded by connecting the inputs to the output of a previous stage. The number of inputs that can be connected depends on the input circuit used and the repetition rate desired.

The fundamental limit on the degree of loading permissible is the deterioration of the output fall time under load to the point that triggering voltages consistent with figure 250-1 are not obtained. The limit imposed by this consideration is 10 set-reset loads, or 5 counter stages, per either or both outputs. The speed-up capacitor C2 or C3 connected to the collector of the loaded side of the flip-flop should be increased by about 200 μμf for each set-reset input connected to the output.

Another consideration when the stages are cascaded is the deterioration of the output rise time under load. First, a deteriorated output rise time may not drive the opposite transistor

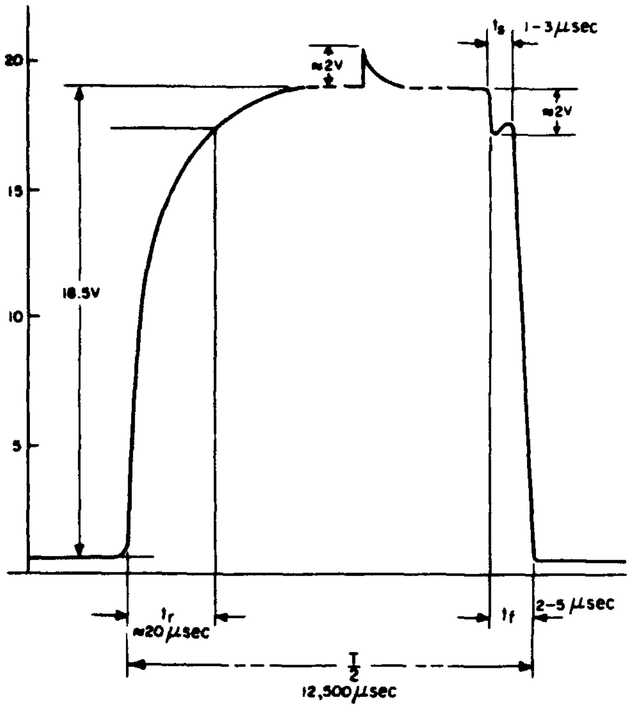


Figure 250-3.—Output waveform.

into saturation under some conditions; second, the time required for the output voltage to increase to its full "off" value exceeds the input pulse duration.

The increase in rise time restricts the upper limit on the circuit frequency response, as shown in table 250-1. The loads are always assumed to be Adaption 3.

A method of connecting four flip-flop stages for decade counter operation is shown in figure

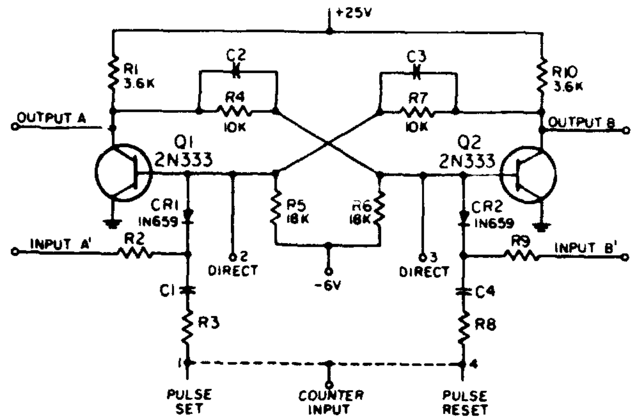


Figure 250-4.—Modification of PC 250 for use in shift registers.

250-2. This circuit has an asymmetrical output at terminal A of the fourth stage, a positive pulse of 20% duty cycle. The outputs have the same general characteristics as the binary circuit.

The saturating bistable multivibrator may be modified as shown in figure 250-4 to allow its use in a shift register. One method of interconnection is shown in figure 250-5.

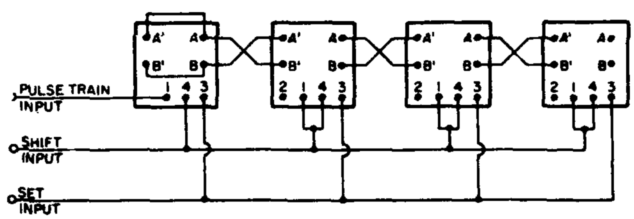
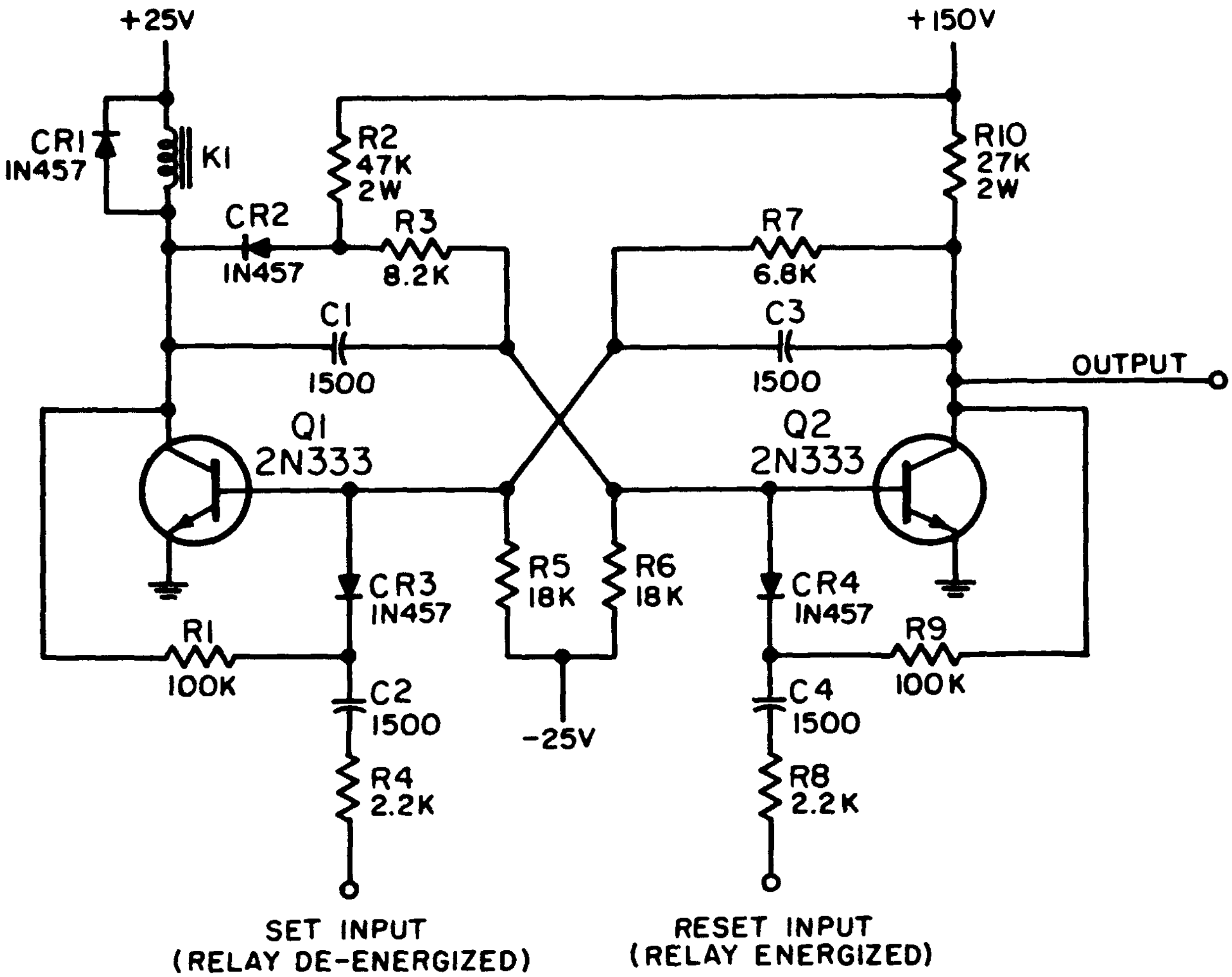


Figure 250-5.—Interconnection of modified PC 250 for shift registers.

NBS PREFERRED CIRCUIT NO. 251
RELAY CONTROL SATURATING MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 251
RELAY CONTROL SATURATING MULTIVIBRATOR



Unless otherwise stated: R in ohms; C in $\mu\mu$f

Components: R2 and R10: ±5% limits; all other R: ±10% limits. All C: ±20% limits. (Note 1.)

Operating characteristics:

Input: 20 volt negative-going waveform or pulse with 10 μsec maximum rise time and minimum duration at −20 volt level of 3 μsec.

Input impedance: 2.5KΩ, or 400Ω with R4 and R8 omitted.

Outputs: Relay K1 energized by 8 ma (on); de-energized by 0.5 ma (off).
Voltage output: 30 ±6 volts.

Relay characteristics: Winding resistance of 2.7KΩ ±10% and power requirement of 100 mw or less.

Power requirement: 1.5 watts total.

Temperature range: −65° C to 125° C.

NOTE:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 251 RELAY CONTROL SATURATING MULTIVIBRATOR

1. APPLICATION

PC 251 is intended for on-off control of electromechanical devices such as relays where the current ratio must be 10 between the on and off condition. The rate usually is limited by the control device response time. If desired, the control current can be reversed in direction between the on-off states.

2. DESIGN CONSIDERATIONS

This circuit is a modification of the saturating multivibrator PC 250. The diode CR2 and resistors R2, R3 are added to isolate the load K1 when Q1 is off. If the values of the resistors are chosen within the proper limits, the off current through the relay is the sum of the leakage currents through Q1 and CR2, or less than 0.5 ma at 125° C. This provides a relay current ratio from on to off of at least 15. For comparison, PC 250 using 2N333 transistors has an on-off ratio of less than 5 for the load currents. The modifications provide an improvement of three times in the current resolution.

2.1 *Circuit Operation:* The circuit operation is that of an ordinary transistor Eccles-Jordan, except that the current drive to hold Q2 in the on state is furnished through R2 and R3 rather than through Q1 collector load. Diode CR2 is nonconducting.

The collector power dissipation limit and the high saturation resistance of the 2N333 require that the collector current not exceed approximately 11 ma for operation to 125° C. Collector resistors of lower value than that shown will cause the collector currents to exceed this limit and will reduce the temperature range accordingly. An increase of impedances would be desirable to decrease dissipation, but the relay coil resistance would have to be increased.

2.2 *Transistor Type:* The high forward resistance of grown junction silicon transistors is incompatible with subminiature relays. The circuit power efficiency falls off sharply as the current is increased above a few milliamperes. Small relays usually require from 5 to 15 ma at a low voltage. The 2N333 was specified as a moderately priced unit in large quantity use. A diffused junction transistor such as the 2N550 has a lower resistance and higher dissipation rating but is more expensive. Lower circuit impedance could be achieved with transistors similar to the 2N550 with a resulting improvement in circuit power efficiency because of the lower permissible collector and base supply voltages.

2.3 *Relay Type:* The relay or other electromechanical device under control must have the characteristic of being energized by 8 ma coil current and being de-energized when the current drops to 0.5 ma. This specification is based on the dc load presented to the multivibrator and the power furnished to the relay winding. The inductance of the coil is unimportant, even though the rise and fall times are somewhat increased. The speed of response depends only on the relay response time.

The maximum power dissipation rating of the coil should be not less than 250 milliwatts.

3. PERFORMANCE

3.1 *Trigger Input:* The input signal required for triggering is approximately the same as that for PC 250, the simple saturating multivibrator. Since a high repetition frequency is not a major consideration, the coupling capacitors C2 and C4 have been increased.

A trigger of 14 volts with a rise time of 10 μsec is usually adequate, but with high h_{FE} transistors at the high limit temperature, a level of about 20 volts provides more dependable operation. The input circuit should be allowed at least 5 milliseconds to recover from a positive signal before the next trigger is applied.

If the source impedance is low enough, R4 and R8 may be omitted. The input impedance is then approximately 400 ohms. Capacitors

C2 and C4 should be increased to 4700 $\mu\mu$f to maintain the proper trigger pulse duration at the base o. the transistor.

3.2 *Voltage Output:* A voltage output in phase with the relay closing may be taken from the collector of Q2. The level will be 30 volts, and a 10% variation in the 150-volt supply and the variability of transistors and resistors will cause a variation of about 6 volts. The source impedance at this output is 5KΩ for the positive excursion and is the saturation resistance of Q2 for the negative excursion.

NOTES TO THE PREFERRED CIRCUITS MANUAL

502632 O-59-4

16. CRYSTAL OSCILLATORS

Crystal oscillators are used as sources of stable signals. They are also used in frequency synthesis systems of electronic communications and test equipment. In these systems, crystal oscillators are usually associated with frequency multipliers and mixers. The frequency stability of such oscillators is generally measured in parts per million, whereas stability measurements for frequency standards are in parts in 10^8 or 10^9.

There are two basic types of crystal oscillators:[1] the type whose frequencies of oscillation are dependent upon the antiresonant or high-impedance properties of the crystal and the type dependent upon the series resonant or low-impedance properties of the crystal. The former type is usually restricted to frequencies below 20 mc, while the latter is useful up to frequencies of 100 mc and higher.

The circuits discussed here will be limited to those operating in the antiresonant mode in the frequency range from 0.8 to 20 mc.

16.1 *Examples of Oscillator Circuits in Current Use:* A total of 27 equipments, 16 Air Force and 11 Navy, were surveyed to determine the most commonly used oscillator circuits and their performance requirements. Sixty-nine oscillators were used in the 27 equipments. The basic types and the number of each type used are listed below.

Cathode Coupled	23
Colpitts	15
Electron-Coupled Colpitts	15
Pierce	6
Electron-Coupled Pierce	2
Miller	2
Electron-Coupled Miller	1
Transformer Coupled	1
Quintuplex	1
Grounded Plate Hartley	3

The first three types comprise more than 75% of the total. Essentially, all military oscillator requirements can be met by use of these three types. Certain design changes may be necessary to meet special requirements. These design changes will be discussed later.

16.2 *Characteristics of Piezoelectric Crystal Units:* The equivalent circuit of a piezoelectric quartz crystal is characterized by a series *RLC* combination shunted by C_o, the holder static capacitance. For this type of network, there are two frequencies at which the reactance becomes zero. The lower frequency is called the series resonant frequency and the crystal impedance is low. The higher frequency is called the anti- or parallel-resonant frequency, where the crystal acts as a high impedance.

In practical oscillator circuits, the antiresonant crystal is associated with a load capacitance, and the crystal equivalent circuit is inductive, forming a parallel resonant circuit at a frequency slightly less than that of the antiresonant frequency of the crystal alone. The impedance of this arrangement is high.

In the frequency range of the Preferred Circuits (PC 101 and 102), the crystals used are of the thickness shear mode of oscillation and oscillate in the fundamental mode.

16.3 *Description of Various Oscillator Circuit Types:* An analysis and description of the more common types of antiresonant oscillators listed in section 16.1 are given below. A more detailed analysis is presented for those types chosen as preferred circuits.

(*a*) Pierce oscillator: The Pierce oscillator, shown schematically in figure N16-1, is an antiresonant type. The equivalent crystal reactance is inductive and forms a tuned tank circuit with the series combination of C_g and C_p in parallel with C_{pg}. The capacitance presented to the crystal is called the load

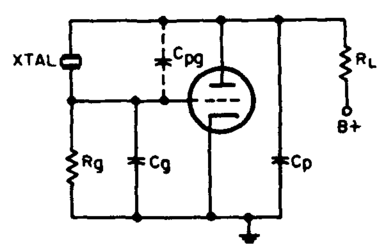


Figure N16-1.—Pierce oscillator.

[1] William A. Edson, *Vacuum-Tube Oscillators*, John Wiley & Sons, New York, N.Y., 1953, pp. 197-226.

capacitance, C_t. The output is developed across the load resistor, R_L. With an untuned load, the output voltage is low, but frequency changes can be accomplished by simply switching crystals on a plug-in basis. For operation at a single frequency, the output may be tuned, resulting in voltage levels considerably greater than those for the untuned output. The circuit is not critical in operation and will oscillate with variations in external circuit component values. The oscillator requires a minimum number of circuit components.

(*b*) Miller oscillator: The Miller oscillator circuit schematic is shown in figure N16-2. Although the operating frequency is more de-

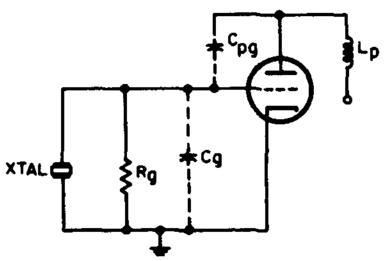


Figure N16-2.—Miller oscillator.

pendent on plate tuning conditions than is that of the Pierce, and the circuit is more complex in design, this oscillator is widely used, since the output voltage is larger than that of the Pierce. The load capacitance of the crystal is a function of C_g, C_{pg}, L_p, and frequency. The frequency dependence precludes use of the oscillator at more than a single frequency on a crystal plug-in basis. Instead, a tuning adjustment is required for operation at a new frequency. Generally, this is accomplished by using a variable capacitor or inductor in the plate circuit. The plate tank is tuned to a frequency above that of the crystal so that the plate impedance will appear inductive, and thus provide the proper phase condition for oscillation. Since C_{pg} is small for pentode tubes, use of this type of tube normally requires the addition of a small capacitor from plate to grid.

(*c*) Colpitts oscillator: The Colpitts, or grounded plate Pierce, circuit is shown in figure N16-3. The plate is ac grounded and the output voltage is developed between cath-

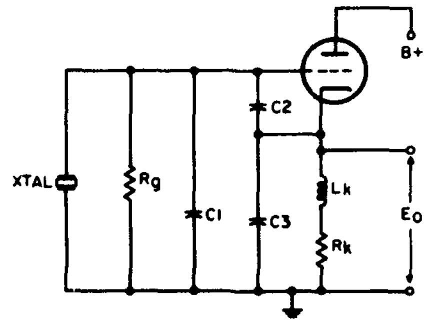


Figure N16-3.—Colpitts oscillator.

ode and ground. The feedback voltage is developed across the grid cathode portion, C2, of the capacitive voltage divider C2, C3. Grid bias is developed on positive voltage peaks when the grid conducts and charges the grid ground capacitance C1. R_g acts as a grid leak and together with C1 performs an amplitude regulating function. The capacitance across the crystal, together with that of the voltage divider, provides the required capacitive load for the crystal. The antiresonant tank is composed of this load capacitance and the equivalent inductance of the crystal.

If C1 of figure N16-3 is kept constant, and the ratio of C3/C2 is changed to keep the total capacitance looking out from the crystal terminals constant at 32 $\mu\mu f$, then the voltage amplitude across the crystal and the voltage amplitude across the load will vary as shown in figure N16-4.[2] These voltage amplitudes have been normalized with respect to the maximum voltage across the crystal. The measured quantities are shown as dashed lines, and the computed quantities are shown as solid lines. In the computed case the factor due to grid loading was neglected. This factor effectively reduces the C3/C2 ratio, and a higher output results. The measured data does not go below a ratio of 1.0 because the output load and distributed capacitances make a value less than 1.0 impractical. The broken line curve shows the change in parts per million of the output frequency as a function of capacitance ratio for a 10% change in supply voltage. This is a measure of the stability of the circuit, since a decrease in transconductance with tube life will tend to change the plate resistance of the tube in the same direction

[2] H. E. Gruen, "How to Design Colpitts Crystal Oscillators," Electronics, January 1, 1957.

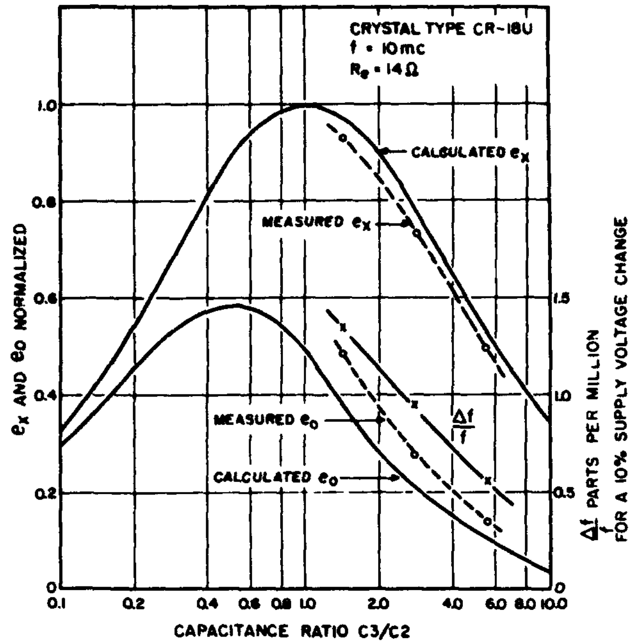


Figure N16-4.—Circuit performance, Δf/f, vs. capacitance ratio, C3/C2, for total capacitance C_t=32 μμf. (e_x is the voltage across the crystal; e_0 is the output voltage.)

as a decrease in supply voltage. This change in plate resistance will be translated into a change in output frequency.

(*d*) Electron-coupled oscillators: The oscillators described in the preceding sections (a) through (c) are all adaptable to electron coupling. Generally, the oscillators as given utilize triode tube sections. For electron coupling, pentodes are used.

The most commonly used electron-coupled pentode is the electron-coupled Colpitts oscillator (see list in section 16.1). The pertinent circuit parameters of this oscillator are shown in figure N16-5. The load is well isolated from the oscillator portion of the circuit, and the load circuit is readily adjustable to obtain harmonics of the crystal frequency.

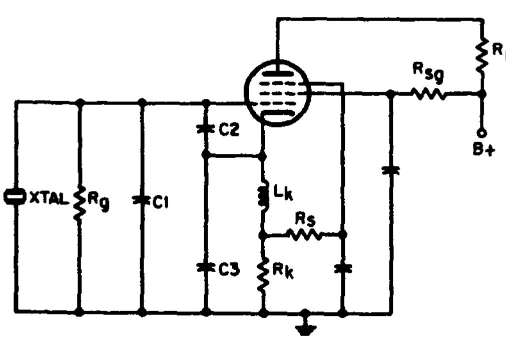


Figure N16-5.—Electron-coupled Colpitts oscillator

Pentode tube types having internal suppressor-to-cathode connections are not the most desirable types for electron-coupled circuits, since the capacitance from plate to cathode allows coupling external to the electron stream. Use of a pentode with an external suppressor lead allows grounding of the suppressor by a capacitor. The suppressor-to-cathode dc potential may be maintained substantially at zero by returning the suppressor through a resistor (R_s) to the junction of the cathode inductor (L_k) and the cathode bias resistor (R_k).

16.4 *Criteria for the Selection of the Preferred Circuits:* The factors influencing the selection of Preferred Circuits 101 and 102 are discussed below.

(*a*) Selection of PC 101: The primary advantage of the Colpitts oscillator is circuit simplicity. Output is fair over the range of crystal resistances specified by MIL-C-3098B. Frequency change is accomplished by utilizing crystals on a plug-in basis. From an operational standpoint, the Colpitts and Pierce oscillators are similar, but the former circuit offers greater advantage when operation over a range of frequencies is required.

In the Colpitts design, only adjustments for proper load capacitance and capacitance ratio values are necessary. These adjustments are made by measuring the grid-to-cathode, cathode-to-ground, and grid-to-ground capacitances and adding physical capacitors to obtain the desired values of each. For most military type crystals, the load capacitance, C_t, is 32 ±0.5 μμf, which is the value used in PC 101.

Although the Miller circuit produces higher output voltage than do the Colpitts or Pierce circuits, it has the disadvantage of requiring a tuning adjustment, which must be accurately set for each operating frequency. Its frequency is also more sensitive to changes in load impedance. Comparison of the characteristics and information on usage of these circuits formed the basis for selection of the Colpitts oscillator as a preferred circuit for low frequency operation where a reliable circuit providing reasonable output into low to medium impedance loads is required.

(*b*) Selection of PC 102: The electron-coupled Colpitts oscillator has advantages similar to those of the Colpitts circuit, plus the desirable characteristics of isolating the effects of load impedance changes from the oscillator portion of the circuit. Harmonics of the crystal frequency may be obtained by tuning the plate circuit for the desired frequency. Tuning is accomplished by adjusting the plate tank to obtain a maximum output voltage at the desired frequency, be it fundamental or harmonic. Changes in fundamental frequency are made on a crystal plug-in basis, as in the Colpitts. The electron-coupled Colpitts oscillator produces nearly as high a voltage as the Miller, and can be made almost completely independent of loading effects. It was thus selected for a preferred circuit to provide a stable fundamental or harmonic signal for use in control and synthesis systems.

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