CHAPTER 16

OPERATING PRINCIPLES OF A REPRESENTATIVE H-F RADIO TRANSMITTER, AN/WRT-2

INTRODUCTION

Radio Transmitting Equipment, Navy model AN/WRT-2, is capable of delivering an average power output of 500 watts and a peak envelope power (PEP) of 1000 watts in one-kc steps (or continuously) over a frequency range of 2.0 to 30.0 megacycles. The AN/WRT-2 provides for emission of machine (MACH) or break-in (C-W) hand-keyed telegraphy, frequency-shift-keyed (FSK) teletype, compatible amplitude-modulated speech, single sideband suppressed carrier (SSB), independent sideband (ISB), and facsimile by using appropriate terminal equipment. This communications equipment may be installed aboard ships, submarines, and at shore stations.

GENERAL DESCRIPTION

The major components of the AN/WRT-2 radio transmitting equipment (fig. 16-1) are the transmitter group, (radio-frequency amplifier, radio-frequency oscillator, electrical frequency control, amplifier power supply, and power supply) and the radio frequency tuner.

The radio transmitter group contains all of the equipment required for transmission by machine or break-in c-w, independent sideband (ISB), single sideband (SSB), a-m phone, and/or frequency-shift-keying (FSK), except such accessories as the key (machine or hand), antenna, and remote operating components. Facsimile transmission requires additional terminal equipment.

The transmitter may be operated from a three-phase, 60-cps ship's supply of 115 v, 220 v, or 440 volts. The transmitter group is coupled to an antenna (not shown) through a radio-frequency tuner and associated antenna control circuits.

Provision is made for a total of 6 audio inputs. Front panel handset jacks are furnished for local phone operation of the equipment with a handset. Remote phone- and/or hand-key operation is also possible.

Provision is made for interconnections to teletype and telegraphy equipment and to a remote transmitter standby control. An internal dummy load is provided for transmitter tuneup.

OVERALL BLOCK DIAGRAM

The AN/WRT-2 consists of the following functional sections: r-f generating, power amplifier, modulating, primary power, and low voltage power supply, as shown in figure 16-2.

The r-f generating section produces the r-f signal in conventional master oscillator-frequency multiplier circuits and applies it to the power amplifier. The master oscillator is slaved to the assigned operating frequency by a unique frequency control circuit treated in detail later in this chapter.

The power amplifier section raises the r-f signal input power from the r-f generating section to the desired operating power level. The output of the power amplifier is fed to the antenna via the r-f tuner circuits.

The modulating section accepts audio signals or d-c keying signals (for C-W or FSK operation) and suitably transforms these signals to modulate or control the r-f energy generated by the r-f generating section. The output of the modulating section is applied to the input mixer in the power amplifier section.

The low voltage section contains all the circuits which supply low d-c voltages to the transmitting set. The high voltage supply is contained in the power amplifier section and supplies the plate voltage for the power amplifier tubes.

The primary power section supplies all a-c voltages for the transmitting set. The transformers in the primary power section have taps to provide input voltages of 115 v, 220 v, and 440 v at 60 cps.
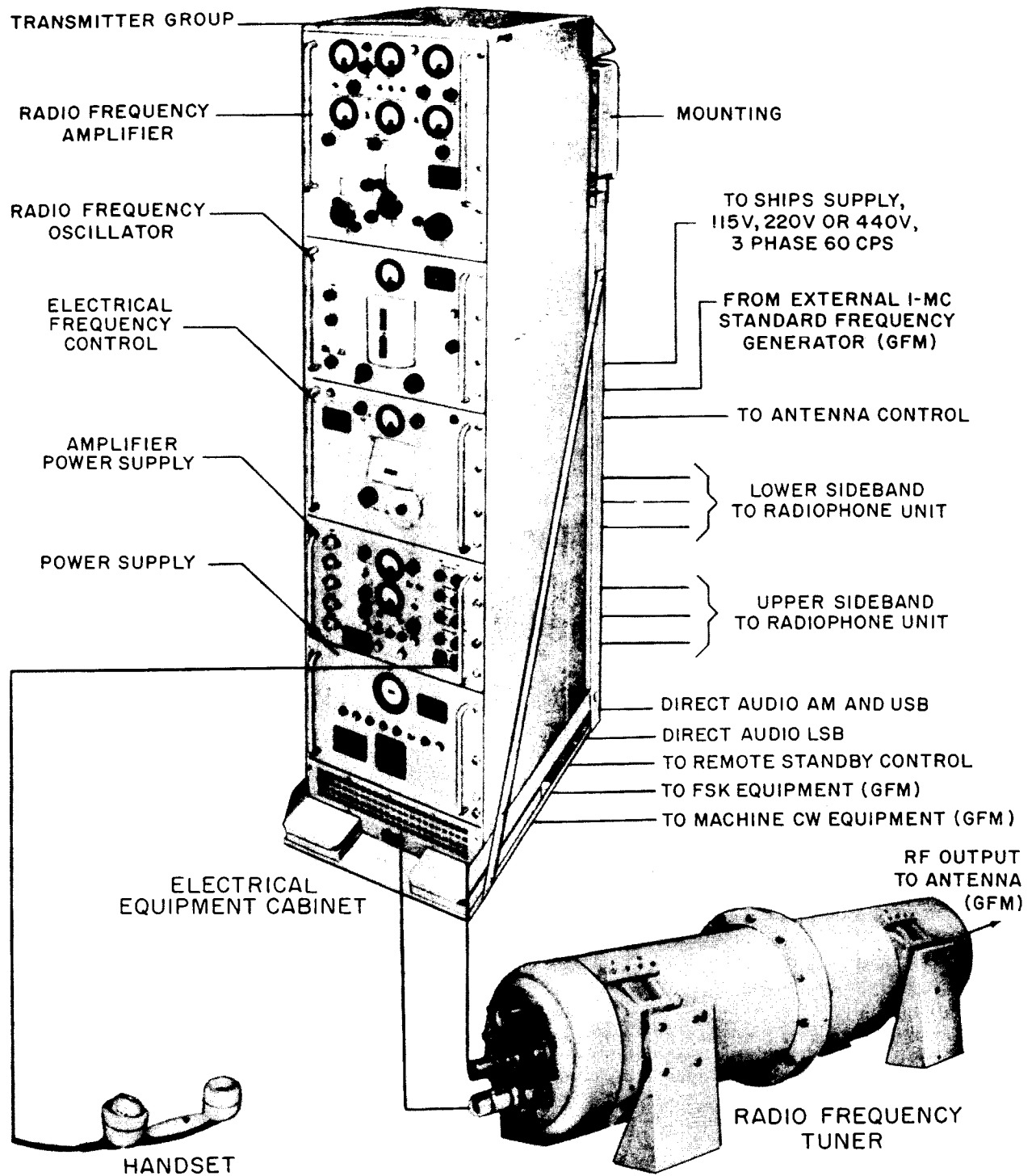
TRANSMITTER GROUP

RADIO FREQUENCY AMPLIFIER

RADIO FREQUENCY OSCILLATOR

ELECTRICAL FREQUENCY CONTROL

AMPLIFIER POWER SUPPLY

POWER SUPPLY

MOUNTING

TO SHIPS SUPPLY, 115V, 220V OR 440V, 3 PHASE 60 CPS

FROM EXTERNAL 1-MC STANDARD FREQUENCY GENERATOR (GFM)

TO ANTENNA CONTROL

LOWER SIDEBAND TO RADIOPHONE UNIT

UPPER SIDEBAND TO RADIOPHONE UNIT

DIRECT AUDIO AM AND USB

DIRECT AUDIO LSB

TO REMOTE STANDBY CONTROL

TO FSK EQUIPMENT (GFM)

TO MACHINE CW EQUIPMENT (GFM)

RF OUTPUT TO ANTENNA (GFM)

ELECTRICAL EQUIPMENT CABINET

RADIO FREQUENCY TUNER

HANDSET

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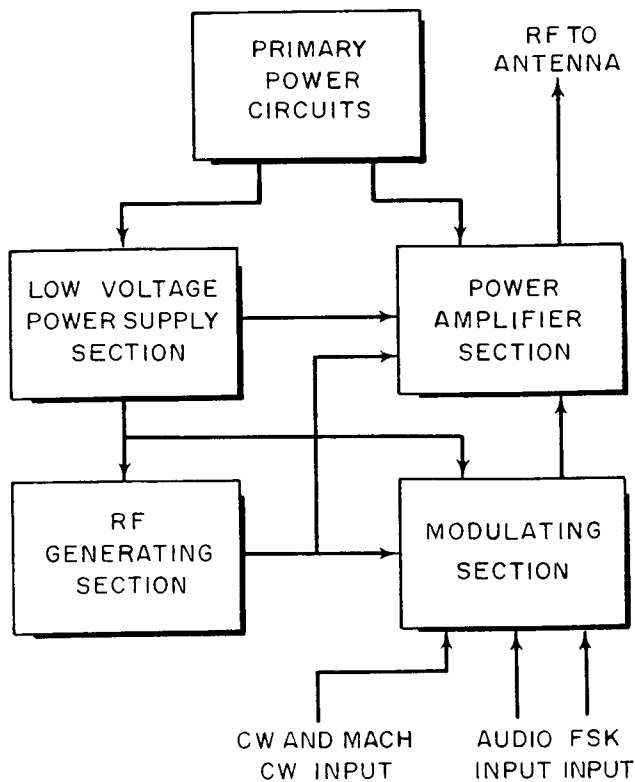Figure 16-1.—Radio Transmitting Set AN/WRT-2, relationship of units.

Figure 16-2.—Overall block diagram. 32.279

R-F GENERATING SECTION

The complete frequency coverage of Transmitting Set AN/WRT-2 is accomplished in 12 bands. The master oscillator, V301 (fig. 16-3) which is located in the radio-frequency oscillator chassis, generates r-f signals from 1.5 mc to 7.5 mc. These signals are amplified by V302. For bands 1 through 6, the fundamental frequencies (1.5 to 7.5 mc) of the master oscillator are fed directly to the power amplifier section through S302. For bands 7 through 9 the fundamental frequencies of bands 4 through 6 (3.75 to 6.75 mc) are doubled by the first doubler, V303, and fed through S302 to the power amplifier section. For bands 10 through 12 the fundamental frequencies of bands 4 through 6 are multiplied four times by the action of the first and second doublers, V303 and V304, before being applied to the power amplifier section.

In addition to supplying the power amplifier section input, the S302 output is also fed to the electrical frequency control circuit (fig. 16-4). This circuit supplies a frequency correction voltage to the master oscillator V301 which keeps the oscillator operating at the selected frequency with the stability of 1 part in 10^8 cps.

The control of the master oscillator frequency is accomplished by two independent operations. First, the output of the master oscillator (via amplifier V302 and the frequency doublers) is compared with that of an interpolation oscillator in a master oscillator phase detector. Any difference between these two frequencies causes a correction voltage to be applied to the master oscillator (MO), and thereby forces the oscillator to return to the proper operating frequency.

Second, when operating in 1 kc steps, the interpolation oscillator is frequency stabilized in order to provide improved accuracy in correcting the master oscillator frequency. The control of the interpolation oscillator (IO) involves the locking-in of this circuit to multiplies of 1 kc. This action is accomplished by comparing the output of the interpolation oscillator with a 1-kc crystal stabilized reference signal to
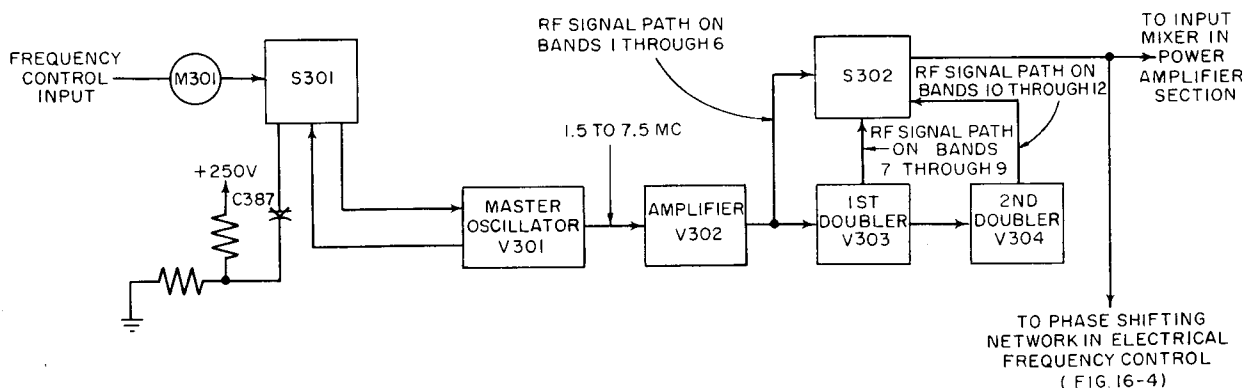

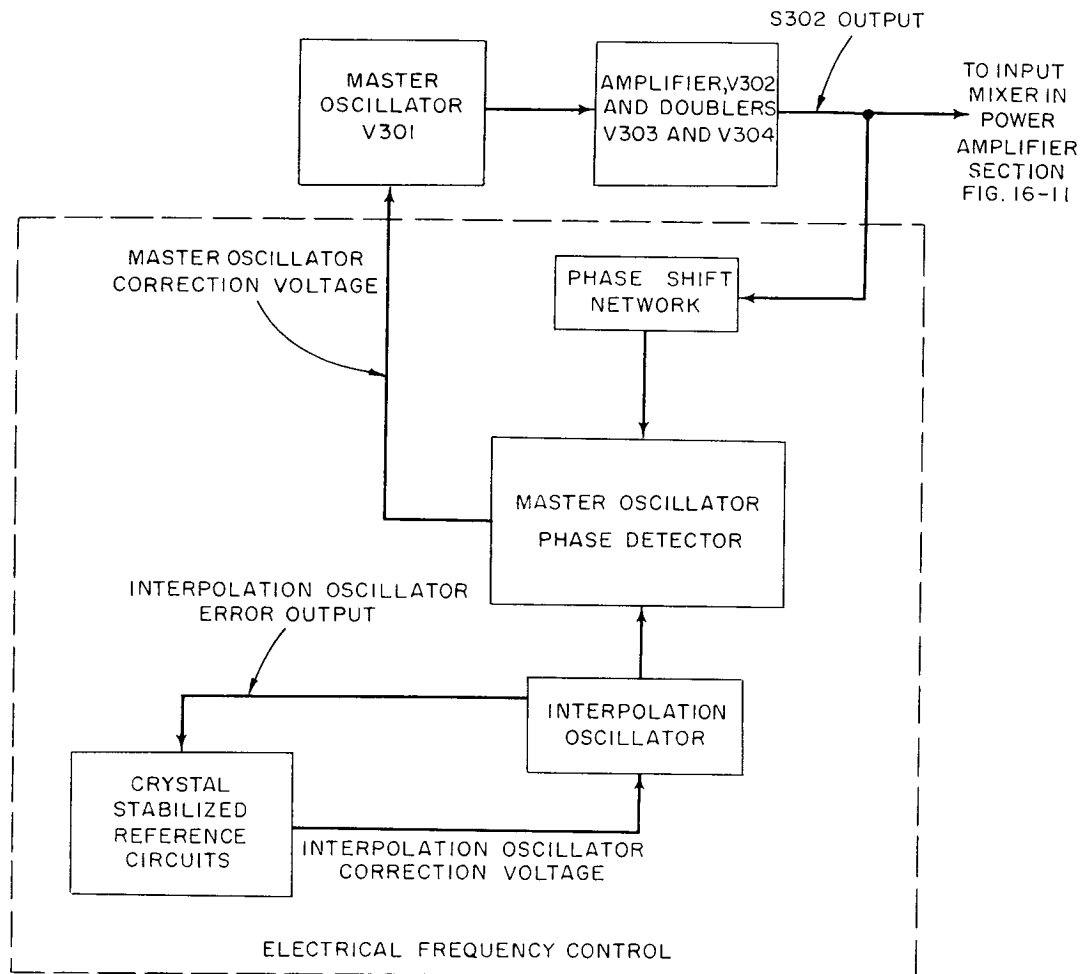Figure 16-3.—Radiofrequency oscillator. 32.280

Figure 16-4.—Electrical frequency control circuit, simplified block diagram.

32.281

develop an interpolation oscillator correction voltage. The correction voltage is applied to the interpolation oscillator and holds it at the required frequency. Thus, the controlled stability of the IO results in an added stability of the MO.

DETAILED BLOCK DIAGRAM

The front panel of the radio-frequency oscillator and electrical frequency control chassis showing the indicators and controls is shown in figure 16-5. A more detailed block diagram of the electrical frequency control circuit is shown in figure 16-6.

The r-f input from the radio-frequency oscillator circuit (fig. 16-3) is applied to the

frequency control circuits through a phase-shift network consisting of FL603. Sealed unit FL603 contains two independent phase-shift networks. The networks are so designed that the signal coupled to the top balanced mixer always leads the signal coupled to the bottom mixer by 90°. The outputs of the phase-shift network (FL603) are therefore sine and cosine functions of the r-f signal.
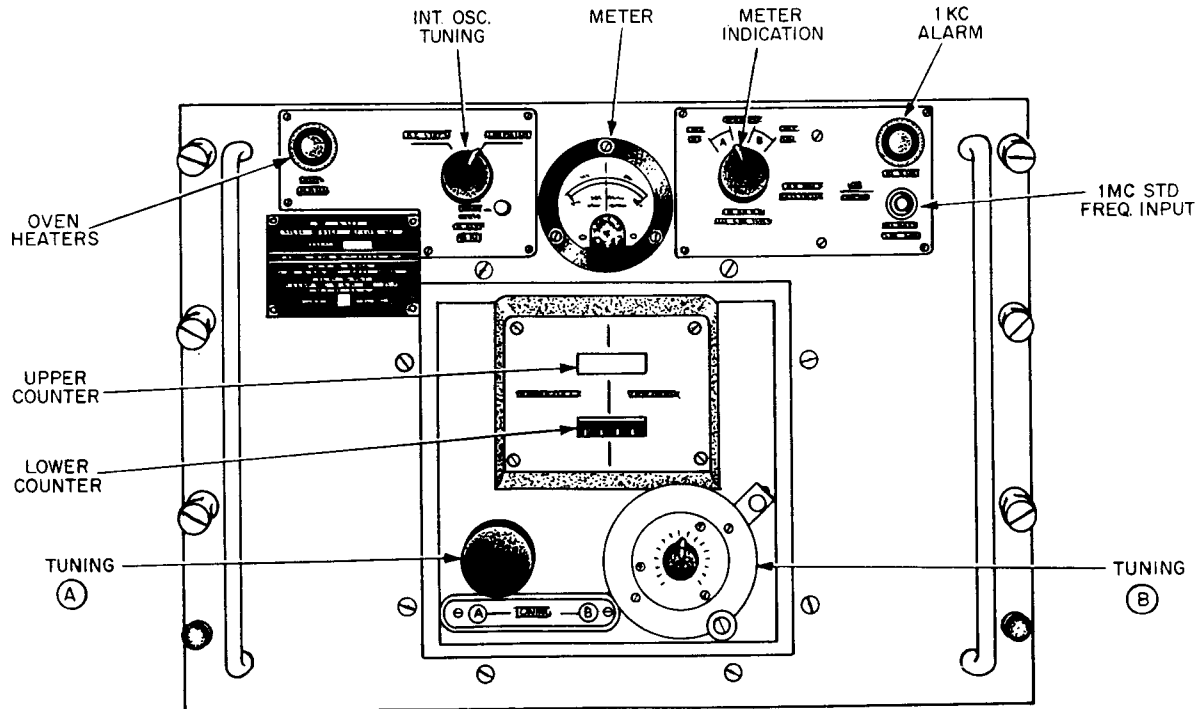
A second input to the mixers is received from the 1-mc oscillator and divider circuits from T608.

1-mc Crystal Oscillator

The 1-mc crystal oscillator (Q1301 and Q1302) is used as a frequency standard to
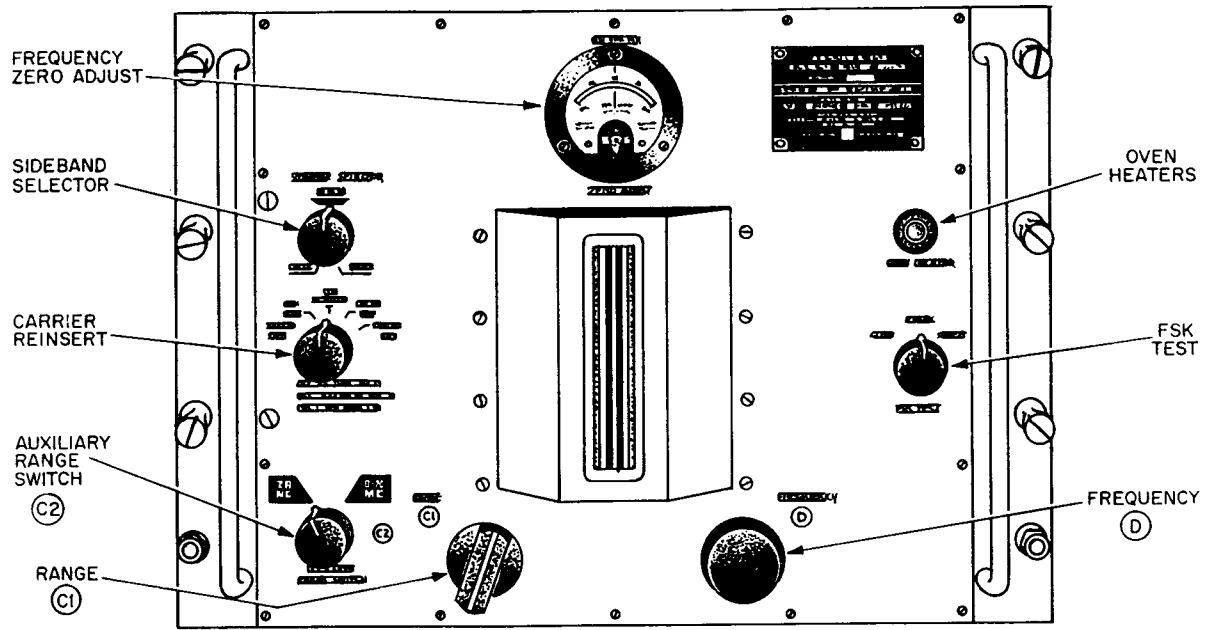
A. Radiofrequency oscillator.   B. Electrical frequency control (front panels).

Figure 16-5.—Pictorial diagrams AN/WRT-2.

provide maximum frequency stability of 1 part in 10^8. The crystal operates in a precisely controlled constant-temperature oven (not shown). The 1-mc output is amplified by 1-mc amplifiers Q1303 and Q1304 and applied to a 10:1 frequency divider circuit consisting of transistors Q1305 through Q1308, and Q1313 through Q1316. The first stage of the divider circuits divides the 1-mc frequency in half. This 500-kc signal is applied to the 500-kc selector in the modulator section, the 1-mc phase detector, and to the rest of the divider circuits. The purpose of the modulator section input is treated later.

The final output of the frequency divider is a 100-kc signal.

The 100-kc signal is amplified by 100-kc amplifier Q1317 and buffer amplifier V605 and applied to T608. The signal appearing at terminal T3, of T608 is coupled to saturable core reactor L614 where a harmonic-rich peaked waveform is produced. The 100-kc signal and its harmonics are applied to the balanced mixer stages where, due to the simultaneous application of the master oscillator signal, sum and difference fr quency components of the two applied signals are produced. The sum and difference frequencies (upper and lower sidebands) contain the r-f oscillator error frequency component.

Sideband Generating Method

The phase-shift method of generating sideband (sum and difference) frequencies is employed. The r-f input signal is shifted 90° in phase by FL603 and applied to the balanced mixers as previously discussed. The mixers are connected in a push-pull circuit arrangement. The combined action of the mixers and phase-shift networks FL1 and FL2 (at the mixer outputs) assure that the desired sideband frequencies add and the other sideband frequencies are canceled in the output. This action produces only one of the sidebands at the grid of i-f amplifier V601A, and the need for narrow band filters is eliminated.

For example, a master oscillator (MO) frequency of 2460 kc is heterodyned with 2400- and 2500-kc harmonics of the L614 output to produce 2460 -2400 or 60-kc, and 2500 -2460 or 40-kc sidebands in each of two mixers. The 40-kc sidebands are shifter 180°, and cancel at the output of FL1 and FL2. The 60-kc sidebands are brought into phase (0°), and the amplitudes add at the V601A grid.

When the MO frequency is 2440 kc there are 2500 -2440 or 60-kc, and 2440 -2400 or 40-kc sidebands produced. In this case the 60-kc and 40-kc phase relations in the two mixers are reversed from their original relation. For the two 60-kc sidebands the reversal is due to the fact that in the first case the 2460-kc MO frequency is above the 2400-kc harmonic and in the second case the 2440-kc MO frequency is below the 2500-kc harmonic. Thus the 60-kc sidebands are shifted to cancel and the 40-kc sidebands are shifted to add.

The acceptable sideband signal is then passed through five cascaded amplifiers, V601A & B, V602A & B and V603A (fig. 16-6). A band-pass filter (not shown) between the first and second i-f amplifiers limits the response of the i-f amplifier strip to the frequency range of 50 to 100 kc. The plate output of the fifth i-f amplifier, V603A, is applied to the master oscillator-phase detector (MOPD). The cathode output of V603A is applied to the 100-kc phase detector for purposes described later.

The selected sideband signal is heterodyned in the master oscillator-phase detector with a signal input from the interpolation oscillator (IO) to produce the master oscillator error voltage. For comparison with the interpolation oscillator output, the range of which is 50 to 100 kc in 5 bands, the sideband frequencies generated at the balanced mixers must be limited to the range of 50 to 100 kc. Therefore, when the last 10-kc digits of the sideband frequency are in the range of 0 to 50 kc, the output of one of the balanced mixers is reversed by mechanical means and the sideband phase relationships are maintained as in the first example. A relay (not shown) which is energized by the IO tuning A control, located on the electrical frequency control (fig. 16-5B), controls the output switching when the last 10-kc digits of the sideband frequency are less than 50 kc.

MASTER OSCILLATOR-PHASE DETECTOR

The master oscillator-phase detector (MOPD) provides a d-c correction voltage stabilizing signal for the master oscillator (MO) when the oscillator is not operating at the proper frequency. The polarity depends upon the direction of the error and the amplitude upon the amount of error. The MOPD (fig. 16-7, A) consists of crystal diodes CR606 through CR609, current limiting resistors R653 through R656, and transformers T604 and T605. The i-f signal

from the fifth i-f amplifier V603A is applied (via T604) to the junction of crystal diodes CR606-CR607, and CR608-CR609. The signal from the interpolation oscillator (IO) is applied to the T605 secondary which is connected between points B and D of the circuit. The MOPD output is a d-c correction voltage developed across C652.

When the MO is locked on frequency, the i-f signal is 90° out of phase with the IO signal (i-f signal leading) and no correction voltage is fed back to the MO circuit.

Let us assume that the amplitudes of both the i-f and IO signals (fig. 16-7, A) are 2.0 volts peak-to-peak. The polarities shown on the bridge (fig. 16-7, A) are for the first quarter-cycle of the waveforms. The waveforms represent the voltage variations to ground at the four corners of the bridge.

The IO signal is used as a reference frequency. Figure 16-7B illustrates the relative phase of the IO and i-f signals for zero error (i-f leading the IO by 90°), lagging error (i-f leading the IO by 45°) and leading error (i-f leading the IO by 135°). Also shown is the conducting period for each diode (CR606 through CR609) for one complete cycle.

Phase error is generally limited to a few degrees or even a fraction of a degree. In most cases, large errors exist only when the equipment is first turned on or when the circuit is not properly aligned. A large error (45°) is assumed here because it lends itself better for a simple circuit analysis.

When the i-f leads the IO by exactly 90° (the zero error condition), the phase detector will not produce a d-c correction voltage output across C652. Instead, an a-c voltage is produced. The manner by which this voltage is produced is indicated in figure 16-7C.

At t = 0°, the i-f voltage is positive maximum and the IO voltage is zero. Diodes CR607 and CR609 are conducting as shown by the arrows representing electron flow. Tracing around path FCDGF, the voltage from F to C is equal and opposed to the drop from C to D, so that there is no charge accumulated on C652 (C652 is relatively large).

Likewise, at t = 45° (fig. 16-7C) the arrows and polarities indicate the applied voltage and conducting diodes. The series aiding voltages in the lower half of the T604 secondary and the right half of the T605 secondary cause a current which charges C652 negative to ground.

At 90° (fig. 16-7B) the i-f voltage is zero and the IO voltage is positive maximum. Diodes CR609 and CR608 are conducting and again

there is zero voltage across C652. Note when either the i-f voltage or the IO voltage is zero, the output voltage is zero. At 135° (fig. 16-7C), the series aiding voltages in the lower half of the T604 and left half of the T605 secondaries cause a current flow which charges C652 positive to ground. A similar analysis at 180°, 225°, 270° and 315° will further indicate that the C652 output voltage for zero error is alternately negative and positive to ground, and no d-c error voltage is fed to the RFO when the IO and i-f signals are exactly 90° out of phase.

Now consider the phase detector action to produce a d-c correction voltage when the i-f signal leads the IO signal by only 45° (lagging error, fig. 16-7D). At zero degrees no voltage is developed across C652. At 67.5°, the series aiding voltages in the lower half of the T604 secondary and the right half of the T605 secondary cause a current which charges C652 negative to ground. Likewise, at 90°, C652 is still charged negative to ground. However, at 135°, no charge is accumulated on C652.

At 135° (fig. 16-7B) diodes CR608 and CR609 are conducting and the output voltage on C652 is positive to ground (135° to 180°, fig. 16-7D). However, the output voltage is predominantly negative (0° to 135°) for a lagging phase error (i-f leading the IO by only 45°). Thus, the voltage fed to the RFO for this error condition will be a negative d-c voltage with an a-c component (pulsating direct current).

A leading phase error between the IO and IF signals exists when the i-f leads the IO by more than 90°. This condition will produce an a-c voltage across C652 which is predominantly positive to ground. Figure 16-7E shows the polarities, conducting diodes, and C652 charge at 112.5° and 292.5° of the reference IO signal.

The C652 output (fig. 16-7A) is fed through a filter (L621-R692), switch section S302H, and the selected portion of a voltage divider to a voltage-sensitive capacitor (C387). The filter removes the a-c component of the correction voltage.

The voltage-sensitive capacitor is placed in shunt with the master oscillator tuned circuit. The capacitance of C387 changes in accordance with the magnitude of the d-c correction voltage from the MOPD. The change in the oscillator tank capacitance corrects the oscillator frequency.

The action of S302H and the voltage divider (comprising R396 through R399 and R401 through R407) corrects the amount of error voltage fed back on the selected band so that the amount of oscillator frequency change on all

bands is the same for a given d-c error voltage developed at the MOPD.

100-KC PHASE DETECTORS

The fundamental 100-kc signal at L614 (fig. 16-6) is of greater amplitude than any of the generated harmonics. If the mixers are not in exact balance, it is possible for the 100-kc signal to be fed through the balanced mixers and the i-f stages to the master oscillator-phase detector. This action would cause an erroneous d-c correction signal to be fed from the master oscillator-phase detector to the master oscillator and thereby cause the oscillator to operate at an undesired frequency.

Because the i-f band pass will accept and pass the 100-kc fundamental, it is necessary to keep the mixer stages extremely well balanced. Aging of circuit components and ambient temperature variations inevitably introduce some imbalance; therefore an automatic balancing circuit is provided to null the unwanted 100-kc signal.

The 100-kc balancing network consists of two 100-kc phase detectors. A sample of the i-f signal is taken from the cathode of V603A and applied to both of the 100-kc phase detectors. As shown in figure 16-6, a 100-kc reference signal is also applied to the phase detectors via T608 from buffer amplifier V605.

The 100-kc signal output of one of the balanced mixers is 90° out of phase with the output of the other mixer as discussed previously. Because of this relationship, a phase shift at the detector input shifts the phase of the reference signal applied to one of the 100-kc phase detectors. When no i-f error is introduced, no correction voltage is developed. The presence of an i-f error input from the V603 A cathode causes a d-c correction voltage to be developed at the 100-kc phase detector output. The phase of the i-f input from V603A indicates which mixer is unbalanced. The polarity of the 100-kc phase detector output voltage is proper to provide bias to the mixer which is passing the 100-kc signal. This action causes the 100-kc signal in the two balanced mixers to again cancel and thus nullify any master oscillator error which might otherwise be caused by the 100-kc signal.

INTERPOLATION OSCILLATOR

Interpolation oscillator V606, provides a stabilized reference signal which is compared in the master oscillator-phase detector with the signal delivered through the i-f amplifiers.

The comparison i-f signal from V603A and the IO signal from V606 (via V603B) are fed to the MOPD. As shown earlier, when the two signals are exactly 90° out of phase, no correction voltage is fed back to a voltage-sensitive capacitor (shown later) in the MO circuit and the MO frequency remains unchanged. When any other phase difference is present, due to a shift in the frequency of the MO, a correction signal of proper polarity is applied to the MO to bring this circuit back to the proper frequency. FREQUENCY ZERO ADJUST meter M301 (fig. 16-5) in the r-f oscillator indicates the magnitude and polarity of the correction current.

Frequently it is necessary to determine the interpolation frequency. The IO circuit is designed so that only signals in the 50- to 100-kc range are produced, although the frequency applied to the MOPD can be varied over the 2- to 30-mc range. In order to determine the IO frequency it is important to interpret the frequency readings on the front panel counters of the frequency control group correctly. The following steps should be accomplished. When the two last place digits of the master oscillator frequency are greater than 50 kc (such as 2355, 2460, 1670, or 1990 kc), the IO frequency is the same as that indicated by the last two digits on the upper counter (fig. 16-5). If the MO frequency is 2460 kc, the i-f and also the IO frequencies are 60 kc.

However, when the two last place digits of the MO output are less than 50 kc (such as 2345, 2440, 1630, or 1910 kc) the IO frequency is 100 kc minus the last two digits of the frequency indicated by the lower counter. Thus, when the MO frequency is 2430 kc, the i-f signal and the IO frequencies are 100 - 30 = 70 kc.

The d-c correction voltage for the MO contains some harmonics of the comparison i-f signal frequency. These harmonics are removed by a 10-kc low-pass filter inserted between the MOPD and voltage-sensitive capacitor in the master oscillator. However, low frequency spurious signals may still be present in the output of the low-pass filter. In order to remove such spurious signals, feedback amplifiers V607A & B and V608A have been inserted in this circuit. Any spurious signals appearing at the output of the low-pass filter are fed to grid 7 of first feedback amplifier V607A. The first, second, and third feedback amplifiers amplify the spurious signals. The V608A is applied as a degenerative feedback to the MO input to cancel the spurious signal.

The d-c correction voltage is not affected by the feedback circuit because the amplifiers do not pass the d-c component of the correction voltage. Meter M601 is used to zero the MO tuning. This meter is also used to measure the amount of deviation between the 1-mc crystal oscillator (Q1301, Q1302) and an external 1-mc standard frequency.

In order to keep the frequency control loop as stable and rapid-acting as possible, it is necessary to keep the gain in the a-c loop containing the 10-kc filter and feedback amplifiers approximately constant. However, at high operating frequencies a given d-c control signal to the voltage-sensitive capacitor in the master oscillator produces a greater amount of frequency correction than that which occurs at low frequencies.

In order to overcome this change in sensitivity, the input to V607A is shunted by a capacitive feedback network which is connected between the V607B cathode and the V607A control grid. The feedback network (not shown) is contained in the frequency compensating attenuator. The voltage at the V607A input thus lags the applied voltage. As the operating frequency increases, the voltage developed across the input network decreases. This action, in effect, lower the input impedance to the feedback amplifiers and slows down the correction response as the operating frequency increases.

A third feedback signal from the feedback amplifier applies a regenerating control signal from the V607B cathode through the network containing L623 and C708 to the V607A control grid. This signal permits the feedback amplifier circuit to oscillate at approximately 2 cps when the oscillator control circuit is not locked-in at the proper operating frequency. The oscillator sweeps across a limited frequency range until the control circuits lock-in. When the frequency is correct the regenerative feedback drops to zero and oscillations in the feedback amplifiers are no longer sustained.

It was stated earlier that frequency error in the interpolation oscillator frequency is corrected by comparing the IO frequency with that of the 1-mc crystal oscillator reference frequency. The crystal oscillator frequency is first converted to a 1-kc signal. This frequency is compared with the IO frequency to produce a correcting voltage when operating in 1 kc steps.

The 100-kc pulse signal, which is derived from the 1-mc crystal oscillator, Q1301 and 1302 (fig. 16-6), is applied from L614 to buffer amplifier V604A. The 100-kc input is divided 100 times to produce a 1-kc output by the combined actions of two 5:1 dividers (V604B and V610A) and a 4:1 divider V610B.

The 1-kc signal from V610B is delivered to the 1-kc phase detector circuit consisting of T616 and crystal diodes CR632 and CR633. Here it is compared with the signal from the IO and a d-c correction voltage is developed. This correction voltage is applied to sweep oscillator and d-c amplifier circuit V609A.

When the IO circuit is not locked-in at a multiple of 1 kc, a positive-going error voltage signal is applied to the grid of sweep oscillator and d-c amplifier V609A. The plate voltage decrease of V609A is applied to the grid of sweep oscillator V609B. The resultant plate output of V609B is applied through an isolation network as a regenerative input to the V609A grid. This action produces a sweeps voltage which is fed from the cathode of V609A through M601 to the interpolation oscillator phase detector reactance modulator which causes the IO to sweep over a narrow band and "hunt" for the proper lock frequency. Meter M601 provides an indication of the amount of the correction voltage.

MASTER OSCILLATOR-FREQUENCY MULTIPLIER CIRCUIT ANALYSIS

The circuit discussion of the AN/WRT-2 transmitter is limited to a treatment of non-conventional transmitter circuitry. Many of the circuits contained in the AN/WRT-2 are common to transmitters and are discussed in detail in other chapters of this text. These circuit treatments are not repeated here. The circuit operation of the MOPD is treated earlier in this chapter.

MASTER OSCILLATOR

The circuit of the master oscillator is shown in figure 16-8. The circuit arrangement is that of a Colpitts oscillator.

The oscillator functions the same on all bands. The component changes necessary to produce the required output frequency at the oscillator is accomplished by switch S301. Because of doubling or quadrupling in subsequent stages (discussed later) the transmitter can be tuned over more than one band while S301 is in a given position.

All of the master oscillator frequency determining elements are mounted in a temperature-controlled oven (not shown). These elements consist of voltage-sensitive capacitor C387, L304, and all of the capacitors in the grid

circuit of V301. Tuning within the selected band is accomplished by frequency ⒟ capacitor C313. Variable capacitor C308 provides a tuning control for the high end of the frequency band during alignment. Variable coil L304 is used to set the low frequency end of the band.

A gear train (not shown) controls the oscillator tuning. The RANGE ⒞ (fig. 16-5A) and FREQUENCY ⒟ controls are the two driven tuning controls for the oscillator. The RANGE ⒞ control selects the frequency band, and the FREQUENCY ⒟ control tunes the oscillator to the frequency within the selected band.

The plate output of V301 (fig. 16-8) is amplified in buffer V302. This stage isolates the oscillator from the frequency multiplier stages of the transmitter and thus prevents the low impedance input to the multipliers from acting as a load on the oscillator. This action improves the stability of the oscillator.

FREQUENCY MULTIPLIER CIRCUITS

The frequency range of each of the twelve combinations of master oscillator-frequency multiplier circuit arrangements, the position of S302, and the associated band is shown in the table in the middle of figure 16-8. For simplicity, only the master oscillator tank circuits of bands 4, 7, and 10 are shown in the simplified schematic since the MO operates at the same frequency for each of these bands. Switch S302 selects the proper arrangement of tuned circuits in the multiplier stages to produce the desired transmitter output frequency.

The master oscillator signal is coupled to the multiplier stages (or PA) via T301. Note that on bands 1 through 6 switch section S302C applies a ground to terminal 4 of T301 and the oscillator input is fed from terminal 3 of T301 through any one of the contacts 1 through 6 of S302G (depending on the selected band) to the input mixer stage in the power amplifier and to the master oscillator-phase detector.

On bands 7 through 9 (S302 positions 10 through 12), the ground is removed from terminal 4 of T301 and applied to the center-tap of R308. This action permits the oscillator input voltage to be developed in the 5-6 and 7-8 windings, respectively, of T301, and applied to the grid of first doubler V303. (Doubling takes place in the grid circuit of V303 due to the diodes CR301 and CR302.) Simultaneously, S302E applies a ground to terminal 4 of T302 at the first doubler output. Thus, a frequency output of V303 which is twice the oscillator frequency is fed from terminal 3 of T302 through

the selected contact (10, 11, or 12) of S302G to the output circuit.

Finally, on bands 10 through 12 (S302 positions 16, 17, and 18), the ground is removed from terminal 4 of T302 and applied to the arm of R313. The R308 arm remains grounded by the action of S302G. This action permits the first doubler output to be again doubled in the grid circuit of the second doubler V304. The second doubler plate output is fed through S302F to the primary of T303. The output is fed from the T303 secondary through contacts 16, to the output circuit. Similar circuits (not shown) with separate output coupling transformers are used on bands 11 and 12.

Transformer T303, FREQUENCY ⒟ tuning capacitor C341C and trimmer capacitor C376 tune the V304 doubler plate tank. Capacitor C341B tunes the first doubler plate tank with trimmer C361. Resistors R308 and R313 are used as balance potentiometers for their respective doublers. When these resistors are properly set, the associated crystal diodes conduct equally on peaks of the applied r-f voltage.

MODULATING SECTION

The modulating section accepts audio signals or d-c keying signals and suitably transforms them to modulate or control the r-f energy generated by the r-f generating section. The circuits of the modulating section are contained in two units of the transmitter: the radio frequency oscillator and the amplifier-power supply.

The filter method of generating single sidebands is used in the modulator. With this method, sideband operation must be accomplished at a low frequency level since accurate filter design is difficult to achieve at high frequencies. After generation, the sidebands may be heterodyned to the desired transmitter operating frequency. In the transmitter group, a 2.0-mc carrier is applied to balanced modulators for sideband generation. The sidebands are then mixed with the MO signal to obtain sum frequencies at the desired frequency level of operation.

BLOCK DIAGRAM

A block diagram of the modulation section is shown in figure 16-9. Three types of emission are available with audio input signals: single sideband (A3a), independent sideband (A3b), or compatible amplitude modulation (USB and carrier).

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Audio Stage

The audio input from the microphone is fed via T1407 or T1408 and filter FL1401 to either of two identical speech amplifier channels. The channels are the upper sideband (USB) and lower sideband (LSB) channels, respectively. Because the channels are the same, only those blocks in the USB channel are shown.

For amplitude modulation operation, only the upper sideband speech amplifier circuits are used and only one sideband plus the carrier (compatible a-m) is transmitted. For single sideband (SSB) operation either the upper sideband or lower sideband speech amplifier circuits may be used. For independent sideband (ISB) operation, two independent audio signals may be applied simultaneously to the two separate speech amplifier circuit. The desired type of operation is selected through EMISSION SELECTOR switch S508.

Speech signals generated by the USB telephone handset are coupled through T1407 to band-pass filter FL1401. The filtered signal is then applied to the USB speech amplifier and the USB-AGC control.

A portion of the audio signal output of the second USB speech amplifier is diverted to the USB sidetone amplifier. This signal is fed back to the phone handset for monitoring purposes. TEST TONE switch S511 substitutes the output of the 425-cycle test oscillator, Q1411 and Q1412, for that of the audio when a single-tone test signal is desired. Meter amplifier Q501 and Mod level meter M502 provide a visual indication of the speech amplifier output levels. Meter M502 is connected in the output circuit by MOD LEVEL switch S512.

The output of the USB speech amplifier is applied through switch S508 to the grids of USB modulator V1201. The modulator contains a twin-triode tube with its control grid driven 180° out of phase by an audio signal, while the common cathodes receive a 2.0-mc carrier signal.

The 2.0-mc signal which is applied to both the carrier reinsert cathode followers and the sideband modulators is derived from the 1-mc crystal-stabilized reference oscillator in the r-f generating section (fig. 16-6). The oscillator output is applied to the 10:1 frequency divider circuit. The 500-kc output from binary No. 1 is applied to 500-kc amplifier stage V1207A (fig. 16-9). The output of V1207A is coupled to two half-wave diode rectifier circuits (not shown) for harmonic generation. Tuned tanks at the control grids of the 2.0-mc

selector V1208 and 1500-kc selector V1209 select the 2.0-mc and 1500-kc harmonics, respectively, from the rectifier outputs. Stages V1208 and V1209 amplify their respective harmonic. The purpose of the 1500-kc selector is treated later.

As stated above, the 2.0-mc input is applied to the common cathodes of the twin-triode USB balanced modulator V1201 while the audio speech amplifier output is applied to the twin-triode control grids 180° out of phase. The plates of the modulator are connected in push-pull. The action of a balanced modulator cancels the carrier (2.0 mc) input. The signal appearing at the input USB filter, FL1201, consists of sum and difference frequencies and a carrier frequency signal of negligible magnitude if the push-pull balanced modulator stage is properly balanced.

USB filter FL1201 allows only upper sideband frequency components to pass (without severe attenuation) to the grid of sideband combiner V1203. The bandpass of FL1201 is from 2,000,300 to 2,008,000 cps.

The sideband combiner consists of a twin triode tube. The 2,000,300- to 2,008,000-cps output from FL1201 is applied to the control grid of the A section of V1203, while a similar range of frequencies below the 2.0-mc carrier signal is applied to the V1203B grid from the LSB filter FL1202 (not shown). The plates of V1203A & B have separate plate loads in the carrier reject filter FL1203. The filter (filter components not shown) rejects the 2.0 mc carrier at the V1203 output. The common secondary coil connected between terminals 2 and 4 of FL1203 receive both the USB and LSB signal components as separate signals. These outputs are fed to either the 2.0-mc amplifier, V1206, or to the 500-kc modulator V1204, depending on the transmitter operating frequency, and the position of auxiliary range switch section S1202A.

The 2.0-mc carrier signal from V1208 is also applied to carrier reinsert cathode follower V1207B. The cathode circuit of V1207B contains a voltage divider network from which various voltage levels of the 2.0-mc carrier signal can be selected by CARRIER REINSERT switch S1201. Varying degrees of carrier reinsertion are required to facilitate signal recovery at the receiver. A higher level of carrier reinsertion is possible during c-w operation than during a-m operation because the peaks of the speech signals limit the amount of drive that can be applied to the power amplifier stages. Attenuation settings of -∞, -20, -10, 0,

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and +3 db are provided. For a-m, MACH c-w, and c-w operation it is necessary to transmit a carrier signal.

Keying Circuits

Three classes of d-c keying signals are accepted by the modulating section: frequency-shift neutral keying from a teletype or multiplex unit, machine or c-w keying signals from an automatic coder, or hand-keyed c-w signals.

In FSK operation, the S508C & D contacts are closed. Switch section S508B is open and S508A is in the FSK position. The FSK or MACH c-w input signals are applied through S508C to a keying multivibrator, Q1401 and Q1402. The output of the 425-cps test oscillator Q1411 and Q1412 is applied through S508D to the FSK switch. This circuit comprises CR1402 through CR1409 and is a symmetrical electronic switch which is driven by keying multivibrator Q1401 and Q1402.

When a space signal is on the line, the keying multivibrator causes the FSK switch to route the 425-cps signal to the LSB modulator. When a mark signal is on the line, the keying multivibrator changes state and the FSK switch transfers the 425-cps signal to the USB modulator. Thus, the mark signal is 425 cycles above the carrier frequency and the space signal is 425 cycles below the carrier frequency.

During c-w operation, the c-w key actuates a bias keying stage, Q502, the output of which is applied through S508A to the grid of the 2.0-mc amplifier, V1206, to the grid of the 500-kc amplifier, V1205, and to the grids of the mixer and driver stages of the radio frequency amplifier (shown later). This action cuts off the transmitter carrier when the key is open.

As stated earlier, the master oscillator in the RFO (fig. 16-6) operates from 1.5 to 7.5 mc. The use of the fundamental MO frequencies for band 1 through 6 (2.0 to 8.0 mc) necessitates the inclusion of the 1500-kc selector, V1209 (fig. 16-9) and the 500-kc modulator, V1204. On the lowest transmitter range, the MO frequency is 1.5 mc. Because of the action of S302 (fig. 16-8), the master oscillator output on the lowest range bypasses the frequency multiplier stages and is fed directly to an input mixer. A 500-kc signal must also be introduced into the input mixer if the transmitter output frequency is to be 2 megacycles, which is the lowest frequency that can be transmitted.

When the transmitter output is to be in the 2.0- to 8.0-mc range auxiliary range switch sections S1202A & C (fig. 16-9) apply the sideband combiner output (via FL1203) and the output of 1500-kc selector V1209 to the 500-kc modulator V1204. The 500-kc modulator is identical in operation to the USB modulator described earlier. The push-pull output of V1204 suppresses the 1500-kc signal and a tuned tank in the grid circuit of the 500-kc amplifier V1205 selects only the difference-frequency components generated by the modulator, plus or minus the modulation (intelligence) contained in the original 2.0-mc signal. The 500-kc signal then passes through auxiliary range switch S1202B to the mixer in the PA section.

The 500-kc signal serves as the injection frequency to the PA mixer throughout the frequency coverage of bands 1 through 6.

When tuning the transmitter to a frequency between 8.0 and 9.5 mc, the operator should be careful to select the proper output frequency from the modulating section which will produce the desired transmitter output frequency after mixing in the input mixer stage with the master oscillator frequency. For example, if it is desired to operate the transmitter on a frequency of 8.20 mc, the bandswitch, S302, would be positioned on band 5. The master oscillator can then be tuned to 6.20 mc. By placing the auxiliary range switch S1202A in the 8 - 30-MC position, the 2.0-mc (plus modulation) output, of the modulating section is selected for application of V951. After mixing in V951, the transmitter output will be 8.20 mc. By tuning the master oscillator over the band 5 range (5.0 to 6.25 mc), transmitter output frequencies between 7.0 and 8.25 mc can be obtained by using the 2.0-mc injection frequency in the input mixer.

Similarly, to tune the transmitter to any frequency between 8.25 and 9.5 mc, S302 should be adjusted to select band 6. The master oscillator can now be tuned over the range of 6.25 to 7.5 mc. If the auxiliary range switch is placed in the 8 - 30-MC position, the 2.0-mc modulation output will be heterodyned in the input mixer. The sum frequencies are passed through the power amplifier section and the transmitter can be tuned over the desired 8.25- to 9.5-mc range. Proper selection of the injection frequency from the modulating section makes possible the operation of the transmitter on any frequency within its 2.0- to 30.0-mc range.

POWER AMPLIFIER AND ANTENNA SECTION

The power amplifier and antenna section are contained in the radio frequency amplifier (fig. 16-10).

BLOCK DIAGRAM

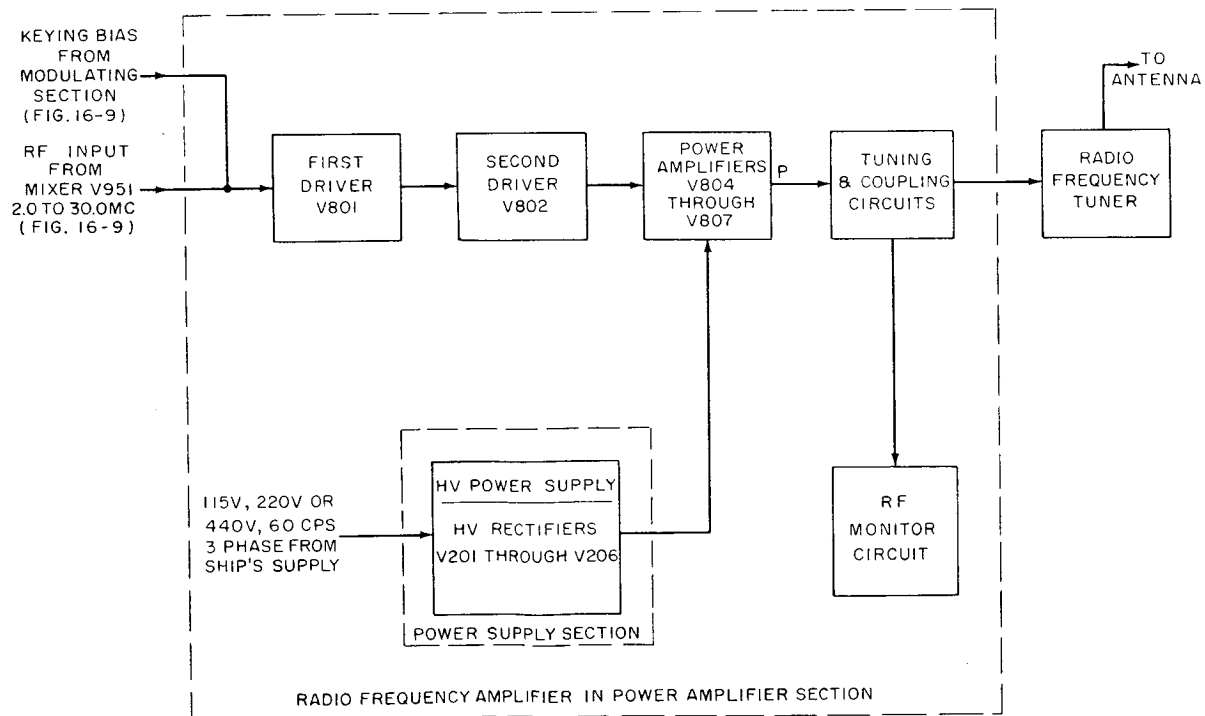A block diagram of the power amplifier and antenna sections is shown in figure 16-11.
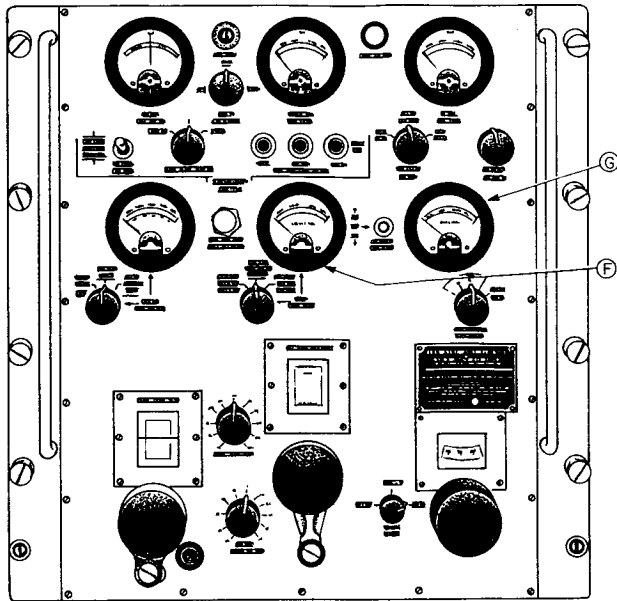
32.287

Figure 16-10.—Radiofrequency amplifier, front panel controls.

These sections include driver and power amplifier stages, tuning and coupling circuits, and the r-f monitor.

After mixing in the input mixer stage of the modulating section (fig. 16-9), the r-f signal contains the modulation component and is in the frequency range from 2.0 to 30.0 mc as selected by the operator. The output of the mixer is amplified in the first and second driver stages, V801 and V802, in the power amplifier section (fig. 16-10). The amplified r-f is then applied to the power amplifier stages, V804 through V807.

The power amplifier stages consist of four 4CX300 tetrode tubes connected in parallel (not shown). Plate voltages for these tubes is supplied by high voltage rectifiers V201 through V206. The power amplifier output is fed through the tuning and coupling circuits and the radio frequency tuner to the antenna.

A portion of the output from the tuning circuit is fed to the r-f monitor circut, which consists of a modulation monitor for measuring the modulation percentage, and a reflectometer for measuring the output power level and voltage standing wave ratio on the line which feeds the antenna. A circuit analysis of the r-f monitor is treated later.

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Figure 16-11.—Power amplifier section, block diagram.

CIRCUIT ANALYSIS

Because the circuits of the driver and power amplifier stages are conventional in most respects, the circuit analysis of these stages is not treated in this discussion. The antenna tuning and coupling circuits used in the AN/WRT-2 are not conventional and are therefore treated with the aid of schematic diagrams.

Tuning and Coupling Circuits

The plate output of the power amplifier tubes is fed into the tuning and coupling circuits by C827 (fig. 16-12). The resonant frequency of tuning components L803 through L805

T803 secondary winding is of the same phase as the output voltage. The T804 secondary winding is of the same phase as the output current. The vector sums of these voltages is applied to the detector circuits.

When READ SWR switch S807 is in its closed position (as shown), 17 volts a-c is applied to the cathodes of CR806 and CR812, and CR807 and CR813. The 17 volts a-c places a bias on these diodes so that they operate as square-law detectors, their d-c output voltage being proportional to the square of the applied voltage. The output of one set of diodes is proportional to incident power and the output of the other set of diodes is proportional to reflected power due to a mismatch of impedances. R-F OUTPUT
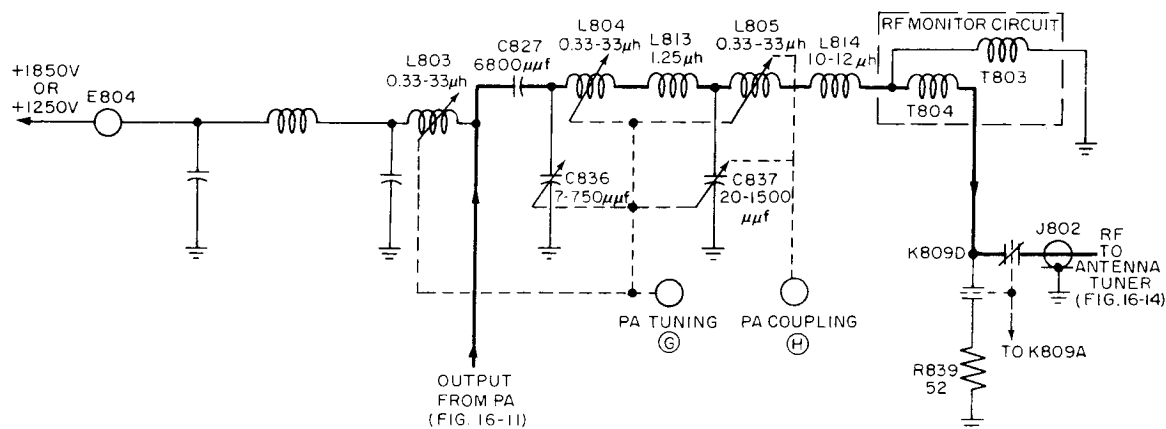

Figure 16-12.—Tuning and coupling circuits.

and C836 and C837 is adjusted by a PA TUNING Ⓖ control and PA COUPLING Ⓗ control located on the radio frequency amplifier front panel. These components form a pi network low-pass filter at the operating frequency. The PA tuning control adjusts all five tuning components simultaneously while the Ⓗ control adjusts only C837 and L805.
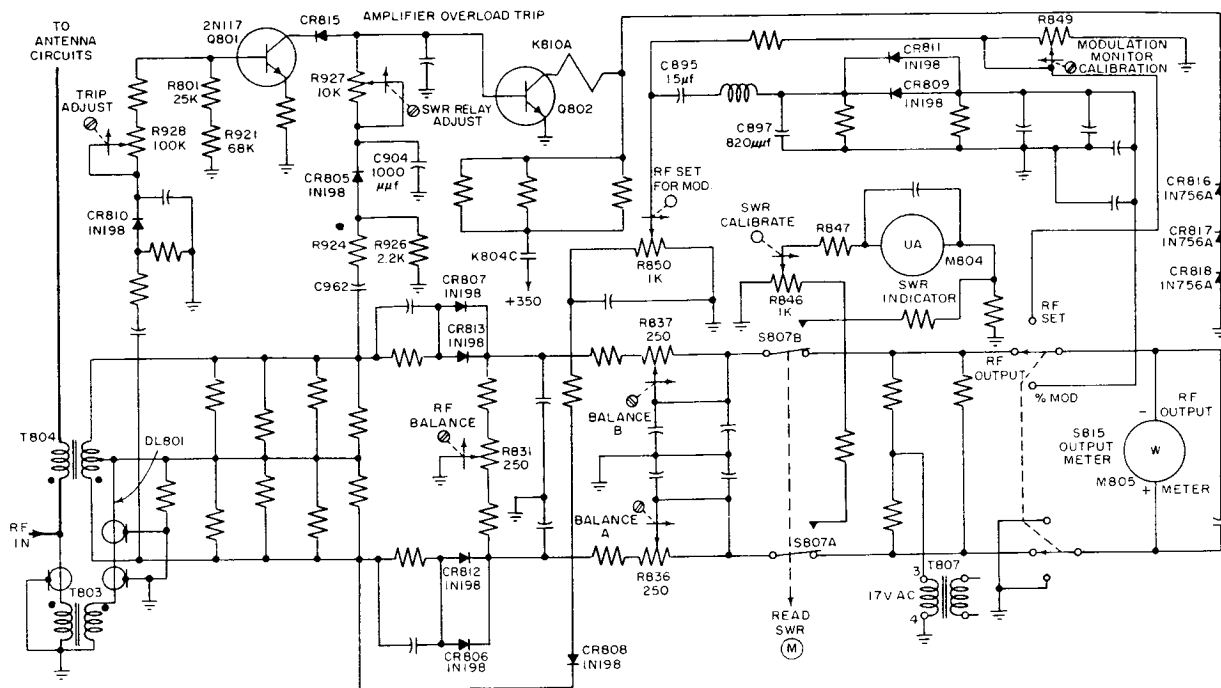
R-f Monitor

As forestated, the r-f monitoring circuit contains a modulation monitor circuit which indicates percentage of modulation, and a reflectometer circuit which measures the transmitter power output and the VSWR on the line of the antenna. Figure 16-13 is a simplified schematic of the r-f monitor circuit.

The T803 primary winding is connected from the antenna feed line to ground. A portion of the transmitter output is developed across the transformer. The voltage induced in the

meter M805, connected to the two output lines through OUTPUT METER switch S815, measures the difference between the incident and reflected power or the true power. BALANCE A control R836 and BALANCE B control R837 provide for zero adjustment and upper scale calibration of meter M805.

READ SWR switch S807 is spring loaded and normally in the position shown. R-F BALANCE control R831 is used as a means of balancing conduction irregularities in the two sets of diodes, CR806, CR812, CR807, and CR813. To measure the standing wave ratio, the switch is pushed to its momentary position, and the power monitoring circuit is removed. The removal of the 17 volts a-c from the sets of diodes permit the diodes to become linear detectors. SWR INDICATOR meter M804 is connected into the monitor circuit when switch S807 is closed to its upper contacts and the SWR is indicated.

For monitoring modulation, an r-f sample of the transmitter output is obtained from the

32.290

Figure 16-13.—R-f monitoring circuit, simplified schematic diagram.

bottom of T804 and applied to CR808. A negative d-c voltage is developed across R-F SET FOR MOD control R850. When OUTPUT METER switch S815 is in R-F SET position, a portion of the d-c voltage across R850 is applied to OUTPUT METER M805 and R850 is adjusted so that M805 deflects to its R-F SET marker. When switch S815 is in % MOD position, a pulsating voltage is applied from the arm of R850 through C895. The d-c voltage from R850 is rectified by parallel diodes CR809 and CR811 and filtered to remove the r-f and permit an a-f signal to be applied to M805.

When a known modulation % is applied to a carrier, OUTPUT METER switch S815 is placed in R-F SET position and MOD MON CAL potentiometer R849 is adjusted to indicate the known modulation %. Thereafter, when switch S815 is placed in % MOD position, and the transmitter emission is of the A3 type, M805 indicates percentage of modulation.

To avoid possible equipment damage, SWR protection stages (Q801 and Q802) are provided to remove the high voltage from the PA stage when the SWR becomes excessive. When no SWR exists on the feeder line to the antenna the base voltage of Q802 (developed across R926 in parallel with Q801) is 180° out of phase with the voltage applied to the base of Q801. This voltage relationship exists because the base

signal input for Q801 and Q802 is obtained from opposite ends of the T804 secondary. The 180° phase shift in Q801 causes the signal from the Q801 collector to be in phase with the R426 voltage at the Q802 base. The voltage across R926 increases as the SWR increases. When the ratio becomes greater than 4:1, the collector current of Q802 is sufficient to energize relay K810; and initiates the removal of all d-c voltages. The setting of SWR relay adjust R926 determines the amount of voltage that must be developed across R926 before the overload relay, K810, energizes.

Transistor Q801 is provided in order that the overload circuit may still function properly at low power levels. The collector resistance of Q801 is a function of the base-emitter bias developed across R801 and R921. When operating at low power levels, the base bias of Q801 decreases and therefore its collector resistance increases. At the same time the voltage across R926 has decreased, but the base-emitter bias for Q802 does not decrease substantially due to the increased collector resistance of Q801. Thus, an excessive SWR will still cause relay K810 to energize even when the power output level is reduced. The setting of SWR ALARM TRIP ADJUST potentiometer R928 determines the amount of base-emitter bias applied to Q801.

Antenna Tuner

The radio frequency tuner increases or de-
creases the effective physical length of the an-
tenna by removing or inserting inductance in
series with the antenna. As shown in figure
16-14, drive motor B3301 and 2-speed drive
MP3301 drive a sliding short up and down the
main coil L3302 which can be switched in
series with the antenna via antenna transfer

switch S3301. A pictorial illustration of L3302
is shown in figure 16-15. The arm of R3301
(fig. 16-14) is geared to the mechanical drive
mechanism and an electrical contact is made to
POSITION INDICATOR meter M806 on the front
panel of the RFA. The meter indicates the rela-
tive position of the sliding short on the main coil.

Fixed capacitance may also be inserted in
series or in parallel with the antenna for tuning
purposes.
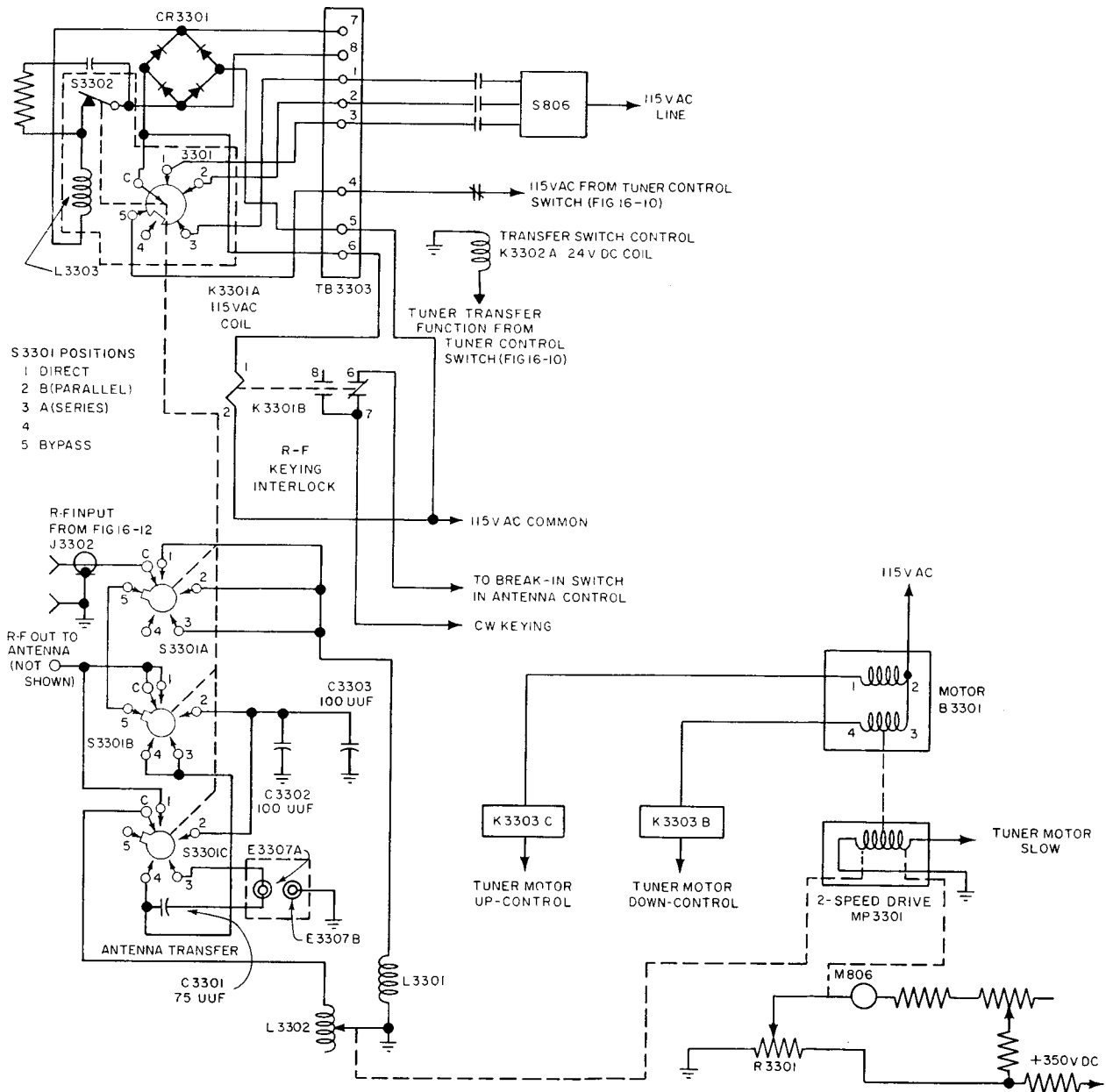
32.291

Figure 16-14.—Radiofrequency tuner, schematic diagram.
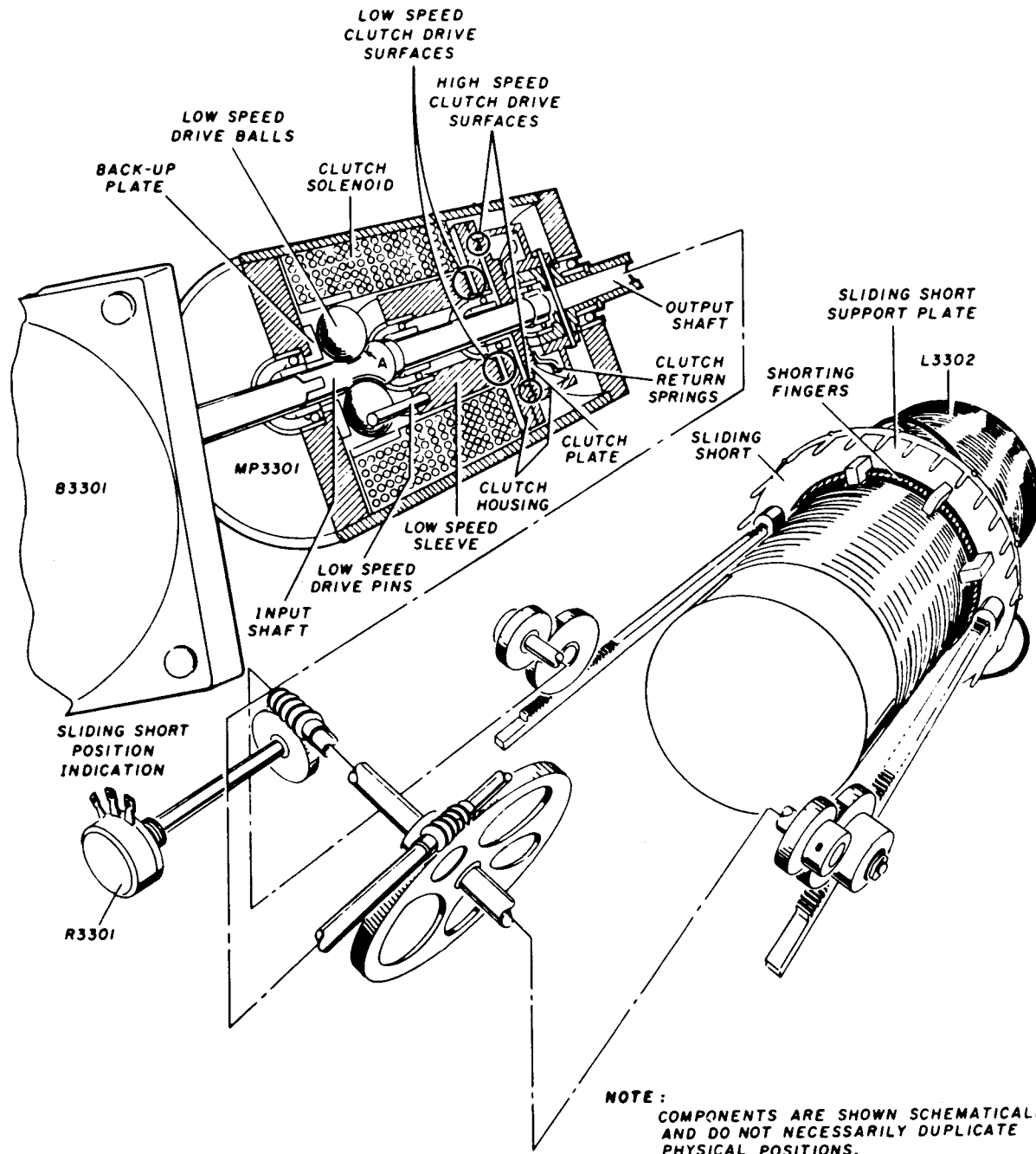
Figure 16-15.—Antenna tuner coil, L3302.

Switch S806 (COUPLER ANTENNA Ⓙ control on the RFA in fig. 16-10), provides 115 volts a-c for the actuator L3303 (fig. 16-14) when placed in the DIRECT, A, or B position. These positions correspond to positions 1, 2, and 3 on S3301. A tuner control switch on the front panel applies 115 volts a-c to the actuator when the bypass function is desired. In this position (as shown) relay K3302A is energized. When the tuner components are to be used, the

tuner control switch is placed in the TUNER-IN position, and K3302A deenergizes. This again permits the desired tuning components to be selected by S806.

Switches S3307 and S3301, driven by actuator L3303, place C3302 and C3303 in parallel with the antenna when COUPLER ANTENNA (J) switch S806 is in the B position. When S806 is in the A position, C3301 is placed in series with the antenna, and when in the DIRECT position, only L3302 is in series with the antenna. The setting of COUPLER (J) switch S806 depends on the operating frequency of the transmitter. If the transfer switch control relay, K3302, is energized, switches S3307 and S3301 automatically return to position 5 and the tuner is bypassed.

Antenna tuner up, down, and slow controls on the RFA front panel enable the operator to select the desired movement of the L3302 arm (sliding short) and also to control the speed of tuning. Limit switches (not shown) limit the upper and lower travel of the shorting arm.

POWER SUPPLY SECTION

A block diagram of the power section is shown in figure 16-16. The high voltage rectifiers supply d-c voltage to the PA tubes. The low voltage power supply supplies all the d-c

voltages needed for proper operation, such as the +350-volt, -350-volt, -24-volt, +12-volt, -12-volt, 250-volt regulated, +24-volt regulated, and a -6-volt regulated supply.

The primary power input of 115 volts, 220 volts, or 440 volts, depending upon the ship's supply, is applied to the T501 and T202 through T203 primary windings. Tapped terminals on T501, T201, T202, and T203 provide an output of 220 and 115 volts. Transformers T201 through T203 are connected in a delta-wye circuit.

In TUNE or 100-watt operation, approximately 266 volts is supplied by the respective transformer secondary to the rectifier tubes. In 500-watt operation approximately 545 volts is supplied to the tubes.

The output of T501 is applied to the circuits of the low voltage power supply section through FILAMENT POWER switch S502. The 220 volts is applied to the primaries of T502 and T503 while the 115 volts is applied to T617 in the electrical frequency control.

The output of T502 is rectified by the plus and minus 350-volt rectifiers, and applied to the circuits of the RFA. Part of the output of the 350-volt rectifier is also applied to the 250-volt regulator. The 250-volt regulator consists of series regulators V321 and V322, regulator amplifier V323, and voltage reference
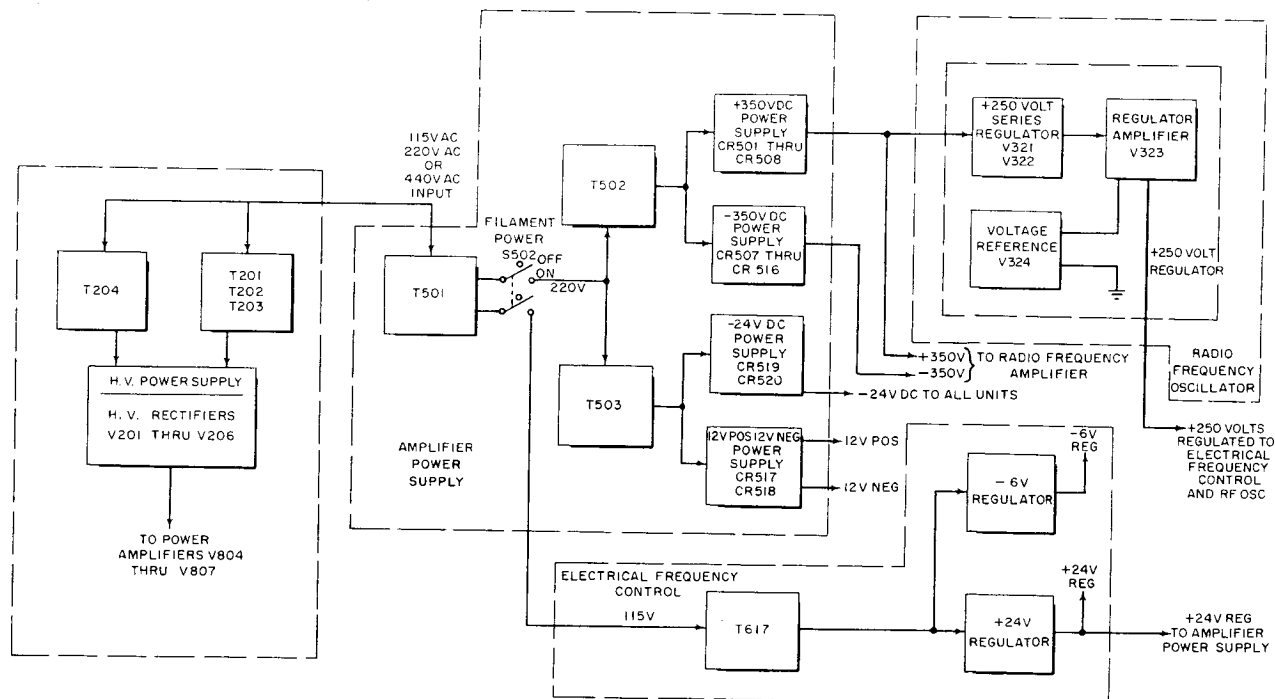

32.293

Figure 16-16.—Power supply section, block diagram.

tube V324. The regulated output is applied to stages in the electrical frequency control circuit and r-f oscillator.

The output of T503 is rectified by the -24-volt rectifiers, and fed to the various circuits throughout the transmitter which require this potential. A second output of T503 is applied to the 12-volt rectifier. The negative output of the 12-volt power supply is fed to the speech amplifier and control circuits. The positive output is fed only to control circuits in the amplifier-power supply and mike circuits.

The output of T617 is rectified by the 24-volt and -6-volt regulators, respectively. The 24-volt output is regulated and fed to the circuit of the r-f generating and modulating sections. The -6-volt regulated supply is used by circuits of the 1-mc oscillator.

Rectifiers V201 through V206 are connected in a three-phase bridge circuit. Filament voltage is supplied by transformer T204. The high voltage output is applied to the plates of the power amplifier tubes in the power amplifier section.
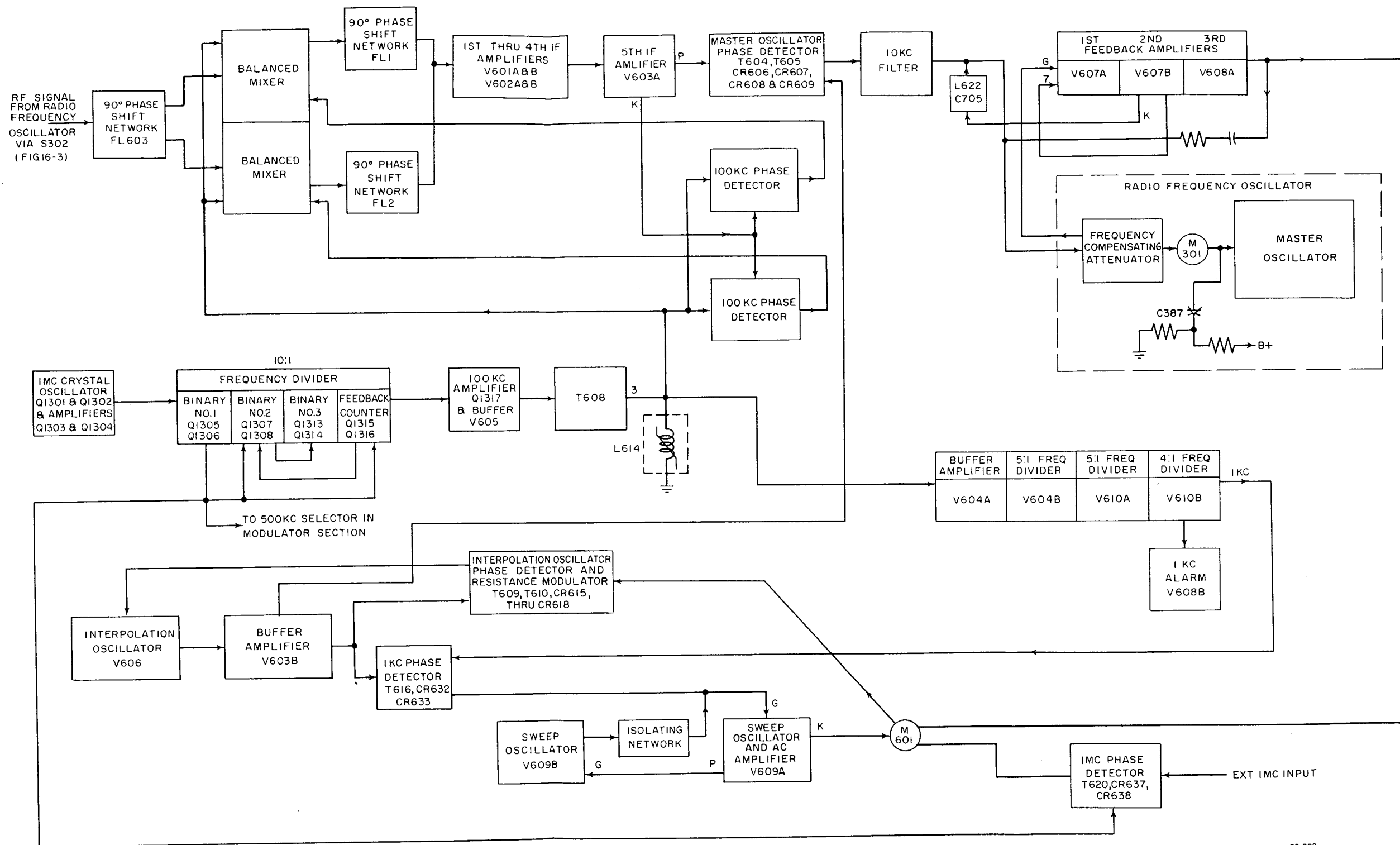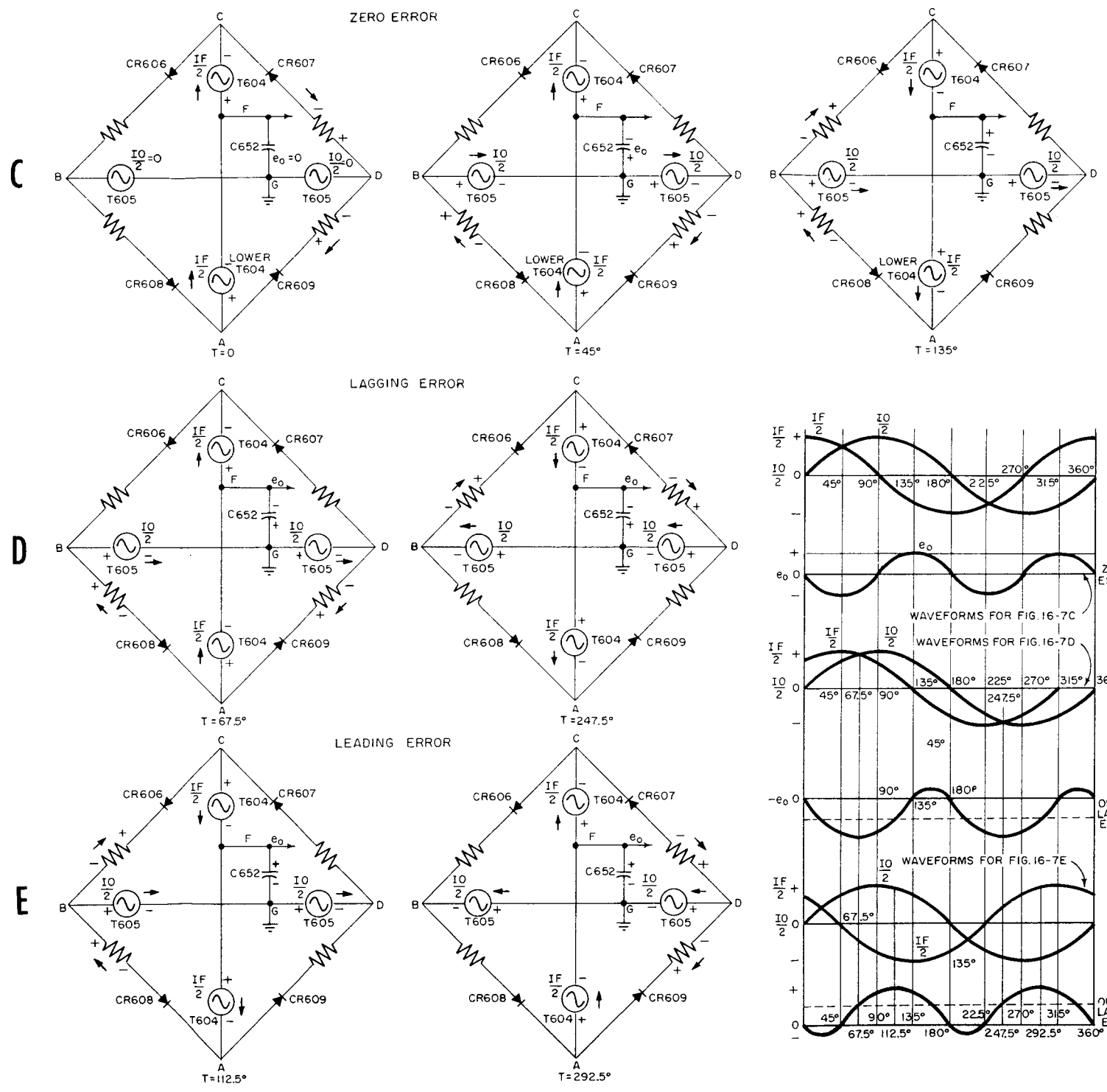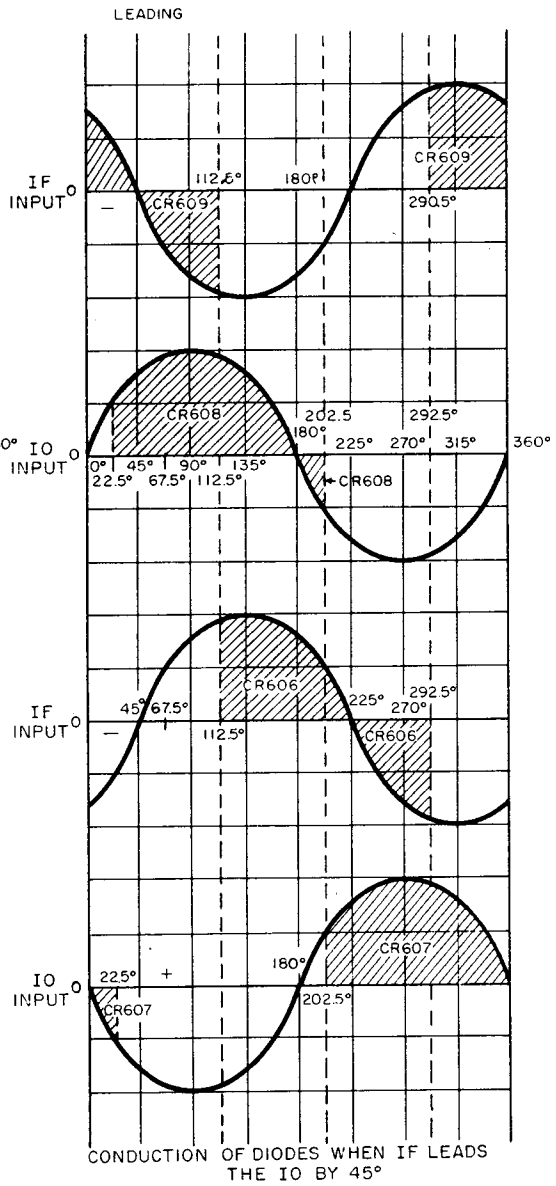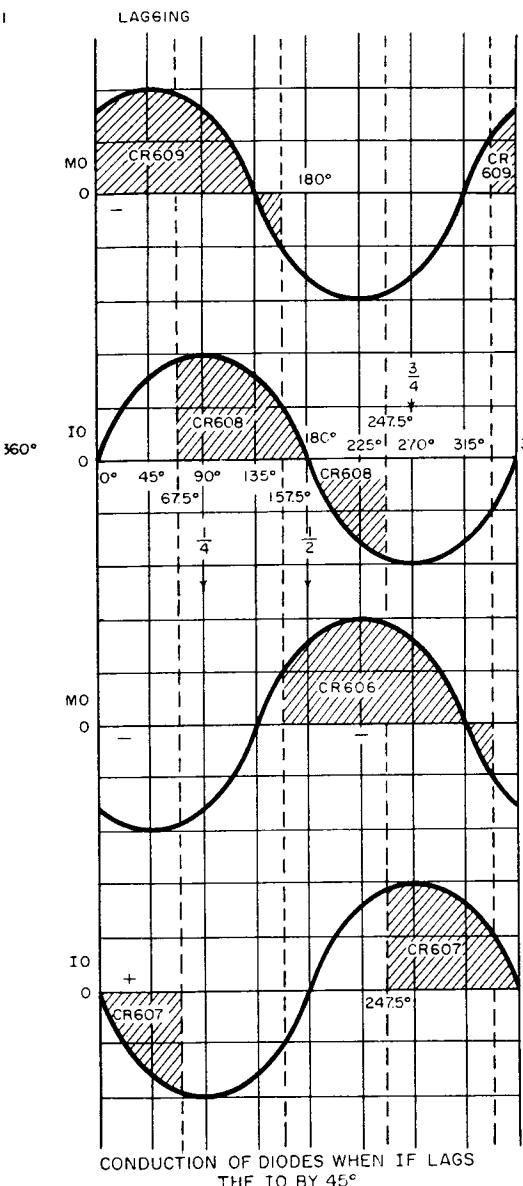
Figure 16-6.—Electrical frequency control, detailed block diagram.

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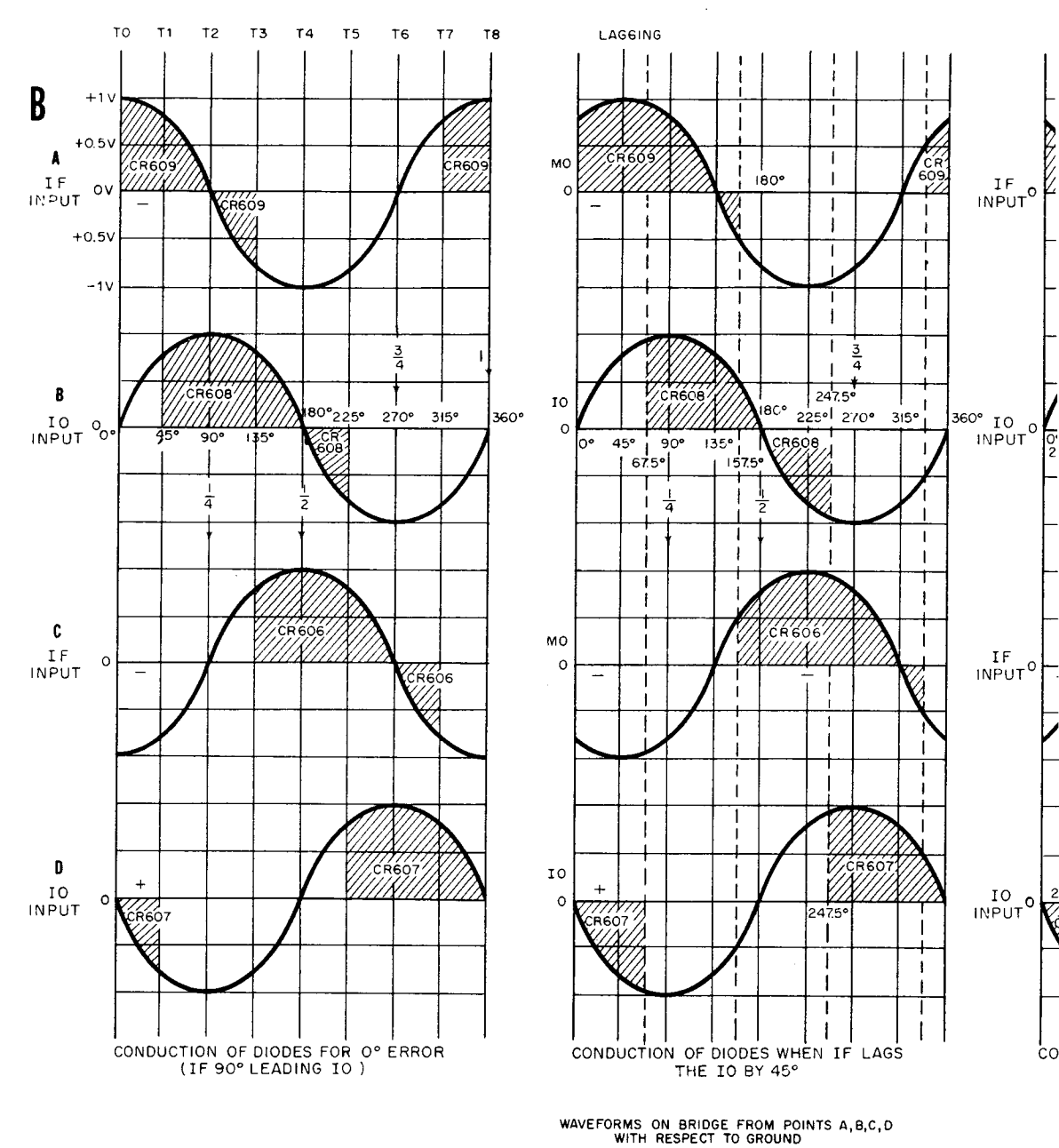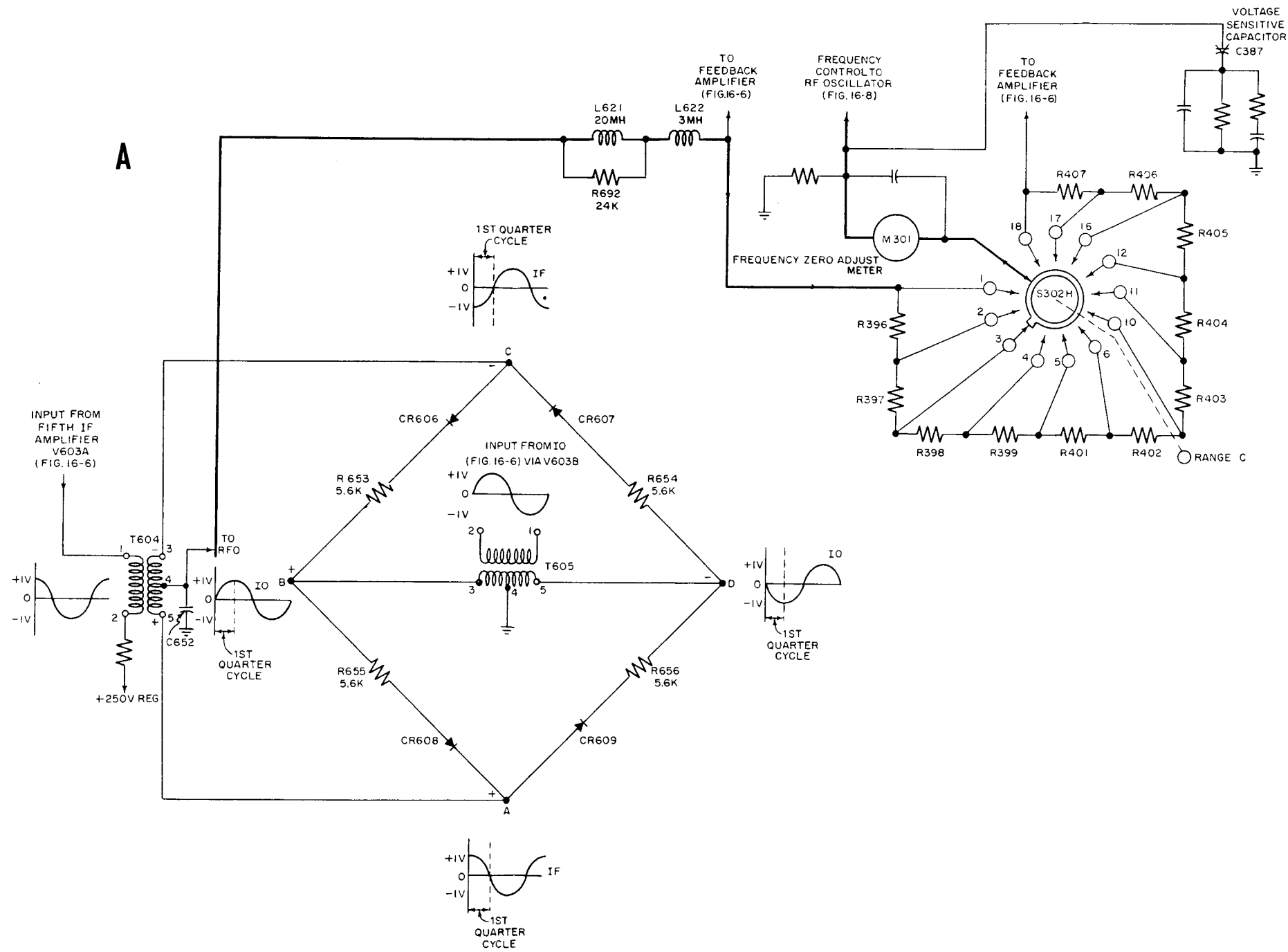
32.284

A. Simplified diagram with waveforms.
B. Conduction of diodes.
C. Zero error.
D. Lagging error.
E. Leading error.

Figure 16-7.—Master oscillator-phase detector analysis.

CONDUCTION OF DIODES WHEN IF LAGS
THE IO BY 45°

CONDUCTION OF DIODES WHEN IF LEADS
THE IO BY 45°

WAVEFORMS ON BRIDGE FROM POINTS A,B,C,D
WITH RESPECT TO GROUND

ZERO ERROR

LAGGING ERROR

LEADING ERROR

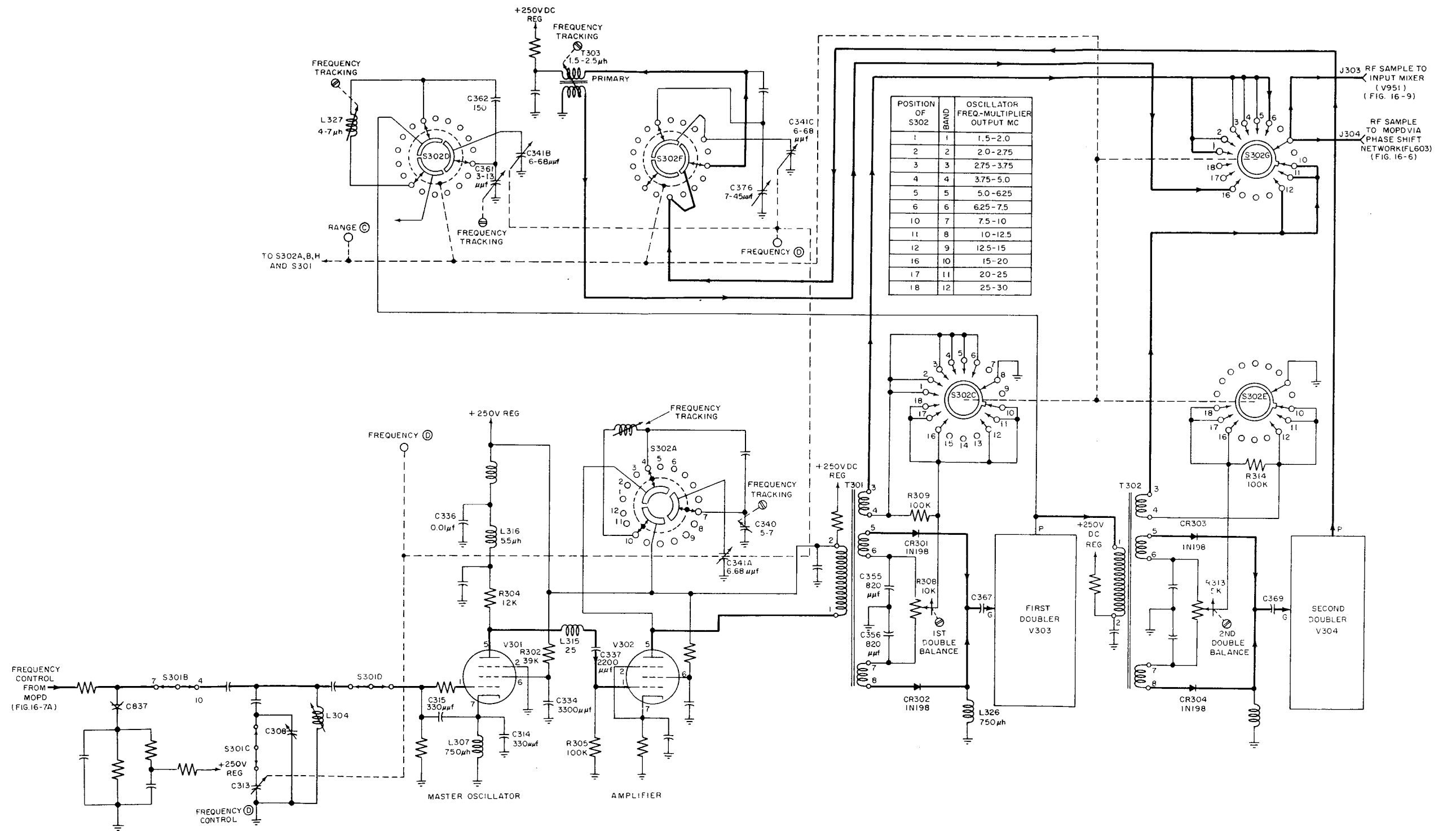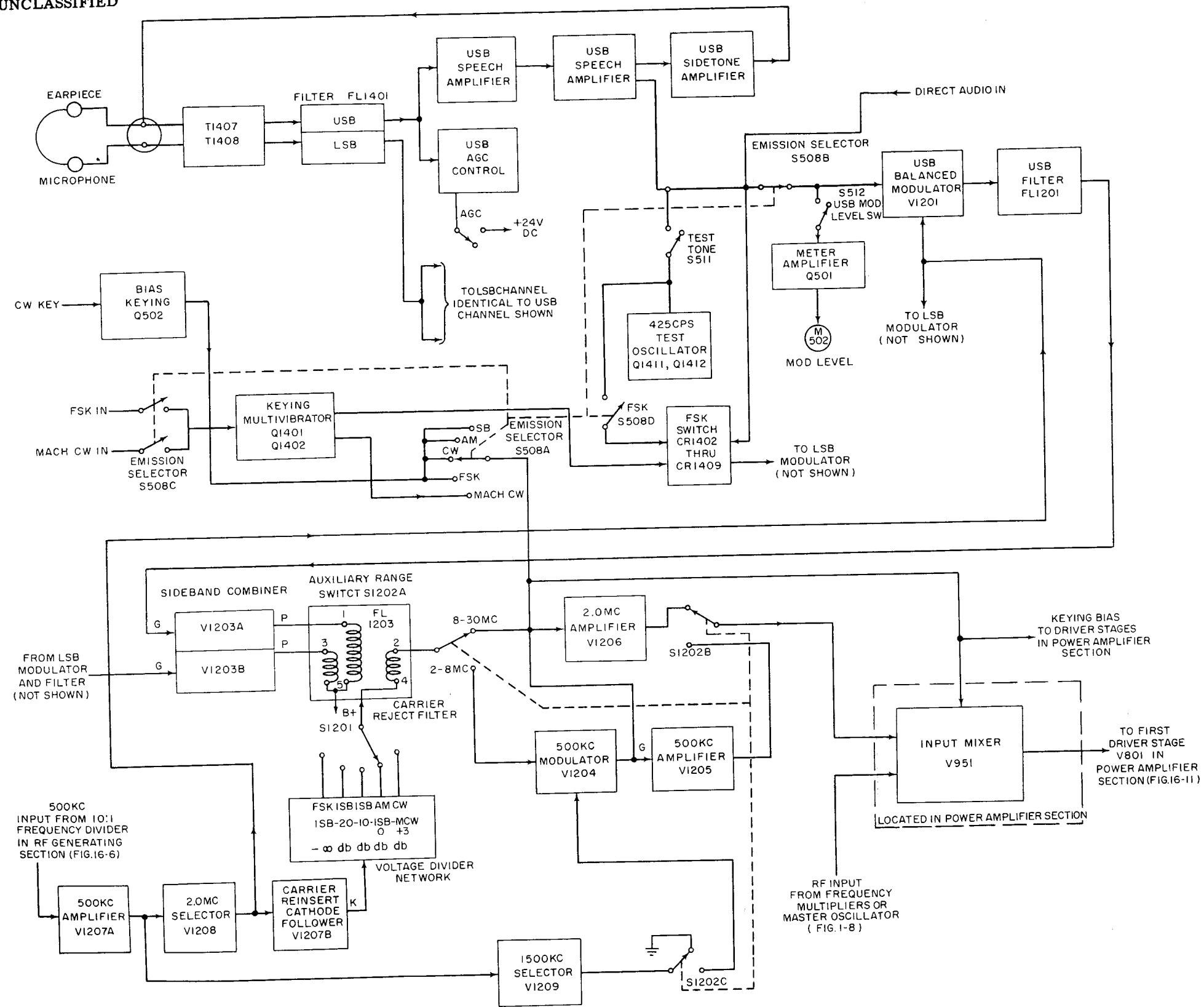| POSITION OF S302	BAND	OSCILLATOR FREQ-MULTIPLIER OUTPUT MC
1	1	1.5-2.0
2	2	2.0-2.75
3	3	2.75-3.75
4	4	3.75-5.0
5	5	5.0-6.25
6	6	6.25-7.5
10	7	7.5-10
11	8	10-12.5
12	9	12.5-15
16	10	15-20
17	11	20-25
18	12	25-30

Figure 16-8.—Master oscillator-frequency multiplier, simplified schematic diagram.

32.285

32.286
Figure 16-9.—Modulating section, block diagram.